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# **High Efficiency Thyristor**

1200 V

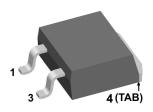
20 A

1,37 V

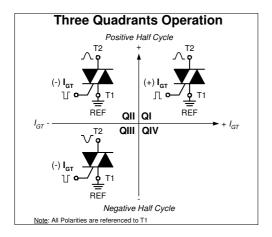
Three Quadrants operation: QI - QIII 1~ Triac

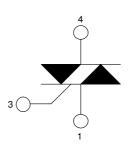
Part number

### CLA40MT1200NPZ



Backside: anode/cathode





### Features / Advantages:

- Triac for line frequency
- Three Quadrants Operation
- QI QIII
- Planar passivated chip
- Long-term stability of blocking currents and voltages

### **Applications:**

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter AC power control
- Lighting and temperature control
- Package: TO-263 (D2Pak-HV)
- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0
- High creepage distance between terminals

#### Terms \_Conditions of usage:

The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact the sales office, which is responsible for you.

Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact the sales office, which is responsible for you. Should you intend to use the product in aviation, in health or live endangering or life support applications, please notify. For any such application we urgently recommend

- to perform joint risk and quality assessments; the conclusion of quality agreements;
- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

IXYS reserves the right to change limits, conditions and dimensions.

Data according to IEC 60747 and per semiconductor unless otherwise specified

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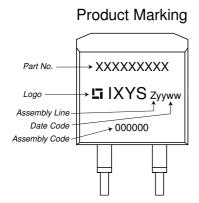


Rectifier				1 _	Ratings		1
Symbol	Definition	Conditions	T 0550	min.	typ.	max.	Un
V <sub>RSM/DSM</sub>	max. non-repetitive reverse/forward		$T_{VJ} = 25^{\circ}C$			1300	
V <sub>RRM/DRM</sub>	max. repetitive reverse/forward blo	<u> </u>	$T_{VJ} = 25^{\circ}C$			1200	'
R/D	reverse current, drain current	$V_{R/D} = 1200 \text{ V}$	$T_{VJ} = 25^{\circ}C$			10	μ
		$V_{R/D} = 1200 \text{ V}$	T <sub>VJ</sub> = 125°C			1,5	m
V <sub>T</sub>	forward voltage drop	$I_T = 20 \text{ A}$	$T_{VJ} = 25^{\circ}C$			1,37	,
		$I_T = 40 \text{ A}$				1,71	١
		$I_T = 20 A$	$T_{VJ} = 125$ °C			1,37	١
		$I_T = 40 \text{ A}$				1,83	1
ITAV	average forward current	$T_C = 115$ °C	$T_{VJ} = 150$ °C			20	1
I <sub>RMS</sub>	RMS forward current per phase	180° sine				44	,
V <sub>T0</sub>	threshold voltage		$T_{VJ} = 150$ °C			0,89	١
r <sub>T</sub>	slope resistance	ss calculation only				24	m۵
R <sub>thJC</sub>	thermal resistance junction to case	)				0,8	K/V
R <sub>thCH</sub>	thermal resistance case to heatsing	k			0,25		K/V
P <sub>tot</sub>	total power dissipation		$T_{\rm C} = 25^{\circ}{\rm C}$		,	155	٧
I <sub>TSM</sub>	max. forward surge current	t = 10 ms; (50 Hz), sine	$T_{v,l} = 45^{\circ}C$			200	,
ISM	-	t = 8,3 ms; (60 Hz), sine	$V_R = 0 V$			215	
		t = 10  ms; (50 Hz), sine	T <sub>v.1</sub> = 150°C			170	,
		t = 8,3  ms; (60 Hz), sine	$V_R = 0 V$			185	
l²t	value for fusing	t = 10 ms; (50 Hz), sine	$T_{VJ} = 45^{\circ}C$			200	A <sup>2</sup>
	value ter teenig	t = 8,3 ms; (60 Hz), sine	$V_R = 0 V$			190	A <sup>2</sup>
		t = 0.0  ms; (50  Hz),  sine t = 10  ms; (50  Hz),  sine	T <sub>v,i</sub> = 150°C			145	A <sup>2</sup>
		t = 8,3 ms; (60 Hz), sine	$V_R = 0 V$			140	A <sup>2</sup>
C,	junction capacitance	$V_{\rm B} = 400  \text{V}  \text{f} = 1  \text{MHz}$	$T_{VJ} = 25^{\circ}C$		12	140	pl
	<u> </u>	$t_{P} = 30 \mu s$	$T_{\rm C} = 150^{\circ}{\rm C}$		12	5	۷
P <sub>GM</sub>	max. gate power dissipation		1 <sub>C</sub> = 150 C				۷
<b>D</b>		$t_{P} = 300  \mu s$				1	] 
P <sub>GAV</sub>	average gate power dissipation	T 45000 ( 5011				0,2	۷
(di/dt) <sub>cr</sub>	critical rate of rise of current		epetitive, $I_T = 60 \text{ A}$			150	A/μ
		$t_P = 200 \mu s; di_G/dt = 0.3 A/\mu s; -$					
			on-repet., $I_T = 20 \text{ A}$			500	i
(dv/dt) <sub>cr</sub>	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150$ °C			500	V/μ
		R <sub>GK</sub> = ∞; method 1 (linear volta					
$V_{GT}$	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$			1,3	'
			$T_{VJ} = -40$ °C			1,6	١
I <sub>GT</sub>	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$			± 40	m
			$T_{VJ} = -40$ °C			± 60	m
V <sub>GD</sub>	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150$ °C			0,2	١
I <sub>GD</sub>	gate non-trigger current					± 1	m
I <sub>L</sub>	latching current	t <sub>p</sub> = 10 μs	$T_{VJ} = 25$ °C			70	m
		$I_{G} = 0.3 \text{ A}; \text{ di}_{G}/\text{dt} = 0.3 \text{ A}/\mu\text{s}$	3				į
I <sub>H</sub>	holding current	V <sub>D</sub> = 6 V R <sub>GK</sub> = ∞	$T_{VJ} = 25$ °C			50	m
t <sub>gd</sub>	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25$ °C			2	μ
gu	· · ·	$I_{G} = 0.3 \text{ A}; \text{ di}_{G}/\text{dt} = 0.3 \text{ A}/\mu\text{s}$				_	٣
+	turn-off time	$V_R = 100 \text{ V}; I_T = 20 \text{ A}; V = \frac{2}{3}$			150		- 11
t <sub>q</sub>	tan on and		$t_{p} = 200  \mu s$		130		μ



# CLA40MT1200NPZ

Package TO-263 (D2Pak-HV)				Ratings			
Symbol	Definition Conditions		min.	typ.	max.	Unit	
I <sub>RMS</sub>	RMS current per terminal				35	Α	
T <sub>VJ</sub>	virtual junction temperature		-40		150	°C	
T <sub>op</sub>	operation temperature		-40		125	°C	
T <sub>stg</sub>	storage temperature		-40		150	°C	
Weight				1,5		g	
F <sub>c</sub>	mounting force with clip		20		60	N	
d <sub>Spp/App</sub>	creepage distance on surface   striking distance through air	terminal to terminal	4,2			mm	
$d_{Spb/Apb}$	creepage distance on surface   striking distance through an	terminal to backside	4,7			mm	



## Part description

C = Thyristor (SCR) L = High Efficiency Thyristor

A = (up to 1200V)

40 = Current Rating [A]

MT = 1~ Triac

1200 = Reverse Voltage [V]

N = Three Quadrants operation: QI - QIII PZ = TO-263AB (D2Pak) (2HV)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA40MT1200NPZ	CLA40MT1200NPZ	Tape & Reel	800	515974

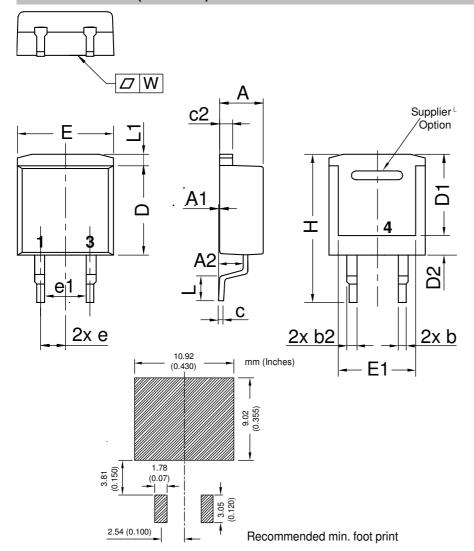
Similar Part	Package	Voltage class
CLA40MT1200NPB	TO-220AB (3)	1200

Equiva	alent Circuits for	Simulation	* on die level	T <sub>VJ</sub> = 150 °C
$I \rightarrow V_0$	)— <u>R</u> o	Thyristor		
V <sub>0 max</sub>	threshold voltage	0,89		V
$R_{0 \text{ max}}$	slope resistance *	21		$m\Omega$



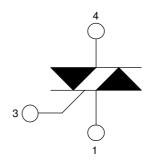


# Outlines TO-263 (D2Pak-HV)



Dim.	Millimeter		Inches		
DIIII.	min	max	min	max	
Α	4.06	4.83	0.160	0.190	
A1	typ.	0.10	typ. 0	0.004	
A2	2.	41	0.0	95	
b	0.51	0.99	0.020	0.039	
b2	1.14	1.40	0.045	0.055	
С	0.40	0.74	0.016	0.029	
c2	1.14	1.40	0.045	0.055	
D	8.38	9.40	0.330	0.370	
D1	8.00	8.89	0.315	0.350	
D2	2	.3	0.091		
Е	9.65	10.41	0.380	0.410	
E1	6.22	8.50	0.245	0.335	
е	2,54 BSC		0,100 BSC		
e1	4.28		0.169		
Н	14.61	15.88	0.575	0.625	
L	1.78	2.79	0.070	0.110	
L1	1.02	1.68	0.040	0.066	
W	typ. 0.02	0.040	typ. 0.0008	0.002	

All dimensions conform with and/or within JEDEC standard.





# **Thyristor**

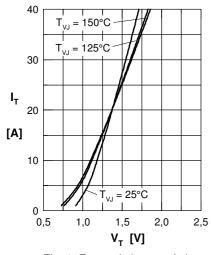


Fig. 1 Forward characteristics

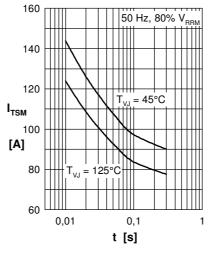


Fig. 2 Surge overload current

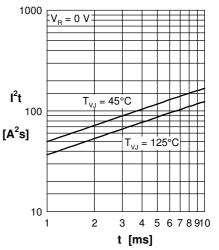


Fig. 3 I<sup>2</sup>t versus time (1-10 ms)

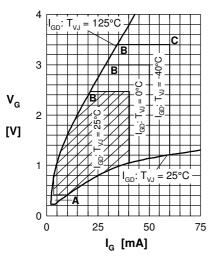


Fig. 4 Gate trigger characteristics

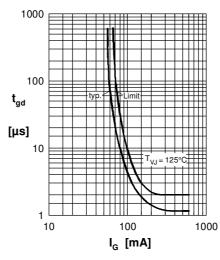


Fig. 5 Gate controlled delay time

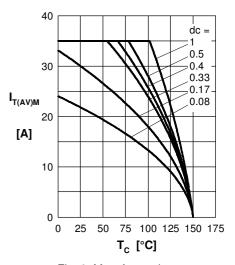


Fig. 6 Max. forward current at case temperature

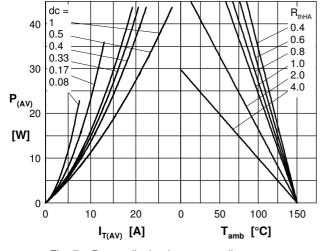


Fig. 7a Power dissipation versus direct output current Fig. 7b and ambient temperature

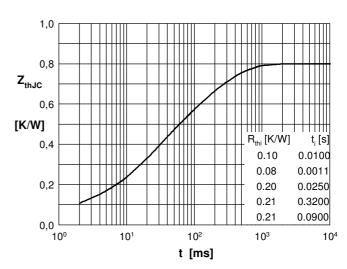


Fig. 8 Transient thermal impedance