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Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

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CLA50E1200TC

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Ξ

1200 V

1,27 V

50 A

 V_{RRM}

I _{TAV}

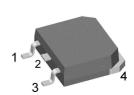
VT

High Efficiency Thyristor

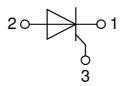
Sing	е	Thy	risto	or
- 3	-			

Part number

CLA50E1200TC



Backside: anode



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-268AA (D3Pak)

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

Terms Conditions of usage:

The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact the sales office, which is responsible for you. Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact the sales office, which is responsible for you. Should you intend to use the product in aviation, in health or live endangering or life support applications, please notify. For any such application we urgently recommend

to perform joint risk and quality assessments;
the conclusion of quality agreements;

- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

IXYS reserves the right to change limits, conditions and dimensions.

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CLA50E1200TC

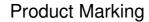
Thyristo					Ratings		!
Symbol	Definition	Conditions		min.	typ.	max.	Uni
V _{RSM/DSM}	max. non-repetitive reverse/forwa	rd blocking voltage	$T_{VJ} = 25^{\circ}C$			1300	١
V _{RRM/DRM}	max. repetitive reverse/forward bl	ocking voltage	$T_{VJ} = 25^{\circ}C$			1200	٧
R/D	reverse current, drain current	V _{R/D} = 1200 V	$T_{VJ} = 25^{\circ}C$			50	μA
		V _{R/D} = 1200 V	$T_{VJ} = 125^{\circ}C$			4	mA
V _T	forward voltage drop	Ι _τ = 50 A	$T_{VJ} = 25^{\circ}C$			1,32	٧
		$I_{T} = 100 \text{ A}$				1,60	V
		I _T = 50 A	$T_{vJ} = 125 \degree C$			1,27	V
		I _T = 100 A				1,65	٧
I TAV	average forward current	T _c = 125°C	T _{vJ} = 150°C			50	A
T(RMS)	RMS forward current	180° sine				79	A
ν _{το}	threshold voltage		T _{v.I} = 150°C			0,88	٧
r _T	slope resistance } for power lo	oss calculation only				7,7	mΩ
R _{thJC}	thermal resistance junction to cas	e				0,25	K/W
R _{thCH}	thermal resistance case to heatsi				0,15		K/W
P _{tot}	total power dissipation		$T_c = 25^{\circ}C$,	500	W
I _{TSM}	max. forward surge current	t = 10 ms; (50 Hz), sine	$T_{v,l} = 45^{\circ}C$			650	A
- 1 5 M	C C	t = 8,3 ms; (60 Hz), sine	$V_{R} = 0 V$			700	Α
		t = 10 ms; (50 Hz), sine	T _{v.i} = 150°C			555	Α
		t = 8,3 ms; (60 Hz), sine	$V_{\rm R} = 0 V$			595	A
l²t	value for fusing	t = 0,0 ms; (50 Hz), sine	$\frac{V_{R}}{T_{VJ}} = 45^{\circ}C$			2,12	, kA²s
		t = 8,3 ms; (60 Hz), sine	$V_{\rm R} = 0 V$			2,04	kA ² s
		t = 0,5 ms; (50 Hz), sine t = 10 ms; (50 Hz), sine	$T_{VJ} = 150^{\circ}C$			1,54	kA ² s
		t = 8,3 ms; (60 Hz), sine	$V_{\rm R} = 0 V$			1,48	kA ² s
CJ	junction capacitance	$V_{\rm B} = 400 \text{V}$ f = 1 MHz	$\frac{V_{R}}{T_{VJ}} = 25^{\circ}C$		25	1,40	pF
P _{GM}		$t_{\rm P} = 30 \mu {\rm s}$	$T_{c} = 150^{\circ}C$		25	10	рі W
FGM	max. gate power dissipation		$1_{\rm C} = 150$ C			5	w
_		t _P = 300 μs				-	
P _{GAV}	average gate power dissipation	T 45000 (50 Hz				0,5	W
(di/dt) _{cr}	critical rate of rise of current		petitive, $I_{T} = 150 \text{ A}$			150	A/μs
		$t_{\rm P} = 200 \mu {\rm s}; di_{\rm G}/dt = 0.3 {\rm A}/\mu {\rm s}; -$					• /
			pn-repet., $I_{T} = 50 \text{ A}$				A/μs
(dv/dt) _{cr}	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{vJ} = 150^{\circ}C$			1000	V/με
		$R_{GK} = \infty$; method 1 (linear volta)					
V _{gt}	gate trigger voltage	$V_{D} = 6 V$	$T_{vJ} = 25^{\circ}C$			1,5	۷
			$T_{vJ} = -40 ^{\circ}C$			1,6	V
I _{GT}	gate trigger current	$V_{D} = 6 V$	$T_{vJ} = 25^{\circ}C$			50	mA
			$T_{vJ} = -40^{\circ}C$			80	mA
V _{gd}	gate non-trigger voltage	$V_{D} = \frac{2}{3} V_{DRM}$	$T_{vJ} = 150^{\circ}C$			0,2	۷
I _{GD}	gate non-trigger current					3	mA
I.	latching current	t _p = 10 μs	$T_{vJ} = 25 ^{\circ}C$			125	mA
		$I_{G} = 0,3 A; di_{G}/dt = 0,3 A/\mu s$	5				
I _H	holding current	$V_{D} = 6 V R_{GK} = \infty$	$T_{vJ} = 25 ^{\circ}C$			100	mA
t _{gd}	gate controlled delay time	$V_{\rm D} = \frac{1}{2} V_{\rm DRM}$	$T_{vJ} = 25 \degree C$			2	με
		$I_{G} = 0.3 \text{ A}; \ di_{G}/dt = 0.3 \text{ A}/\mu \text{s}$	5				
t _q	turn-off time	$V_{\rm B} = 100 \text{ V}; \ I_{\rm T} = 50 \text{ A}; \ V = \frac{2}{2}$		<u> </u>	200		μs
•		$di/dt = 10 \text{ A}/\mu \text{s} dv/dt = 20 \text{ V}/\mu \text{s}$			1		•

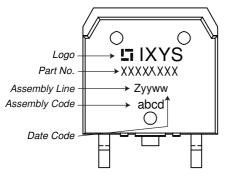
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CLA50E1200TC

Package TO-268AA (D3Pak)			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I _{RMS}	RMS current	per terminal			70	Α
T _{vj}	virtual junction temperature		-40		150	°C
T _{op}	operation temperature		-40		125	°C
T _{stg}	storage temperature		-40		150	°C
Weight				5		g
F _c	mounting force with clip		20		120	Ν





Part description

- C = Thyristor (SCR)
- L = High Efficiency Thyristor
- A = (up to 1200V)
- 50 = Current Rating [A] E = Single Thyristor
- 1200 = Reverse Voltage [V]TC = TO-268AA (D3Pak) (2)

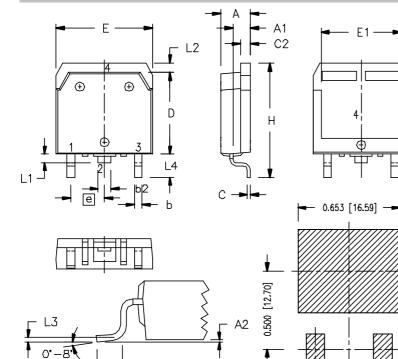
Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA50E1200TC	CLA50E1200TC	Tube	30	502708

Similar Part	Package	Voltage class
CLA50E1200HB	TO-247AD (3)	1200

Equiva	lent Circuits for	Simulation	* on die level	$T_{VJ} = 150 \ ^{\circ}C$
)[R	Thyristor		
V _{0 max}	threshold voltage	0,88		V
$\mathbf{R}_{0 \text{ max}}$	slope resistance *	5,2		mΩ

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Outlines TO-268AA (D3Pak)



Dim.	Millimeter		Inc	hes
Dini.	min	max	min	max
Α	4.90	5.10	0.193	0.201
A1	2.70	2.90	0.106	0.114
A2	0.02	0.25	0.001	0.100
b	1.15	1.45	0.045	0.057
b2	1.90	2.10	0.075	0.083
С	0.40	0.65	0.016	0.026
C2	1.45	1.60	0.057	0.063
D	13.80	14.00	0.543	0.551
D1	12.40	12.70	0.488	0.500
Е	15.85	16.05	0.624	0.632
E1	13.30	13.60	0.524	0.535
е	5.45	BSC	0.215 BSC	
Н	18.70	19.10	0.736	0.752
L	2.40	2.70	0.094	0.106
L1	1.20	1.40	0.047	0.055
L2	1.00	1.15	0.039	0.045
L3	0.25 BSC		0.100 BSC	
L4	3.80	4.10	0.150	0.161



-

0.215 [5.46]

E1 -

4

Ð ф

F

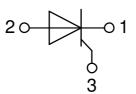
D1

0.197 [5.00]

t

– b.118 [3.00]

0.864 [21.95]



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CLA50E1200TC

Thyristor

٧_G

[V]

0,1

100

80

60

40

20

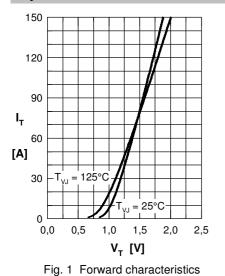
0

 $\mathbf{P}_{(AV)}$

[W]

1

10



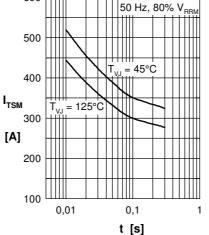


Fig. 2 Surge overload current

 I_{TSM} : crest value, t: duration

600

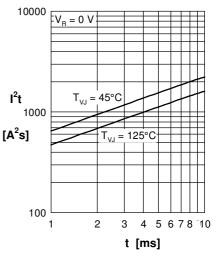
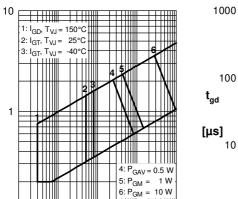


Fig. 3 I²t versus time (1-10 s)

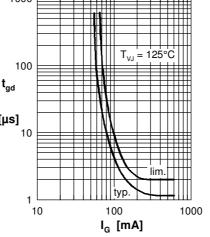


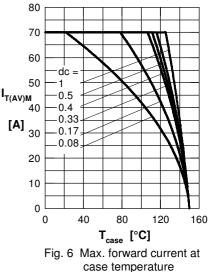
I_G [mA] Fig. 4 Gate voltage & gate current

100

10000

1000





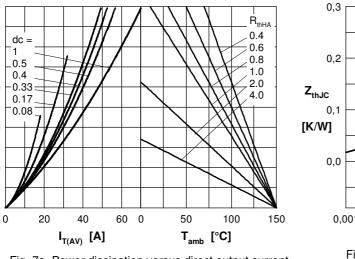
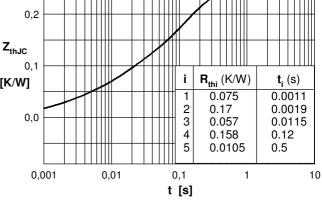
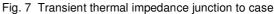


Fig. 7a Power dissipation versus direct output current Fig. 7b and ambient temperature

Fig. 5 Gate controlled delay time $\rm t_{gd}$





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