Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

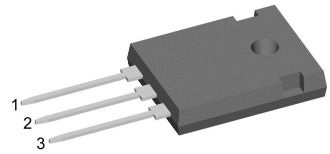
High Efficiency Thyristor

V_{RRM} = 1200 V
I_{TAV} = 30 A
V_T = 1,25 V

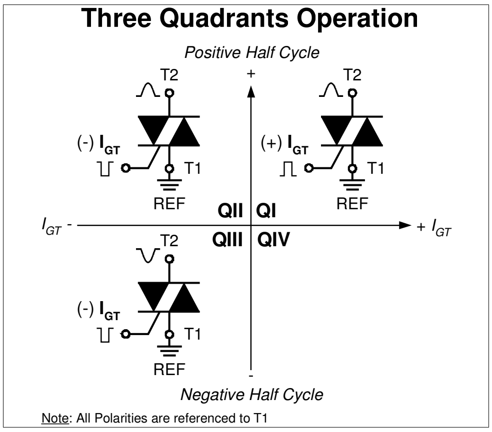
Three Quadrants operation: QI - QIII
1~ Triac

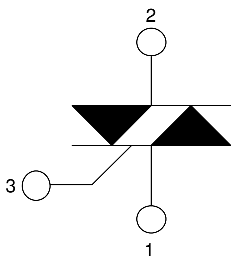
Part number

CLA60MT1200NHB



Backside: Terminal 2





Features / Advantages:

- Triac for line frequency
- Three Quadrants Operation
  - QI - QIII
- Planar passivated chip
- Long-term stability
  of blocking currents and voltages

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

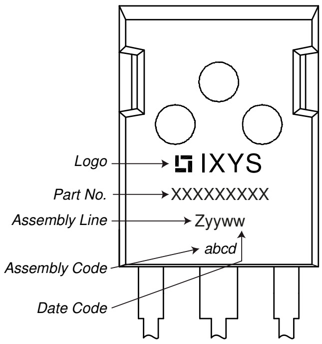
Package: TO-247

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

Rectifier				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
$V_{RSM/DSM}$	*max. non-repetitive reverse/forward blocking voltage*		T_{VJ} = 25°C			1300	V
$V_{RRM/DRM}$	*max. repetitive reverse/forward blocking voltage*		T_{VJ} = 25°C			1200	V
$I_{R/D}$	*reverse current, drain current*	$V_{R/D}$ = 1200 V	T_{VJ} = 25°C			10	µA
		$V_{R/D}$ = 1200 V	T_{VJ} = 125°C			2	mA
V_T	*forward voltage drop*	I_T = 30 A	T_{VJ} = 25°C			1,28	V
		I_T = 60 A				1,56	V
		I_T = 30 A	T_{VJ} = 125°C			1,25	V
		I_T = 60 A				1,61	V
I_{TAV}	*average forward current*	T_C = 120°C	T_{VJ} = 150°C			30	A
I_{RMS}	*RMS forward current per phase*	180° sine				66	A
V_{T0}	*threshold voltage*	*for power loss calculation only*	T_{VJ} = 150°C			0,86	V
r_T	*slope resistance*					12,5	mΩ
R_{thJC}	*thermal resistance junction to case*					0,55	K/W
R_{thCH}	*thermal resistance case to heatsink*				0,25		K/W
P_{tot}	*total power dissipation*		T_C = 25°C			230	W
I_{TSM}	*max. forward surge current*	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			380	A
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			410	A
		t = 10 ms; (50 Hz), sine	T_{VJ} = 150°C			325	A
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			350	A
I^2t	*value for fusing*	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			720	A²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			700	A²s
		t = 10 ms; (50 Hz), sine	T_{VJ} = 150°C			530	A²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			510	A²s
C_J	*junction capacitance*	V_R = 400 V f = 1 MHz	T_{VJ} = 25°C		25		pF
P_{GM}	*max. gate power dissipation*	t_P = 30 µs	T_C = 150°C			10	W
		t_P = 300 µs				5	W
P_{GAV}	*average gate power dissipation*					0,5	W
$(di/dt)_{cr}$	*critical rate of rise of current*	T_{VJ} = 150 °C; f = 50 Hz	repetitive, I_T = 90 A			150	A/µs
		t_P = 200 µs; di_G/dt = 0,3 A/µs;					
		I_G = 0,3 A; V = ⅔ V_{DRM}	non-repet., I_T = 30 A			500	A/µs
$(dv/dt)_{cr}$	*critical rate of rise of voltage*	V = ⅔ V_{DRM}	T_{VJ} = 150°C			500	V/µs
		R_{GK} = ∞; method 1 (linear voltage rise)					
V_{GT}	*gate trigger voltage*	V_D = 6 V	T_{VJ} = 25°C			1,7	V
			T_{VJ} = -40°C			1,9	V
I_{GT}	*gate trigger current*	V_D = 6 V	T_{VJ} = 25°C			± 60	mA
			T_{VJ} = -40°C			± 80	mA
V_{GD}	*gate non-trigger voltage*	V_D = ⅔ V_{DRM}	T_{VJ} = 150°C			0,2	V
I_{GD}	*gate non-trigger current*					± 1	mA
I_L	*latching current*	t_p = 10 µs	T_{VJ} = 25°C			90	mA
		I_G = 0,3 A; di_G/dt = 0,3 A/µs					
I_H	*holding current*	V_D = 6 V R_{GK} = ∞	T_{VJ} = 25°C			60	mA
t_{gd}	*gate controlled delay time*	V_D = ½ V_{DRM}	T_{VJ} = 25°C			2	µs
		I_G = 0,3 A; di_G/dt = 0,3 A/µs					
t_q	*turn-off time*	V_R = 100 V; I_T = 30 A; V = ⅔ V_{DRM}	T_{VJ} = 125 °C		150		µs
		di/dt = 10 A/µs dv/dt = 20 V/µs	t_p = 200 µs				

Package TO-247			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	*RMS current*	per terminal			70	A
T_{VJ}	*virtual junction temperature*		-40		150	°C
T_{op}	*operation temperature*		-40		125	°C
T_{stg}	*storage temperature*		-40		150	°C
Weight				6		g
M_D	*mounting torque*		0,8		1,2	Nm
F_C	*mounting force with clip*		20		120	N

Product Marking



Part description

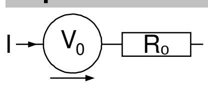
C = Thyristor (SCR)
L = High Efficiency Thyristor
A = (up to 1200V)
60 = Current Rating [A]
MT = 1~ Triac
1200 = Reverse Voltage [V]
N = Three Quadrants operation: QI - QIII
HB = TO-247AD (3)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA60MT1200NHB	CLA60MT1200NHB	Tube	30	512073

Similar Part	Package	Voltage class
CLA60MT1200NHR	ISO247 (3)	1200
CLA60MT1200NTZ	TO-268AA (D3Pak)	1200

Equivalent Circuits for Simulation

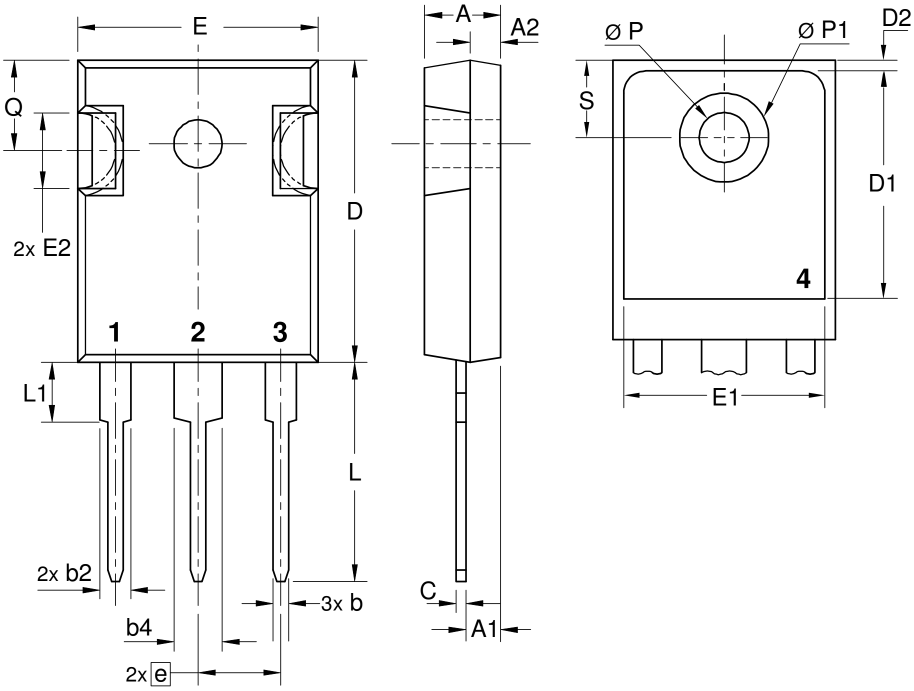
** on die level* $T_{VJ} = 150\,°C$



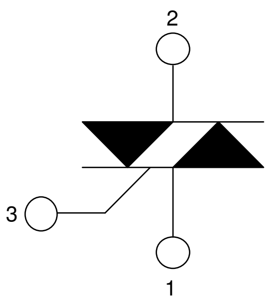
Thyristor

$V_{0\,max}$	*threshold voltage*	0,86	V
$R_{0\,max}$	*slope resistance **	10	mΩ

Outlines TO-247



Sym.	Inches		Millimeter	
	min.	max.	min.	max.
A	0.185	0.209	4.70	5.30
A1	0.087	0.102	2.21	2.59
A2	0.059	0.098	1.50	2.49
D	0.819	0.845	20.79	21.45
E	0.610	0.640	15.48	16.24
E2	0.170	0.216	4.31	5.48
e	0.215 BSC		5.46 BSC	
L	0.780	0.800	19.80	20.30
L1	-	0.177	-	4.49
Ø P	0.140	0.144	3.55	3.65
Q	0.212	0.244	5.38	6.19
S	0.242 BSC		6.14 BSC	
b	0.039	0.055	0.99	1.40
b2	0.065	0.094	1.65	2.39
b4	0.102	0.135	2.59	3.43
c	0.015	0.035	0.38	0.89
D1	0.515	-	13.07	-
D2	0.020	0.053	0.51	1.35
E1	0.530	-	13.45	-
Ø P1	-	0.29	-	7.39



Thyristor

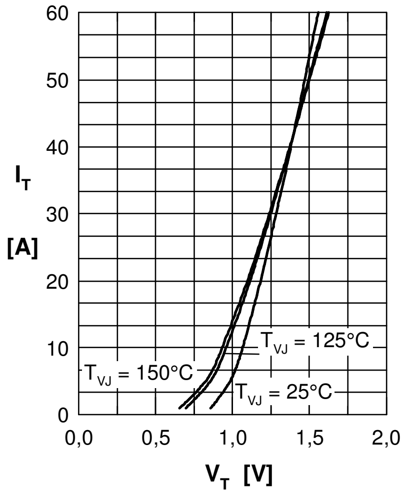


Fig. 1 Forward characteristics

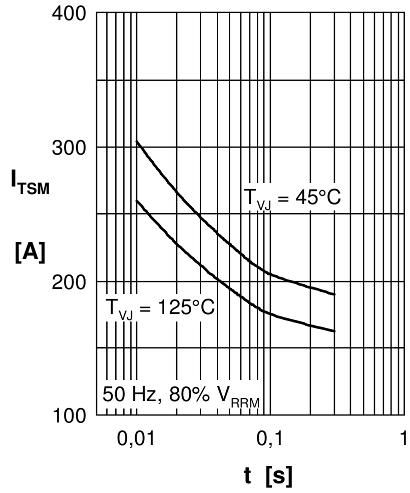


Fig. 2 Surge overload current
I_{TSM}: crest value, t: duration

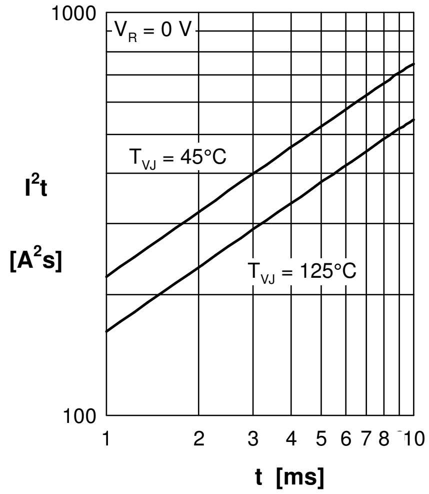


Fig. 3 I^2t versus time (1-10 s)

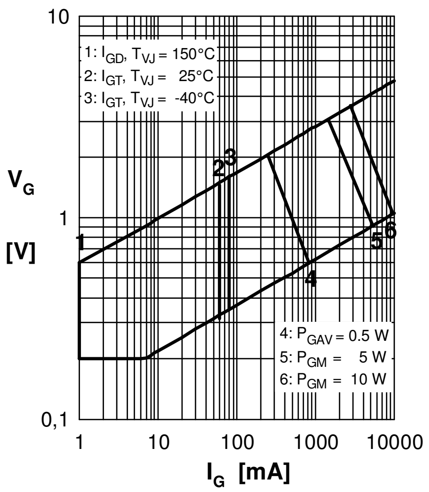


Fig. 4 Gate voltage & gate current

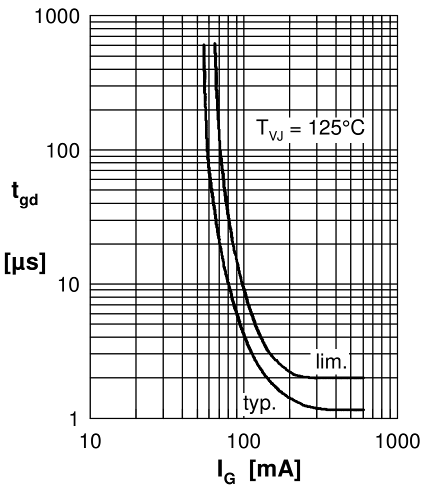


Fig. 5 Gate controlled delay time t_{gd}

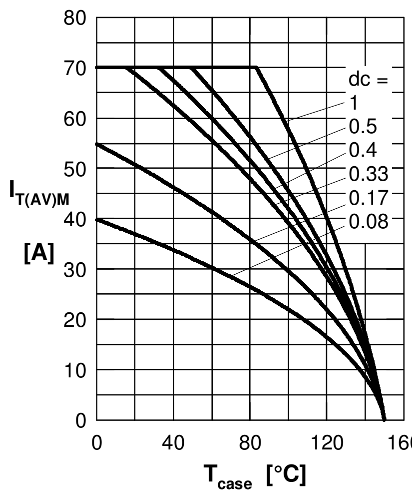


Fig. 6 Max. forward current at case temperature

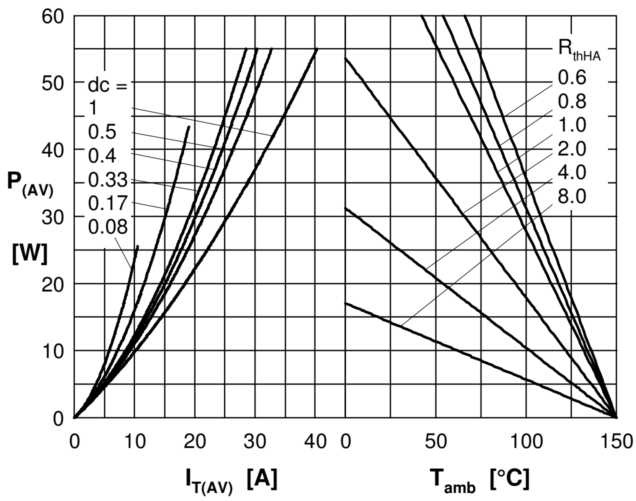
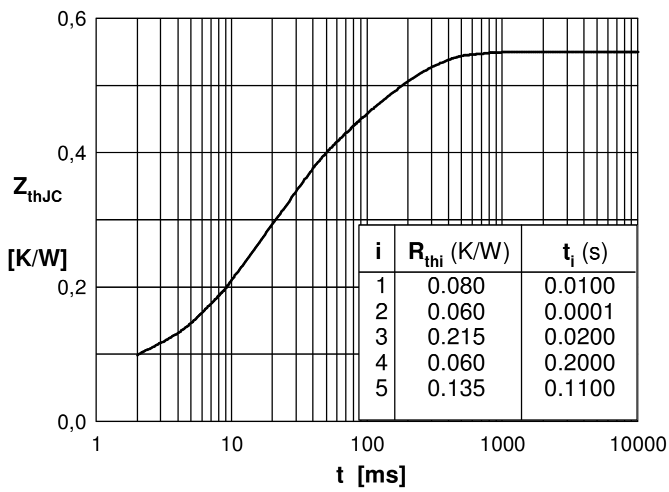


Fig. 7a Power dissipation versus direct output current
Fig. 7b and ambient temperature



i	R_{thi} (K/W)	t_i (s)
1	0.080	0.0100
2	0.060	0.0001
3	0.215	0.0200
4	0.060	0.2000
5	0.135	0.1100

Fig. 7 Transient thermal impedance junction to case