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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# CLRC663

## High performance multi-protocol NFC frontend CLRC663 and CLRC663 *plus*

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Product data sheet
COMPANY PUBLIC

## 1 General description

CLRC663, the high performance multi-protocol NFC frontend.

The CLRC663 multi-protocol NFC frontend IC supports the following operating modes

- Read/write mode supporting ISO/IEC 14443 type A and MIFARE Classic
- Read/write mode supporting ISO/IEC 14443B
- Read/write mode supporting JIS X 6319-4 (comparable with FeliCa[1] (see Section 20.5) scheme)
- Passive initiator mode according to ISO/IEC 18092
- Read/write mode supporting ISO/IEC 15693
- Read/write mode supporting ICODE EPC UID/ EPC OTP
- Read/write mode supporting ISO/IEC 18000-3 mode 3/ EPC Class-1 HF

The CLRC663's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A and MIFARE Cassic IC-based cards and transponders without additional active circuitry. The digital module manages the complete ISO/IEC 14443A framing and error detection functionality (parity and CRC).

The CLRC663 supports MIFARE Classic with 1 kB memory, MIFARE Classic with 4 kB memory, MIFARE Ultralight, MIFARE Ultralight C, MIFARE Plus and MIFARE DESFire products. The CLRC663 supports higher transfer speeds of the MIFARE product family of up to 848 kbit/s in both directions.

The CLRC663 supports layer 2 and 3 of the ISO/IEC 14443B reader/writer communication scheme except anticollision. The anticollision needs to be implemented in the firmware of the host controller as well as in the upper layers.

The CLRC663 is able to demodulate and decode FeliCa coded signals. The FeliCa receiver part provides the demodulation and decoding circuitry for FeliCa coded signals. The CLRC663 handles the FeliCa framing and error detection such as CRC. The CLRC663 supports FeliCa higher transfer speeds of up to 424 kbit/s in both directions.

The CLRC663 is supporting the P2P passive initiator mode in accordance with ISO/IEC 18092.

The CLRC663 supports the vicinity protocol according to ISO/IEC15693, EPC UID and ISO/IEC 18000-3 mode 3/ EPC Class-1 HF.

The following host interfaces are supported:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependent on pin voltage supply)
- $I^2C$-bus interface (two versions are implemented: I2C and I2CL)

The CLRC663 supports the connection of a secure access module (SAM). A dedicated separate I2C interface is implemented for a connection of the SAM. The SAM can be

1 In the following the word FeliCa is used for JIS X 6319-4

used for high secure key storage and acts as a very performant crypto-coprocessor. A dedicated SAM is available for connection to the CLRC663.

In this document the term „MIFARE Classic card“ refers to a MIFARE Classic IC-based contactless card.

## 2 Features and benefits

- Includes NXP ISO/IEC14443-A and Innovatron ISO/IEC14443-B intellectual property licensing rights
- High performance multi-protocol NFC frontend for transfer speed up to 848 kbit/s
- Supports ISO/IEC 14443 type A, MIFARE Classic, ISO/IEC 14443 B and FeliCa reader modes
- P2P passive initiator mode in accordance with ISO/IEC 18092
- Supports ISO/IEC15693, ICODE EPC UID and ISO/IEC 18000-3 mode 3/ EPC Class-1 HF
- Supports MIFARE Classic product encryption by hardware in read/write mode
  Allows reading cards based on MIFARE Ultralight, MIFARE Classic with 1 kB memory , MIFARE Classic with 4 kB memory, MIFARE DESFire EV1, MIFARE DESFire EV2 and MIFARE Plus ICs
- Low-Power Card Detection
- Compliance to EMV contactless protocol specification on RF level can be achieved
- Supported host interfaces:
  - SPI up to 10 Mbit/s
  - $I^2C$-bus interfaces up to 400 kBd in Fast mode, up to 1000 kBd in Fast mode plus
  - RS232 Serial UART up to 1228.8 kBd, with voltage levels dependent on pin voltage supply
- Separate $I^2C$-bus interface for connection of a secure access module (SAM)
- FIFO buffer with size of 512 bytes for highest transaction performance
- Flexible and efficient power-saving modes including hard power down, standby and low-power card detection
- Cost saving by integrated PLL to derive system clock from 27.12 MHz RF quartz crystal
- 3.0 V to 5.5 V power supply (CLRC66301, CLRC66302)
  2.5 V to 5.5 V power supply (CLRC66303)
- Up to 8 free programmable input/output pins
- Typical operating distance in read/write mode for communication to a ISO/IEC 14443 type A and MIFARE Classic card up to 12 cm, depending on the antenna size and tuning
  The version CLRC66303 offers a more flexible configuration for Low-Power Card detection compared to the CLRC66301 and CLRC66302 with the new register LPCD_OPTIONS. In addition, the CLRC66303 offers new additional settings for the Load Protocol which fit very well to smaller antennas. The CLRC66303 is therefore the recommended version for new designs.

# 3 Quick reference data

**Table 1. Quick reference data CLRC66301HN and CLRC66302HN**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | 3.0 | 5.0 | 5.5 | V |
| $V_{DD(PVDD)}$ | PVDD supply voltage | | [1] | 3.0 | 5.0 | $V_{DD}$ | V |
| $V_{DD(TVDD)}$ | TVDD supply voltage | | | 3.0 | 5.0 | 5.5 | V |
| $I_{pd}$ | power-down current | PDOWN pin pulled HIGH | [2] | - | 8 | 40 | nA |
| $I_{DD}$ | supply current | | | - | 17 | 20 | mA |
| $I_{DD(TVDD)}$ | TVDD supply current | | | - | 100 | 250 | mA |
| $T_{amb}$ | operating ambient temperature | | | -25 | +25 | +85 | °C |
| $T_{stg}$ | storage temperature | no supply voltage applied | | -55 | +25 | +125 | °C |

[1] VDD(PVDD) must always be the same or lower voltage than VDD.
[2] $I_{pd}$ is the sum of all supply currents

**Table 2. Quick reference data CLRC66303HN**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | 2.5 | 5.0 | 5.5 | V |
| $V_{DD(PVDD)}$ | PVDD supply voltage | | [1] | 2.5 | 5.0 | $V_{DD}$ | V |
| $V_{DD(TVDD)}$ | TVDD supply voltage | | | 2.5 | 5.0 | 5.5 | V |
| $I_{pd}$ | power-down current | PDOWN pin pulled HIGH | [2] | - | 8 | 40 | nA |
| $I_{DD}$ | supply current | | | - | 17 | 20 | mA |
| $I_{DD(TVDD)}$ | TVDD supply current | | | - | 180 | 350 | mA |
| | | absolute limiting value | | - | - | 500 | mA |
| $T_{amb}$ | operating ambient temperature | device mounted on PCB which allows sufficient heat dissipation | | -40 | +25 | +105 | °C |
| $T_{stg}$ | storage temperature | no supply voltage applied | | -55 | +25 | +125 | °C |

[1] VDD(PVDD) must always be the same or lower voltage than VDD.
[2] $I_{pd}$ is the sum of all supply currents

# 4 Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| CLRC66301HN/TRAYB[1] | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; MSL2, 32 terminals + 1 central ground; body 5 × 5 × 0.85 mm | SOT617-1 |
| CLRC66301HN/TRAYM[2] | | | |
| CLRC66302HN/TRAYB[1] | | plastic thermal enhanced very thin quad flat package; no leads; MSL1, 32 terminals + 1 central ground; body 5 × 5 × 0.85 mm | SOT617-1 |
| CLRC66302HN/TRAYBM[2] | | | |
| CLRC66302HN/T/R[3] | | | |
| CLRC66303HN/TRAYB[1] | | plastic thermal enhanced very thin quad flat package; no leads; MSL2, 32 terminals + 1 central ground; body 5 x 5 x 0.85 mm, wettable flanks | SOT617-1 |
| CLRC66303HN/T/R[3] | | | |

[1] Delivered in one tray, MOQ (Minimum order quantity) : 490 pcs
[2] Delivered in five trays; MOQ: 5x 490 pcs
[3] Delivered on reel with 6000 pieces; MOQ: 6000 pcs

# 5 Block diagram

The analog interface handles the modulation and demodulation of the antenna signals for the contactless interface.

The contactless UART manages the protocol dependency of the contactless interface settings managed by the host.

The FIFO buffer ensures fast and convenient data transfer between host and the contactless UART.

The register bank contains the settings for the analog and digital functionality.

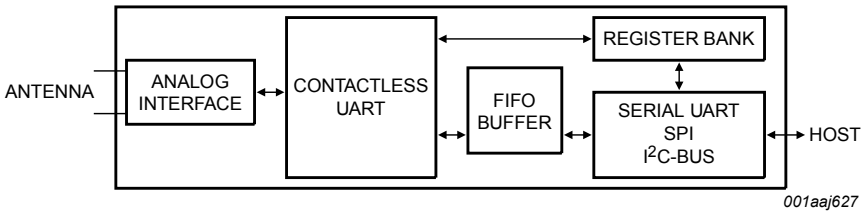
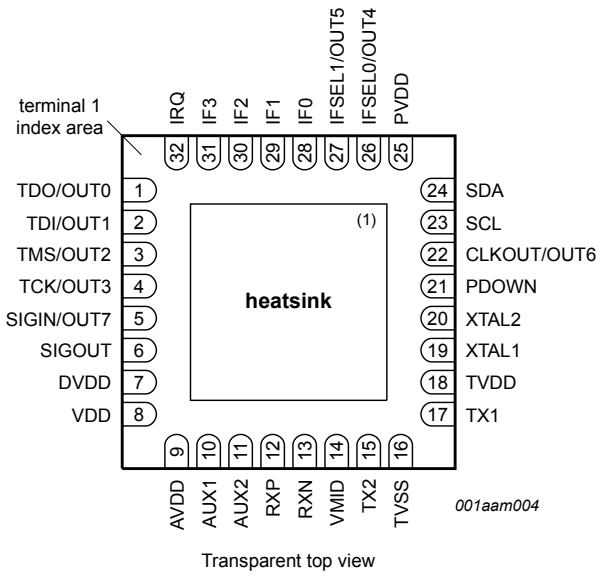



**Figure 1. Simplified block diagram of the CLRC663**

# 6 Pinning information




Transparent top view

1. VSS - heat sink connection

**Figure 2. Pinning configuration HVQFN32 (SOT617-1)**

## 6.1 Pin description

**Table 4. Pin description**

| Pin | Symbol | Type | Description |
|---|---|---|---|
| 1 | TDO / OUT0 | O | test data output for boundary scan interface / general purpose output 0 |
| 2 | TDI / OUT1 | I | test data input boundary scan interface / general purpose output 1 |
| 3 | TMS / OUT2 | I | test mode select boundary scan interface / general purpose output 2 |
| 4 | TCK / OUT3 | I | test clock boundary scan interface / general purpose output 3 |
| 5 | SIGIN /OUT7 | I | Contactless communication interface output. / general purpose output 7 |
| 6 | SIGOUT | O | Contactless communication interface input. |
| 7 | DVDD | PWR | digital power supply buffer [1] |
| 8 | VDD | PWR | power supply |
| 9 | AVDD | PWR | analog power supply buffer [1] |
| 10 | AUX1 | O | auxiliary outputs: Pin is used for analog test signal |
| 11 | AUX2 | O | auxiliary outputs: Pin is used for analog test signal |
| 12 | RXP | I | receiver input pin for the received RF signal. |
| 13 | RXN | I | receiver input pin for the received RF signal. |
| 14 | VMID | PWR | internal receiver reference voltage [1] |
| 15 | TX2 | O | transmitter 2: delivers the modulated 13.56 MHz carrier |
| 16 | TVSS | PWR | transmitter ground, supplies the output stage of TX1, TX2 |
| 17 | TX1 | O | transmitter 1: delivers the modulated 13.56 MHz carrier |

| Pin | Symbol | Type | Description |
|---|---|---|---|
| 18 | TVDD | PWR | transmitter voltage supply |
| 19 | XTAL1 | I | crystal oscillator input: Input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (fosc = 27.12 MHz) |
| 20 | XTAL2 | O | crystal oscillator output: output of the inverting amplifier of the oscillator |
| 21 | PDOWN | I | Power Down (RESET) |
| 22 | CLKOUT / OUT6 | O | clock output / general purpose output 6 |
| 23 | SCL | O | Serial Clock line |
| 24 | SDA | I/O | Serial Data Line |
| 25 | PVDD | PWR | pad power supply |
| 26 | IFSEL0 / OUT4 | I | host interface selection 0 / general purpose output 4 |
| 27 | IFSEL1 / OUT5 | I | host interface selection 1 / general purpose output 5 |
| 28 | IF0 | I/O | interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, $I^2C$, $I^2C$-L |
| 29 | IF1 | I/O | interface pin, multifunction pin: Can be assigned to host interface SPI, $I^2C$, $I^2C$-L |
| 30 | IF2 | I/O | interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, $I^2C$, $I^2C$-L |
| 31 | IF3 | I/O | interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, $I^2C$, $I^2C$-L |
| 32 | IRQ | O | interrupt request: output to signal an interrupt event |
| 33 | VSS | PWR | ground and heat sink connection |

[1] This pin is used for connection of a buffer capacitor. Connection of a supply voltage might damage the device.

# 7 Functional description

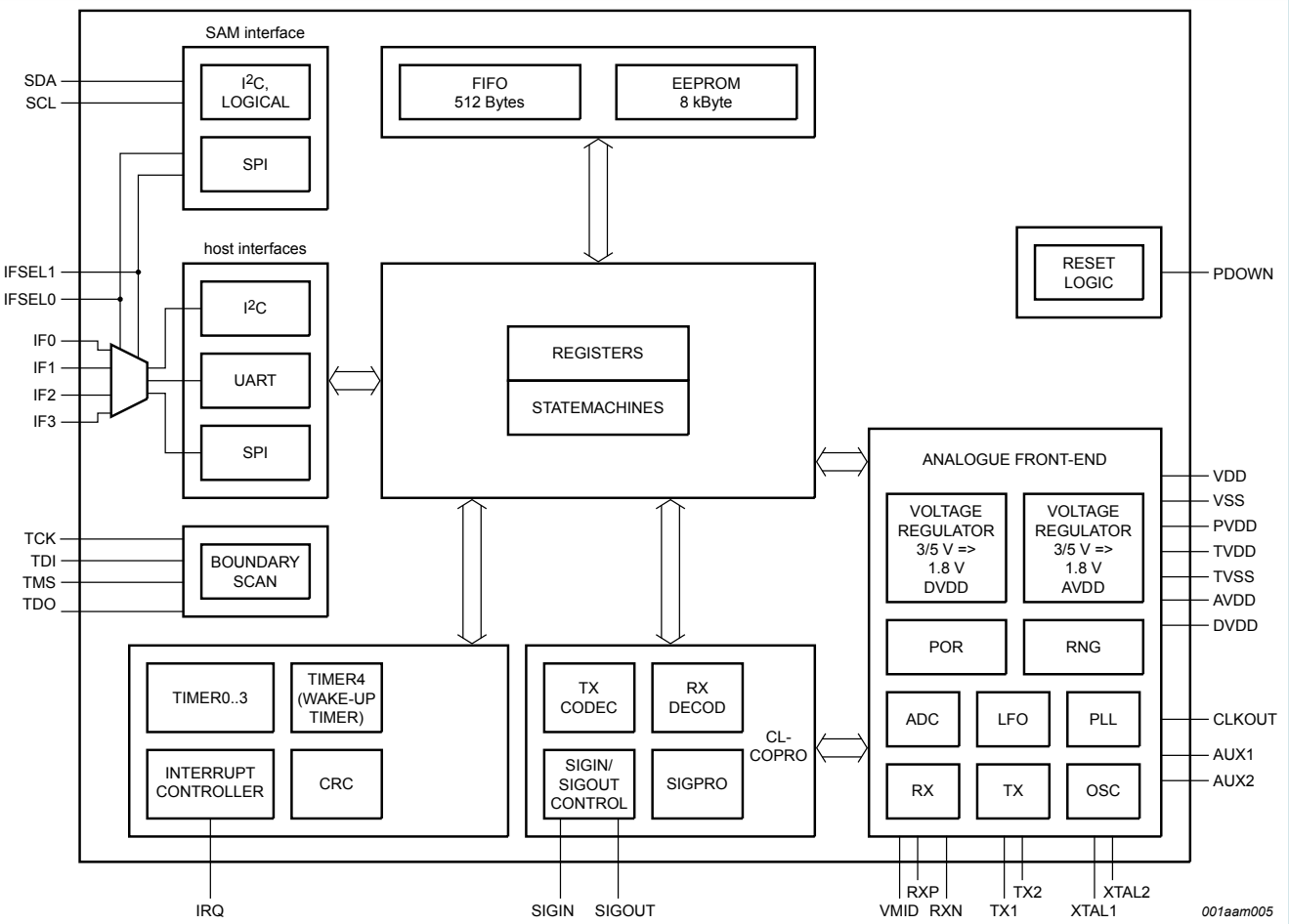



**Figure 3. Detailed block diagram of the CLRC663**

## 7.1 Interrupt controller

The interrupt controller handles the enabling/disabling of interrupt requests. All of the interrupts can be configured by firmware. Additionally, the firmware has possibilities to trigger interrupts or clear pending interrupt requests. Two 8-bit interrupt registers IRQ0 and IRQ1 are implemented, accompanied by two 8-bit interrupt enable registers IRQ0En and IRQ1En. A dedicated functionality of bit 7 to set and clear bits 0 to 6 in this interrupt controller register is implemented.

The CLRC663 indicates certain events by setting bit IRQ in the register Status1Reg and additionally, if activated, by pin IRQ. The signal on pin IRQ may be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

Table 4. shows the available interrupt bits, the corresponding source and the condition for its activation. The interrupt bits Timer0IRQ, Timer1IRQ, Timer2IRQ, Timer3OIRQ, in register IRQ1 indicate an interrupt set by the timer unit. The setting is done if the timer underflows.

The TxIRQ bit in register IRQ0 indicates that the transmission is finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit sets the interrupt bit automatically.

The bit RxIRQ in register IRQ0 indicates an interrupt when the end of the received data is detected.

The bit IdleIRQ in register IRQ0 is set if a command finishes and the content of the command register changes to idle.

The register WaterLevel defines both - minimum and maximum warning levels - counting from top and from bottom of the FIFO by a single value.

The bit HiAlertIRQ in register IRQ0 is set to logic 1 if the HiAlert bit is set to logic 1, that means the FIFO data number has reached the top level as configured by the register WaterLevel and bit WaterLevelExtBit.

The bit LoAlertIRQ in register IRQ0 is set to logic 1 if the LoAlert bit is set to logic 1, that means the FIFO data number has reached the bottom level as configured by the register WaterLevel.

The bit ErrIRQ in register IRQ0 indicates an error detected by the contactless UART during receive. This is indicated by any bit set to logic 1 in register Error.

The bit LPCDIRQ in register IRQ0 indicates a card detected.

The bit RxSOFIRQ in register IRQ0 indicates a detection of a SOF or a subcarrier by the contactless UART during receiving.

The bit GlobalIRQ in register IRQ1 indicates an interrupt occurring at any other interrupt source when enabled.

**Table 5. Interrupt sources**

| Interrupt bit | Interrupt source | Is set automatically, when |
|---|---|---|
| Timer0IRQ | Timer Unit | the timer register T0 CounterVal underflows |
| Timer1IRQ | Timer Unit | the timer register T1 CounterVal underflows |
| Timer2IRQ | Timer Unit | the timer register T2 CounterVal underflows |
| Timer3IRQ | Timer Unit | the timer register T3 CounterVal underflows |
| TxIRQ | Transmitter | a transmitted data stream ends |
| RxIRQ | Receiver | a received data stream ends |
| IdleIRQ | Command Register | a command execution finishes |
| HiAlertIRQ | FIFO-buffer pointer | the FIFO data number has reached the top level as configured by the register WaterLevel |
| LoAlertIRQ | FIFO-buffer pointer | the FIFO data number has reached the bottom level as configured by the register WaterLevel |
| ErrIRQ | contactless UART | a communication error had been detected |
| LPCDIRQ | LPCD | a card was detected when in low-power card detection mode |
| RxSOFIRQ | Receiver | detection of a SOF or a subcarrier |
| GlobalIRQ | all interrupt sources | will be set if another interrupt request source is set |

## 7.2 Timer module

Timer module overview

The CLRC663 implements five timers. Four timers -Timer0 to Timer3 - have an input clock that can be configured by register T(x)Control to be 13.56 MHz, 212 kHz, (derived from the 27.12 MHz quartz) or to be the underflow event of the fifth Timer (Timer4). Each timer implements a counter register which is 16 bit wide. A reload value for the counter is defined in a range of 0000h to FFFFh in the registers TxReloadHi and TxReloadLo. The fifth timer Timer4 is intended to be used as a wake-up timer and is connected to the internal LFO (Low Frequency Oscillator) as input clock source.

The TControl register allows the global start and stop of each of the four timers Timer0 to Timer3. Additionally, this register indicates if one of the timers is running or stopped. Each of the five timers implements an individual configuration register set defining timer reload value (e.g. T0ReloadHi,T0ReloadLo), the timer value (e.g. T0CounterValHi, T0CounterValLo) and the conditions which define start, stop and clockfrequency (e.g. T0Control).

The external host may use these timers to manage timing relevant tasks. The timer unit may be used in one of the following configurations:

- Time-out counter
- Watch-dog counter
- Stop watch
- Programmable one-shot timer
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event has occurred after an elapsed time. The timer register content is modified by the timer unit, which can be used to generate an interrupt to allow a host to react on this event.

The counter value of the timer is available in the registers T(x)CounterValHi, T(x)CounterValLo. The content of these registers is decremented at each timer clock.

If the counter value has reached a value of 0000h and the interrupts are enabled for this specific timer, an interrupt will be generated as soon as the next clock is received.

If enabled, the timer event can be indicated on the pin IRQ (interrupt request). The bit Timer(x)IRQ can be set and reset by the host controller. Depending on the configuration, the timer will stop counting at 0000h or restart with the value loaded from registers T(x)ReloadHi, T(x)ReloadLo.

The counting of the timer is indicated by bit TControl.T(x)Running.

The timer can be started by setting bits TControl.T(x)Running and TControl.T(x)StartStopNow or stopped by setting the bits TControl.T(x)StartStopNow and clearing TControl.T(x)Running.

Another possibility to start the timer is to set the bit T(x)Mode.T(x)Start. This can be useful if dedicated protocol requirements need to be fulfilled.

### 7.2.1 Timer modes

#### 7.2.1.1 Time-Out- and Watch-Dog-Counter

Having configured the timer by setting *register T(x)ReloadValue* and starting the counting of Timer(x) by setting bit TControl.T(x)StartStop and TControl.T(x)Running, the timer unit decrements the *T(x)CounterValue* Register beginning with the configured start event. If the configured stop event occurs before the Timer(x) underflows (e.g. a bit is received from the card), the timer unit stops (no interrupt is generated).

If no stop event occurs, the timer unit continues to decrement the counter registers until the content is zero and generates a timer interrupt request at the next clock cycle. This allows indicating to a host that the event did not occur during the configured time interval.

#### 7.2.1.2 Wake-up timer

The wake-up Timer4 allows to wake-up the system from standby after a predefined time. The system can be configured in such a way that it is entering the standby mode again in case no card had been detected.

This functionality can be used to implement a low-power card detection (LPCD). For the low-power card detection, it is recommended to set T4Control.T4AutoWakeUp and T4Control.T4AutoRestart, to activate the Timer4 and automatically set the system in standby. The internal low frequency oscillator (LFO) is then used as input clock for this Timer4. If a card is detected, the host-communication can be started. If bit T4Control.T4AutoWakeUp is not set, the CLRC663 will not enter the standby mode again in case no card is detected but stays fully powered.

#### 7.2.1.3 Stop watch

The elapsed time between a configured start- and stop event may be measured by the CLRC663 timer unit. By setting the registers *T(x)ReloadValueHi, T(x)reloadValueLo* the timer starts to decrement as soon as activated. If the configured stop event occurs, the timer stops decrementing. The elapsed time between start and stop event can then be calculated by the host dependent on the timer interval TTimer:

$$\Delta T = \left( Treload_{value} - Timer_{value} \right) * T_{Timer} \quad (1)$$

If an underflow occurred which can be identified by evaluating the corresponding IRQ bit, the performed time measurement according to the formula above is not correct.

#### 7.2.1.4 Programmable one-shot timer

The host configures the interrupt and the timer, starts the timer and waits for the interrupt event on pin IRQ. After the configured time, the interrupt request will be raised.

#### 7.2.1.5 Periodical trigger

If the bit *T(x)Control.T(x)AutoRestart is set and the interrupt is activated*, an interrupt request will be indicated periodically after every elapsed timer period.

## 7.3 Contactless interface unit

The contactless interface unit of the CLRC663 supports the following read/write operating modes:

- ISO/IEC14443A/MIFARE
- ISO/IEC14443B
- FeliCa
- ISO/IEC15693/ICODE
- ICODE EPC UID
- ISO/IEC 18000-3 mode 3/ EPC Class-1 HF

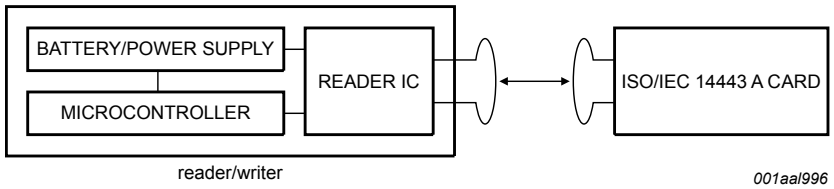
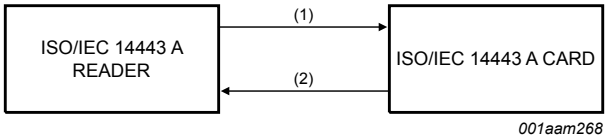



**Figure 4. Read/write mode**

A typical system using the CLRC663 is using a microcontroller to implement the higher levels of the contactless communication protocol and a power supply (battery or external supply).

### 7.3.1 Communication mode for ISO/IEC 14443 type A and for MIFARE Classic

The physical level of the communication is shown in the following figure:




1. Reader to Card 100 % ASK, Miller Coded, Transfer speed 106 kbit/s to 848 kbit/s
2. Card to Reader, Subcarrier Load Modulation Manchester Coded or BPSK, transfer speed 106 kbit/s to 848 kbit/s

**Figure 5. Read/write mode for ISO/IEC 14443 type A and read/write mode for MIFARE Classic**

The physical parameters are described in the following table:

**Table 6. Communication overview for ISO/IEC 14443 type A and read/write mode for MIFARE Classic**

| Communication direction | Signal type | Transfer speed | | | |
|---|---|---|---|---|---|
| | | 106 kbit/s | 212 kbit/s | 424 kbit/s | 848 kbit/s |
| Reader to card (send data from the CLRC663 to a card)<br>fc = 13.56 MHz | reader side modulation | 100 % ASK | 100% ASK | 100% ASK | 100% ASK |
| | bit encoding | modified Miller encoding | modified Miller encoding | modified Miller encoding | modified Miller encoding |
| | bit rate [kbit/s] | fc / 128 | fc / 64 | fc / 32 | fc / 16 |

| Communication direction | Signal type | Transfer speed | | | |
|---|---|---|---|---|---|
| | | 106 kbit/s | 212 kbit/s | 424 kbit/s | 848 kbit/s |
| Card to reader (CLRC663 receives data from a card) | card side modulation | subcarrier load modulation | subcarrier load modulation | subcarrier load modulation | subcarrier load modulation |
| | subcarrier frequency | fc / 16 | fc / 16 | fc / 16 | fc / 16 |
| | bit encoding | Manchester encoding | BPSK | BPSK | BPSK |

The CLRC663 connection to a host is required to manage the complete ISO/IEC 14443 type A and MIFARE Classic communication protocol. The following figure shows the data coding and framing according to ISO/IEC 14443 type A and MIFARE Classic..

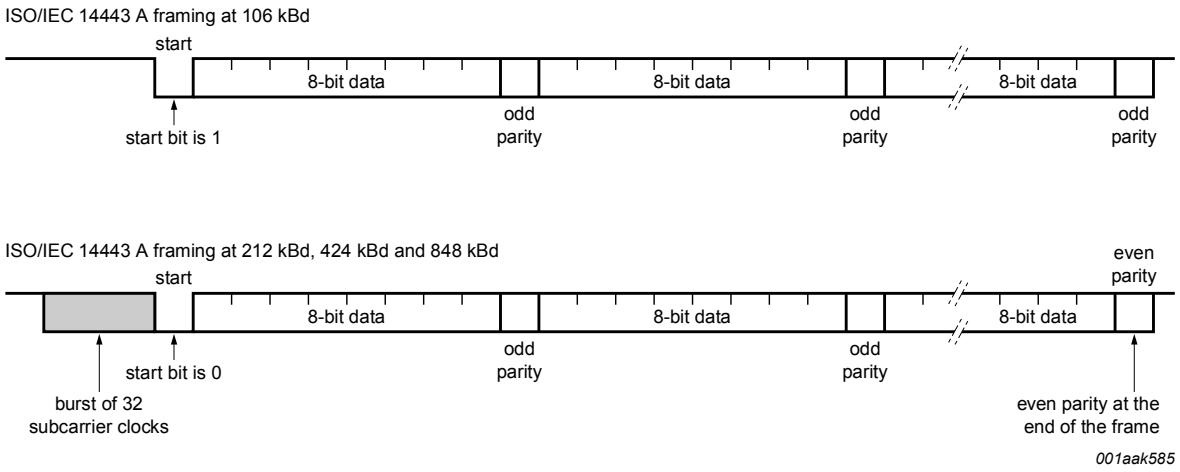
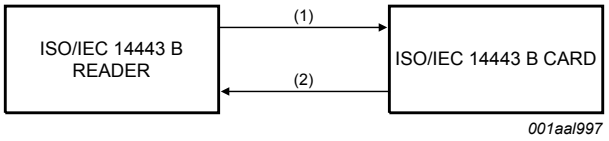



**Figure 6. Data coding and framing according to ISO/IEC 14443 A**

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally according to the transfer speed.

### 7.3.2 ISO/IEC14443 type B functionality

The physical level of the communication is shown in the following figure:




1. Reader to Card NRZ, Miller coded, transfer speed 106 kbit/s to 848 kbit/s
2. Card to reader, Subcarrier Load Modulation Manchester Coded or BPSK, transfer speed 106 kbit/s to 848 kbit/s

**Figure 7. ISO/IEC 14443 type B communication diagram**

The physical parameters are described in the following table:

**Table 7. Communication overview for ISO/IEC 14443 B reader/writer**

| Communication direction | Signal type | Transfer speed | | | |
|---|---|---|---|---|---|
| | | 106 kbit/s | 212 kbit/s | 424 kbit/s | 848 kbit/s |
| Reader to card (send data from the CLRC663 to a card) fc = 13.56 MHz | reader side modulation | 10 % ASK | 10 % ASK | 10 % ASK | 10 % ASK |
| | bit encoding | NRZ | NRZ | NRZ | NRZ |
| | bit rate [kbit/s] | 128 / fc | 64 / fc | 32 / fc | 16 / fc |
| Card to reader (CLRC663 receives data from a card) | card side modulation | subcarrier load modulation | subcarrier load modulation | subcarrier load modulation | subcarrier load modulation |
| | subcarrier frequency | fc / 16 | fc / 16 | fc / 16 | fc / 16 |
| | bit encoding | BPSK | BPSK | BPSK | BPSK |

The CLRC663 connected to a host is required to manage the complete ISO/IEC 14443 B protocol. The following figure shows the ISO/IEC 14443B SOF and EOF.

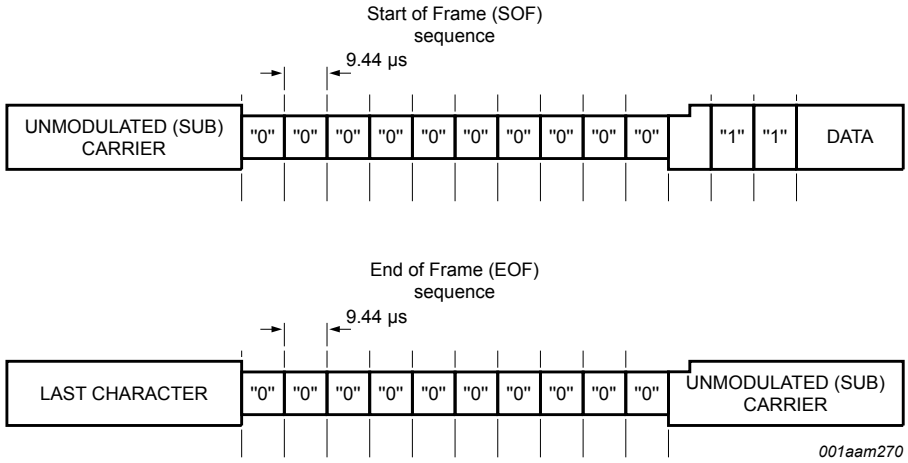



**Figure 8. SOF and EOF according to ISO/IEC 14443 B**

### 7.3.3 FeliCa functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The communication on a physical level is shown in the following figure:

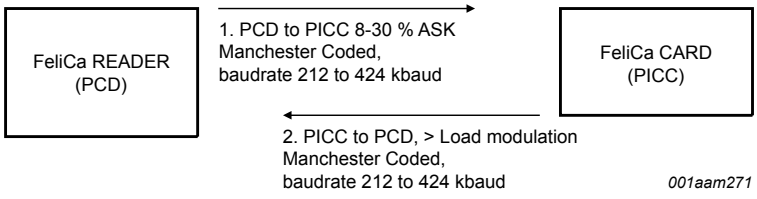



**Figure 9. FeliCa read/write communication diagram**

The physical parameters are described in the following table:

**Table 8. Communication overview for FeliCa reader/writer**

| Communication direction | Signal type | Transfer speed FeliCa | FeliCa higher transfer speeds |
|---|---|---|---|
| | | 212 kbit/s | 424 kbit/s |
| Reader to card (send data from the CLRC663 to a card)<br>fc = 13.56 MHz | reader side modulation | 8 % to 30 % ASK | 8 % to 30 % ASK |
| | bit encoding | Manchester encoding | Manchester encoding |
| | bit rate | fc/64 | fc/32 |
| Card to reader (CLRC663 receives data from a card) | card side load modulation | Load modulation | Load modulation |
| | bit encoding | Manchester encoding | Manchester encoding |

The CLRC663 needs to be connected to a dedicated host to be able to support the complete FeliCa protocol.

#### 7.3.3.1 FeliCa framing and coding

**Table 9. FeliCa framing and coding**

| Preamble (Hex.) | | | | | | Sync (Hex.) | | Len | n-Data | | | | CRC | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | 00 | 00 | 00 | 00 | 00 | B2 | 4D | | | | | | | |

To enable the FeliCa communication a 6 byte preamble (00h, 00h, 00h, 00h, 00h, 00h) and 2 bytes sync bytes (B2h, 4Dh) are sent to synchronize the receiver.

The following Len byte indicates the length of the sent data bytes plus the LEN byte itself.

The CRC calculation is done according to the FeliCa definitions with the MSB first.

To transmit data on the RF interface, the host controller has to send the Len- and data-bytes to the CLRC663's FIFO-buffer. The preamble and the sync bytes are generated by the CLRC663 automatically and must not be written to the FIFO by the host controller. The CLRC663 performs internally the CRC calculation and adds the result to the data frame.

### 7.3.4 ISO/IEC15693 functionality

The physical parameters are described in the following table:

**Table 10. Communication overview for ISO/IEC 15693 reader/writer reader to label**

| Communication direction | Signal type | Transfer speed | |
|---|---|---|---|
| | | fc / 8192 kbit/s | fc / 512 kbit/s |
| Reader to label (send data from the CLRC663 to a card) | reader side modulation | 10 % to 30 % ASK or 100 % ASK | 10 % to 30 % ASK 90 % to 100 % ASK |
| | bit encoding | 1/256 | 1/4 |
| | data rate | 1.66 kbit/s | 26.48 kbit/s |

**Table 11. Communication overview for ISO/IEC 15693 reader/writer label to reader**

| Communication direction | Signal type | Transfer speed | | | |
|---|---|---|---|---|---|
| | | 6.62 (6.67) kbit/s | 13.24 kbit/s[1] | 26.48 (26.69) kbit/s | 52.96 kbit/s |
| Label to reader (CLRC663 receives data from a card) fc = 13.56 MHz | card side modulation | not supported | not supported | single (dual) subcarrier load modulation ASK | single subcarrier load modulation ASK |
| | bit length (µs) | - | - | 37.76 (37.46) | 18.88 |
| | bit encoding | - | - | Manchester coding | Manchester coding |
| | subcarrier frequency [MHz] | - | - | fc / 32 (fc / 28) | fc / 32 |

[1] Fast inventory (page) read command only (ICODE proprietary command).

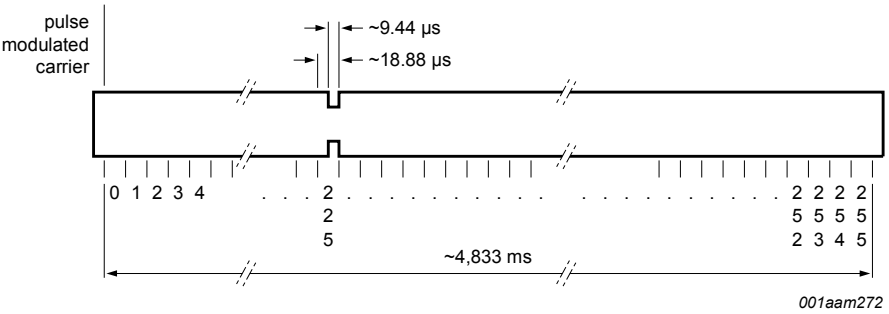



**Figure 10. Data coding according to ISO/IEC 15693. standard mode reader to label**

### 7.3.5 EPC-UID/UID-OTP functionality

The physical parameters are described in the following table:

**Table 12. Communication overview for EPC/UID**

| Communication direction | Signal type | Transfer speed | |
|---|---|---|---|
| | | 26.48 kbit/s | 52.96 kbit/s |
| Reader to card (send data from the CLRC663 to a card) | reader side modulation | 10 % to 30 % ASK | |
| | bit encoding | RTZ | |
| | bit length | 37.76 µs | |
| Card to reader (CLRC663 receives data from a card) | card side modulation | | single subcarrier load modulation |
| | bit length | | 18.88 µs |
| | bit encoding | | Manchester coding |

Data coding and framing according to EPC global 13.56 MHz ISM (industrial, scientific and medical) Band Class 1 Radio Frequency Identification Tag Interface Specification (Candidate Recommendation, Version 1.0.0).

### 7.3.6 ISO/IEC 18000-3 mode 3/ EPC Class-1 HF functionality

The ISO/IEC 18000-3 mode 3/ EPC Class-1 HF is not described in this document. For a detailed explanation of the protocol, refer to the ISO/IEC 18000-3 mode 3/ EPC Class-1 HF standard.

#### 7.3.6.1 Data encoding ICODE

The ICODE protocols have mainly three different methods of data encoding:

- "1" out of "4" coding scheme
- "1" out of "256" coding scheme
- "Return to Zero" (RZ) coding scheme

Data encoding for all three coding schemes is done by the ICODE generator.

The supported EPC Class-1 HF modes are:

- 2 pulse for 424 kbit subcarrier
- 4 pulse for 424 kbit subcarrier
- 2 pulse for 848 kbit subcarrier
- 4 pulse for 848 kbit subcarrier

### 7.3.7 ISO/IEC 18092 mode

The CLRC663 supports Passive Initiator Communication mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the ISO/IEC 18092 standard.

- Passive communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.
- Initiator: generates RF field at 13.56 MHz and starts the ISO/IEC 18092 communication.
- Target: responds to initiator command either in a load modulation scheme in Passive communication mode or using a self-generated and self-modulated RF field for Active Communication mode.

#### 7.3.7.1 Passive communication mode

Passive communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active meaning generating the RF field.

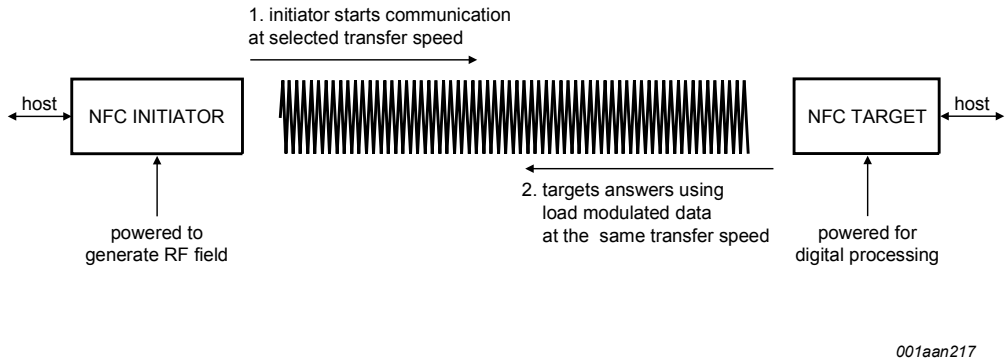



**Figure 11. Passive communication mode**

**Table 13. Communication overview for Passive communication mode**

| Communication direction | 106 kbit/s | 212 kbit/s | 424 kbit/s |
|---|---|---|---|
| Initiator → target | According to ISO/IEC 14443A<br>100 % ASK, Modified Miller Coded | According to FeliCa, 8 % to 30 % ASK Manchester Coded | |
| Target → initiator | According to ISO/IEC 14443A subcarrier load modulation, Manchester Coded | According to FeliCa, > 12 % ASK Manchester Coded | |

The contactless UART of CLRC663 and a dedicated host controller are required to handle the ISO/IEC 18092 passive initiator protocol.

#### 7.3.7.2 ISO/IEC 18092 framing and coding

The ISO/IEC 18092 framing and coding in Passive communication mode is defined in the ISO/IEC 18092 standard.

**Table 14. Framing and coding overview**

| Transfer speed | Framing and Coding |
|---|---|
| 106 kbit/s | According to the ISO/IEC 14443 type A and MIFARE scheme |
| 212 kbit/s | According to the FeliCa scheme |
| 424 kbit/s | According to the FeliCa scheme |

#### 7.3.7.3 ISO/IEC 18092 protocol support

The ISO/IEC 18092 protocol is not described in this document. For a detailed explanation of the protocol, refer to the ISO/IEC 18092 standard.

## 7.4 Host interfaces

### 7.4.1 Host interface configuration

The CLRC663 supports direct interfacing of various hosts as the SPI, $I^2C$, $I^2CL$ and serial UART interface type. The CLRC663 resets its interface and checks the current host interface type automatically having performed a power-up or resuming from power down. The CLRC663 identifies the host interface by the means of the logic levels on the control pins after the Cold Reset Phase. This is done by a combination of fixed pin connections.The following table shows the possible configurations defined by IFSEL1,IFSEL0:

**Table 15. Connection scheme for detecting the different interface types**

| Pin | Pin Symbol | UART | SPI | $I^2C$ | $I^2C$-L |
|---|---|---|---|---|---|
| 28 | IF0 | RX | MOSI | ADR1 | ADR1 |
| 29 | IF1 | n.c. | SCK | SCL | SCL |
| 30 | IF2 | TX | MISO | ADR2 | SDA |
| 31 | IF3 | PAD_VDD | NSS | SDA | ADR2 |
| 26 | IFSEL0 | VSS | VSS | PAD_VDD | PAD_VDD |
| 27 | IFSEL1 | VSS | PAD_VDD | VSS | PAD_VDD |

### 7.4.2 SPI interface

#### 7.4.2.1 General

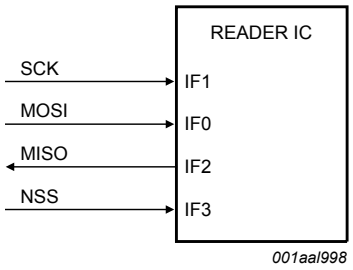



**Figure 12. Connection to host with SPI**

The CLRC663 acts as a slave during the SPI communication. The SPI clock SCK has to be generated by the master. Data communication from the master to the slave uses the Line MOSI. Line MISO is used to send data back from the CLRC663 to the master.

A serial peripheral interface (SPI compatible) is supported to enable high-speed communication to a host. The implemented SPI compatible interface is according to a standard SPI interface. The SPI compatible interface can handle data speed of up to 10 Mbit/s. In the communication with a host, CLRC663 acts as a slave receiving data from the external host for register settings and to send and receive data relevant for the communication on the RF interface.

NSS (Not Slave Select) enables or disables the SPI interface. When NSS is logical high, the interface is disabled and reset. Between every SPI command, the NSS must go to logical high to be able to start the next command read or write.

On both data lines (MOSI, MISO) each data byte is sent by MSB first. Data on MOSI line shall be stable on rising edge of the clock line (SCK) and is allowed to change on

falling edge. The same is valid for the MISO line. Data is provided by the CLRC663 on the falling edge and is stable on the rising edge.The polarity of the clock is low at SPI idle.

#### 7.4.2.2 Read data

To read out data from the CLRC663 by using the SPI compatible interface, the following byte order has to be used.

The first byte that is sent defines the mode (LSB bit) and the address.

**Table 16. Byte Order for MOSI and MISO**

| | byte 0 | byte 1 | byte 2 | byte 3 to n-1 | byte n | byte n+1 |
|---|---|---|---|---|---|---|
| MOSI | address 0 | address 1 | address 2 | …….. | address n | 00h |
| MISO | X | data 0 | data 1 | …….. | data n - 1 | data n |

**Remark:** The Most Significant Bit (MSB) has to be sent first.

#### 7.4.2.3 Write data

To write data to the CLRC663 using the SPI interface, the following byte order has to be used. It is possible to write more than one byte by sending a single address byte (see.8.5.2.4).

The first send byte defines both, the mode itself and the address byte.

**Table 17. Byte Order for MOSI and MISO**

| | byte 0 | byte 1 | byte 2 | 3 to n-1 | byte n | byte n + 1 |
|---|---|---|---|---|---|---|
| MOSI | address 0 | data 0 | data 1 | …….. | data n - 1 | data n |
| MISO | X | X | X | …….. | X | X |

**Remark:** The Most Significant Bit (MSB) has to be sent first.

#### 7.4.2.4 Address byte

The address byte has to fulfill the following format:

The LSB bit of the first byte defines the used mode. To read data from the CLRC663, the LSB bit is set to logic 1. To write data to the CLRC663, the LSB bit has to be cleared. The bits 6 to 0 define the address byte.

NOTE: When writing the sequence [address byte][data0][data1][data2]..., [data0] is written to address [address byte], [data1] is written to address [address byte + 1] and [data2] is written to [address byte + 2].

Exception: This auto increment of the address byte is not performed if data is written to the FIFO address

**Table 18. Address byte 0 register; address MOSI**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| address 6 | address 5 | address 4 | address 3 | address 2 | address 1 | address 0 | 1 (read)<br>0 (write) |
| MSB | | | | | | | LSB |

#### 7.4.2.5 Timing Specification SPI

The timing condition for SPI interface is as follows:

**Table 19. Timing conditions SPI**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SCKL}$ | SCK LOW time | 50 | - | - | ns |
| $t_{SCKH}$ | SCK HIGH time | 50 | - | - | ns |
| $t_{h(SCKH-D)}$ | SCK HIGH to data input hold time | 25 | - | - | ns |
| $t_{su(D-SCKH)}$ | data input to SCK HIGH set-up time | 25 | - | - | ns |
| $t_{h(SCKL-Q)}$ | SCK LOW to data output hold time | - | - | 25 | ns |
| $t_{(SCKL-NSSH)}$ | SCK LOW to NSS HIGH time | 0 | - | - | ns |
| $t_{NSSH}$ | NSS HIGH time | 50 | - | - | ns |

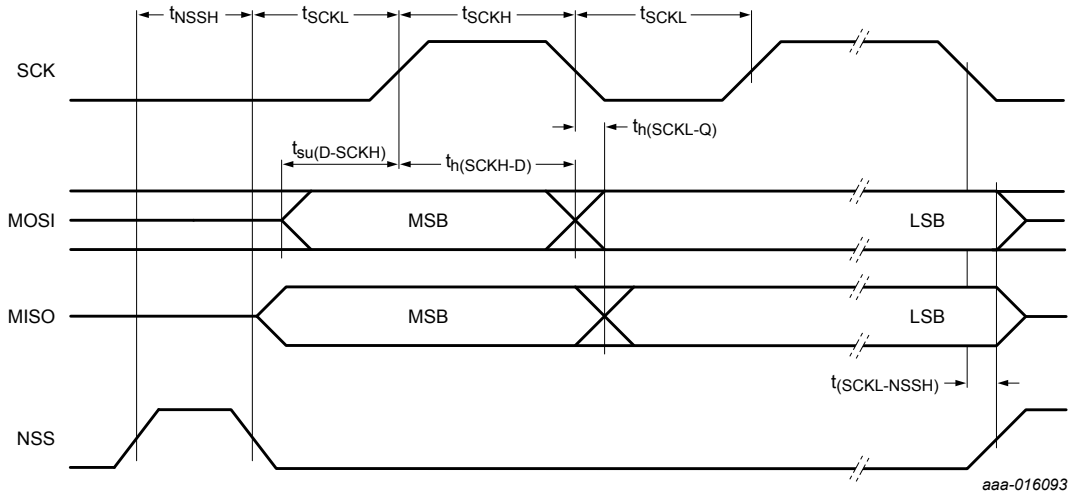



**Figure 13. Connection to host with SPI**

**Remark:** To send more bytes in one data stream, the NSS signal must be LOW during the send process. To send more than one data stream, the NSS signal must be HIGH between each data stream.

### 7.4.3 RS232 interface

#### 7.4.3.1 Selection of the transfer speeds

The internal UART interface is compatible to an RS232 serial interface. The levels supplied to the pins are between VSS and PVDD. To achieve full compatibility of the voltage levels to the RS232 specification, an RS232 level shifter is required.

Table 21 describes examples for different transfer speeds and relevant register settings. The resulting transfer speed error is less than 1.5 % for all described transfer speeds. The default transfer speed is 115.2 kbit/s.

To change the transfer speed, the host controller has to write a value for the new transfer speed to the register SerialSpeedReg. The bits BR_T0 and BR_T1 define factors to set the transfer speed in the SerialSpeedReg.

Table 20 describes the settings of BR_T0 and BR_T1.

**Table 20. Settings of BR_T0 and BR_T1**

| BR_T0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| factor BR_T0 | 1 | 1 | 2 | 4 | 8 | 16 | 32 | 64 |
| range BR_T1 | 1 to 32 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 |

**Table 21. Selectable transfer speeds**

| Transfer speed (kbit/s) | Serial SpeedReg (Hex.) | Transfer speed accuracy (%) |
|---|---|---|
| 7.2 | FA | -0.25 |
| 9.6 | EB | 0.32 |
| 14.4 | DA | -0.25 |
| 19.2 | CB | 0.32 |
| 38.4 | AB | 0.32 |
| 57.6 | 9A | -0.25 |
| 115.2 | 7A | -0.25 |
| 128 | 74 | -0.06 |
| 230.4 | 5A | -0.25 |
| 460.8 | 3A | -0.25 |
| 921.6 | 1C | 1.45 |
| 1228.8 | 15 | 0.32 |

The selectable transfer speeds as shown are calculated according to the following formulas:

if BR_T0 = 0: transfer speed = 27.12 MHz / (BR_T1 + 1)
if BR_T0 > 0: transfer speed = 27.12 MHz / (BR_T1 + 33)/$2^{(BR\_T0 - 1)}$

**Remark:** Transfer speeds above 1228.8 kBits/s are not supported.

### 7.4.3.2 Framing

**Table 22. UART framing**

| Bit | Length | Value |
|---|---|---|
| Start bit (Sa) | 1 bit | 0 |
| Data bits | 8 bit | Data |
| Stop bit (So) | 1 bit | 1 |

**Remark:** For data and address bytes, the LSB bit has to be sent first. No parity bit is used during transmission.

**Read data:** To read out data using the UART interface, the flow described below has to be used. The first send byte defines both the mode itself and the address. The Trigger on pin IF3 has to be set, otherwise no read of data is possible.

**Table 23. Byte Order to Read Data**

| Mode | byte 0 | byte 1 |
|---|---|---|
| RX | address | - |
| TX | - | data 0 |

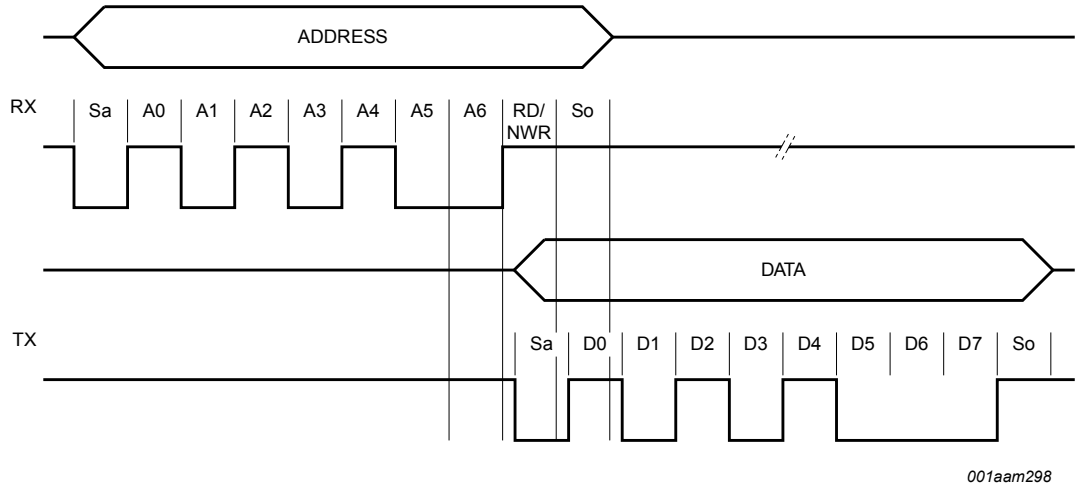



**Figure 14. Example for UART Read**

**Write data:**

To write data to the CLRC663 using the UART interface, the following sequence has to be used.

The first send byte defines both, the mode itself and the address.

**Table 24. Byte Order to Write Data**

| Mode | byte 0 | byte 1 |
|---|---|---|
| RX | address 0 | data 0 |
| TX | | address 0 |

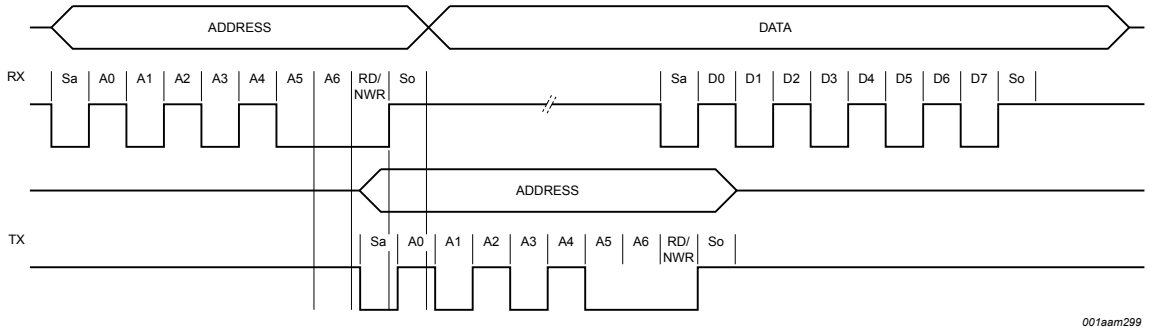



**Figure 15. Example diagram for a UART write**

**Remark:** Data can be sent before address is received.

## 7.4.4 I²C-bus interface

### 7.4.4.1 General

An Inter IC ($I^2C$) bus interface is supported to enable a low cost, low pin count serial bus interface to the host. The implemented $I^2C$ interface is mainly implemented according to the NXP Semiconductors $I^2C$ interface specification, rev. 3.0, June 2007. The CLRC663 can act as a slave receiver or slave transmitter in standard mode, fast mode and fast mode plus.

The following features defined by the NXP Semiconductors $I^2C$ interface specification, rev. 3.0, June 2007 are not supported:

- The CLRC663 I2C interface does not stretch the clock
- The CLRC663 I2C interface does not support the general call. This means that the CLRC663 does not support a software reset
- The CLRC663 does not support the I2C device ID
- The implemented interface can only act in slave mode. Therefore no clock generation and access arbitration is implemented in the CLRC663.
- High-speed mode is not supported by the CLRC663

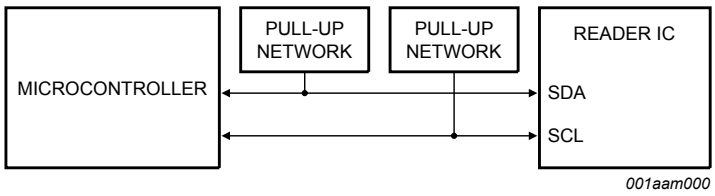



**Figure 16. $I^2C$-bus interface**

The voltage level on the I2C pins is not allowed to be higher than PVDD.

SDA is a bidirectional line, connected to a positive supply voltage via a pull-up resistor. Both lines SDA and SCL are set to HIGH level if no data is transmitted. Data on the $I^2C$-bus can be transferred at data rates of up to 400 kbit/s in fast mode, up to 1 Mbit/s in the fast mode+.

If the $I^2C$ interface is selected, a spike suppression according to the $I^2C$ interface specification on SCL and SDA is automatically activated.