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# CM1216

## 6 and 8-Channel Low Capacitance ESD Arrays

### Product Description

The CM1216 family of diode arrays provide sESD protection for electronic components or sub-systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive ( $V_P$ ) or negative ( $V_N$ ) supply rail. The CM1216 protects against ESD pulses up to  $\pm 15$  kV per the IEC 61000-4-2 standard.

This device is particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

### Features

- Six and Eight Channels of ESD Protection
- Provides  $\pm 15$  kV ESD Protection on Each Channel per the IEC 61000-4-2 ESD Requirements
- Channel Loading Capacitance of 1.6 pF Typical
- Channel I/O to GND Capacitance Difference of 0.04 pF Typical
- Mutual Capacitance of 0.13 pF Typical
- Minimal Capacitance Change with Temperature and Voltage
- Each I/O Pin Can Withstand Over 1000 ESD Strikes
- SOIC and MSOP Packages
- These Devices are Pb-Free and are RoHS Compliant

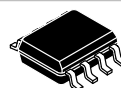
### Applications

- IEEE1394 Firewire® Ports at 400 Mbps / 800 Mbps
- DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays
- Serial ATA Ports in Desktop PCs and Hard Disk Drives
- PCI Express Ports
- General Purpose High-Speed Data Line ESD Protection

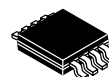


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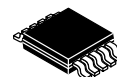
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**SOIC-8**  
**SM SUFFIX**  
**CASE 751AC**

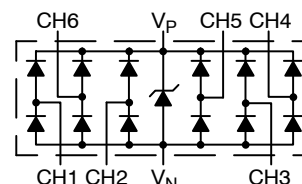


**MSOP-8**  
**MR SUFFIX**  
**CASE 846AD**

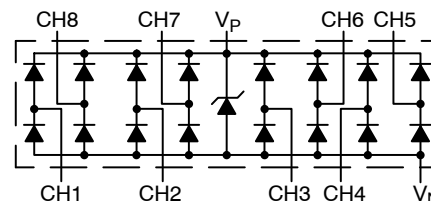


**MSOP-10**  
**MR SUFFIX**  
**CASE 846AE**

### BLOCK DIAGRAM

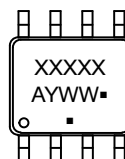


CM1216-06SM  
CM1216-06MR



CM1216-08MR

### MARKING DIAGRAM



XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

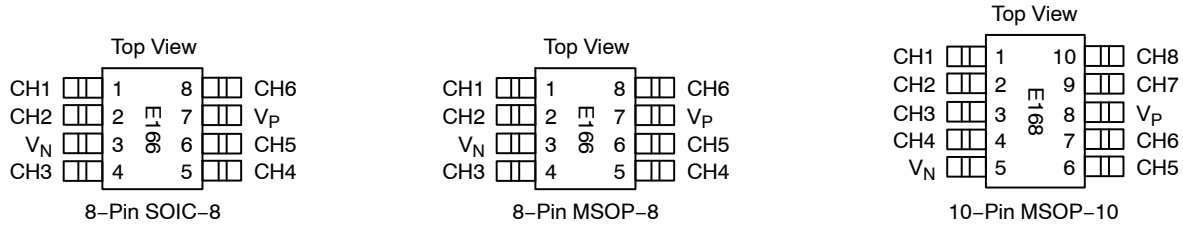
### ORDERING INFORMATION

Device	Package	Shipping†
CM1216-06SM	SOIC (Pb-Free)	2500/Tape & Reel
CM1216-06MR	MSOP (Pb-Free)	4000/Tape & Reel
CM1216-08MR	MSOP (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# CM1216

## PACKAGE / PINOUT DIAGRAMS



**Table 1. PIN DESCRIPTIONS**

Pin Name	MSOP-8	SOIC-8	MSOP-10	Type	Description
	Pin No.	Pin No.	Pin No.		
CH1	1	1	1	I/O	ESD Channel
CH2	2	2	2	I/O	ESD Channel
CH3	4	4	3	I/O	ESD Channel
CH4	5	5	4	I/O	ESD Channel
$V_N$	3	3	5	GND	Negative voltage supply rail
CH5	6	6	6	I/O	ESD Channel
CH6	8	8	7	I/O	ESD Channel
$V_P$	7	7	8	PWR	Positive voltage supply rail
CH7	–	–	9	I/O	ESD Channel
CH8	–	–	10	I/O	ESD Channel

## SPECIFICATIONS

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameter	Rating	Units
Operating Supply Voltage ( $V_P$ – $V_N$ )	6	V
Diode Forward DC Current	20	$\mu$ A
DC Voltage at any Channel Input	( $V_N$ –0.5) to ( $V_P$ +0.5)	V
Operating Temperature Range Ambient Junction	–40 to +85 –40 to +125	$^{\circ}$ C
Storage Temperature Range	–40 to +150	$^{\circ}$ C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. STANDARD OPERATING CONDITIONS**

Parameter	Rating	Units
Temperature Range (Ambient)	–40 to +85	$^{\circ}$ C
Package Power Rating MSOP8 Package (CM1216–06MR) SOIC8 Package (CM1216–06SM) MSOP10 Package (CM1216–08MR)	400 600 400	mW

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_P$	Operating Supply Voltage ( $V_P - V_N$ )			3.3	5.5	V
$I_P$	Operating Supply Current	$(V_P - V_N) = 3.3$ V			8	$\mu$ A
$V_F$	Diode Forward Voltage Top Diode Bottom Diode	$I_F = 20$ $\mu$ A; $T_A = 25^\circ$ C	0.6 0.6	0.8 0.8	0.95 0.95	V
$I_{LEAK}$	Channel Leakage Current	$T_A = 25^\circ$ C; $V_P = 5$ V, $V_N = 0$ V		$\pm 0.1$	$\pm 1.0$	$\mu$ A
$C_{IN}$	Channel Input Capacitance	At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V (Note 2)		1.6	2.0	pF
$\Delta C_{IN}$	Channel Input Capacitance Matching			0.04		pF
$C_{MUTUAL}$	Mutual Capacitance	$(V_P - V_N) = 3.3$ V		0.13		pF
$V_{ESD}$	ESD Protection Peak Discharge Voltage at any channel input, in system, contact discharge per IEC 61000-4-2 standard	$T_A = 25^\circ$ C (Notes 2 and 3)	$\pm 15$			kV
$V_{CL}$	Channel Clamp Voltage Positive Transients Negative Transients	$I_{PP} = 1$ A, $t_P = 8/20$ $\mu$ S; $T_A = 25^\circ$ C		+9.0 -1.5		V
$R_{DYN}$	Dynamic Resistance Positive transients Negative transients	$I_{PP} = 1$ A, $t_P = 8/20$ $\mu$ S; $T_A = 25^\circ$ C		0.6 0.4		$\Omega$

1. All parameters specified at  $T_A = -40^\circ$ C to  $+85^\circ$ C unless otherwise noted.
2. Standard IEC 61000-4-2 with  $C_{Discharge} = 150$  pF,  $R_{Discharge} = 330$   $\Omega$ ,  $V_P = 3.3$  V,  $V_N$  grounded.
3. From I/O pins to  $V_P$  or  $V_N$  only.  $V_P$  bypassed to  $V_N$  with low ESR 0.2  $\mu$ F ceramic capacitor.

## PERFORMANCE CHARACTERISTICS

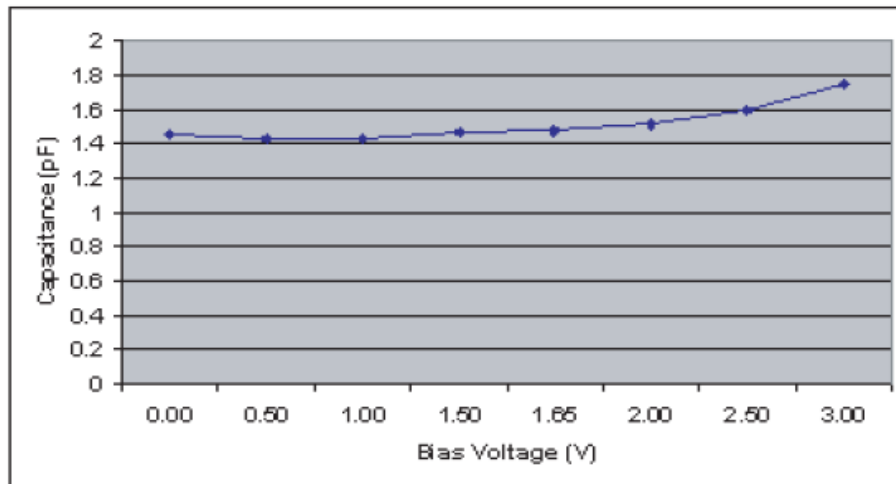


Figure 1. Typical Variation of  $C_{IN}$  vs.  $V_{IN}$   
( $f = 1$  MHz,  $V_P = 3.3$  V,  $V_N = 0$  V, 0.1  $\mu$ F Chip Capacitor between  $V_P$  and  $V_N$ ,  $T_A = 25^\circ$ C)

## APPLICATION INFORMATION

## Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Application of Positive ESD Pulse between Input Channel and Ground, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by  $L_1$  and  $L_2$ . The voltage  $V_{CL}$  on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{\text{SUPPLY}} + L_1 \times d(I_{\text{ESD}}) / dt + L_2 \times d(I_{\text{ESD}}) / dt$$

where  $I_{\text{ESD}}$  is the ESD current pulse, and  $V_{\text{SUPPLY}}$  is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1 ns. Here  $d(I_{\text{ESD}})/dt$  can be approximated by  $\Delta I_{\text{ESD}}/\Delta t$ , or  $30/(1 \times 10^{-9})$ . So just 10 nH of series inductance ( $L_1$  and  $L_2$  combined) will lead to a 300 V increment in  $V_{CL}$ !

Similarly for negative ESD pulses, parasitic series inductance from the  $V_N$  pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1213 has an integrated Zener diode between  $V_P$  and  $V_N$ . This greatly reduces the effect of supply rail inductance  $L_2$  on  $V_{CL}$  by clamping  $V_P$  at the breakdown voltage of the Zener diode. However, for the lowest possible  $V_{CL}$ , especially when  $V_P$  is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22  $\mu\text{F}$  ceramic chip capacitor be connected between  $V_P$  and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the  $V_P$  pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

## Additional Information

See also ON Semiconductor Application Note, “Design Considerations for ESD Protection”, in the Applications section.

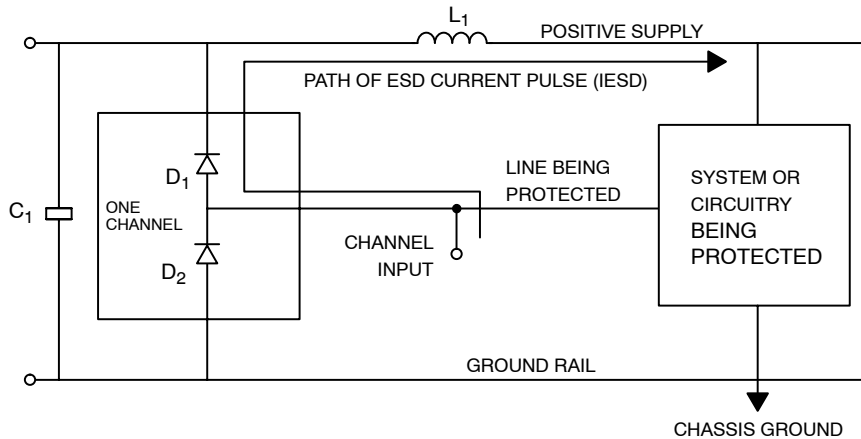
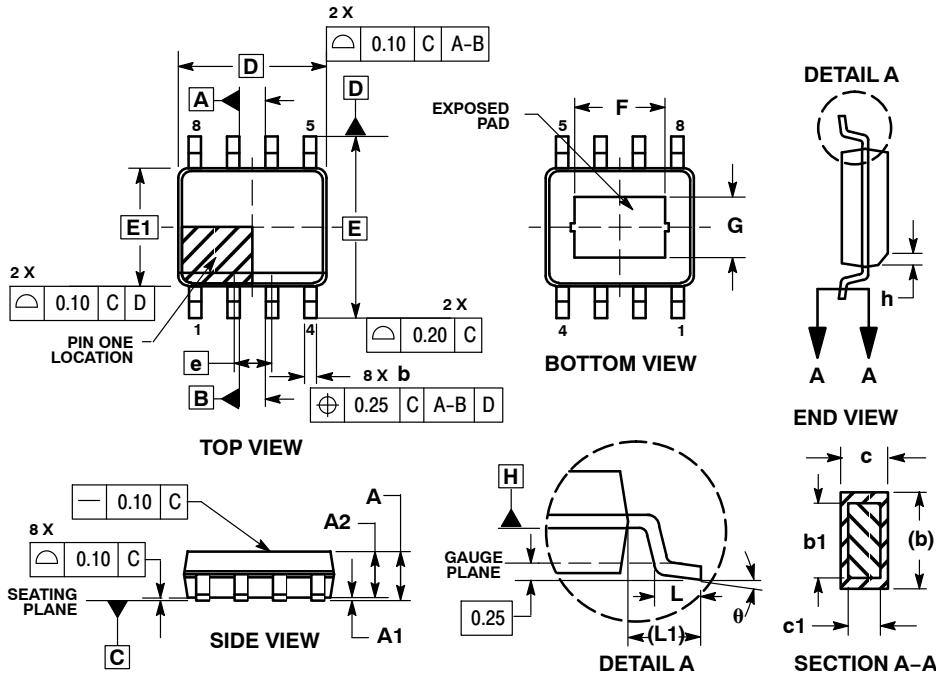


Figure 2. Application of Positive ESD Pulse between Input Channel and Ground

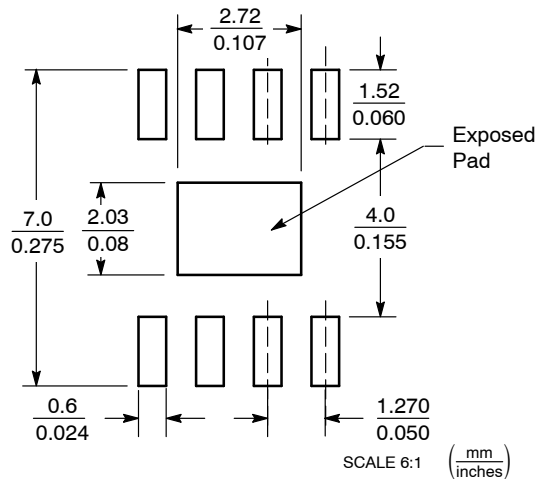
# CM1216

## PACKAGE DIMENSIONS

### SOIC-8 EP CASE 751AC-01 ISSUE B



### SOLDERING FOOTPRINT\*



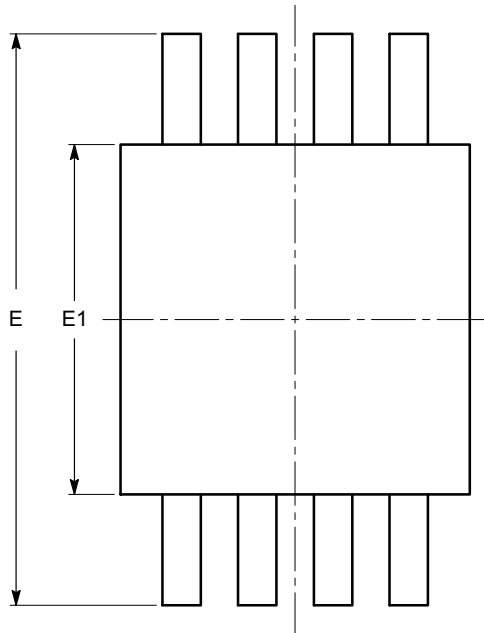
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



# CM1216

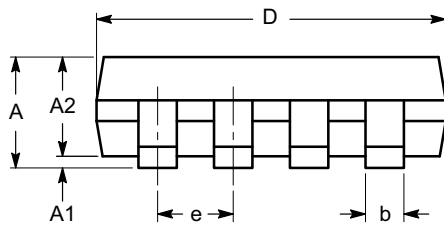
## PACKAGE DIMENSIONS

**MSOP 8, 3x3**  
CASE 846AD-01  
ISSUE O

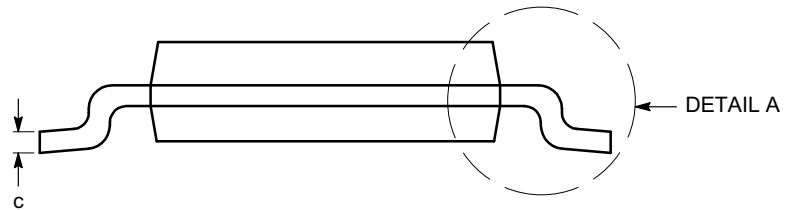


TOP VIEW

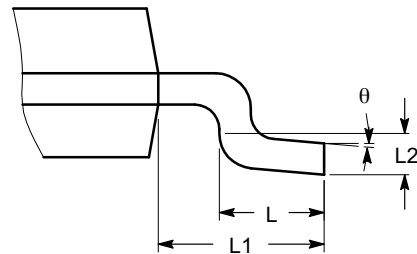
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
$\theta$	0°		6°



SIDE VIEW



END VIEW



DETAIL A

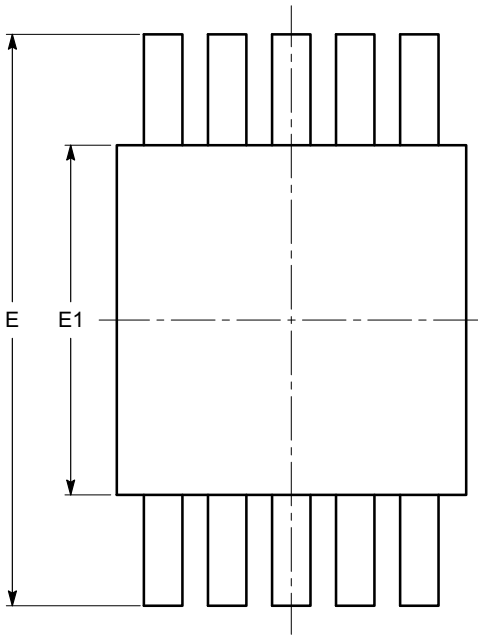
### Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-187.

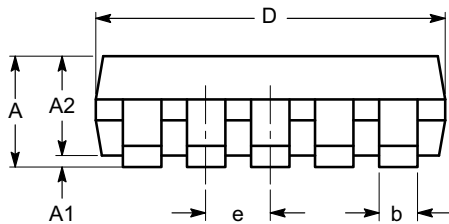
# CM1216

## PACKAGE DIMENSIONS

MSOP 10, 3x3  
CASE 846AE-01  
ISSUE O

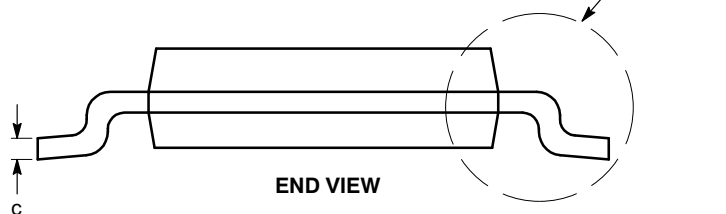


TOP VIEW

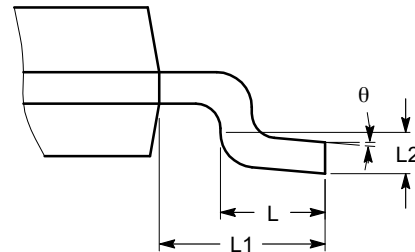


SIDE VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.00	0.05	0.15
A2	0.75	0.85	0.95
b	0.17		0.27
c	0.13		0.23
D	2.90	3.00	3.10
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
e	0.50 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°		8°



END VIEW



DETAIL A

### Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-187.

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