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Dual Input SmartOR™ Power Switch

Features

- Implements logical "Input V_{CC1} OR Input V_{CC2}"
- Integrated low impedance switches (0.2Ω TYP)
- Operating supply range from 2.8V to 5.5V
- Provides up to 600mA output current
- Glitch-free output during supply switching transitions
- Low operating supply current of 20µA (TYP)
- User-selectable hysteresis for supply selection
- 8-pin MSOP package
- RoHS compliant (lead-free) finishing

Applications

- PCI cards for Wake-On-LAN/Wake-On-Ring
- Dual power systems
- Systems with standby capabilities
- Battery backup systems
- See also Application Note AP-211
- USB enabled mobile electronics such as MP3 Players, PDAs, Digital Cameras and Wireless Handsets

Product Description

California Micro Devices' SmartOR™ CMPWR025 is a dual input power switch that selects between two different power inputs and delivers it to one output. The device integrates two very low impedance power switches and automatically implements an OR function that selects the higher of the two inputs. Hysteresis is built in (and is user selectable) to prevent switch chatter.

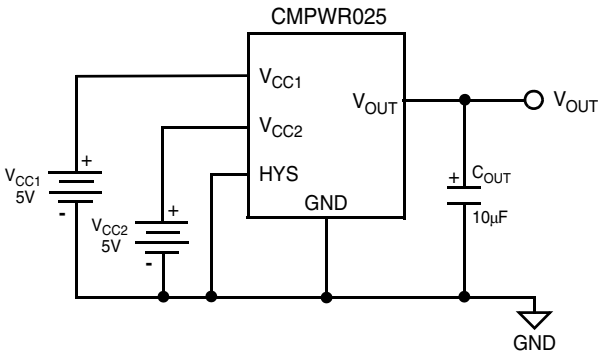
The CMPWR025 is a much-improved solution over simply ORing two diodes, due to the greatly reduced losses of the CMPWR025 when compared to low forward drop Schottky diodes.

The CMPWR025 is designed to operate above the 1W (375mA at 3.3V) sleep mode rating stated in the PCI Rev 2.2 spec. In fact the CMPWR025 current rating is dependent upon the power dissipation resulting from the voltage drop across the internal switch elements. See the Typical DC Characteristics section in this data sheet for details.

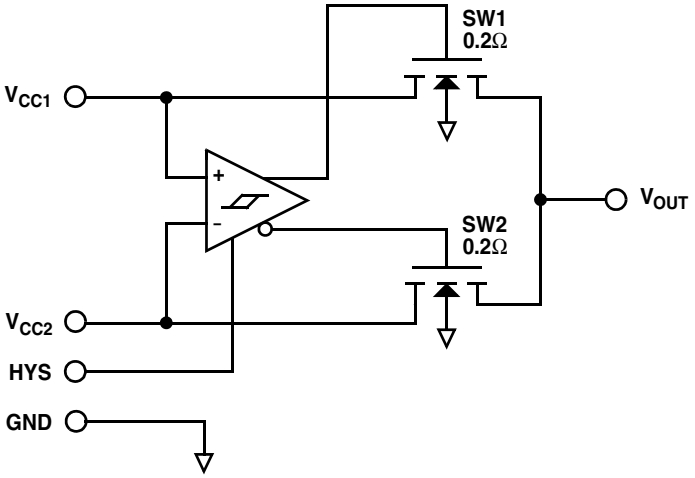
For IAPC (Instantly Available Personal Computer) applications see CMD Application Note AP-211 "Instantly Available PCI Card Power Management".

The CMPWR025 is housed in a 8-lead MSOP package and is available with RoHS compliant lead-free finishing.

Typical Application Circuit

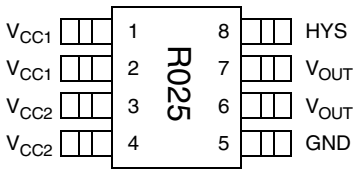


Simplified Electrical Schematic



PACKAGE / PINOUT DIAGRAM

Top View



8-pin MSOP
CMPWR025R

Note: This drawing is not to scale.

PIN DESCRIPTIONS

PIN(S)	NAME	DESCRIPTION
1,2	V_{CC1}	V_{CC1} is the primary power source, which is given priority when present. If pin 8 (HYS) is unconnected, then the hysteresis level is 75mV (typ.). Whenever the primary power source drops below the secondary supply V_{CC2} by more than 125mV, it will immediately become deselected. When the primary power source is restored to within 50mV of the secondary supply, the primary power source will once again be selected and provide all the output current. When V_{CC1} is selected, it will supply all the internal current requirements which are typically 20µA. When V_{CC1} is not selected, there will be no current loading on this input. **Pins 1 & 2 must be connected together externally.**
3,4	V_{CC2}	V_{CC2} is the secondary power source and is selected when the primary source has fallen below it by more than 125mV (or 200mV if pin 8 is grounded). The secondary source will be deselected immediately once the primary source is restored to within 50mV of V_{CC2} . When V_{CC2} is selected, it will supply all the internal current requirements which are typically 20µA. When V_{CC2} is not selected, there will be no current loading on this input. **Pins 3 & 4 must be connected together externally.**
5	GND	Negative reference for all voltages.
6,7	V_{OUT}	Positive voltage output switched from V_{CC1} or V_{CC2} inputs. During normal operation the impedance from V_{OUT} to the selected supply is typically less than 0.28Ω which results in minimal voltage loss from input to output. During the cold-start interval when both inputs are initially applied, the internal circuitry provides a soft turn-on for the switches, which limits peak in-rush current. **Pins 6 & 7 must be connected together externally.**
8	HYS	HYS is the user-selectable hysteresis input. The hysteresis level is set to 150mV when pin 8 is grounded. The default hysteresis level is set to 75mV by leaving pin 8 unconnected. Using 150mV hysteresis is recommended, especially in environments with noisy power supplies, high power supply resistances or high load currents. If the hysteresis level is set to 150mV, the primary supply V_{CC1} must now fall 200mV below the secondary supply V_{CC2} before it becomes deselected.

Ordering Information

PART NUMBERING INFORMATION

Regulator	Pins	Package	Ordering Part Number[1]	Part Marking
CMPWR025	8	MSOP	CMPWR025R	R025

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
ESD Protection (HBM)	±2000	V
Pin Voltages V_{CC1} V_{CC2}	 [GND - 0.5] to [+6.0] [GND - 0.5] to [+6.0]	 V V
Maximum DC Output Current	750	mA
Storage Temperature Range	-65 to +150	°C
Operating Temperature Range Ambient Junction	 -20 to +70 -20 to +125	 °C °C
Power Dissipation	0.3	W

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
V_{CC1} and V_{CC2} Input Voltage	2.8 to 5.5	V
Ambient Operating Temperature Range	0 to +70	°C
I_{LOAD}	0 to 600	mA

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{CCDES1}	V_{CC1} Deselect	V_{CC1} deselect level below V_{CC2}; HYS input (Pin 8) floating	50	125	200	mV
V_{CCDES2}	V_{CC2} Deselect 2	V_{CC1} deselect level below V_{CC2}; HYS input (Pin 8) grounded	90	200	300	mV
V_{CC1SEL}	V_{CC1} Select Preference		10	50	100	mV
	Hysteresis					
V_{HYS1}	V_{CC1SEL}-V_{CC1DES}	HYS input (Pin 8) floating; Note 2	40	75	100	mV
V_{HYS2}	V_{CC1SEL}-V_{CC1DES}	HYS input (Pin 8) grounded; Note 2	80	150	200	mV
t_{DL}	Switching Delay	$V_{CC1,2}$ falltime < 100ns; Note 3		200		ns
t_{DH}		$V_{CC1,2}$ risetime < 100ns; Note 3		200		ns
R_{SW}	Switch Resistance	I_{LOAD} = 0 to 600mA; $V_{CC1,2}$ = 2.8V; Note 4		0.28	0.4	Ω
		I_{LOAD} = 0 to 600mA; $V_{CC1,2}$ = 5.0V; Note 4		0.21	0.3	Ω
V_{SW}	Voltage Drop Across Switch ($V_{CC1,2}$ - V_{OUT})	I_{OUT} = 100mA; $V_{CC1,2}$ = 2.8V; Note 4		28	40	mV
		I_{OUT} = 200mA; $V_{CC1,2}$ = 2.8V; Note 4		56	80	mV
		I_{OUT} = 600mA; $V_{CC1,2}$ = 2.8V; Note 4		168	240	mV
		I_{OUT} = 100mA; $V_{CC1,2}$ = 5.0V; Note 4		21	30	mV
		I_{OUT} = 200mA; $V_{CC1,2}$ = 5.0V; Note 4		42	60	mV
		I_{OUT} = 600mA; $V_{CC1,2}$ = 5.0V; Note 4		125	180	mV
I_{RCC1}	Reverse Leakage	V_{CC1}=0V; V_{CC2} = 5.0V			100	µA
I_{RCC2}		V_{CC1}=5.0V; V_{CC2} = 0V			100	µA
I_{CC1}, I_{CC2}	Supply Current	When selected (I_{OUT} = 0)		20		µA
		When NOT selected		1		µA
I_{GND}	Ground Pin Current	V_{CC1} = V_{CC2} = 5.0V; I_{LOAD} = 0mA to 600mA		20	50	µA

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.

Note 2: Hysteresis level defines the maximum level of acceptable noise on V_{CC} during switching. Excessive parasitic inductance on V_{CC} board traces to the CMPWR025 may require an input capacitor to adequately filter the supply noise to below the hysteresis level. This will ensure that precise switching occurs between V_{CC1} and V_{CC2} supply inputs.

Note 3: This is the time, after the select/deselect threshold is reached, for the switches to react. Not tested, guaranteed by device design and characterization.

Note 4: Guaranteed by design and characterization.

Selection Threshold Diagrams

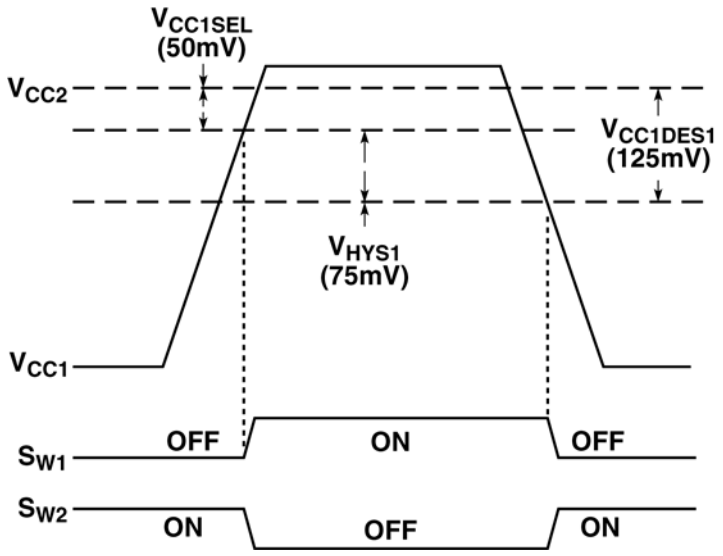


Figure 1. Supply Threshold Diagram
(Hysteresis input pin floating, see Typical Application Circuit, pg. 1)

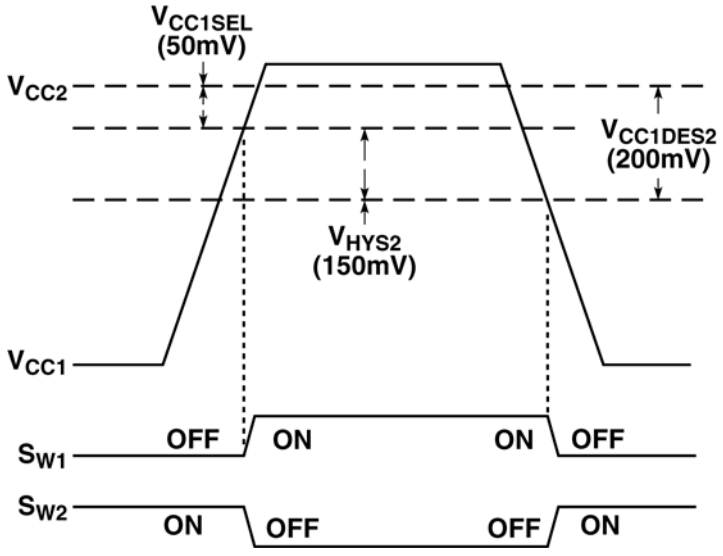


Figure 2. Supply Threshold Diagram
(Hysteresis input tied to GROUND, see Typical Application Circuit, pg. 1)

CMPWR025 Typical DC Characteristics

The **Switch Resistance vs. Temperature** curve shown in Figure 3 illustrates the switch resistance measured at 600mA load with V_{CC} equal to 3.3V and 5V. The resistance is shown at a temperatures range of -40°C to 70°C. When the temperature rises from 25° to 70°C, the switch resistance increases by about 20%.

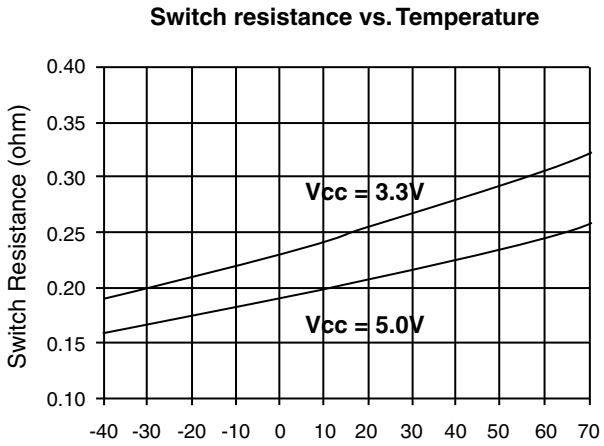


Figure 3. Switch Resistance vs. V_{CC} with Temperature

The **Supply Current vs. Temperature** curve shown in Figure 4 illustrates the internal supply current with V_{CC} equal to 3.3V and 5V. This current is drawn from the selected V_{CC} input, and is dissipated through the ground pin (pin 5). This current is independent of load current.

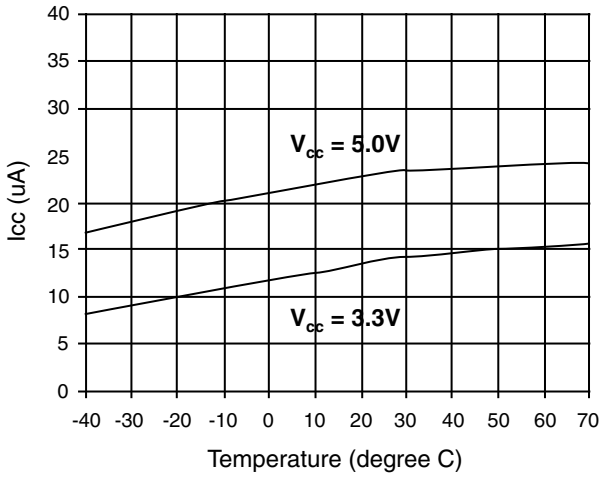


Figure 4. Supply Current vs. Temperature

The **Hysteresis Voltage vs. Temperature** curve shown in Figure 5 illustrates how the hysteresis voltages vary with temperature. '$V_{HYS}1$' is the hysteresis value if pin 8 is left unconnected, '$V_{HYS}2$' is the hysteresis value if pin 8 is connected to ground. '$V_{CC}1sel$' is the voltage below $V_{CC}2$ at which Vcc1 will be selected (refer to selection threshold diagrams on page 5). These three voltages are independent of the V_{CC} operating voltage.

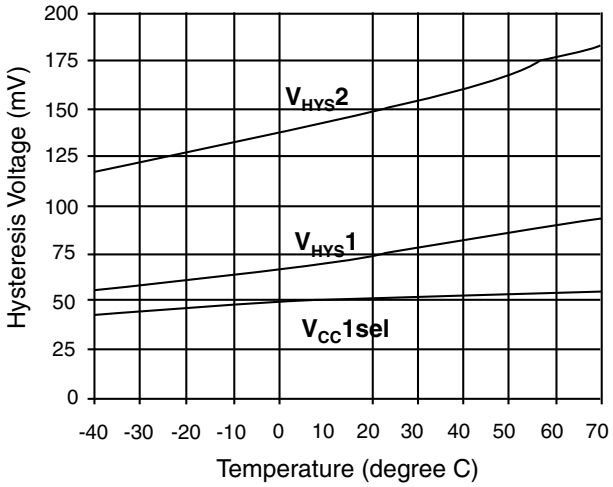


Figure 5. Hysteresis Voltage vs. Temperature

Power Dissipation and Output Current Considerations

The CMPWR025 is supplied in an MSOP package which has a maximum power dissipation rating of 0.3W. It is important that the heat generated within the part does not exceed this rating. The heat generated by the load current is given by:

$$P_{DISS} = V_{SW} \times I_{LOAD}$$

or

$$P_{DISS} = R_{SW} \times (I_{LOAD})^2$$

At a typical load of 375mA the P_{DISS} is just 0.4 x $(0.375)^2$ = 56mW.

Typical DC Characteristics (cont'd)

A primary consideration is Maximum Junction Temperature, $T_{J(max)}$, which can be calculated using the following formula:

$$T_{J(max)} = T_A + \theta_{JA} \times P_{DISS}$$

Where: T_A = The Ambient Temperature

θ_{JA} = Thermal Resistance = 100 °C/W

P_{DISS} = Power Dissipation

In the above example operating at an ambient of 70°C, $T_{J(max)}$ would be:

$$T_{J(max)} = 70°C + (0.056W)(100°C/W) = 75.6°C$$

Maximum power dissipation, including the power from the other circuitry within the device, suggests a current rating of approximately:

$$\sqrt{\frac{P_{DISS} - P_{INT}}{R_{SW}}} = I_{LOAD}$$

$$\sqrt{\frac{0.3W - 100\mu W}{0.4}} = 865mA$$

Note that this is beyond the maximum current rating of the device, which is 750mA maximum.

Typical Transient Characteristics

The circuit schematic in Figure 6 below shows the transient characterization test setup. It includes the power supply source impedances R_{S1} and R_{S2}, which represent the power supplies' output impedances and interconnection parasitics to the V_{CC1} and V_{CC2} input pins. In this test set-up, the series resistances on V_{CC1} and V_{CC2} are respectively R_{S1} = 0.16Ω and R_{S2} = 0.06Ω, unless specified otherwise. A load resistance R_L of 11Ω is used, setting a load current of about 450mA at 5V.

The hysteresis level is increased by connecting pin 8 to ground, which will improve the transient performance in noisy environments. In the transient analysis, the rise time and fall time of V_{CC1} is very long, in the 20msec range, providing a worst case situation.

Important note: The power supply source impedance must be as low as possible to avoid chatter during power transition. When operating in a high load and long rise time power-up condition, we recommend not exceeding a value of 0.15Ω on both source resistances.

$V_{HYS} > I (R_S + R_T)$

Where: V_{HYS} = The Minimum Hysteresis Voltage = 80mV

R_S = The Power Supply Output Impedance

R_T = The PCB Trace Impedance

For a rated load of 600mA, $R_S + R_T < 0.15\Omega$

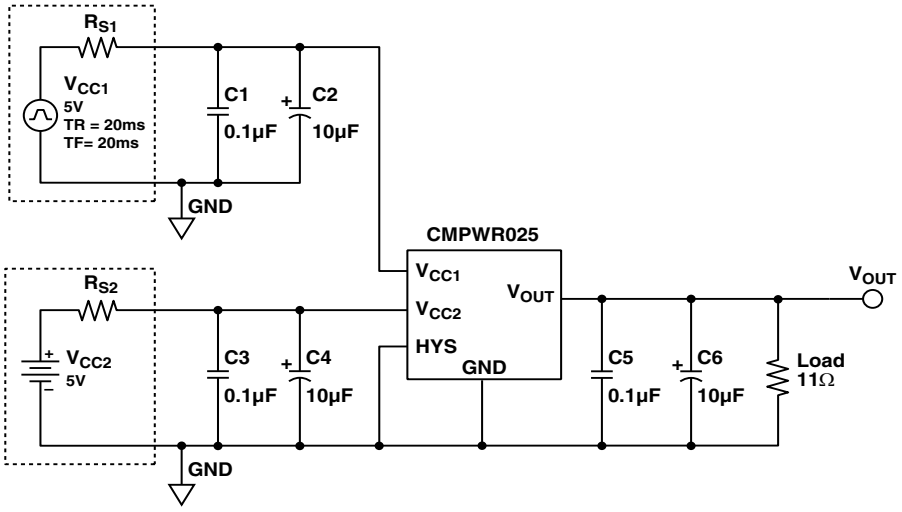


Figure 6. Transient Characterization Test Set-up

Typical DC Characteristics (cont'd)

Input and Output Capacitors

Filtering is typically unnecessary on the inputs, however power supply source impedance and parasitic resistance or inductance on the interconnections may result in chattering during the supply changeover. When an input is deselected and the input current drops to zero, the voltage at the input terminals will rise. If this voltage rise exceeds the hysteresis (75mV typical), the switch may chatter.

There are four ways to eliminate this chatter:

a) Connect pin 8 to GND to select 150mV hysteresis,

b) position the device as close as possible to the power supply connectors,

c) use low-impedance PCB traces, or

d) include low-ESR input bypass capacitors at the V_{CC1} and V_{CC2} input pins. Capacitors of 10µF or greater are recommended.

V_{OUT} provides the power for the load. To ensure the output is glitch-free during dynamic switching of the inputs, it is recommended that an external capacitor of 10µF or greater is included. This will restrict any transient output disturbances to less than 300mV at 600mA loading during dynamic switching of the inputs.

The test set-up used in Figure 7 and Figure 8 is described on page 7. The set-up for Figure 9 has larger series resistances on V_{CC1} and V_{CC2}.

V_{CC1} Rising from 0V to 5V/(V_{CC2} = 5V). Figure 7 shows the primary supply V_{CC1} becoming selected during a 0V to 5V transition. The secondary supply V_{CC2} is set to 5V DC. The channel 1 switch is turned on when V_{CC1} rises to within about 70mV of V_{CC2}. V_{CC1} drops when it is selected due to power supply source resistance R_{S1}. A positive glitch appears on V_{CC2} when channel 2 switch is turned off, due to power supply inductance. This has no effect on the output voltage.

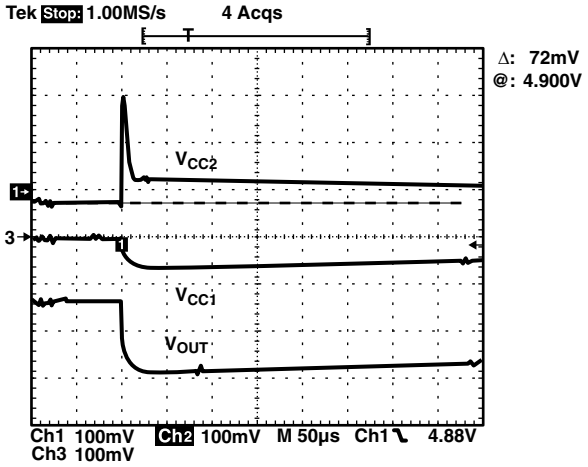


Figure 7. V_{CC1} rising from 0V to 5V, V_{CC2} = 5V. Ch1 and Ch2: V_{CC1} and V_{CC2}, offset = 5V. Ch3: V_{OUT} , offset = 5V.

V_{CC1} Falling from 5V to 0V (V_{CC2} = 5V). Figure 8 shows the primary supply V_{CC1} becoming deselected during a 5V to 0V transition. The test conditions are the same as in Figure 7. Channel 2 switch is turned on as soon as V_{CC2} and V_{CC1} are about 200mV. A negative glitch appears on V_{CC2}, when channel 2 is turned on. This has no effect on the output voltage.

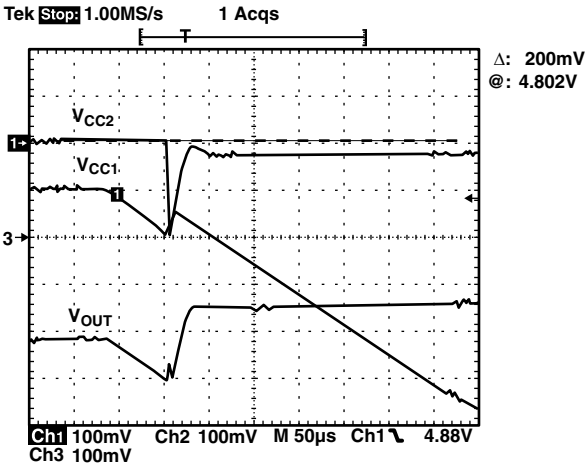


Figure 8. V_{CC1} falling from 0V to 5V (V_{CC2} = 5V). Ch1 and Ch2: V_{CC1} and V_{CC2}, offset = 5V. Ch3: V_{OUT} , offset = 5V.

Typical DC Characteristics (cont'd)

V_{CC1} Rising (V_{CC2} = 5V). Figure 9 is a bad test set-up that shows what may happen if either power supply source resistance R_{S1} or R_{S2} is too large. In this example, R_{S2} is increased to 0.3Ω

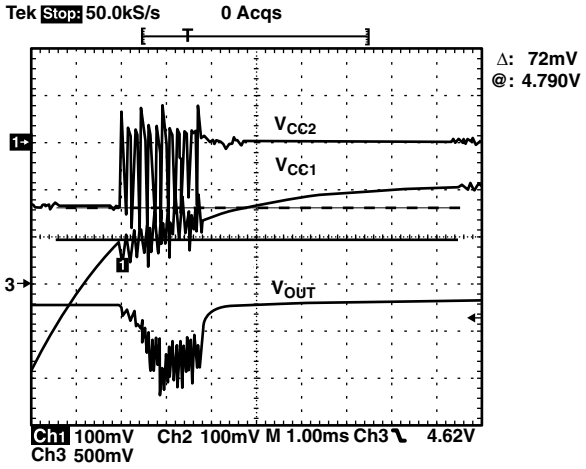


Figure 9. V_{CC1} Rising (V_{CC2}@ = 5V).
Ch1 and Ch2: V_{CC1} and V_{CC2}@, offset = 5V.
Ch3: V_{OUT}, offset = 3.3V.

The oscillation during the power transition is caused by the cumulative voltage change across R_{S1} and R_{S2} being greater than the hysteresis. The behavior is exacerbated by:

- a high load current,
- too many parasitics on power lines, and
- noisy power sources.

To avoid such behavior, the solution is to reduce the load or parasitic capacitance on power supply and lay-out, or use a more stable power supply.

Parallel Operation

Two CMPWR025 devices may be symmetrically ganged in parallel to increase total current capacity. Careful attention must be paid to minimizing series resistance and PCB parasitics during layout, both between the dual CMPWR025's inputs and also between the supplies and the devices, as described above.

In a well designed layout, a pair of CMPWR025's can provide an output approaching twice that of a single device.

See Application Note AP-211 for more information.

Mechanical Details

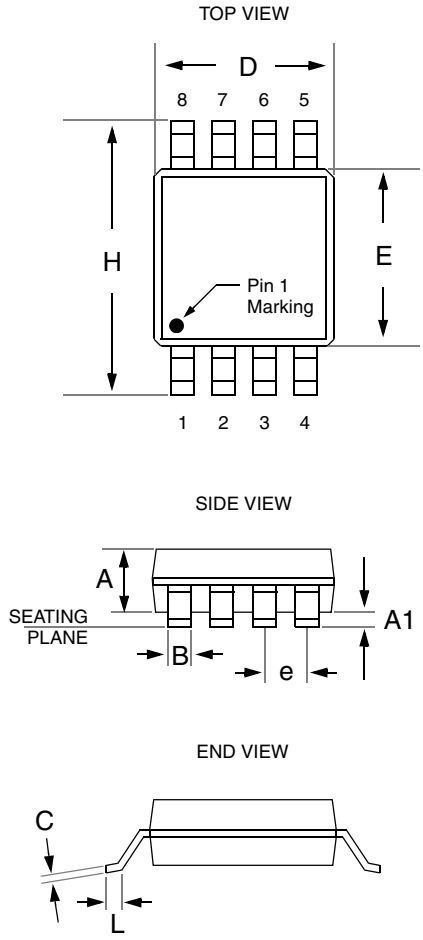
MSOP-8 Mechanical Specifications, 8 pin

The CMPWR025 is supplied in a 8-pin MSOP package. Dimensions are presented below.

For complete information on the MSOP-8, see the California Micro Devices MSOP Package Information document.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.75	0.95	0.030	0.037
A1	0.05	0.15	0.002	0.006
B	0.28	0.38	0.011	0.015
C	0.13	0.23	0.005	0.009
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.65 BSC		0.026 BSC	
H	4.90 BSC		0.193 BSC	
L	0.40	0.70	0.016	0.028
# per tape and reel	4000 pieces			
Controlling dimension: millimeters				

Mechanical Package Diagrams



Dimensions for MSOP-8 Package