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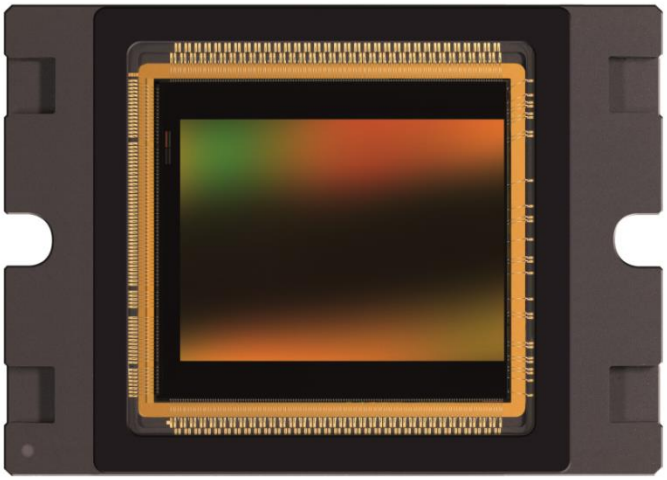
12 Megapixel machine vision CMOS image sensor

Datasheet



Change record

Issue	Date	Modification
v2.0	10/9/2013	Origination Splitting up the datasheets for v1 (300MHz) and v2 (600MHz) devices.
V2.1	20/01/2014	Removed: - High-grade variant from ordering info as all devices are now high grade. Updated: - Supply settings - Figures 21, 23 - Title of 4.3 - References Added: - Chapter 5.13: Power Control
V2.2	14/02/2014	Updated: - Frame rate formula (ch 3.6) of XY-subsampling (frame rate x2) - Frame rate overview (ch 3.6) - Additional required register settings (ch 5.17) - Offset register values (ch 5.14.1)
V2.3	13/03/2014	Removed: - Preliminary annotations Updated: - Figure 54: Color binning, pixel to output remapping - Exposure time calculation and FOT overlap Added: - ADC range multipliers for slow clock speeds - ADC range vs. clock speed plot
V2.4	04/07/2014	Updated: - VDD18 peak current → 1.7A - ADC_range vs. clock speed for 8bit - Minimum exposure times - Temperature sensor description - Power consumption 2.2W → 4.2W Added: - Typical LVDS output skew (Figure 35) - Self-heating
V2.5	08/08/2014	Updated: - Temperature sensor formulas now using the CLK_IN frequency. - Digital gain; more detailed - ADC range vs. clock speed charts - Recommended ADC range setting for 8bit to 205 (matches 10b/12b more closely) - Register 110: Set to 12368 - Register 112: Set to 227 - Additional required registers in 5.17 (increase fps and IQ for binning and XY-subsampling, decrease FOT and min. exposure time, less variation in settings) Added: - Reg 107[14:7] vs. clock speed

Issue	Date	Modification
V2.6	22/08/2014	Updated: - Reg 83, 113, 114 for 10bit normal mode (ch 5.17.3) - Reg 112 = 277
V2.7	18/12/2014	Updated: - Figures for multiple slopes. The figures are also correct when using only 1 knee point. - Temperature sensor offset in DN instead of °C/DN - Register 102 to 8302 to decrease column FPN Added: - Tilt and rotation of die in assembly drawing - SPI I/O's pulled low when not used/enabled. - QE and part number of NIR device
V2.8	10/02/2015	Updated: - Binning sums the pixels in the analog domain - In binning mode, only PGA /3 is useable - Changed registers 82, 84, 85, 86, 113, 114 in 5.17.4 for 12b normal mode when using 32 channels per side to increase the useable swing. Maximum frame rate decreases from 140 to 132 fps.
V2.9	04/03/2015	Added: - Internal PLL Updated: - Connect pins C5 & D6 to ground (see also AN10) - Reg98 35852 → 36364 for 12b Subsampling in X and Y mode in chapter 5.17.4.
2.10	27/10/2015	Removed: - Internal PLL because of instability (see also ES01)
2.11	15/03/2016	Updated: - Window size limitations depending on mode - Pins E4, F4, G3, H4: connect to ground - ADC range example - CLK_IN optional, only for temp. sensor - Reflow solder profile - Test Pattern for 8b mode - Register 99: 34952 → 34956 Added: - MSL3 rating - Excessive light caution
2.12	03/10/2016	Updated: - QE and SR plots - Dark current and DSNU figures - Typical slope temperature sensor units Added: - Test Pattern for 8b - Angular response - Package materials
2.13	13/02/2018	Added: - Mandatory dry bake; chapter 13.1

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Table of Contents

1 INTRODUCTION

1.1 OVERVIEW

The CMV12000 is a high speed CMOS image sensor with 4096 by 3072 pixels (22.5mm x 16.9mm) developed for machine vision and other applications. The image array consists of 5.5µm x 5.5µm pipelined global shutter pixels which allow exposure during read-out. The image sensor has 64 8-, 10- or 12-bit digital LVDS outputs (serial). The image sensor also integrates a programmable gain amplifier and offset regulation. Each channel runs at 600 Mbps which results in 132 fps frame rate at full resolution and 12-bit. When 10-bit per pixel is used, the frame rate increases to 300 fps. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read-out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes.

1.2 FEATURES

- 4096 * 3072 active pixels on a 5.5um pitch
- Frame rate 132 frames/sec in 12-bit mode
- Frame rate 300 frames/sec in 10-bit mode
- Frame rate 330 frames/sec in 8-bit mode
- Row windowing capability (up to 32 separate windows)
- X-Y mirroring function
- Master clock max 600 MHz
- 64 LVDS-outputs @ 600 Mbps multiplexable to 32, 16, 8 ,4 ,2 and 1 output(s) at reduced frame rate
- LVDS control line with frame and line information
- LVDS DDR output clock to sample data on the receiving end
- High Dynamic Range modes supported (multiple slope and dual exposure)
- On chip temperature sensor
- On chip timing generation
- SPI-control
- Ceramic µPGA package (237 pins)
- 3.3V signaling

1.3 SPECIFICATIONS

- Full well charge: 13.5 Ke^-
- Sensitivity: 4.64 V/lux.s (with microlenses)
- Dark noise: 13 e^-
- Conversion factor: 0.075 bit/e^-
- Dynamic range: 60 dB
- Parasitic light sensitivity: 1/50 000
- Dark current: 22 LSB/s
- Fixed pattern noise: <1 LSB (<0.1% of full swing in 10-bit mode)
- Power consumption: 4.2 W @ full speed

1.4 CONNECTION DIAGRAM

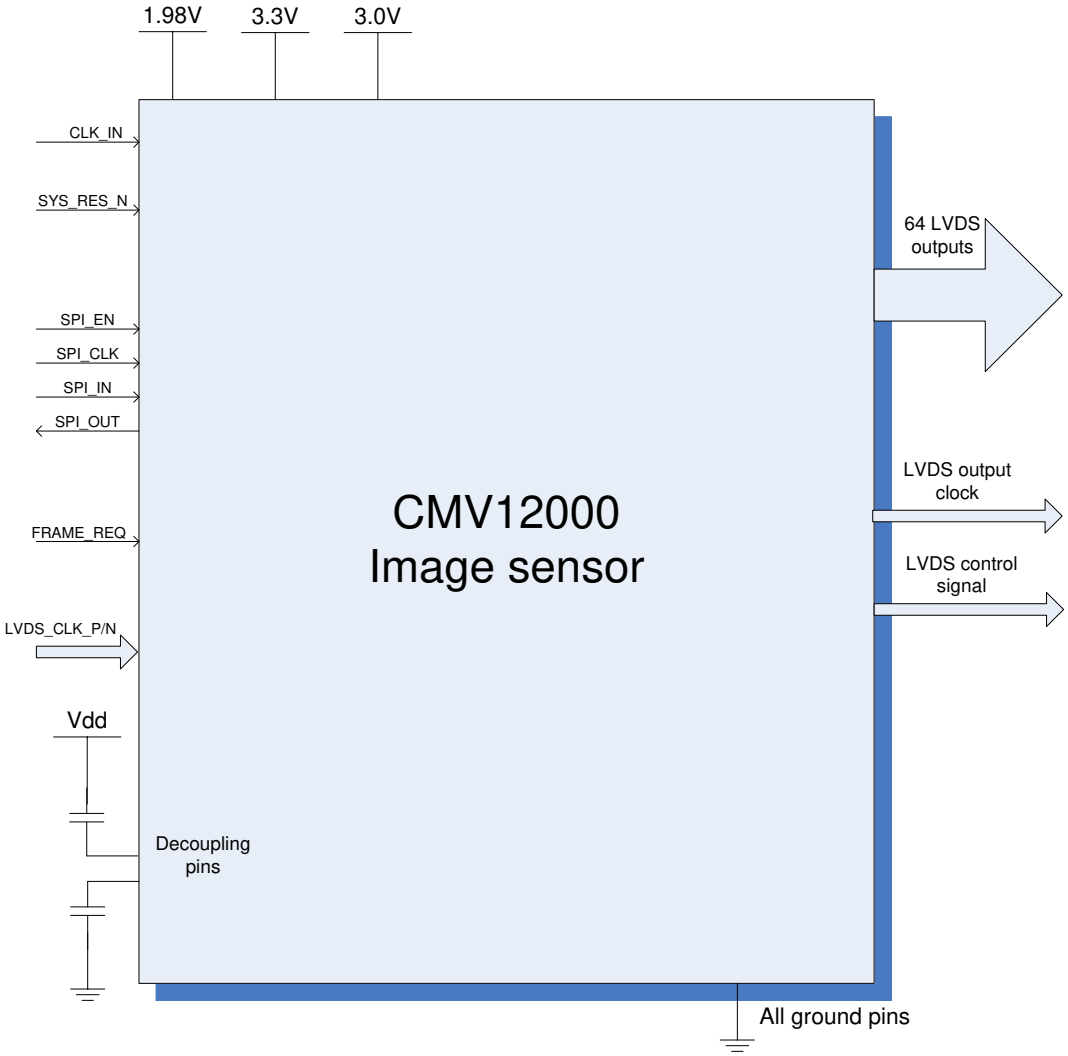

FIGURE 1: CONNECTION DIAGRAM FOR THE CMV12000 IMAGE SENSOR

Please look at the pin list for a detailed description of all pins and their proper connections. Some optional pins are not displayed on the figure above. The exact pin numbers can be found in the pin list and on the package drawing.

2 SENSOR ARCHITECTURE

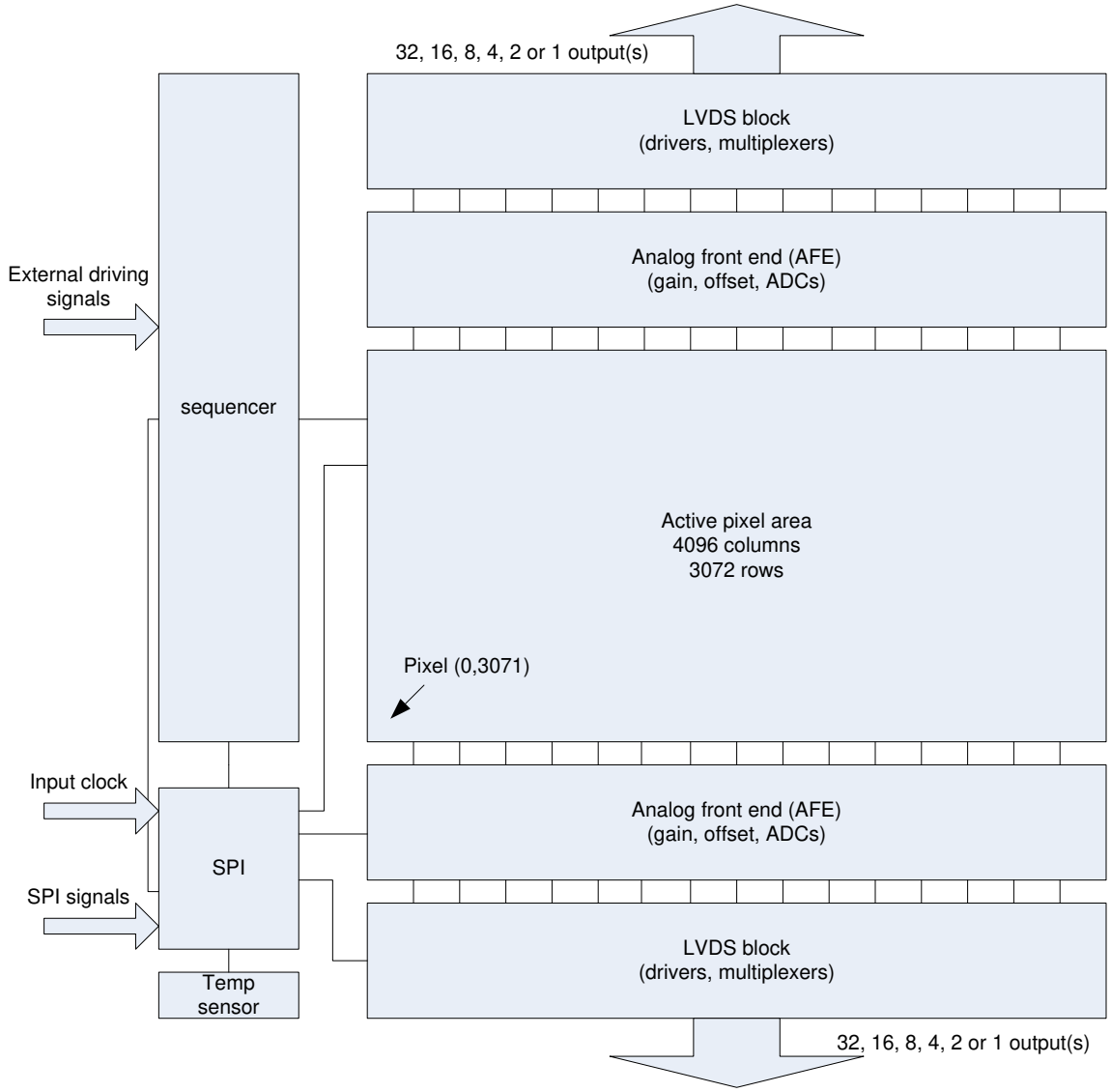

FIGURE 2: SENSOR BLOCK DIAGRAM

Figure 2 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and they are read out sequentially, row-by-row. On the pixel output, an analog gain is possible. The pixel values then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels. Each LVDS channel reads out 128 adjacent columns of the array. The read-out of the pixel array is performed on both sides (top and bottom) of the pixel array to speed up the read-out process and achieve the frame rate of 300 fps at full resolution and 10-bit. In each line read-out cycle, two lines are selected for read-out. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface. A temperature sensor which can be read out over the SPI interface is also included.

2.1 PIXEL ARRAY

The pixel array consists of 4096 x 3072 square global shutter pixels with a pitch of 5.5um (5.5µm x 5.5µm). This results in an optical area of 22.5mm x 16.9mm (28.1mm diameter).

The pixels are designed to achieve maximum sensitivity with low noise (using CDS) and low PLS specifications. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency (>50%).

There are 16 dark reference columns available on the sensor (columns 0 to 7 and 4088 to 4095) which can be enabled/disabled by programming the appropriate sensor register. See chapter 5 for more information.

2.2 ANALOG FRONT END

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface). The column ADC converts the analog pixel value to an 8-, 10- or 12-bit value and can apply a gain. A digital offset can also be applied to the output of the column ADCs. All gain and offset settings can be programmed using the SPI interface.

2.3 LVDS BLOCK

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at maximum 600 Mbps. The sensor has 66 LVDS output pairs:

- 64 Data channels
- 1 Control channel
- 1 Clock channel

The 64 data channels are used to transfer 8-bit, 10-bit or 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock (max 300 MHz), synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels, among other useful sensor status information. Details on the LVDS timing and format can be found in section 4 of this document.

2.4 SEQUENCER

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control signals. This sequencer can be activated and programmed through the SPI interface. A detailed description of the SPI registers and sensor (sequencer) programming can be found in section 5 of this document.

2.5 SPI INTERFACE

The SPI interface is used to load the sequencer registers with data. The data in these registers is used by the sequencer while driving and reading out the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system. Section 5 contains more details on register programming.

2.6 TEMPERATURE SENSOR

A 16-bit digital temperature sensor is included in the image sensor and can be controlled by the SPI-interface. The on-chip temperature can be obtained by reading out the register with address 127.

A calibration of the temperature sensor (read-out the value at specific temperatures to get a calibration factor) is needed by the surrounding system, because the offset can differ per device. The slope is similar for all devices (but a 2-point calibration will improve accuracy). A typical temperature sensor output vs. temperature curve can be found below together with a typical offset and slope formula.

$Typical\ slope = 3.5 * \frac{\text{CLK\_IN}}{30}\ [DN/°C]$	$Typical\ offset\ at\ 0°C = 825 * \frac{\text{CLK\_IN}}{30}\ [DN]$

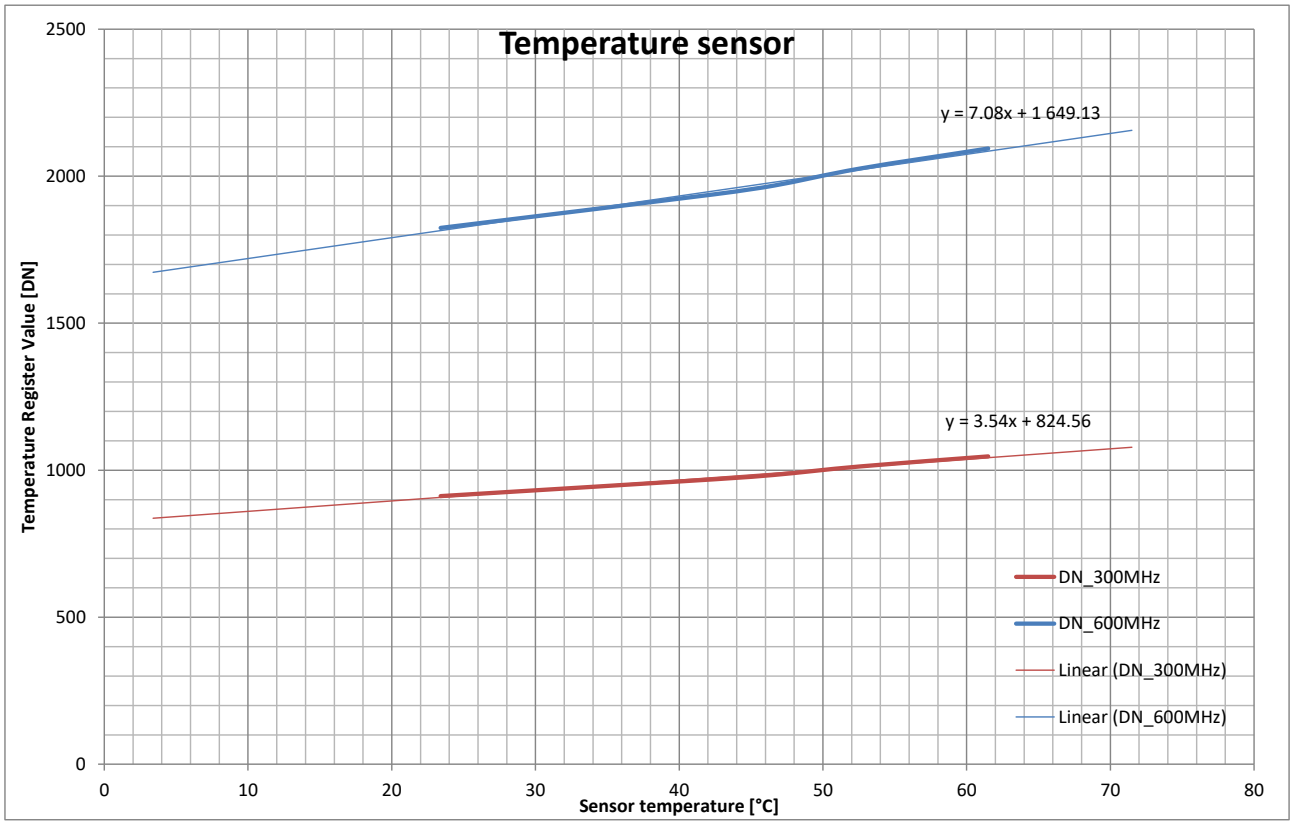

FIGURE 3: TYPICAL OUTPUT OF THE TEMPERATURE SENSOR OF THE CMV12000

3 DRIVING THE CMV12000

3.1 SUPPLY SETTINGS

The CMV12000 image sensor has the following supply settings:

Supply name	Required value	Max. Range	Current nominal	DC Power nom.	Current peak
VDD18	1.98V	1.80V-1.98V	750mA	1500mW	1.7A
VDD33	3.3V	3V-3.6V	180mA	600mW	250mA
VDD_PIX	3.0V	2.3V-3.6V	15mA	75mW	1A
VDD_RES	3.3V	3.0V-3.6V	25mA	17mW	100mA

See pin list for exact pin numbers for every supply.

VDD18 will draw the peak current during read out. The VDD18 peak current scales with the clock speed. The VDD33 has peak currents during read out, although they can be partially caught by decoupling. The VDD_PIX peak happens during FOT (when all pixels will reset). This peak is composed of spikes (1A) and a general DC current increase (~110mA). VDD_RES has its peaks during FOT.

VDD18 and VDD_PIX need the most decoupling to prevent the supplies to dip. For more details on the power figures and peak plots, an application note is available This supply needs therefor decent decoupling to dampen the current peak.

The sensor will heat up above ambient. Below you can see some figures. Decent system heat management is needed to keep the sensors temperature below the specifications limit of 70°C.

LVDS input clock	IDLE	Readout at max. fps
100MHz	+20°C	+24°C
300MHz	+21°C	+30°C
600MHz	+22°C	+40°C

3.2 BIASING

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

3.3 DIGITAL INPUT PINS

The table below gives an overview of the external pins used to drive the sensor

Pin name	Description
CLK_IN	Optional input clock, frequency range between 5 and 60 MHz. Only needed for the internal temperature sensor.
LVDS_CLK_P/N	Input clock, frequency range between 100 and 600MHz, depending on the bit mode. See details in chapter 3.5.
SYS_RES_N	System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up

Pin name	Description
FRAME_REQ	Frame request pin. When a high state is detected on this pin the programmed number of frames is captured and sent by the sensor. The pulse should be at least 8, 10 or 12 * LVDS input clock periods wide to be detected, depending on the used bitmode.
SPI_IN	Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
SPI_EN	SPI enable pin. When this pin is high the data should be written/read on the SPI
SPI_CLK	SPI clock. This is the clock on which the SPI runs (max 30 MHz)
T_EXP1	Input pin which can be used to program the exposure time externally. The pulse should be at least 8, 10 or 12 * LVDS input clock periods wide to be detected, depending on the used bitmode. Optional
T_EXP2	Input pin which can be used to program the exposure time externally in interleaved high dynamic range mode. The pulse should be at least 8, 10 or 12 * LVDS input clock periods wide to be detected, depending on the used bitmode. Optional

3.4 ELECTRICAL IO SPECIFICATIONS

3.4.1 DIGITAL IO CMOS/TTL DC SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{IH}	High level input voltage		2.0		VDD33	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	VDD=3.3V I_{OH}=-2mA	2.4			V
V_{OL}	Low level output voltage	VDD=3.3V I_{OL}=2mA			0.4	V

3.4.2 LVDS RECEIVER SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{ID}	Differential input voltage	Steady state	100	350	600	mV
V_{IC}	Receiver input range	Steady state	0.0		2.4	V
I_{ID}	Receiver input current	$V_{INP\|INN}$=1.2V±50mV, 0≤ $V_{INP\|INN}$≤2.4V			20	µA
ΔI_{ID}	Receiver input current difference	$\|I_{INP} - I_{INN}\|$			6	µA

3.4.3 LVDS DRIVER SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{OD}	Differential output voltage	Steady State, RL = 100Ω	247	350	454	mV
ΔV_{OD}	Difference in V_{OD} between complementary output states	Steady State, RL = 100Ω			50	mV
V_{OC}	Common mode voltage	Steady State, RL = 100Ω	1.125	1.25	1.375	V
ΔV_{OC}	Difference in V_{OC} between complementary output states	Steady State, RL = 100Ω			50	mV
$I_{OS,GND}$	Output short circuit current to ground	V_{OUTP}=V_{OUTN}=GND			24	mA
$I_{OS,PN}$	Output short circuit current	V_{OUTP}=V_{OUTN}			12	mA

3.5 INPUT CLOCK

The LVDS input clock defines the output data rate of the CMV12000. The maximum data rate of the output is 600 Mbps which results in an input LVDS_CLK_P/N clock of 600MHz. The minimum LVDS_CLK_P/N frequency is 100MHz for 12 bit, 10 bit and 8 bit. Any frequency between the minimum and maximum can be applied by the user and will result in a corresponding output data rate.

3.6 FRAME RATE

The frame rate of the CMV12000 is defined by 2 main factors.

1. Exposure time
2. Read-out time

For ease of use we will assume that the exposure time is equal to or shorter than the read-out time. By assuming this the frame rate is completely defined by the read-out time (because the exposure time happens in parallel with the read-out time). The read-out time (and thus the frame rate) is defined by:

1. Output clock speed: max 600 MHz
2. ADC mode: 8-, 10- or 12-bit
3. Number of lines read-out (also subsampling or binning)
4. Number of LVDS outputs used: max 64 outputs

This means that if any of the parameters above is changed, it will have an impact on the frame rate of the CMV12000.

The total read-out time is composed of the FOT (frame overhead time) and the image read-out time.

$$FOT = (reg82[15:8] + 2) * Line\ time$$

$$Line\ time = (reg85 + 1) * \text{LVDS\_CLK\_P/N\_period} * \#\text{bits}$$

When running at 600MHz in 10 bit mode with 64 output channels, register 82[15:8] is 12 and register 85 is 128. This will result in a FOT = 30.1µs and a line time of 2.15µs.

The image read-out time is dependent of the total number of read out lines (#read out lines) and the line time.

$$Readout\ time = Line\ time * \frac{\#read\ out\ lines}{\#\ sides\ used}$$

The number of read out lines will depend on the mode you are using:

$$\begin{aligned} &Normal: && \#read\ out\ lines = Number\_lines\_tot \\ &Subsampling\ in\ X/Y: && \#read\ out\ lines = Number\_lines\_tot/2 \\ &Binning: && \#read\ out\ lines = Number\_lines\_tot/4 \end{aligned}$$

Number_lines_tot is the value of register 1. So with the above conditions and reading the full pixel array we have an image read-out time of 3.3024ms.

The total frame time will be 3.3024ms + 0.0301ms = 3.3368ms which results in a frame rate of 300fps.

If the exposure time is longer than the read-out time the frame rate will depend on the exposure time.

Below you can see an overview of the frame rate in fps for a full resolution image and 64 outputs with a 600MHz LVDS input clock.

Full resolution 64 outputs	Normal	X/Y Subsampling	Binning
Frame rate 8 bit	335	791	251
Frame rate 10 bit	300	1049	267
Frame rate 12 bit	132	528	267

3.7 START-UP SEQUENCE

The following sequence should be followed when the CMV12000 is started up.

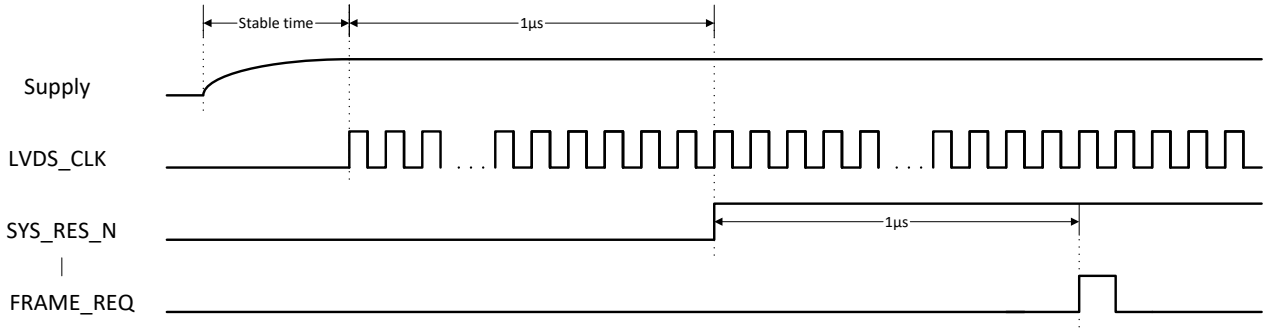

FIGURE 4: START-UP SEQUENCE

The master clock (600 MHz in for 600 Mbps) should only start after the rise time of the supplies. The external reset pin should be released at least 1µs after the supplies have become stable. The first frame can be requested 1µs after the reset pin has been released. An optional SPI upload (to program the sequencer) is possible 1µs after the reset pin has been released. In this case the FRAME_REQ pulse must be postponed until after the SPI upload has been completed.

3.8 RESET SEQUENCE

If a sensor reset is necessary while the sensor is running the following sequence should be followed.

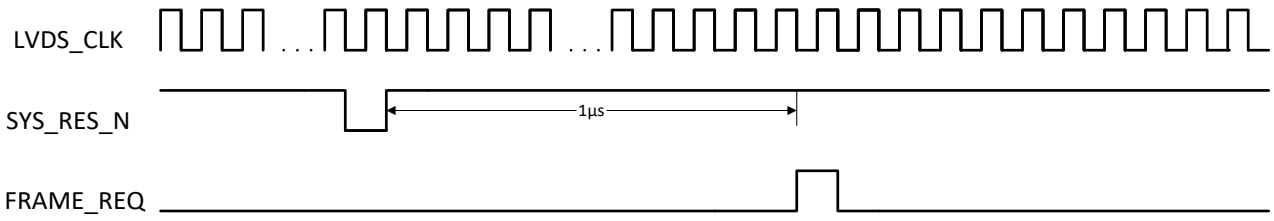

FIGURE 5: RESET SEQUENCE

The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RES_N pin. After the reset there is a minimum time of 1µs needed before a FRAME_REQ pulse can be sent.

When a switch from 12-bit to 10-bit or 8-bit mode (or vice versa) is necessary, the following sequence should be followed.

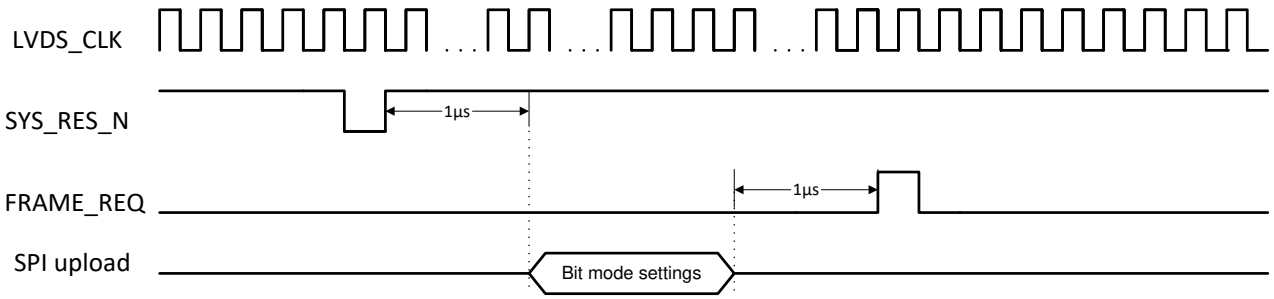

FIGURE 6: RESET SEQUENCE WHEN CHANGING BIT MODE

The following SPI register should be uploaded in this mode: Bit_mode (address 118): set to desired bit resolution mode

3.9 SPI PROGRAMMING

Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

SPI I/O's are pulled low when not used/enabled.

3.9.1 SPI WRITE

The timing to write data over the SPI interface can be found below.

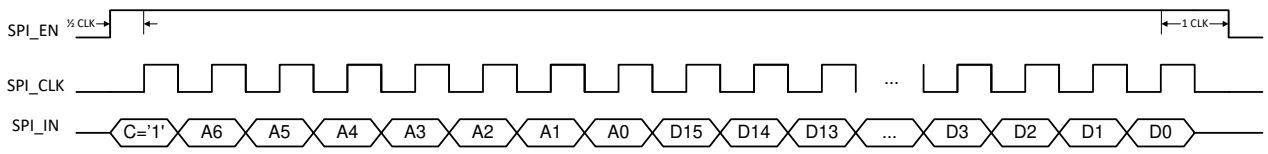

FIGURE 7: SPI WRITE TIMING

The data is sampled by the CMV12000 on the rising edge of the SPI_CLK and read-in at the last falling SPI_CLK edge. The SPI_CLK has a maximum frequency of 30 MHz. The SPI_EN signal has to be high for half a clock period before the first data bit is sampled. SPI_EN has to remain high for 1 clock period after the last data bit is sampled.

One write action contains 24 data bits:

- One control bit: First bit to be sent, indicates whether a read ('0') or write ('1') will occur on the SPI interface.

- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 16 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the figure below for an example of 2 registers being written.

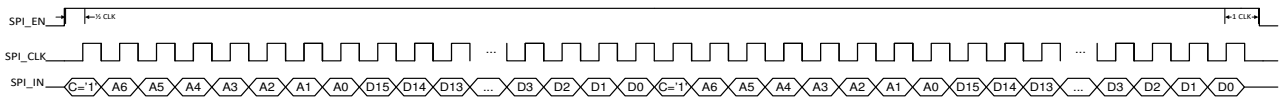

FIGURE 8: SPI WRITE TIMING FOR 2 REGISTERS

3.9.2 SPI READ

The timing to read data from the registers over the SPI interface can be found below.

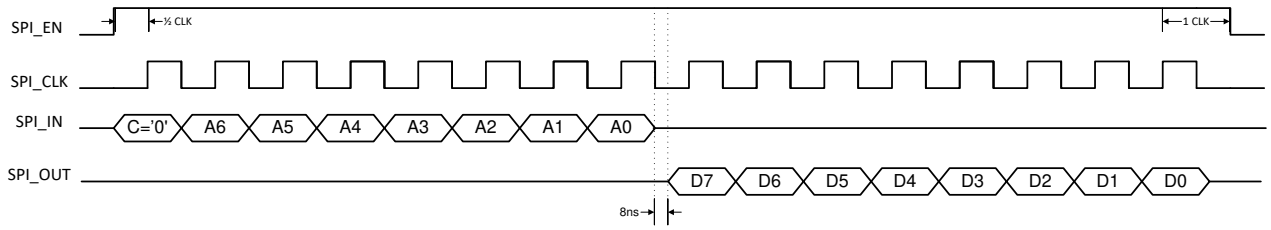

FIGURE 9: SPI READ TIMING

To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made '0'. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK with an 8ns delay (independent of SPI or sensor clock speeds). This means that the data can be sampled by the receiving system on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first.

3.10 REQUESTING A FRAME

After starting up the sensor (see section 3.7), a number of frames can be requested by sending a FRAME_REQ pulse. The number of frames can be set by programming the appropriate register (address 80). The default number of frames to be grabbed is 1.

In internal-exposure-time mode the exposure time will start after this FRAME_REQ pulse. In the external-exposure-time mode the read-out will start after the FRAME_REQ pulse. Both modes are explained into detail in the sections below

3.10.1 INTERNAL EXPOSURE CONTROL

In this mode the exposure time is set by programming the appropriate register (addresses 71-72) of the CMV12000.

After the high state of the FRAME_REQ pulse is detected, the exposure time will start immediately. When the exposure time ends (as programmed in the registers), the pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). Immediately after the FOT, the frame is read out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one. See the diagram below for more details.

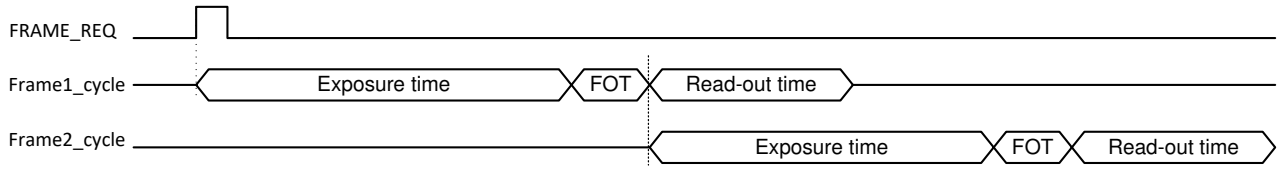

FIGURE 10: REQUEST FOR 2 FRAMES IN INTERNAL-EXPOSURE-TIME MODE

When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame.

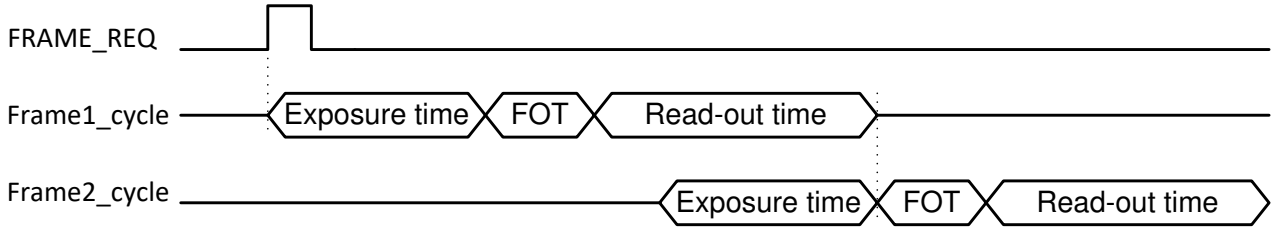

FIGURE 11: REQUEST FOR 2 FRAMES IN INTERNAL-EXPOSURE-TIME MODE WITH EXPOSURE TIME < READ-OUT TIME

When you request a second frame during the read-out of the current frame, the current read-out will always be finished before the FOT of the new requested frame starts. When the new Frame_REQ pulse is too early, it will be delayed internally so that the FOT starts immediately after the readout.

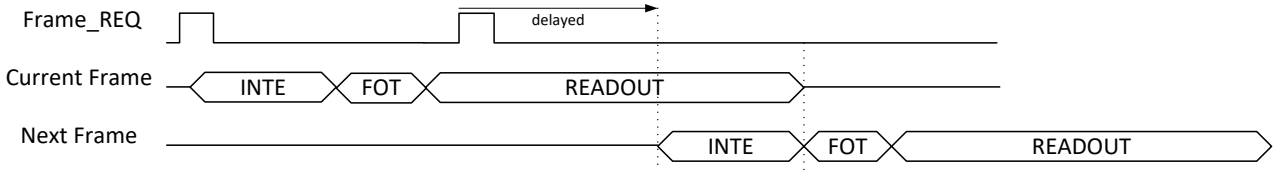

FIGURE 12: DELAY OF FRAME REQUEST

If a 2nd frame request is given during the integration of the current frame, the sensor will remember this and delay the request as described above. This only works for 2 Frame_req pulses during integration.

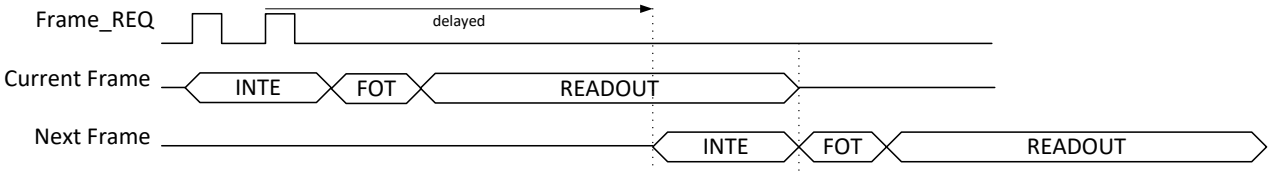

FIGURE 13: 2 FRAME REQUESTS DURING INTEGRATION

When keeping the Frame_REQ pin continuously high, the sensor will continuously read out frames at the maximum achievable frame rate.

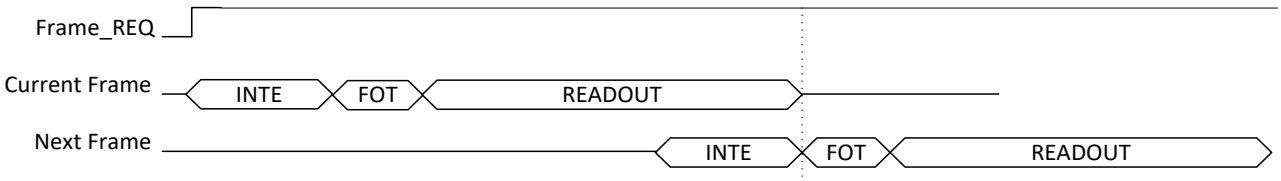

FIGURE 14: CONTINUOUS FRAME_REQ

3.10.2 EXTERNAL EXPOSURE CONTROL

The exposure time can also be programmed externally by using the T_EXP1 (and T_EXP2) input pin. This mode needs to be enabled by setting the appropriate register (address 70[0]). In this case, the exposure starts when a high state is detected on the T_EXP1 pin. When a high value is detected on the FRAME_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the T_EXP1 pin during or after the read-out of the previous frame.

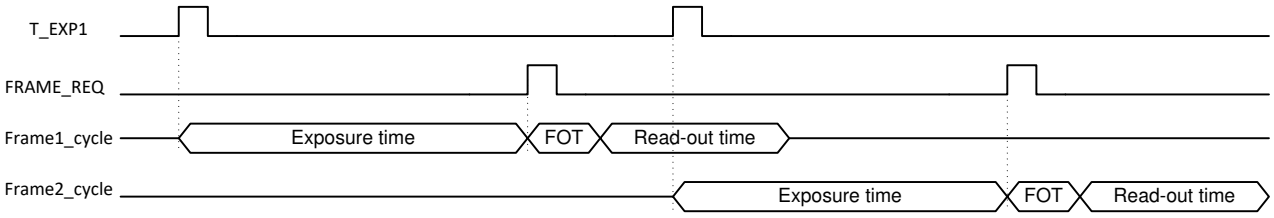

FIGURE 15: REQUEST FOR 2 FRAMES USING EXTERNAL-EXPOSURE-TIME MODE

When the exposures stops too soon (by giving a Frame_REQ pulse during read-out), the current read-out will be finished normally and the exposure time will be extended so that the FOT starts immediately after the read-out.

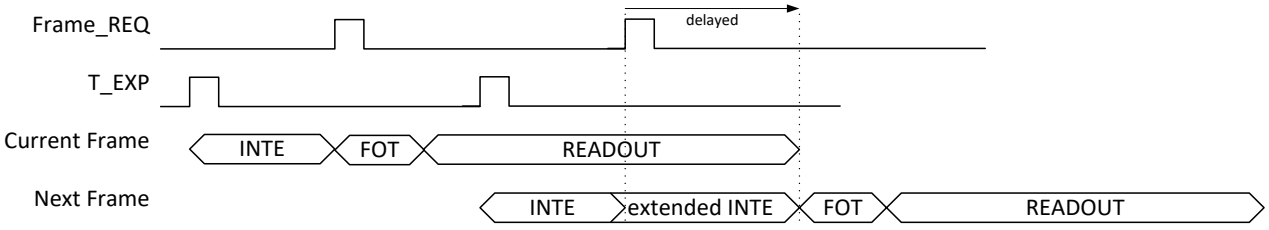

FIGURE 16: EXTENDED INTEGRATION TIME IN EXTERNAL MODE

4 READING OUT THE SENSOR

4.1 LVDS DATA OUTPUTS

The CMV12000 has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 64 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 66 LVDS output pairs (2 pins for each LVDS channel):

- 64 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 132 pins of the CMV12000 are used for the LVDS outputs (128 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs.

The 64 data channels are used to transfer the 12-bit, 10-bit or 8-bit pixel data from the sensor to the receiver in the surrounding system. The 32 bottom channels use pins OUT1_N/P to OUT32_N/P and the top channels use pins OUT33_P/N to OUT64_P/N.

The output clock channel transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 600Mbps output data rate is used, the LVDS output clock will be 300 MHz (half of input clock).

The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 8-bit, 10-bit or 12-bit words that are transferred synchronous to the 64 data channels.

4.2 LOW-LEVEL READ OUT TIMING

The figures below show the timing for transfer of 8-bit, 10-bit and 12-bit pixel data over one LVDS output. To make the timing more clear, the figures show only the p-channel of each LVDS pair. The data is transferred LSB first, with the transfer of bit D[0] during the high phase of the DDR output clock.

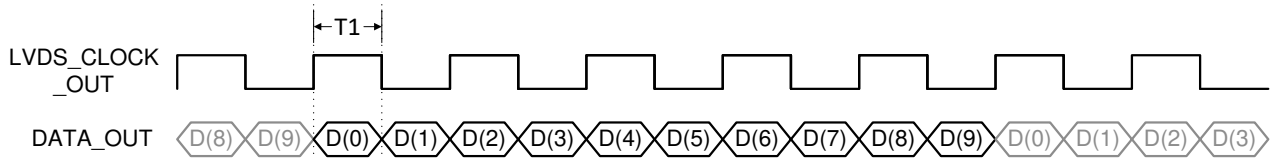

FIGURE 17: 10-BIT PIXEL DATA ON AN LVDS CHANNEL

The time 'T1' in the diagram above is equal to the period of the input clock (LVDS_CLK_P/N) of the CMV12000.

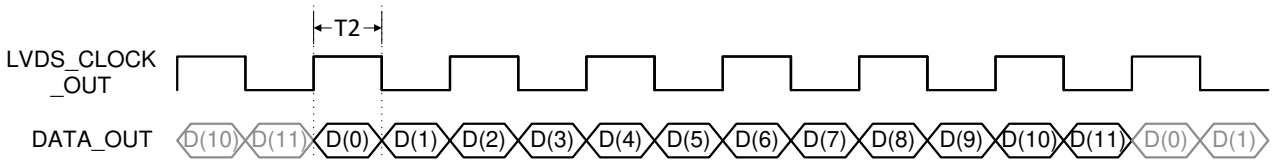

FIGURE 18: 12-BIT PIXEL DATA ON AN LVDS CHANNEL

The time 'T2' in Figure 18 is equal to the period of the input clock (LVDS_CLK_P/N) of the CMV12000.

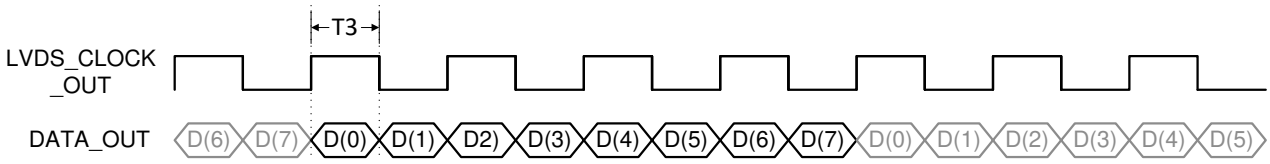

FIGURE 19: 8-BIT PIXEL DATA ON AN LVDS CHANNEL

The time 'T3' in Figure 19 is equal to the period of the input clock (LVDS_CLK_P/N) of the CMV12000.

4.3 PIXEL READ-OUT

The read-out of image data is grouped in bursts of 128 pixels per channel (2 rows at the same time via top and bottom outputs). Each pixel is 8, 10 or 12 bits of data (see section 4.2). For details on pixel remapping and pixel vs. channel location please see section 4.4 of this document. An overhead time exists between two bursts of 128 pixels. This overhead time has the length of one pixel read-out (i.e. the length of 8, 10 or 12 bits at the selected data rate).

Please note that depending on the bit mode (8-bit, 10-bit or 12-bit) and read-out mode (subsampling, binning…), the actual timing of the image data may differ from one mode to another. The sections below show the relative location of the pixel data only.

The sensor is designed to be used with both sides (bottom and top) simultaneously. There is a "one side mode" where only one side (bottom) can be used to read out data, but binning and subsampling in X and Y direction are not supported in this mode.

4.3.1 64 OUTPUT CHANNELS

By default, all 64 data output channels are used to transmit the image data. This means that two entire rows of image data are transferred (one using the top outputs and one using the bottom outputs) in one slot of 128 pixel periods (64 x 128 = 8192). Next figure shows the timing for the top and bottom LVDS channels.

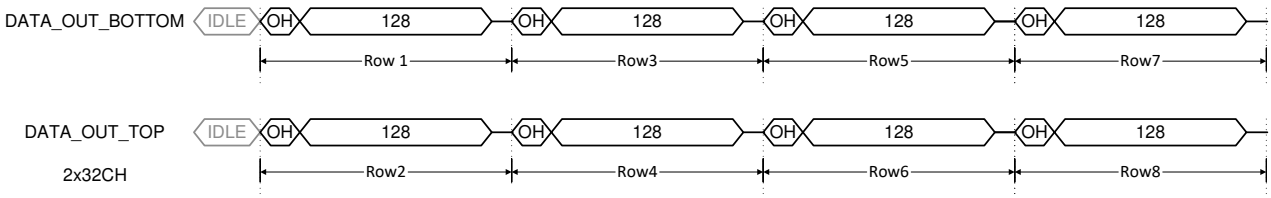

FIGURE 20: OUTPUT TIMING IN DEFAULT 64 CHANNEL MODE

Only when 64 data outputs, running at 600 Mbps and, are used, the frame rate of 300 fps can be achieved in 10 bit (default).

4.3.2 32 OUTPUT CHANNELS

The CMV12000 has possibility to use less than 64 outputs. Also if using 32 or less outputs you can use two sided read-out (using top and bottom outputs) or one sided read-out (using only bottom outputs). In this multiplexed mode the frame rate will be reduced by a factor of 2 compared to the 64 channel output.

4.3.2.1 TWO SIDED READ-OUT

This setting can be programmed with register 81 (see section 5.9). Now you will have 16 channels at each side. In this multiplexed mode the read-out of one row takes 2*128 periods but two rows will be sent out at the same time. Next figure shows the timing, the odd rows are read out by the bottom outputs, the even rows by the top outputs.

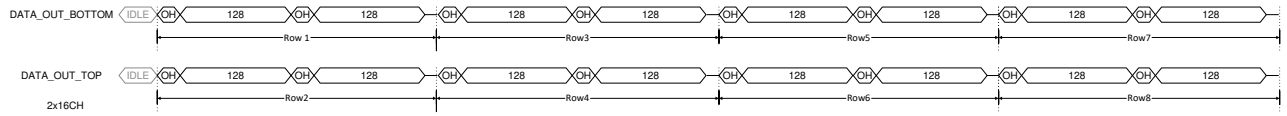

FIGURE 21: OUTPUT TIMING IN TWO SIDED 32 CHANNEL MODE

4.3.2.2 ONE SIDED READ-OUT

This setting can be programmed with register 81 and 66 (see section 5.9). Now you will have 32 channels at the bottom side. In this multiplexed mode the read-out of one row takes 1*128 periods. The rows will be read out following this pattern: row1, row2, row4, row3, row5, row6, row8, row7 … Next figure shows the timing for the bottom LVDS channels.

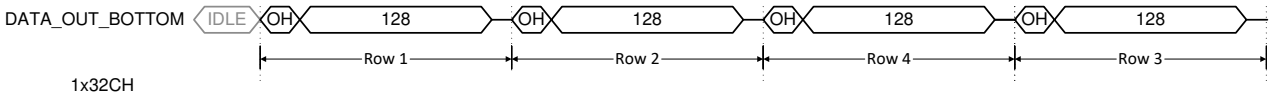

FIGURE 22: OUTPUT TIMING IN ONE SIDED 32 CHANNEL MODE

4.3.3 16 OUTPUT CHANNELS

In this multiplexed mode the frame rate will be reduced by a factor of 4 compared to the 64 channel output.

4.3.3.1 TWO SIDED READ-OUT

This setting can be programmed with register 81 (see section 5.9). Now you will have 8 channels at each side. In this multiplexed mode the read-out of one row takes 4*128 periods but two rows will be sent out at the same time. Next figure shows the timing.

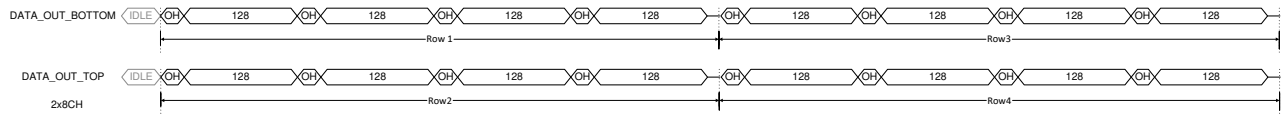

FIGURE 23: OUTPUT TIMING IN TWO SIDED 16 CHANNEL MODE

4.3.3.2 ONE SIDED READ-OUT

This setting can be programmed in the register with address 81 and 66 (see section 5.9). In such multiplexed output mode, only 16 of the bottom 32 LVDS channels are used and the read-out of one row takes 2*128 periods. The rows will be read out following this pattern: row1, row2, row4, row3, row5, row6, row8, row7 … Next figure shows the timing for the bottom LVDS channels.

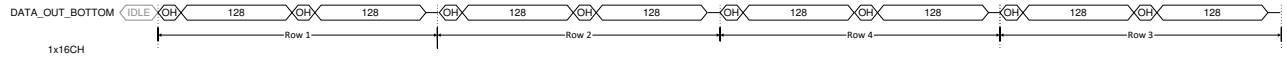

FIGURE 24: OUTPUT TIMING IN ONE SIDED 16 CHANNEL MODE

4.3.4 8 OUTPUT CHANNELS

In this 8 channel mode, the frame rate is reduced with a factor of 8 compared to 64 channel mode.

4.3.4.1 TWO SIDED READ-OUT

This setting can be programmed in the register with address 81 (see section 5.9). In such multiplexed output mode, 4 outputs of each side are used and the read-out of one row takes 8*128 periods but two rows will be sent out at the same time. The timing follows the pattern of the other multiplex modes.