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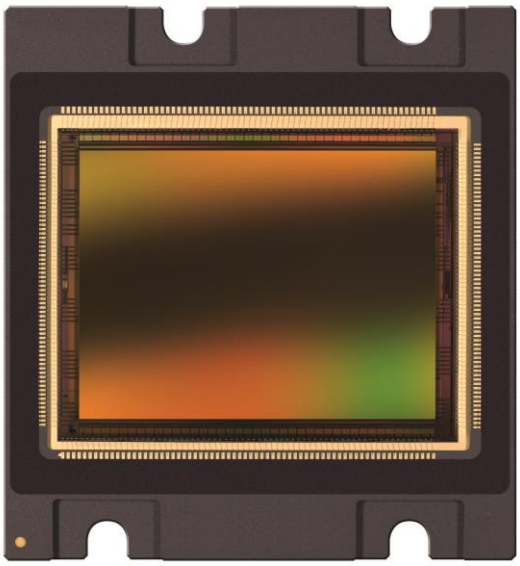
20 Megapixel global shutter CMOS image sensor

Datasheet



Change record

Issue	Date	Modification
1	24/11/211	Origination
1.1	24/5/2013	Changed VDD20 from 2.0V to 2.1V
2	19/06/2013	Removed draft, confidential and preliminary annotations
2.1	12/08/2013	Updated: - FOT, Read out time and exposure time calculations - SPI read out delay (left - right) - VDD20 maximum range to 2.2V - CLK_IN is optional Added: - Angular response - Digital test signals - Detailed frame timing - LVDS output skew
2.2	05/06/2014	Updated: - QE and spectral response for mono devices - Remarks in register overview Added: - QE and spectral response for color devices
2.3	20/05/2015	Updated: - Supply currents - SPI_OUT not tri-state - Reg89[12:8] → [11:8] - PGA gain made relative - Reg103 = 72 → 64 Added: - ADC_gain vs. actual gain - Excessive light precaution - Test Pattern image example

Disclaimer

CMOSIS reserves the right to change the product, specification and other information contained in this document without notice. Although CMOSIS does its best efforts to provide correct information, this is not warranted.

Since the CMV20000 started its design life as a custom imager for traffic applications, the sale of the imager for these applications is excluded.

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1 INTRODUCTION

1.1 OVERVIEW

The CMV20000 is a global shutter CMOS image sensor with 5120 by 3840 pixels. The image array consists of 6.4µm x 6.4µm pipelined global shutter pixels which allow exposure during read out, while performing CDS operation. The image sensor has sixteen 12-bit digital LVDS outputs (serial). The image sensor also integrates a programmable gain amplifier and offset regulation. Each channel runs at 480 Mbps maximum which results in 30 fps frame rate at full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes. Features

1.2 FEATURES

- 5120 * 3840 active pixels on a 6.4um pitch
- frame rate 30 Frames/sec
- row windowing capability
- Window, X-Y mirroring function
- Master clock 40MHz
- 16 LVDS-outputs @ 480MHz, or 8 LVDS-outputs at 15FPS
- LVDS control line with frame and line information
- LVDS DDR output clock to sample data on the receiving end
- 12 bit ADC output
- High Dynamic Range mode supported
- Power dissipation control
- On chip temperature sensor
- On chip timing generation
- SPI-control
- Ceramic PGA package (143 pins)

1.3 SPECIFICATIONS

- Full well charge: 15Ke$^-$
- Sensitivity: 8.3 V/lux.s (with microlenses @ 550nm)
- Dark noise: 8e$^-$ RMS
- Conversion factor: 110µV/e (@ pixel); 0.25DN/e
- Dynamic range: 66 dB
- Extended dynamic range: Piecewise linear response
- Parasitic light sensitivity: 1/50 000
- Dark current: 125 e/s (@ 25C die temp)
- Fixed pattern noise: <0.2% of full swing, standard deviation on full image
- Power consumption: 1100mW

2 SENSOR ARCHITECTURE

Figure 1 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and they are read out sequentially, row-by-row into the analog front-end electronics (AFE) of the columns. On the pixel output, an analog gain of x2.0, x2.4, x2.8 and x3.2 is possible (or 1.6, 1.9, 2.25, 2.55 when column calibration is on). The pixel value then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels. Each LVDS channel reads out 640 adjacent columns of the array. The AFE and LVDs drivers are doubled on opposite sides of the sensor, resulting in 2 rows being read out at the same when all 16 outputs are used. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface. A temperature sensor which can be read out over the SPI interface is also included.

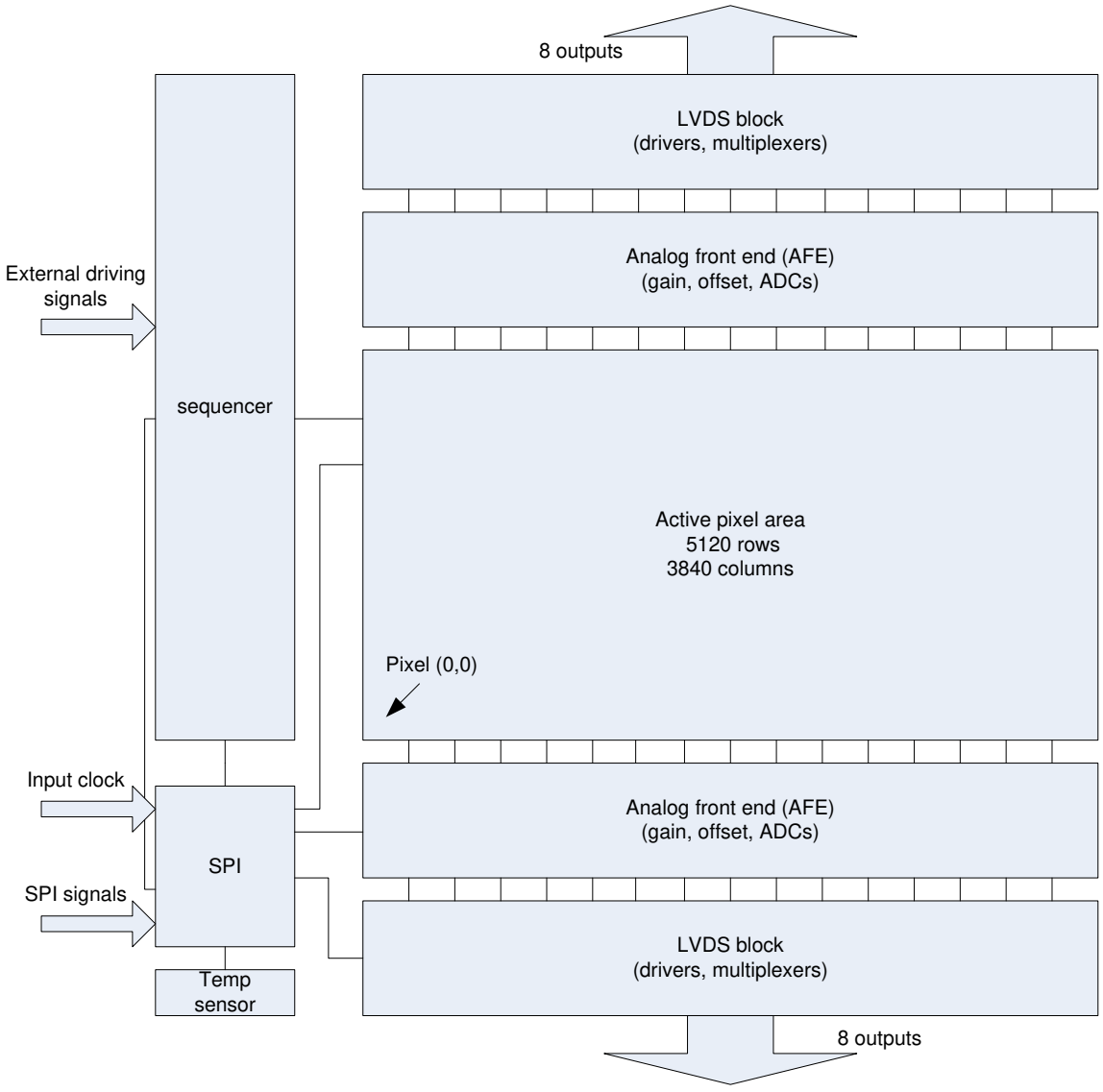


FIGURE 1: BASIC SENSOR ARCHITECTURE

The most important blocks are described more in detail in the following sections.

2.1 PIXEL ARRAY

The CMV20000 sensor has 5120*3840 active pixels with a 6.4um pitch surrounded by two dummy rows and columns. These dummy pixels at the side will ensure that the optical performance, of the active pixels at the edges, is the same as the one in the active array. These dummy pixels cannot be read out and will be set permanent into reset. The pixels are designed to achieve maximum sensitivity with low noise and low PLS specifications. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency.

2.2 ANALOG FRONT-END ELECTRONICS (AFE)

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface). The column ADC converts the analog pixel value to a 12 bit value and can apply a gain. A digital offset can also be applied to the output of the column ADC's. All gain and offset settings can be programmed using the SPI interface.

2.3 LVDS BLOCK

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at maximum 480Mbps. The sensor has 18 LVDS output pairs:

- 16 data channels
- 1 control channel
- 1 clock channel

The 16 data channels are used to transfer 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels, among other useful sensor status information. Details on the LVDS timing and format can be found in section 4 of this document.

2.4 SEQUENCER

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control clocks. This sequencer can be activated and programmed through the SPI interface. A detailed description of the SPI registers and sensor (sequencer) programming can be found in section 5 of this document.

2.5 SPI

The SPI interface is used to load the sequencer registers with data. The data in these registers is used by the sequencer while driving and reading out the image sensor. Features like windowing, sub sampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system. Section 5 contains more details on register programming and SPI timing.

2.6 TEMPERATURE SENSOR

A 16-bit digital temperature sensor is included in the image sensor and can be controlled by the SPI-interface. The on-chip temperature can be obtained by reading out a dedicated SPI register (address 101-102).

A calibration of the temperature sensor is needed by the surrounding system (for absolute temperature measurements).

3 DRIVING THE CMV20000

3.1 SUPPLY SETTINGS

The CMV20000 image sensor has the following supply settings:

Supply name	Recommended Value	Absolute Min - Max Range	Current typical	Current peak
VDD20	2.1V	1.6 - 2.2V	800mA	1A
VDD33	3.3V	3V - 3.6V	170mA	0.6A
VDDpix	3.0V	2.3V - 3.6V	20mA	8A
Vres_h	3.3V	3.0V - 3.6V	5mA	0.1A

See pin list for exact pin numbers for every supply.

The peak current of VDD20 is drawn during read out, while the other supplies draw it during FOT. All supplies should have enough decoupling, especially VDDPIX. Application note AN03 has more details about these peaks waveforms.

3.2 BIASING

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

3.3 DIGITAL INPUT PINS

The table below gives an overview of the external pins used to drive the sensor

Pin name	Description
CLK_IN	Master input clock, frequency range is (LVDS_CLK / 12). This clock is optional.
LVDS_CLK_N/P	High speed LVDS input clock, frequency range between 120 and 480 MHz
SYS_RES_N	System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up
FRAME_REQ	Frame request pin. When a rising edge is detected on this pin the programmed number of frames is captured and sent by the sensor
SPI_IN	Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
SPI_EN	SPI enable pin. When this pin is high the data should be written/read on the SPI
SPI_CLK	SPI clock. This is the clock on which the SPI runs (max 20Mz)
T_EXP1	Input pin which can be used to program the exposure time externally. Optional

3.4 ELECTRICAL IO SPECIFICATIONS

3.4.1 DIGITAL IO CMOS/TTL DC SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{IH}	High level input voltage		2.0		VDD33	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	VDD=3.3V I_{OH}=-2mA	2.4			V
V_{OL}	Low level output voltage	VDD=3.3V I_{OL}=2mA			0.4	V

3.4.2 LVDS RECEIVER SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{ID}	Differential input voltage	Steady state	100	350	600	mV
V_{IC}	Receiver input range	Steady state	0.0		2.4	V
I_{ID}	Receiver input current	$V_{INP\|INN}$=1.2V±50mV, 0≤ $V_{INP\|INN}$≤2.4V			20	µA
ΔI_{ID}	Receiver input current difference	$\|I_{INP} - I_{INN}\|$			6	µA

3.4.3 LVDS DRIVER SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{OD}	Differential output voltage	Steady State, RL = 100Ω	247	350	454	mV
ΔV_{OD}	Difference in V_{OD} between complementary output states	Steady State, RL = 100Ω			50	mV
V_{OC}	Common mode voltage	Steady State, RL = 100Ω	1.125	1.25	1.375	V
ΔV_{OC}	Difference in V_{OC} between complementary output states	Steady State, RL = 100Ω			50	mV
$I_{OS,GND}$	Output short circuit current to ground	V_{OUTP}=V_{OUTN}=GND			24	mA
$I_{OS,PN}$	Output short circuit current	V_{OUTP}=V_{OUTN}			12	mA

3.5 INPUT CLOCK

The high speed LVDS input clock (LVDS_CLK_N/P) defines the output data rate of the CMV20000. The master clock (CLK_IN) must be 12 times slower and this clock but is optional. The maximum data rate of the output is 480Mbps which results in a LVDS_CLK_N/P of 480MHz (and a CLK_IN of 40MHz). The minimum frequencies are 10MHz for CLK_IN and 120MHz for LVDS_CLK_N/P. Any frequency between the minimum and maximum can be applied by the user and will result in a corresponding output data rate.

3.6 FRAME RATE CALCULATION

The frame rate of the CMV20000 is defined by 2 main factors.

1. Exposure time
2. Read out time

For ease of use we will assume that the exposure time is shorter than the read out time. By assuming this, the frame rate is completely defined by the read out time (because the exposure time happens in parallel with the read-out time). The read-out time (and thus the frame rate) is defined by:

1. Output clock speed: max 480Mbps
2. Number of lines read-out
3. Number of outputs used: max 16 LVDS outputs (8 on the top and 8 on the bottom)

This means that if any of the parameters above is changed, it will have an impact on the frame rate of the CMV20000. In normal operation (16 outputs @ 480Mbps, 12 bit and full resolution) this will result in 30 fps.

Total readout time is composed of two parts: FOT (frame overhead time) + image readout time.

$$FOT = \left(\left(80 * reg82 + \frac{reg82}{8}\right) + (2 * 641)\right) * clk\_\text{per}$$

So for reg82 = 80 and running at 480MHz this becomes:

$$FOT = (6410 + 1282) * 25ns = 192.3\mu s$$

The image read out time equals to

$$Read\ Out\ Time = 641 * clk\_\text{per} * \frac{nr\_\text{lines}}{\#\ sides\ used}$$

So for full resolution and running at 480MHz with both output sides used this becomes:

$$Read\ Out\ Time = 641 * 25ns * \frac{3840}{2} = 30.768ms$$

This results in a total frame time of:

$$Frame\ time = FOT + Read\ Out\ time$$

So for the default settings this becomes:

$$Frame\ time = 192.3\mu s + 30768\ \mu s = 30.96ms$$

And the frame rate becomes:

$$Frame\ rate = \frac{1}{Frame\ time} = \frac{1}{0.03096s} = 32.3fps$$

See chapter 5.1.1 for detailed frame timing. Clk_per is the period of the pixel clock. This pixel clock frequency is equal to 1/12th (40MHz) of the LVDS input clock frequency (480MHz).

3.7 START-UP SEQUENCE

The following sequence should be followed when the CMV20000 is started up in default output mode (480Mbps, 12bit resolution).

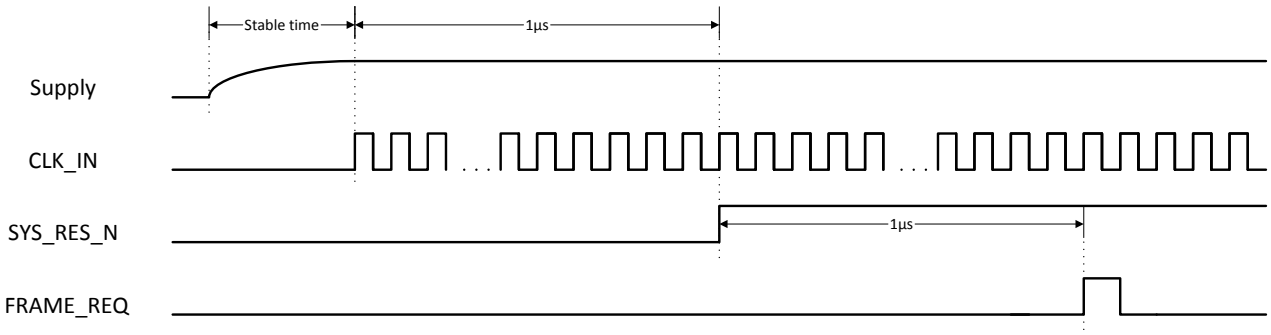


FIGURE 2: START-UP SEQUENCE FOR 480MBPS @ 12-BIT

The CLK_IN and LVDS_CLK_N/P should only start after the rise time of the supplies (VDD33, VDD20, Vddpix and Vres_h go high together). The external reset pin should be released at least 1µs after the supplies have become stable. The first frame can be requested 1µs after the reset pin has been released. An optional SPI upload (to program the sequencer) is possible 1µs after the reset pin has been released. In this case the FRAME_REQ pulse must be postponed until after the SPI upload has been completed.

3.8 RESET SEQUENCE

If a sensor reset is necessary while the sensor is running the following sequence should be followed.

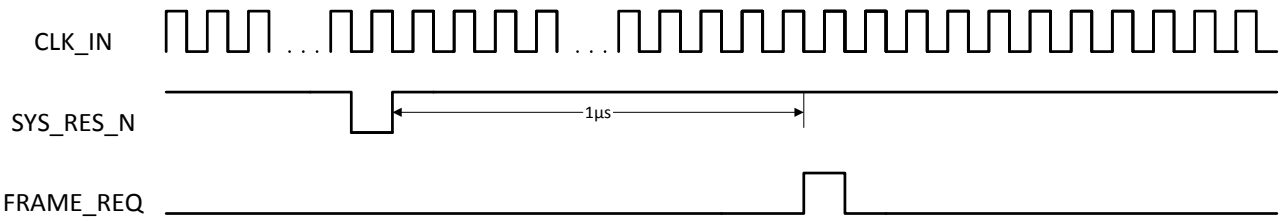


FIGURE 3: RESET SEQUENCE

The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RES_N pin. After the reset there is a minimum time of 1µs needed before a FRAME_REQ pulse can be sent. All recommended register settings must be reloaded after a reset sequence.

3.9 SPI PROGRAMMING

Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

The SPI out doesn't have a tri-state, so multiple SPI outputs cannot be on the same bus without a buffer.

3.9.1 SPI WRITE

The timing to write data over the SPI interface can be found below.

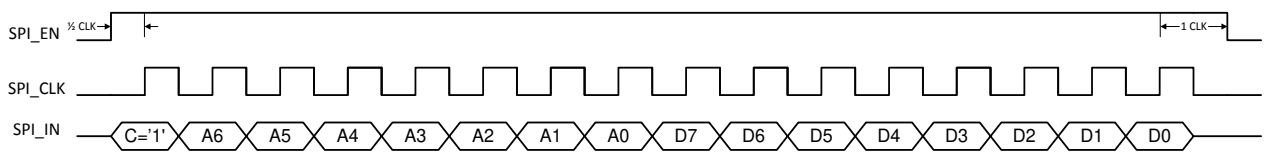


FIGURE 4: SPI WRITE TIMING

The data is sampled by the CMV20000 on the rising edge of the SPI_CLK. The SPI_CLK has a maximum frequency of 20MHz. The SPI_EN signal has to be high for half a clock period before the first databit is sampled. SPI_EN has to remain high for 1 clock period after the last databit is sampled.

One write action contains 16 databits:

- One control bit: First bit to be sent, indicates whether a read ('0') or write ('1') will occur on the SPI interface.
- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 8 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the figure below for an example of 2 registers being written in burst.

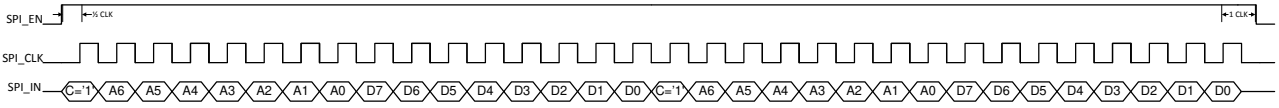


FIGURE 5: SPI WRITE TIMING FOR 2 REGISTERS IN BURST

The sample and hold time is 1/4th of the SPI clock period.

3.9.2 SPI READ

The timing to read data from the registers over the SPI interface can be found below.

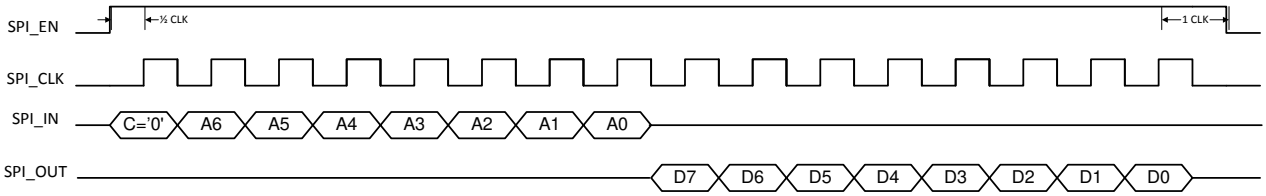


FIGURE 6: SPI READ TIMING

To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made '0'. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK. This means that the data should be sampled by the receiving system on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first.

The CMV20000 has to SPI read out pins: SPI_OUT_LEFT (pin T1) and SPI_OUT_RIGHT (pin R18). SPI_OUT_LEFT will read out every register, while SPI_OUT_RIGHT will only read out registers 103 to 126. Because of the large sensor there is some SPI read out delay. This delay is fixed and independent of the sensor or SPI clock.

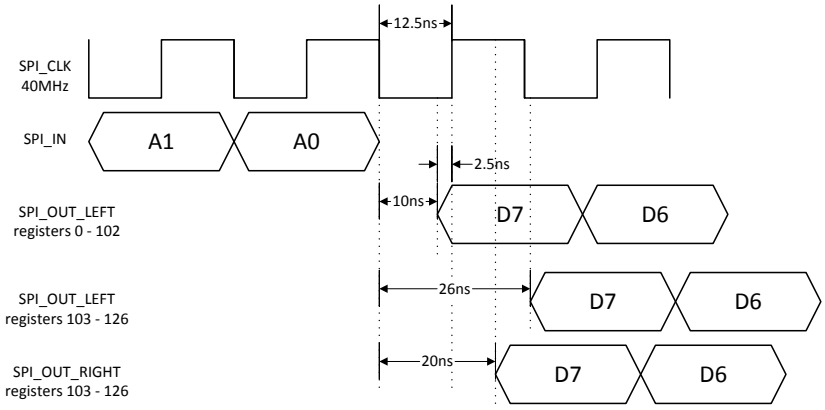


FIGURE 7: SPI DELAY

So when sampling on the rising SPI_CLK edge it is advised to have a SPI_CLK of 10MHz maximum.

3.10 REQUESTING A FRAME

After starting up the sensor (see section 3.7), a number of frames can be requested by sending a FRAME_REQ pulse. The number of frames can be set by programming the appropriate register (addresses 22 and 23). The default number of frames to be grabbed is 1.

In internal-exposure-time mode, the exposure time will start after this FRAME_REQ pulse. In the external-exposure-time mode, the read-out will start after the FRAME_REQ pulse. Both modes are explained into detail in the sections below.

3.10.1 INTERNAL EXPOSURE CONTROL

In this mode, the exposure time is set by programming the appropriate registers (address 32-33) of the CMV20000.

After the high state of the FRAME_REQ pulse is detected, the exposure time will start immediately. When the exposure time ends (as programmed in the registers), the pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). Immediately after the FOT, the frame is read-out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one. See the diagram below for more details.

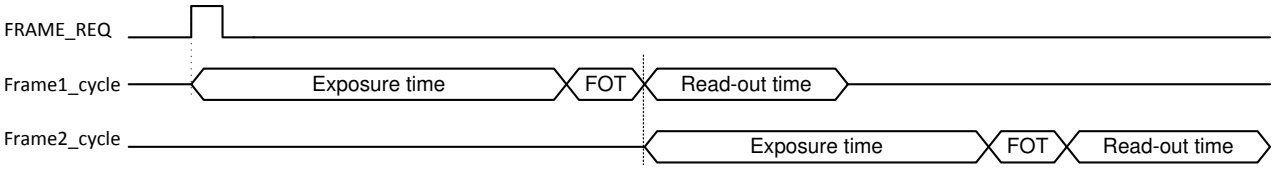


FIGURE 8: REQUEST FOR 2 FRAMES IN INTERNAL- EXPOSURE-TIME MODE

When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame.

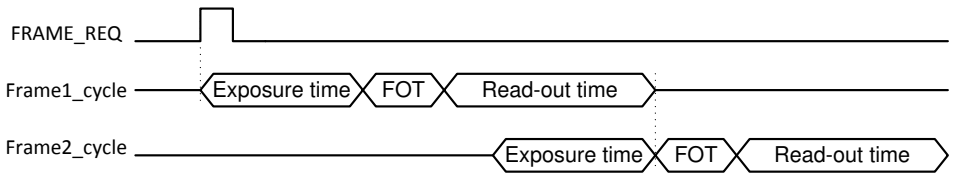


FIGURE 9: REQUEST FOR 2 FRAMES IN INTERNAL-EXPOSURE-TIME MODE WITH EXPOSURE TIME < READ-OUT TIME

3.10.2 EXTERNAL EXPOSURE CONTROL

The exposure time can also be programmed externally by using the T_EXP1 input pin. This mode needs to be enabled by setting the appropriate register (address 81). In this case, the exposure starts when a high state is detected on the T_EXP1 pin. When a high state is detected on the FRAME_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the T_EXP1 pin during or after the read-out of the previous frame.

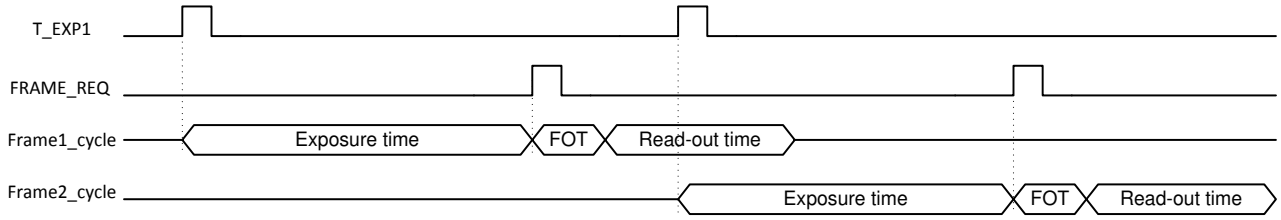


FIGURE 10: REQUEST FOR 2 FRAMES USING EXTERNAL-EXPOSURE-TIME MODE

4 READING OUT THE SENSOR

The CMV20000 has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 16 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 18 LVDS output pairs (2 pins for each LVDS channel):

- 16 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 36 pins of the CMV20000 are used for the LVDS outputs (32 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs. The 16 data channels are used to transfer the 12-bit pixel data from the sensor to the receiver in the surrounding system. The output clock channel transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 480Mbps output data rate is used, the LVDS output clock will be 240MHz. The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 12-bit words that are transferred synchronous to the 16 data channels.

4.1 LVDS LOW-LEVEL PIXEL TIMING

The figure below shows the timing for transfer of 12-bit pixel data over one LVDS output. To make the timing more clear, the figure shows only the p-channel of each LVDS pair. The data is transferred LSB first, with the transfer of bit D[0] during the high phase of the DDR output clock.

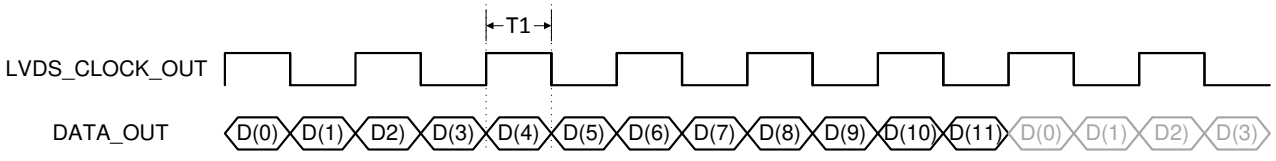


FIGURE 11: 10: 12-BIT PIXEL DATA ON AN LVDS CHANNEL

The time 'T1' in the diagram above is 1/12th of the period of the input clock (CLK_IN) of the CMV20000. If a frequency of 40MHz is used for CLK_IN (max), this results in a 240MHz LVDS_CLOCK_OUT.

4.2 LVDS READOUT TIMING

The readout of image data is grouped in bursts of 640 pixels per channel (2 rows at the same time). Each pixel is 12 bits of data (see section 4.1.1). One complete pixel period equals one period of the master clock input. For details on pixel remapping and pixel vs channel location please see section 4.1.3 of this document. An overhead time exists between two bursts of 640 pixels. This overhead time has the length of one pixel read-out (i.e. the length of 12 bits at the selected data rate) or one master clock cycle.

4.2.1 16 OUTPUT CHANNELS

By default, all 16 data output channels are used to transmit the image data. This means that two entire rows of image data are transferred in one slot of 640 pixel periods (16/2 x 640 = 5120). Next figure shows the timing for the top and bottom LVDS channels.

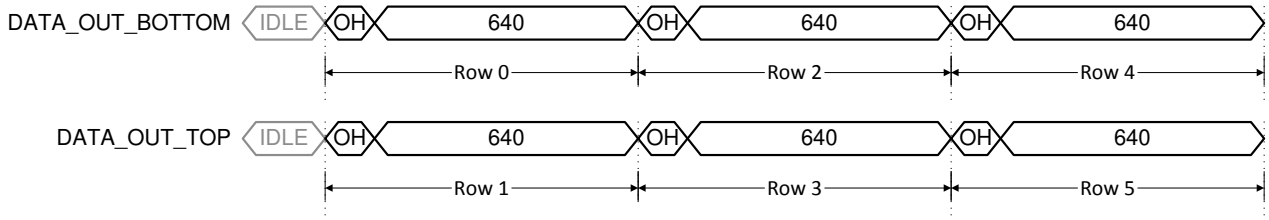


FIGURE 12: OUTPUT TIMING IN DEFAULT 16 CHANNEL MODE

Only when 16 data outputs, running at 480Mbps, are used, the frame rate of 30fps can be achieved (default).

4.2.2 8 OUTPUT CHANNELS

The CMV20000 has the possibility to use only 8 LVDS output channels. This setting can be programmed in the register with address 80 (see section 5.7). In such multiplexed output mode, only the 8 bottom LVDS channels are used. The readout of one row takes 1*640 periods. . This means that ne entire rows of image data are transferred in one slot of 640 pixel periods (8 x 640 = 5120). Next figure shows the timing for the bottom LVDS channels.

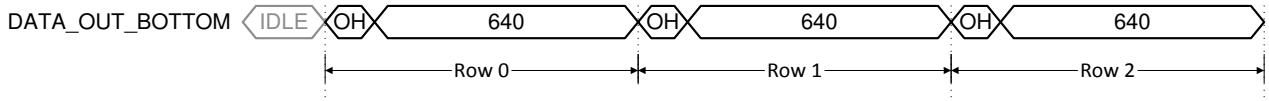


FIGURE 13: OUTPUT TIMING IN 8 CHANNEL MODE

In this 2 channel mode, the frame rate is reduced with a factor of 2 compared to 4 channel mode.

4.3 PIXEL REMAPPING

Depending on the number of output channels, the pixels are read out by different channels and come out at a different moment in time. With the details from the next sections, the end user is able to remap the pixel values at the output to their correct image array location.

4.3.1 16 OUTPUTS

The figure below shows the location of the image pixels versus the output channel of the image sensor.

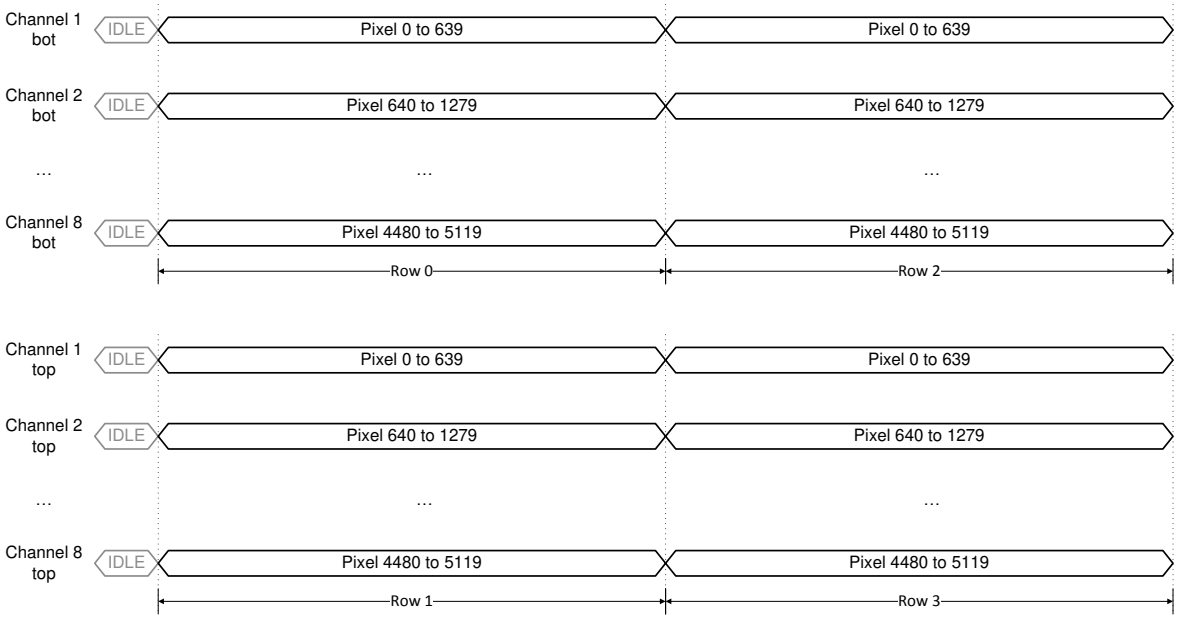


FIGURE 14: PIXEL REMAPPING FOR 16 OUTPUT CHANNELS

16 bursts (8 x 2) of 640 pixels happen in parallel on the data outputs. This means that two complete rows are read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3840 rows being read out.

4.3.2 8 OUTPUTS

When only 8 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 8 bursts of 640 pixels happen in parallel on the data outputs. This means that one complete row is read out in one burst. The time needed to read out two rows is doubled compared to when 16 outputs are used. The top LVDS channels are not being used in this mode, so they can be turned off by setting the correct bits in the register with address 95-97. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 3840 rows being read out.

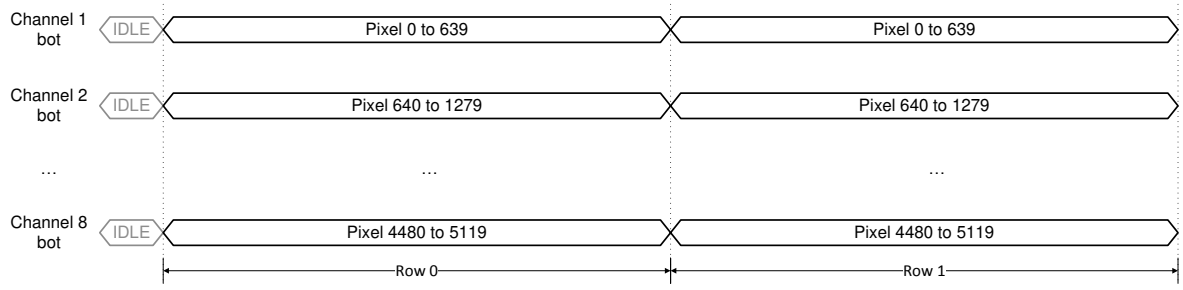


FIGURE 15: PIXEL REMAPPING FOR 8 OUTPUT CHANNELS

4.4 CONTROL CHANNEL

The CMV20000 has one LVDS output channel dedicated for the valid data synchronization and timing of the output channels. The end user must use this channel to know when valid image data or training data is available on the data output channels.

The control channel transfers status information in 12-bit word format. Every bit of the word has a specific function. Next table describes the function of the individual bits.

Bit	Function	Description
[0]	DVAL	Indicates valid pixel data on the outputs
[1]	LVAL	Indicates validity of the readout of a row
[2]	FVAL	Indicates the validity of the readout of a frame
[3]	'0'	Constant zero
[4]	'0'	Constant zero
[5]	FOT	Indicates when the sensor is in FOT (sampling of image data in pixels) (*)
[6]	INTE1	Indicates when pixels of integration block 1 are integrating (*)
[7]	INTE2	Indicates when pixels of integration block 2 are integrating (*)
[8]	'0'	Constant zero
[9]	'1'	Constant one
[10]	'0'	Constant zero
[11]	'0'	Constant zero

(*)Note: The status bits are purely informational. These bits are not required to know when the data is valid. The DVAL, LVAL and FVAL signals are sufficient to know when to sample the image data.

4.4.1 DVAL, LVAL, FVAL

The first three bits of the control word must be used to identify valid data and the readout status. Next figure shows the timing of the DVAL, LVAL and FVAL bits of the control channel with an example of the readout of a frame of 6 rows (default is 3840 rows). This example uses the default mode of 16 outputs (8 outputs on each side).

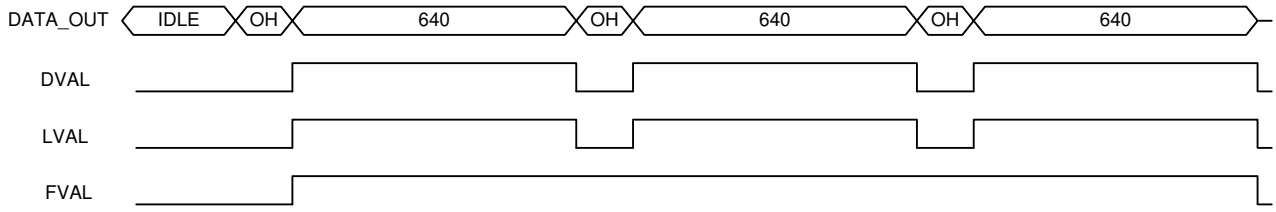


FIGURE 16: DVAL, LVAL AND FVAL TIMING IN 16 OUTPUT MODE

4.4.2 DIGITAL TEST PINS

Pins D1 (Tdig2) and D3 (Tdig1) can be used as digital outputs to monitor the state of the sensor. Register 92 can be used to select a signal on these pins.

Reg92[6:4]	Tdig2
0	LVAL
3	INTE_1
7	CLK_OUT (=LVDS_CLK/12)

Reg92[3:0]	Tdig1
0	FVAL
2	FOT
3	INTE_2

4.5 TRAINING DATA

To synchronize the receiving side with the LVDS outputs of the CMV20000, a known data pattern can be put on the output channels. This pattern can be used to “train” the LVDS receiver of the surrounding system to achieve correct word alignment of the image data. Such a training pattern is put on all 16 data channel outputs when there is no valid image data to be sent (so, also in between bursts of 640 pixels). The training pattern is a 12-bit data word that replaces the pixel data. The sensor has a 12-bit sequencer register (address 90-90) that can be loaded through the SPI to change the contents of the 12-bit training pattern.

The control channel does not send a training pattern, because it is used to send control information at all time. Word alignment can be done on this channel when the sensor is idle (not exposing or sending image data). In this case all bits of the control word are zero, except for bit [9].

The figure below shows the location of the training pattern (TP) on the data channels and control channels when the sensor is in idle mode and when a frame of 6 rows is read-out. The default mode of 16 outputs is selected.

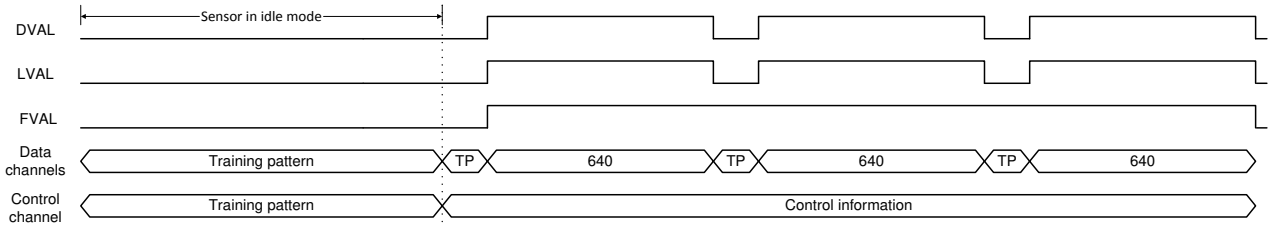


FIGURE 17: TRAINING PATTERN LOCATION IN THE DATA CHANNEL AND CONTROL CHANNEL.

The LVDS outputs are not aligned with the LVDS output clock. Every channel (per odd/even side) has a skew of +600ps compared to the previous channel. The control channel and both odd and even channels 1 are aligned with the clock. This skew will become larger than a LVDS clock period and therefor bit and word alignment is needed in the receiving side.

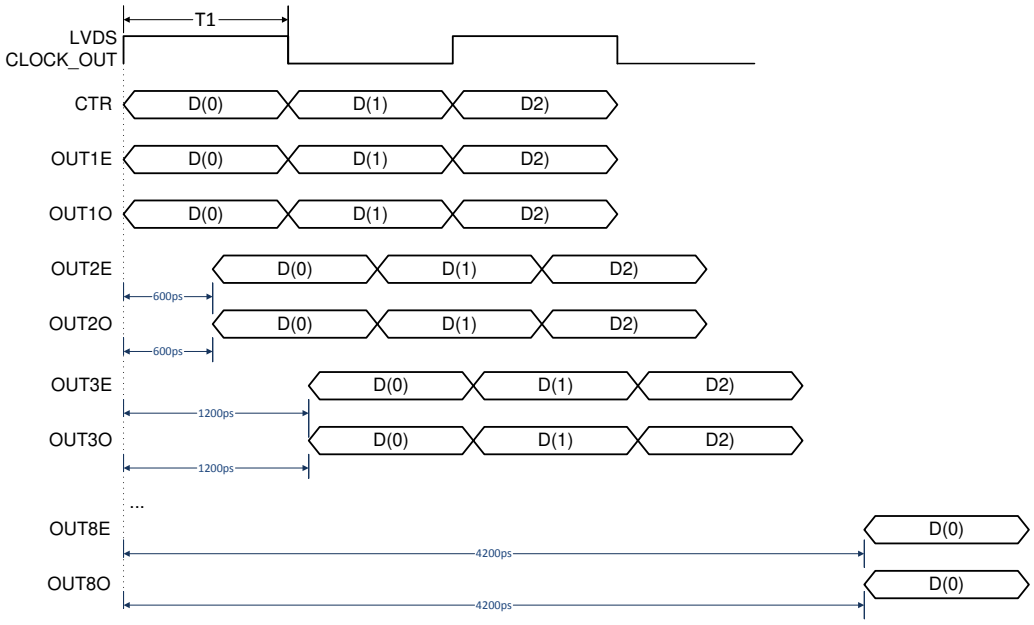


FIGURE 18: LVDS OUTPUT SKEW

4.6 TEST PATTERN

Instead of sending image data, the sensor can generate a fixed two-dimensional test image (after sending a frame request), if the test pattern mode is enabled. This setting can be programmed in the register by setting register 83[0] to 1.

The test pattern is the sum of the row number, the pixel number and the data output channel number. Next figure shows an example of the test pattern data.

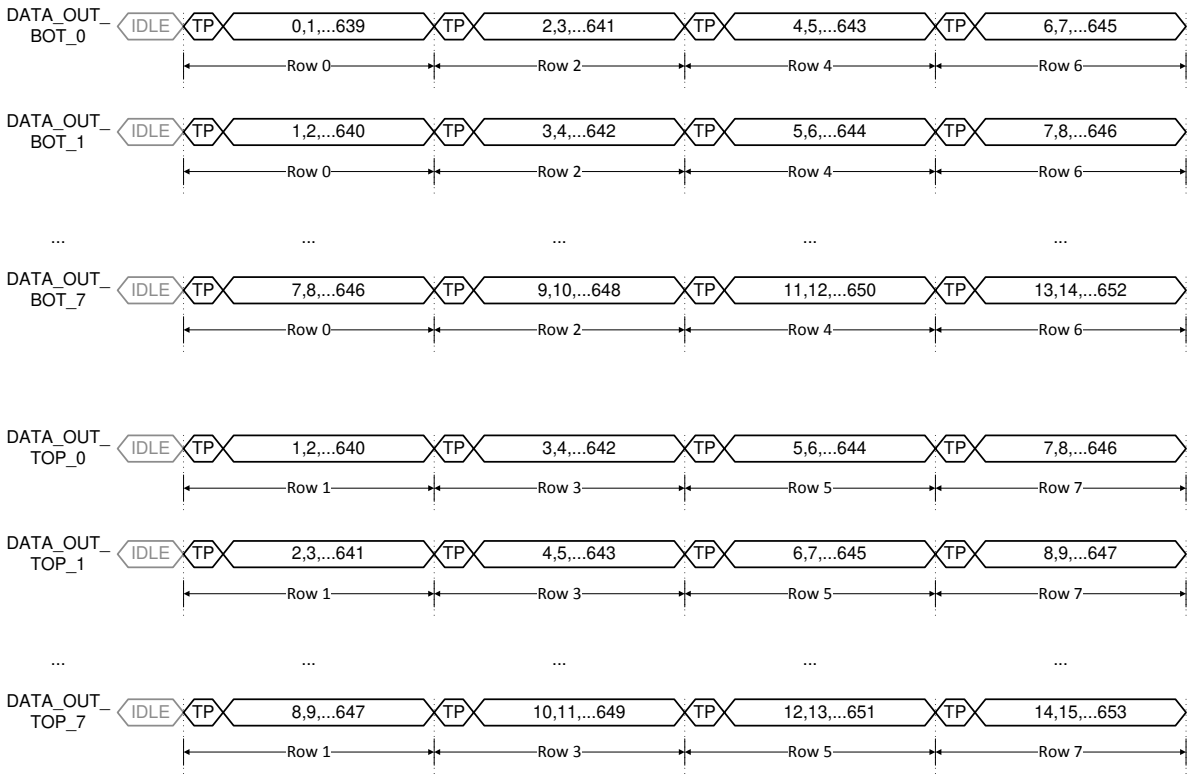


FIGURE 19: TEST PATTERN DATA

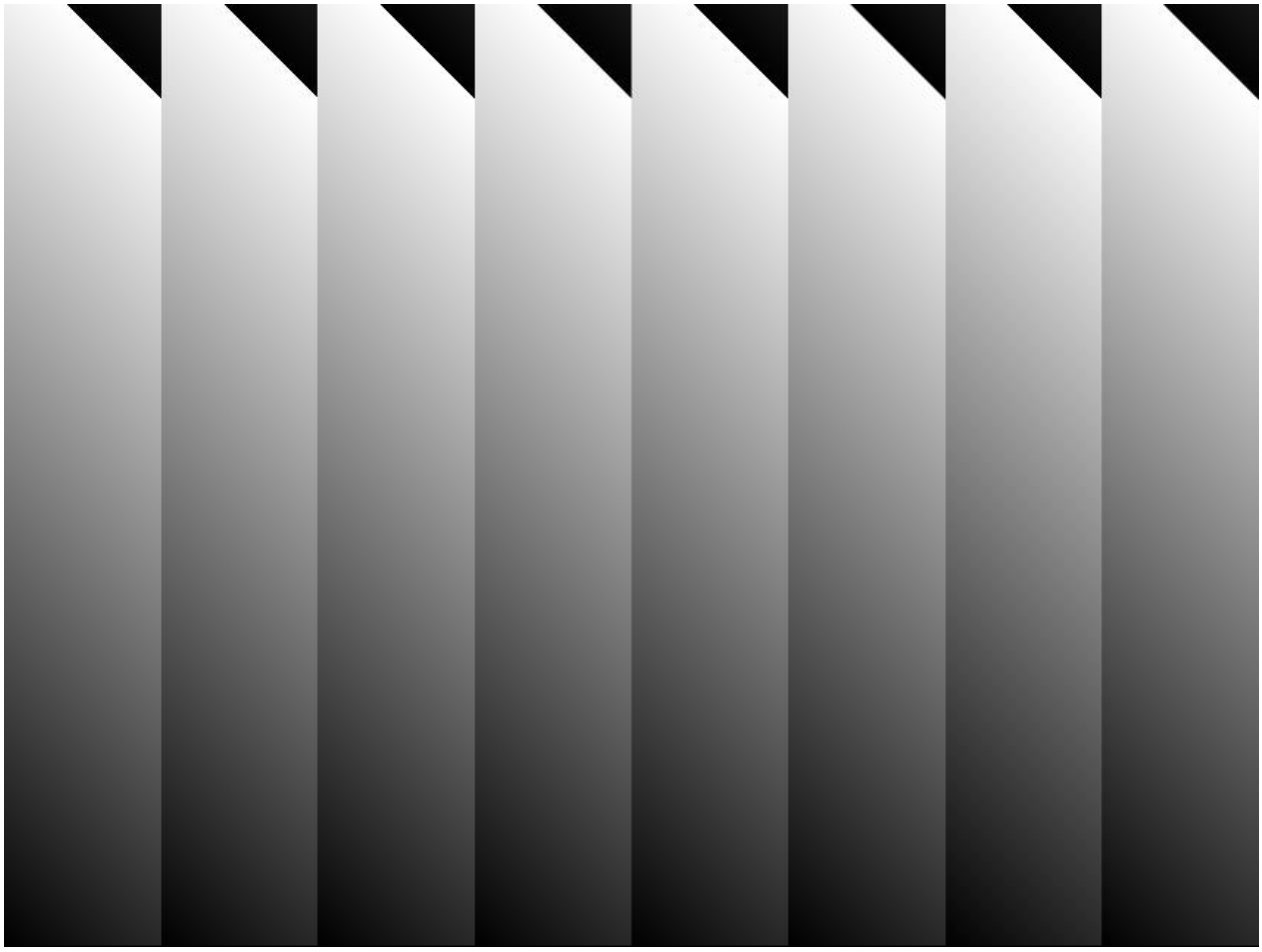


FIGURE 20: TEST PATTERN IMAGE

5 IMAGE SENSOR PROGRAMMING

This section explains how the CMV20000 can be programmed using the on-board sequencer registers.

5.1 EXPOSURE MODES

The exposure time can be programmed in two ways, externally or internally. Externally, the exposure time is defined as the time between the rising edge of T_EXP1 and the rising edge of FRAME_REQ (see section 3.10 for more details). Internally, the exposure time is set by uploading the desired value to the corresponding sequencer register.

The table below gives an overview of the registers involved in the exposure mode.

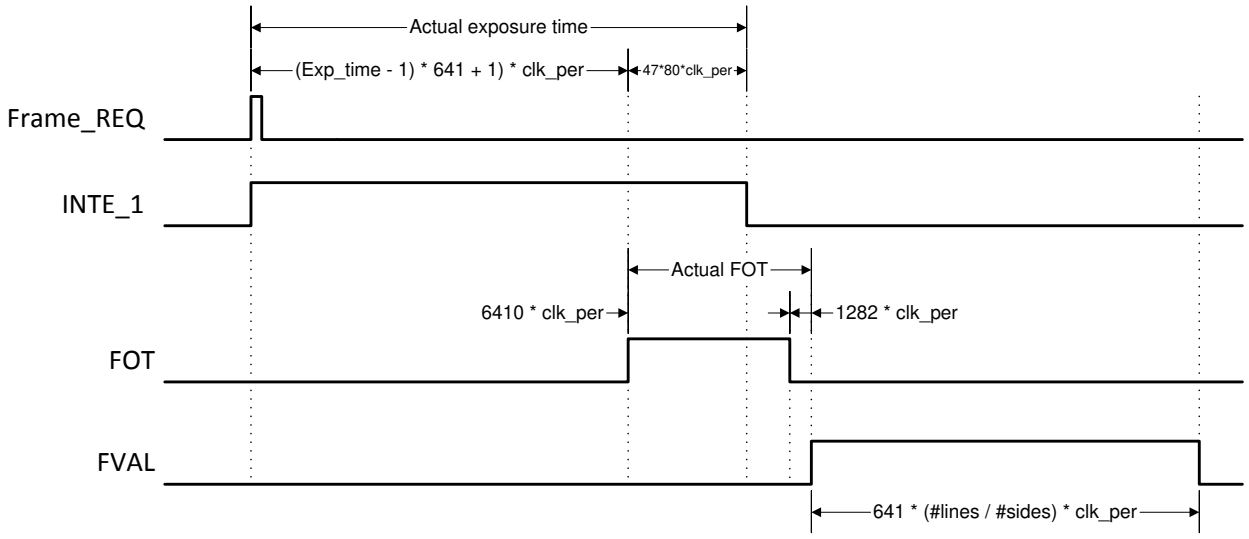
Exposure time settings			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_ext	81[0]	0	0: Exposure time is defined by the value uploaded in the sequencer register (32-33) 1: Exposure time is defined by the pulses applied to the T_EXP1 and FRAME_REQ pins.
Exp_time	32-33	3840	When the Exp_ext register is set to '0', the value in this register defines the exposure time according to the formula below. Minimum = 1.

$$Actual\ Exposure\ time = \big(((Exp\_\text{time} - 1) * 641) + 1 + (47 * reg82)\big) * clk\_per$$

Here clk_per is the period of the input LVDS_CLK multiplied by 12 (so for 480MHz this is 25ns). The minimum exposure time then becomes 94µs.

5.1.1 FRAME TIMING

A detailed view of the frame timing can be seen below.



5.2 HIGH DYNAMIC RANGE MODE

5.2.1 PIECEWISE LINEAR RESPONSE

The CMV20000 has the possibility to achieve a high optical dynamic range by using a piecewise linear response. This feature will clip illuminated pixels which reach a programmable voltage, while leaving the darker pixels untouched.

The clipping level can be adjusted 2 times within one exposure time to achieve a maximum of 3 slopes in the response curve. More details can be found in the figure below.

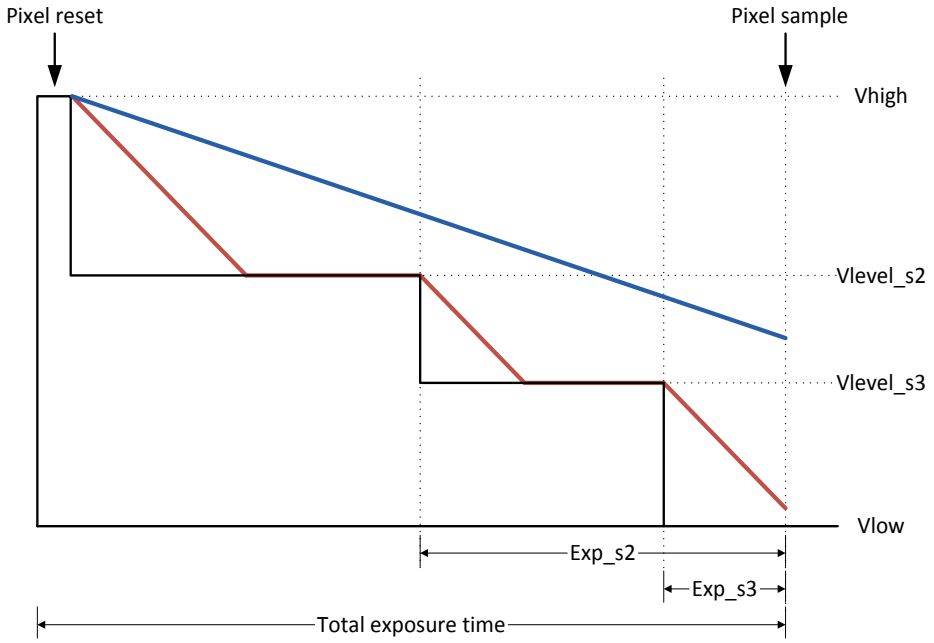


FIGURE 21: PIECEWISE LINEAR RESPONSE DETAILS

In the figure above, the red lines represent a pixel on which a large amount of light is falling. The blue line represents a pixel on which less light is falling. As shown in the figure, the bright pixel is held to a programmable voltage for a programmable time during the exposure time. This happens two times to make sure that at the end of the exposure time the pixel is not saturated. The darker pixel is not influenced and will have a normal response. The Vlevel_s2/3 voltages and different exposure times are programmable using the sequencer registers. Using this feature, a response as detailed in the figure below can be achieved. The placement of the kneepoints in X is controlled by the Vlevel_s2/3 programming, while the slope of the segments is controlled by the programmed exposure times.

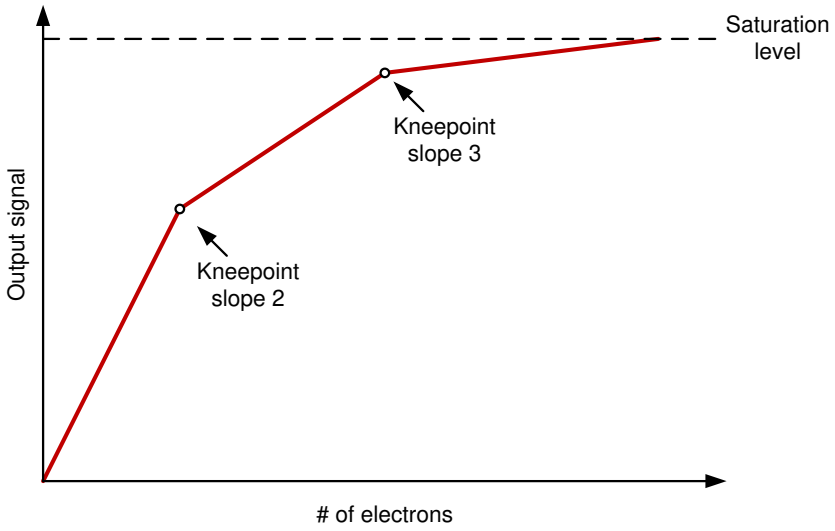


FIGURE 22: PIECEWISE LINEAR RESPONSE

5.2.1.1 PIECEWISE LINEAR RESPONSE WITH INTERNAL EXPOSURE MODE

The following registers need to be programmed when a piecewise linear response in internal exposure mode is desired.

HDR settings – PLR			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_time	32-33	3840	The value in this register defines the total exposure time according following formula: ((*Exp_time - 1) x 641 + 1 + 47 x FOT_mult) x clk_per*, where clk_per is the period of the master input clock.
Nr_slopes	37[1:0]	1	The value in this register defines the number of slopes (min=1, max=3).
Exp_s2	39-40	0	The value in this register defines the exposure time from the start of the second slope to the end of the total exposure time. Formula: ((*Exp_s2 - 1) x 641 + 1 + 47 x FOT_mult) x clk_per*, where clk_per is the period of the master input clock.
Exp_s3	42-43	0	The value in this register defines the exposure time from the start of the third slope to the end of the total exposure time. Formula: ((*Exp_s3 - 1) x 641 + 1 + 47 x FOT_mult) x clk_per*, where clk_per is the period of the master input clock.
Vlevel_s2	114[6:0]	64	Bit[6] = enable Bit[5:0] dac value Low level voltage during dual slope operation. The value in this register defines the Vlevel_s2 voltage (DAC setting). The DAC range goes from 0 to 2.1V.
Vlevel_s3	115[6:0]	64	Bit[6] = enable Bit[5:0] dac value Low level voltage during triple slope operation. The value in this register defines the Vlevel_s3 voltage (DAC setting). The DAC range goes from 0 to 2.1V.

5.2.1.2 PIECEWISE LINEAR RESPONSE WITH EXTERNAL EXPOSURE MODE

When external exposure time is used and a piecewise linear response is desired, the following registers should be programmed.

HDR settings – PLR			
Register name	**Register address**	**Default value**	**Description of the value**
Nr_slopes_ex	15[1:0]	1	The value in this register defines the number of slopes (min=1, max=3).
Vlevel_s2_ex	112[6:0]	64	Bit[6] = enable Bit[5:0] dac value Low level voltage during dual slope operation. The value in this register defines the Vlevel_s2 voltage (DAC setting). The DAC range goes from 0 to 2.1V.
Vlevel_s3_ex	113[6:0]	64	Bit[6] = enable Bit[5:0] dac value Low level voltage during triple slope operation. The value in this register defines the Vlevel_s3 voltage (DAC setting). The DAC range goes from 0 to 2.1V.