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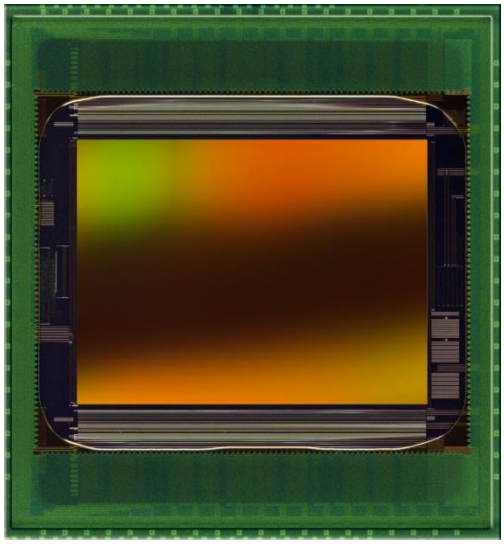
VGA resolution CMOS image sensor

Datasheet



Change record

Issue	Date	Modification
1	13/04/2011	Origination
1.1	5/8/2011	Update after tape out
1.2	20/10/2011	Update after samples test and debug
1.3	25/4/2012	Updated maximum output rate from 600Mbps to 300 Mbps
1.4	22/08/2012	Updated recommended register values Added Spectral Response and QE graphs
1.5	28/09/2012	Updated recommended register values Updated supply settings
1.6	19/12/2012	Removed Draft status Updated Part Numbers
1.7	8/1/2012	Updated VDD18 range
2.0	05/06/2013	Updated: - maximum output rate from 300Mbps to 480Mbps - Full Well Charge: 20ke$^-$ - Conversion factor: 0.2LSB/e$^-$ - Dynamic range: 60dB - Dark current: 125e$^-$/s - Total power: 700mW - VDDPIX: 3.3V - VDD18 renamed to VDD20 - Supply settings - FOT calculation and value - Piecewise Linear Response details - PLR external mode pulse requirements - Bit mode details - Recommended registers Added: - Temperature sensor formulas and graphs - Output skew - Control channel test pin (Test3) programming - Disable PLL - Actual exposure calculations - ADC vs actual gain - Detailed frame cycle timing
V2.1	03/07/2013	Updated: - Detailed frame cycle timing - Exposure calculation
V2.2	08/07/2013	Added: - Color and mono QE Updated: - VDDPIX to 3.0V - Recommended value for reg 106 = 90
V2.3	20/08/2013	Updated: - Exposure time calculation

Issue	Date	Modification
V2.4	05/03/2014	Updated: - Assembly thickness dimensions (details PCN-01) - Added '0'-bits in 8/10bit are LSB - Ch5.7: reg69 to 9 for parallel output mode - Piecewise Linear response Figure 32 - PLL settings ch. 5.10 - Disable PLL settings ch. 5.11 - LVDS output skew - Part Number Added: - Location of pixel(0,0) in assembly drawing - Limitations when using or disabling the PLL (ch. 5.10 & ch.5.11)
V2.5	28/10/2014	Updated: - FOT description (ch 3.6) - Exposure timing (ch 5.1) - SPI_OUT is low when SPI_EN is low - No TP between FOT and FVAL (ch 4.1.5) - Supply settings - Rename VDD18 to VDD20 in pin list - Reflow soldering details (ch 12.1.1) Added: - MSL-5 (ch 12.1) Removed: - Wave soldering
V2.6	19/06/2015	Updated: - Baking condition 24h-48h → 12h - SPI I/O's are pulled low when not enabled - Frame rate calculation ch 3.6 - Fig. Figure 30: Frame cycle timing - Assembly drawing Added: - Figure 27: Detailed timing diagram - Excessive light precaution
V2.7	09/09/2015	Updated: - Removed ES label from part numbers - Temperature sensor typical values - ADC vs. clock speed
V2.8	12/10/2015	Added: - Test image Updated: - Reflow profile
V2.9	23/10/2015	Updated: - MSL and solder profile following J-STD-020 - Replaced "1.8V" notations with VDD20 Added: - ESD level
V2.10	29/02/2016	Updated: - Recommended PLL reg83 187 → 155 (for 40MHz) Added: - Exposure delay - Pin list connection to internal blocks

Disclaimer

This is a preliminary datasheet. CMOSIS reserves the right to change the product, specification and other information contained in this document without notice. Although CMOSIS does its best efforts to provide correct information, this is not warranted.

Table of Contents

1 INTRODUCTION

1.1 OVERVIEW

The CMV300 is a high speed CMOS image sensor with 648 by 488 pixels (1/3 optical inch) developed for machine vision applications. The image array consists of 7.4µm x 7.4µm pipelined global shutter pixels which allow exposure during read out, while performing CDS operation. The image sensor has 4 8, 10 or 12 bit digital LVDS outputs (serial) or one 10 bit parallel CMOS output. The image sensor also integrates a programmable gain amplifier and offset regulation. Each LVDS channel runs at 480 Mbps maximum which results in 480 fps frame rate at full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes.

1.2 FEATURES

- 648 * 488 active pixels on a 7.4µm pitch
- 8 Dark reference and dummy rows and columns
- Frame rate 480 frames/sec @ 640 * 480 resolution
- Row windowing capability
- X-Y mirroring function
- Master clock: 10-40MHz
- 4 LVDS-outputs @ 480Mbit/s (480 fps) multiplexable to 2 (240fps) and 1 (120 fps) outputs
- One 10 bit parallel CMOS output running at maximum 40 MHz (120 fps)
- LVDS control line with frame and line information
- LVDS DDR output clock to sample data on the receiving end
- 12 bit ADC output at maximum frame rate
- Multiple High Dynamic Range modes supported
- On chip temperature sensor
- On chip timing generation
- On chip black reference
- SPI-control
- Chip scale package (8 x 8 BGA pins)
- 3.3V and 2.2V signaling
- Available in panchromatic and Bayer (RGB)

1.3 SPECIFICATIONS

- Full well charge: 20Ke$^-$
- Sensitivity: 6 V/lux.s (with microlenses)
- Dark noise: 20e$^-$ RMS
- Conversion factor: 0.2LSB/e$^-$ (12 bit mode) at recommended gain
- Dynamic range: 60 dB
- Extended dynamic range: piecewise linear response or interleaved read-out
- Parasitic light sensitivity: 1/50 000
- Dark current: 120 e/s (@ 25C die temperature)
- Fixed pattern noise: <4 LSB (12 bit mode, <0.1% of full swing, standard deviation on full image)
- Power consumption: 700mW

1.4 CONNECTION DIAGRAM

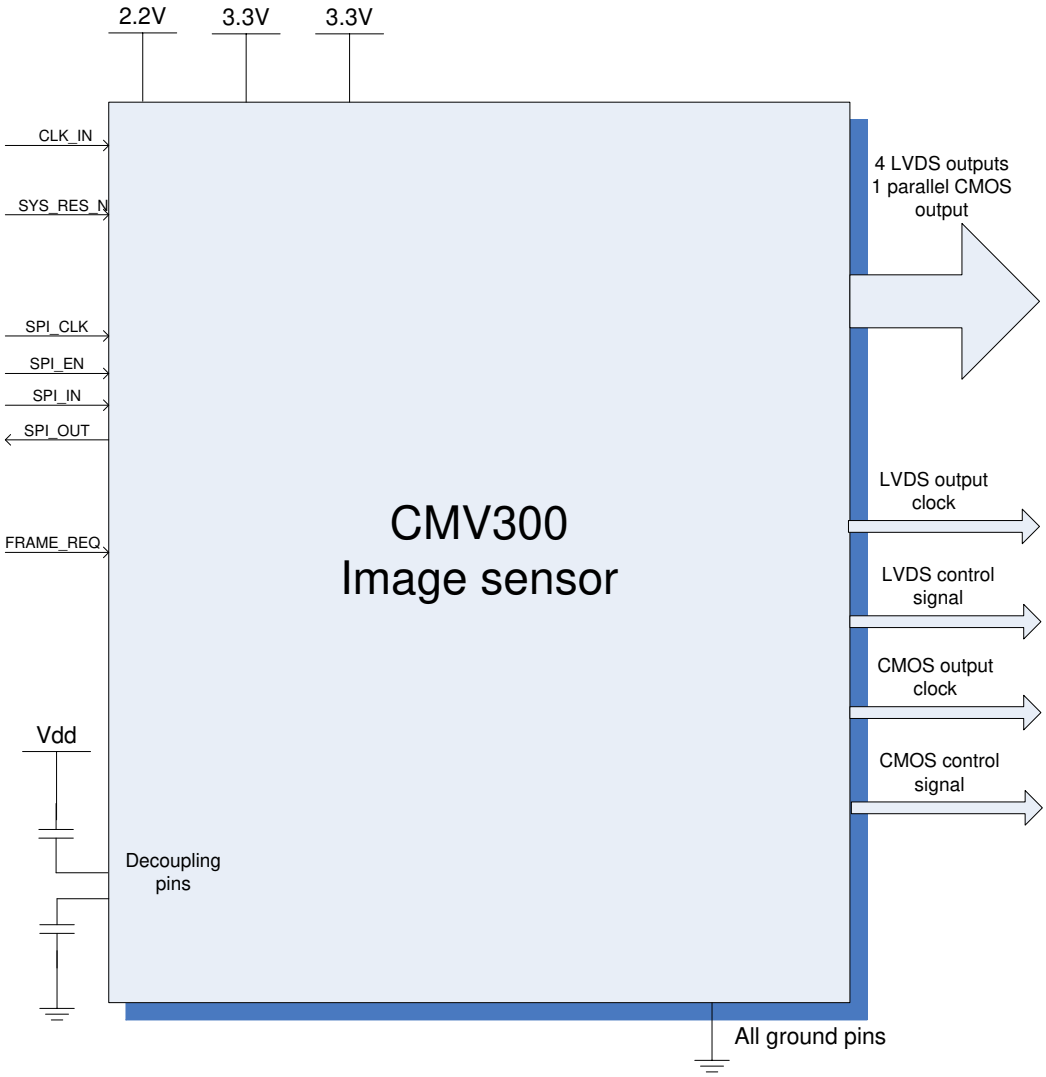


FIGURE 1: CONNECTION DIAGRAM FOR THE CMV300 IMAGE SENSOR

Please look at the pin list for a detailed description of all pins and their proper connections. Some optional pins are not displayed on the figure above. The exact pin numbers can be found in the pin list and on the package drawing.

2 SENSOR ARCHITECTURE

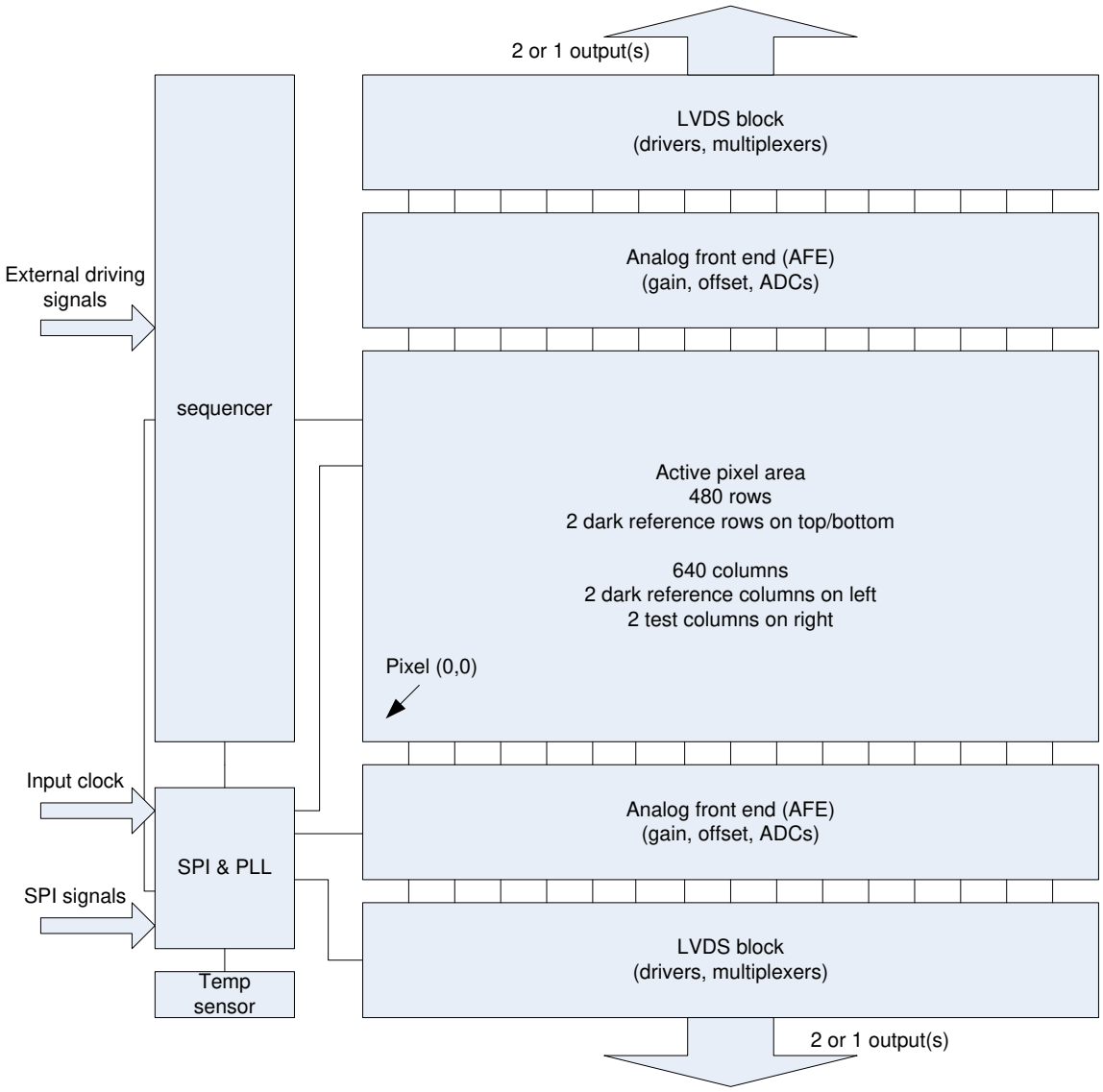


FIGURE 2: SENSOR BLOCK DIAGRAM

Figure 2 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and is then read out sequentially, row-by-row. On the pixel output, an analog gain is possible. The pixel values then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels or one parallel CMOS output. Each LVDS channel reads out 324 adjacent columns of the array. Two rows are being read out at the same time when 4 LVDS channels are used. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface. A temperature sensor which can be read out over the SPI interface is also included.

2.1 PIXEL ARRAY

The pixel array consists of 648 x 488 square global shutter pixels with a pitch of 7.4µm (7.4µm x 7.4µm). The pixels are designed to achieve maximum sensitivity with low noise and low PLS specifications. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency (>50%). There are 4 dark reference rows available on the sensor (rows 0, 1, 486 and 487) and 2 dark reference columns (column 0 and 1). Columns 646 and 647 are test

columns and do not contain useful image data. This means that the useable image data area is 644 x 484. This results in an optical area of 1/3 optical inch (5.9 mm). This means that off-the-shelf C-mount lenses can be used.

2.2 ANALOG FRONT END

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface). The column ADC converts the analog pixel value to a 12 bit value. A digital offset can also be applied to the output of the column ADC's. All gain and offset settings can be programmed using the SPI interface.

2.3 LVDS BLOCK

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at maximum 300Mbps. The sensor has 6 LVDS output pairs:

- 4 Data channels
- 1 Control channel
- 1 Clock channel

The 4 data channels are used to transfer 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels, among other useful sensor status information. Details on the LVDS timing and format can be found in section 4 of this document.

2.4 PARALLEL CMOS OUTPUT BLOCK

The parallel CMOS block sends the digital data coming from the column ADC to a standard CMOS parallel output (supplied by VDD20) running at maximum 25MHz. The parallel output has 13 pins:

- 10 Data channels
- 2 Control channels
- 1 Clock channel

The 10 data channels are used to transfer 10-bit pixel data from the sensor to a receiver. The output clock channel transports a clock, synchronous to the data on the data channels. This clock can be used at the receiving end to sample the data. The data on the control channels contains status information on the validity of the data on the data channels (LVAL, DVAL). Details on the parallel CMOS timing and format can be found in section 4 of this document.

2.5 SEQUENCER

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control signals. This sequencer can be activated and programmed through the SPI interface. A detailed description of the SPI registers and sensor (sequencer) programming can be found in section 5 of this document.

2.6 SPI INTERFACE

The SPI interface is used to load the sequencer registers with data. The data in these registers is used by the sequencer while driving and reading out the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system. Section 5 contains more details on register programming.

2.7 TEMPERATURE SENSOR

A 16-bit digital temperature sensor is included in the image sensor and can be read out through the SPI-interface. The on-chip temperature can be obtained by reading out the registers with address 78 and 79 (in burst mode, see section 3.9.2 for more details on this mode).

A calibration of the temperature sensor is needed for absolute temperature measurements. A typical temperature sensor output vs. temperature curve can be found below. The temperature sensor requires a running input clock (CLK_IN), the other functions of the image sensor can be operational or in standby mode.

A typical value of the sensor at 0°C is about $\frac{f[MHz]}{25} * 5100$ DN. A typical slope will be around $\frac{f[MHz]}{25} * 15.5$ DN/°C. A sensor will typically heat up about 15°C above ambient temperature.

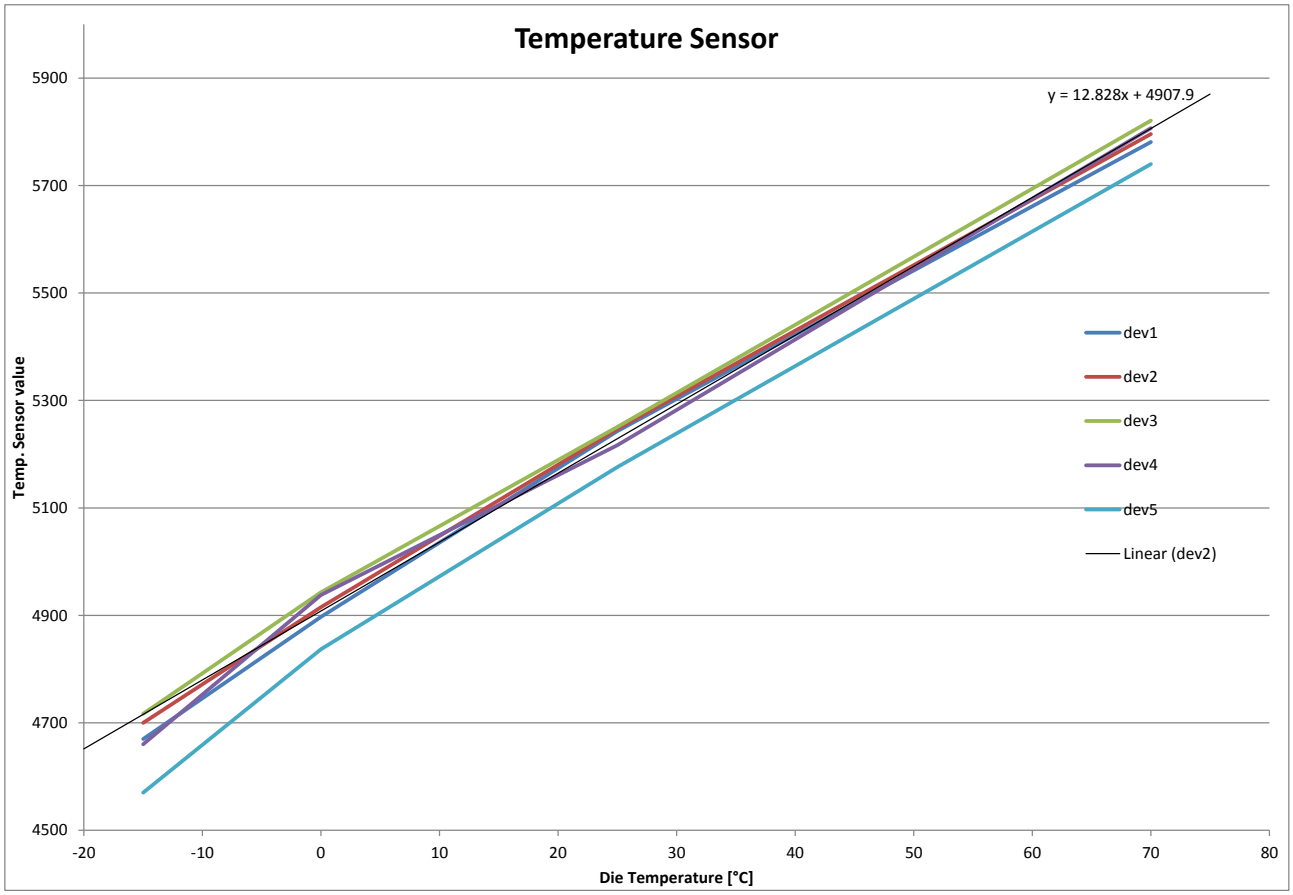


FIGURE 3: TYPICAL OUTPUT OF THE TEMPERATURE SENSOR OF SEVERAL CMV300 SENSORS @ 25MHZ

3 DRIVING THE CMV300

3.1 SUPPLY SETTINGS

The CMV300 image sensor has the following supply settings:

Supply name	Usage	Recommended value	Maximum tolerance	DC Current Idle	DC Current Nom.	DC Current Max.
VDD20	LVDS, ADC	2.2V	-0.4/+0.05V	175mA	220mA	270mA
VDD33	Dig. I/O. SPI, ADC	3.3V	+/-0.3V	25mA	30mA	30mA
VDDpix	Pixel array supply	3.0V	+/-0.3V	1mA	5mA	5mA
			Total DC Power	470mW	600mW	710mW

See pin list for exact pin numbers for every supply.

The maximum currents will be reached during readout. The current of the VDD20 supply depends on the average value of the image (a pure white image will draw 270mA). Idle is when the sensor is idle (not reading out or integrating) and nominal is a 50% grey average image. These values are for a sensor running at 40MHz. The power consumption decreases with the clock speed albeit little.

Besides these DC currents, decoupling should be foreseen to suppress current spikes. VDDPIX can generate current spikes up to 500mA during FOT. Because this supply is the pixel array supply, the voltage should be as noise-free as possible, because noise can ripple through to the image. We propose to use 5x 100nF capacitors on each supply as close to the sensor as possible.

3.2 BIASING

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

3.3 DIGITAL INPUT PINS

The table below gives an overview of the external pins used to drive the sensor.

Pin name	Description
CLK_IN	Master input clock, frequency range between 10 and 40 MHz
SYS_RES_N	System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up
FRAME_REQ	Frame request pin. This signal should be at least one period of CLK_IN long to assure detection.
SPI_IN	Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
SPI_EN	SPI enable pin. When this pin is high the data should be written/read on the SPI
SPI_CLK	SPI clock. This is the clock on which the SPI runs (max 40Mz)

Pin name	Description
T_EXP1	Input pin which can be used to program the exposure time externally. This signal should be at least one period of CLK_IN long to assure detection.
T_EXP2	Input pin which can be used to program the exposure time externally in interleaved high dynamic range mode. This signal should be at least one period of CLK_IN long to assure detection.

3.4 ELECTRICAL IO SPECIFICATIONS

3.4.1 DIGITAL IO CMOS/TTL DC SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{IH}	High level input voltage		2.0		VDD33	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	VDD=3.3V I_{OH}=-2mA	2.4			V
V_{OL}	Low level output voltage	VDD=3.3V I_{OL}=2mA			0.4	V

3.4.2 PARALLEL CMOS OUTPUT DC SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{OH}	High level output voltage	VDD20=2.2V I_{OH}=-2mA	2.0			V
V_{OL}	Low level output voltage	VDD20=2.2V I_{OL}=2mA			0.2	V

3.4.3 LVDS RECEIVER SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{ID}	Differential input voltage	Steady state	100	350	600	mV
V_{IC}	Receiver input range	Steady state	0.0		2.4	V
I_{ID}	Receiver input current	$V_{INP\|INN}$=1.2V±50mV, 0≤ $V_{INP\|INN}$≤2.4V			20	µA
ΔI_{ID}	Receiver input current difference	$\|I_{INP} - I_{INN}\|$			6	µA

3.4.4 LVDS DRIVER SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{OD}	Differential output voltage	Steady State, RL = 100Ω	247	350	454	mV
ΔV_{OD}	Difference in V_{OD} between complementary output states	Steady State, RL = 100Ω			50	mV
V_{OC}	Common mode voltage	Steady State, RL = 100Ω	1.125	1.25	1.375	V

Parameter	Description	Conditions	min	typ	max	Units
ΔV_{OC}	Difference in V_{OC} between complementary output states	Steady State, RL = 100Ω			50	mV
$I_{OS,GND}$	Output short circuit current to ground	V_{OUTP}=V_{OUTN}=GND			24	mA
$I_{OS,PN}$	Output short circuit current	V_{OUTP}=V_{OUTN}			12	mA

3.5 INPUT CLOCK

The input clock (CLK_IN) defines the output data rate of the CMV300. This master clock (CLK_IN) is 12 times slower than the output date rate. The maximum data rate of the output is 480Mbps which results in a CLK_IN of 40MHz. The minimum frequency is 10MHz for CLK_IN. Any frequency between the minimum and maximum can be applied by the user and will result in a corresponding output data rate. The SPI register with address 83 must be programmed to the correct frequency range when the CLK_IN frequency is changed.

3.6 FRAME RATE CALCULATION

The frame rate of the CMV300 is defined by 2 main factors.

1. Exposure time
2. Read out time

For ease of use we will assume that the exposure time is no longer than the read out time. By assuming this the frame rate is completely defined by the read out time (because the exposure time happens in parallel with the read-out time). The read-out time (and thus the frame rate) is defined by:

1. Output clock speed: max 480Mbps
2. Number of lines read-out
3. Number of outputs used: max 4 LVDS outputs (2 on the top and 2 on the bottom) or one parallel CMOS output

This means that if any of the parameters above is changed, it will have an impact on the frame rate of the CMV300. In normal operation (4 outputs @ 480Mbps, 12 bit and full resolution) this will result in 480 fps.

Total readout time is composed of two parts: FOT (frame overhead time) + image readout time.

$$FOT = \left(\frac{4}{\#\ bottom\ outputs\ used} + \frac{reg58}{4}\right) * 325 * clk\_per$$

With clk_per being the period of CLK_IN. The FOT consists of a time where the pixels are prepared for read out:

$$\left(\frac{reg58}{4}\right) * 325 * clk\_per$$

And an idle time until read out starts, depending on the used channels:

$$\left(\frac{4}{\#\ bottom\ outputs\ used}\right) * 325 * clk\_per$$

With clk_per being equal to one period of CLK_IN and reg58 should be a multiple of 4. The FOT consists of the actual FOT (where the control channel FOT bit is '1') and 2 (using 4 outputs) or 4 (using 2 or 1 outputs) line times where the sensor is idle before read out starts.
When running the CMV300 sensor at 40MHz with 4 outputs and recommended FOT settings this results in: 105.625us.

$$Readout\ time = line\ time * \frac{\#\ lines}{\#\ sides\ used}$$

$$Line\ time = \frac{2 * 325 * clk\_per}{\#\ bottom\ outputs\ used}$$

When running the CMV300 sensor at 40MHz with 4 outputs and reading 480 lines this results in: 1950µs
This results in a total read-out time of 105.625us + 1950µs = 2.055625ms → 486fps for 640 * 480 resolution.

3.7 START-UP SEQUENCE

The following sequence should be followed when the CMV300 is started up in default output mode (300Mbps, 12bit resolution).

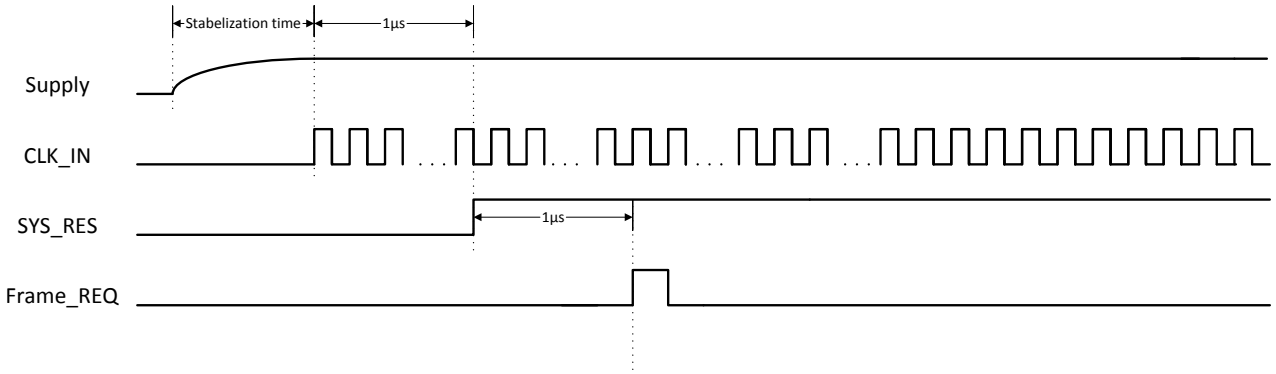


FIGURE 4: START-UP SEQUENCE FOR 300MBPS @ 12-BIT

The master clock (25MHz for 300Mbps in 12-bit mode) should only start after the supplies are stable. The external reset pin should be released at least 1µs after the supplies have become stable. The first frame can be requested 1µs after the reset pin has been released. An optional SPI upload (to program the sequencer) is possible 1µs after the reset pin has been released. In this case the FRAME_REQ pulse must be postponed until after the SPI upload has been completed.

When the CMV300 will be used in 8 or 10-bit mode or at another speed than 300mbps, an SPI upload is necessary to program the sensor. In this case the start-up sequence looks like the diagram below. A PLL lock-time of 1ms should be considered after uploading the register settings and before sending the FRAME_REQ pulse.

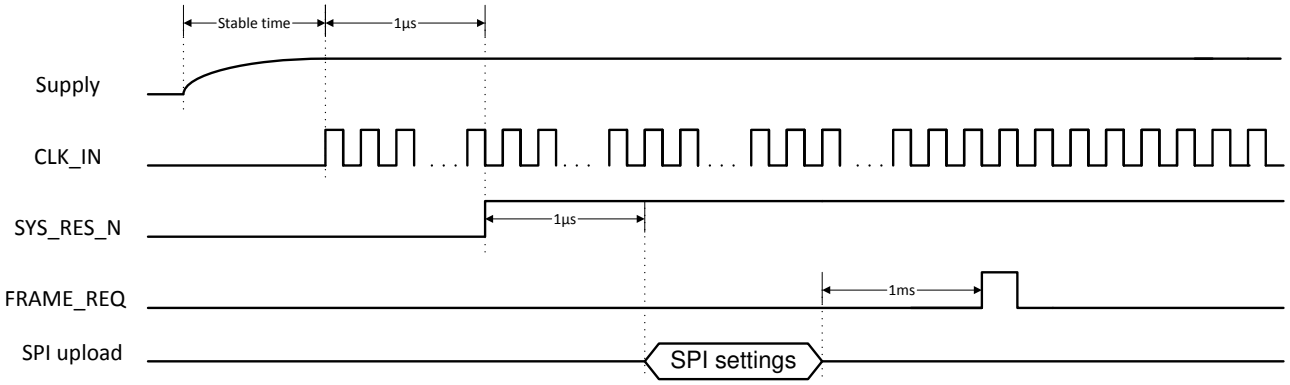


FIGURE 5: START-UP SEQUENCE FOR 8 OR 10 BIT MODE OR ANOTHER SPEED

The following SPI registers should be uploaded in this mode:

1. Bit mode settings (address 68) : set to 8 or 10 bit mode
2. PLL settings (address 83): set to correct PLL range

3.8 RESET SEQUENCE

If a sensor reset is necessary while the sensor is running the following sequence should be followed.

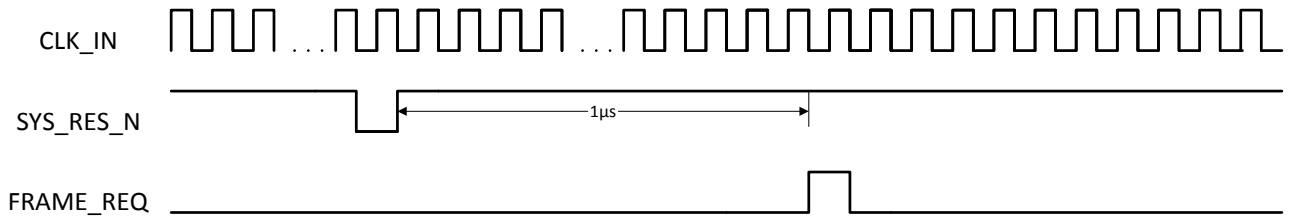


FIGURE 6: RESET SEQUENCE

The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RES_N pin. After the reset there is a minimum time of 1µs needed before a FRAME_REQ pulse can be sent. When a lower clock speed is desired while the sensor is running the reset sequence should be executed. In this case it must be followed by a SPI upload to program the sensor for this lower clock speed.

3.9 SPI PROGRAMMING

Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

SPI I/O's are pulled low when not used/enabled.

3.9.1 SPI WRITE

The timing to write data over the SPI interface can be found below.

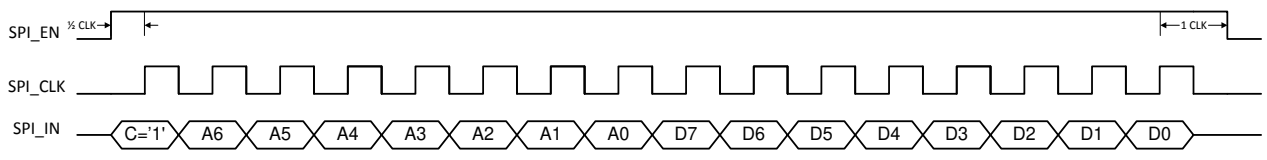


FIGURE 7: SPI WRITE TIMING

The data is sampled by the CMV300 on the rising edge of the SPI_CLK. The SPI_CLK has a maximum frequency of 40MHz. The SPI_EN signal has to be high for half a clock period before the first databit is sampled. SPI_EN has to remain high for 1 clock period after the last databit is sampled. The sampled data will be written in the sequencer on the last falling clock edge, so SPI_CLK has to go low again at the end for the write operation to be successful.

One write action contains 16 databits:

- One control bit: First bit to be sent, indicates whether a read ('0') or write ('1') will occur on the SPI interface.
- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 8 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the figure below for an example of 2 registers being written in burst.

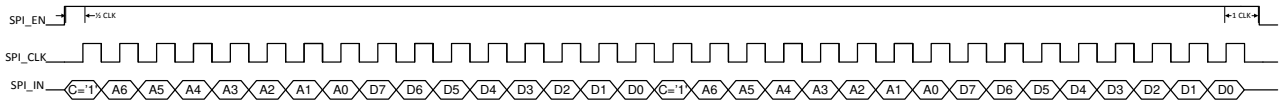


FIGURE 8: SPI WRITE TIMING FOR 2 REGISTERS IN BURST

3.9.2 SPI READ

The timing to read data from the registers over the SPI interface can be found below.

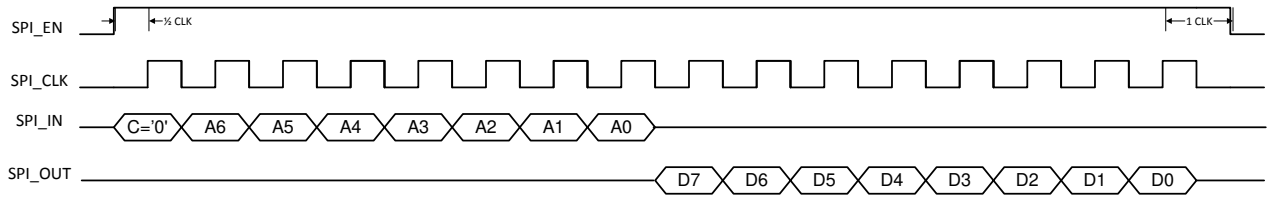


FIGURE 9: SPI READ TIMING

To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made '0'. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK. This means that the data should be sampled by the receiving system on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first. When reading out the temperature sensor over the SPI, addresses 78 and 79 should be read out in burst mode (keep SPI_EN high).

When SPI_EN is low, SPI_OUT will be (pulled) low.

3.10 REQUESTING A FRAME

After starting up the sensor (see section 3.7), a number of frames can be requested by sending a FRAME_REQ pulse. The number of frames can be set by programming the appropriate register (addresses 55 and 56). The default number of frames to be grabbed is 1.

In internal-exposure-time mode, the exposure time will start after this FRAME_REQ pulse. In the external-exposure-time mode, the read-out will start after the FRAME_REQ pulse. Both modes are explained into detail in the sections below.

3.10.1 INTERNAL EXPOSURE CONTROL

In this mode, the exposure time is set by programming the appropriate registers (address 42-44) of the CMV300.

After the high state of the FRAME_REQ pulse is detected, the exposure time will start immediately. When the exposure time ends (as programmed in the registers), the pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). After the FOT, the frame is read-out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one (pipeline mode). See the diagram below for more details.

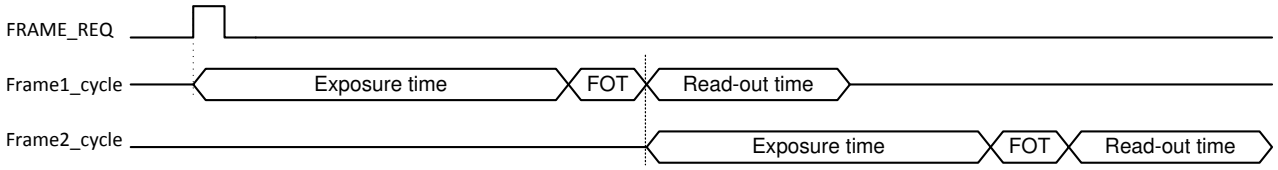


FIGURE 10: REQUEST FOR 2 FRAMES IN INTERNAL- EXPOSURE-TIME MODE

When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame.

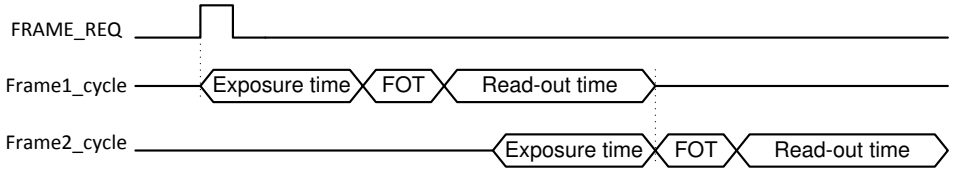


FIGURE 11: REQUEST FOR 2 FRAMES IN INTERNAL-EXPOSURE-TIME MODE WITH EXPOSURE TIME < READ-OUT TIME

3.10.2 EXTERNAL EXPOSURE CONTROL

The exposure time can also be programmed externally by using the T_EXP1 input pin. This mode needs to be enabled by setting the appropriate register (address 41). In this case, the exposure starts when a high state is detected on the T_EXP1 pin. When a high state is detected on the FRAME_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the T_EXP1 pin during or after the read-out of the previous frame.

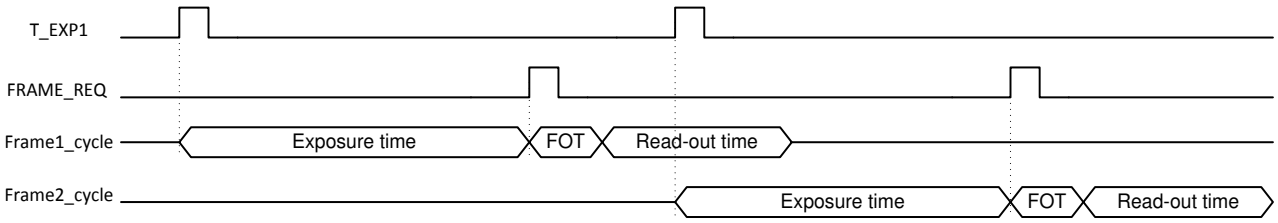


FIGURE 12: REQUEST FOR 2 FRAMES USING EXTERNAL-EXPOSURE-TIME MODE

3.10.3 EXPOSURE DELAY

In internal exposure mode, when reading out an image with an exposure time smaller than the number of lines read out divided by the number outputs used, there will be increase in delay between the frame_req pulse and the actual start of exposure. This delay is equal to:

$$\text{exposure start delay} = (196 * \text{clk\_per}) + \left(\frac{\#\ \text{lines}}{\#\ \text{sides}} - \text{inte\_time}\right)$$

With a minimum of 196 clk_in periods.

For example, when a complete image (488 lines) is read out with 2 sided outputs, and the integration time is 1 line time, the delay will be 244.66 lines. When the integration time is 100 lines, the delay will be 145.66 lines.

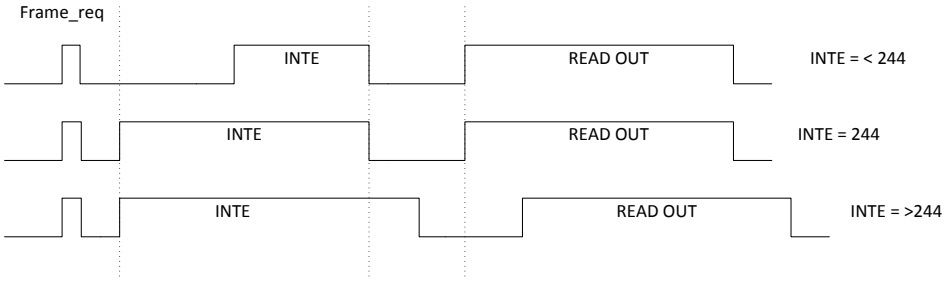


FIGURE 13: EXPOSURE DELAY

If the integration time is longer than the readout time, the delay will always be the minimum. The 1st frame after a reset will always have the minimum delay only.

4 READING OUT THE SENSOR

When reading out the CMV300, the user has a choice to use 4 LVDS outputs (max 480fps) or 1 parallel CMOS output (max 120 fps). This choice is made by connecting pin B2 to VDD33 (LVDS outputs) or GND (parallel CMOS output).

4.1 LVDS DATA OUTPUTS

The CMV300 has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 4 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 6 LVDS output pairs (2 pins for each LVDS channel):

- 4 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 12 pins of the CMV300 are used for the LVDS outputs (8 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs. The 4 data channels are used to transfer the 12-bit, 10-bit or 8-bit pixel data from the sensor to the receiver in the surrounding system. The output clock channel transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 480Mbps output data rate is used, the LVDS output clock will be 240MHz. The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 12-bit words that are transferred synchronous to the 4 data channels.

4.1.1 LVDS LOW-LEVEL PIXEL TIMING

The figures below show the timing for transfer of 8-bit, 10-bit and 12-bit pixel data over one LVDS output. To make the timing more clear, the figures show only the p-channel of each LVDS pair. The data is transferred LSB first, with the transfer of bit D[0] during the high phase of the DDR output clock.

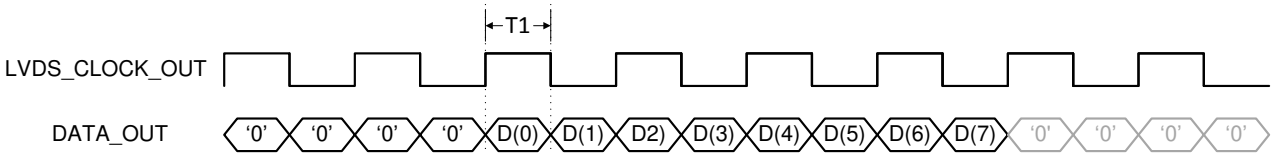


FIGURE 14: 8-BIT PIXEL DATA ON AN LVDS CHANNEL

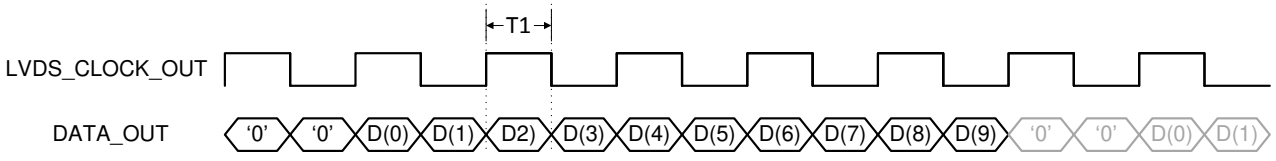


FIGURE 15: 10-BIT PIXEL DATA ON AN LVDS CHANNEL

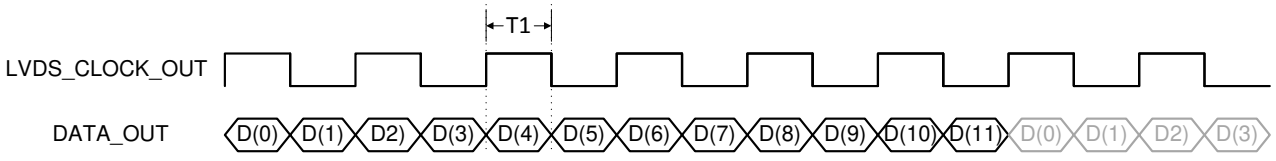


FIGURE 16: 12-BIT PIXEL DATA ON AN LVDS CHANNEL

The time 'T1' in the diagram above is 1/12th of the period of the input clock (CLK_IN) of the CMV300. If a frequency of 40MHz is used for CLK_IN (max), this results in a 240MHz LVDS_CLOCK_OUT.

4.1.2 LVDS READOUT TIMING

The readout of image data is grouped in bursts of 324 pixels per channel (2 rows at the same time). Each pixel is 12 bits of data (see section 4.1.1). One complete pixel period equals one period of the master clock input. For details on pixel remapping and pixel vs channel location please see section 4.1.3 of this document. An overhead time exists between two bursts of 324 pixels. This overhead time has the length of one pixel read-out (i.e. the length of 12 bits at the selected data rate) or one master clock cycle.

4.1.2.1 4 OUTPUT CHANNELS

By default, all 4 data output channels are used to transmit the image data. This means that two entire rows of image data are transferred in one slot of 324 pixel periods (4 x 324 = 1296). Next figure shows the timing for the top and bottom LVDS channels.

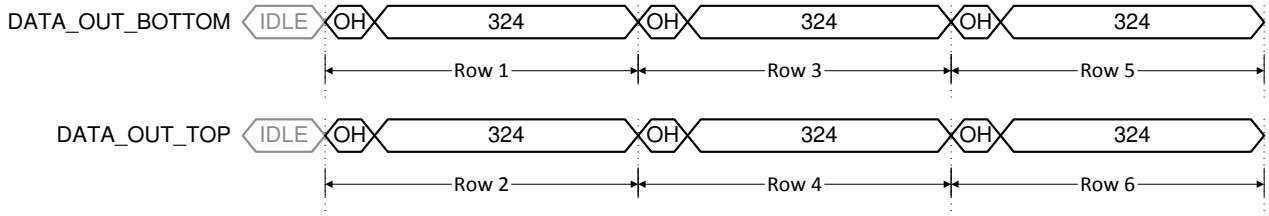


FIGURE 17: OUTPUT TIMING IN DEFAULT 4 CHANNEL MODE

Only when 4 data outputs, running at 300Mbps, are used, the frame rate of 300fps can be achieved (default).

4.1.2.2 2 OUTPUT CHANNELS

The CMV300 has the possibility to use only 2 LVDS output channels. This setting can be programmed in the register with address 57 (see section 5.7). In such multiplexed output mode, only the 2 bottom LVDS channels are used (channel 1 and channel 2). The readout of one row takes 1*324 periods. Next figure shows the timing for the bottom LVDS channels.

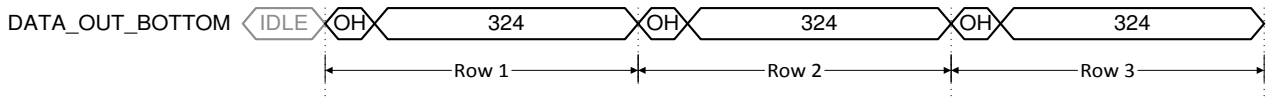


FIGURE 18: OUTPUT TIMING IN 2 CHANNEL MODE

In this 2 channel mode, the frame rate is reduced with a factor of 2 compared to 4 channel mode.

4.1.2.3 1 OUTPUT CHANNEL

The CMV300 has also the possibility to use only 1 LVDS output channel. This setting can be programmed in the register with address 57 (see section 5.7). In such multiplexed output mode, only 1 of the bottom 2 LVDS channels is used (channel 1) and the readout of one row takes 2*324 periods.

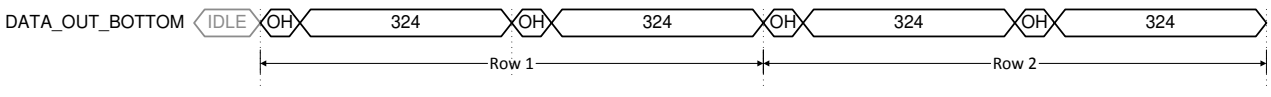


FIGURE 19: OUTPUT TIMING IN OF 1 CHANNEL MODE

In this 1 channel mode, the frame rate is reduced with a factor of 4 compared to 4 channel mode.

4.1.3 PIXEL REMAPPING

Depending on the number of output channels, the pixels are read out by different channels and come out at a different moment in time. With the details from the next sections, the end user is able to remap the pixel values at the output to their correct image array location.

4.1.3.1 4 OUTPUTS

The figure below shows the location of the image pixels versus the output channel of the image sensor.

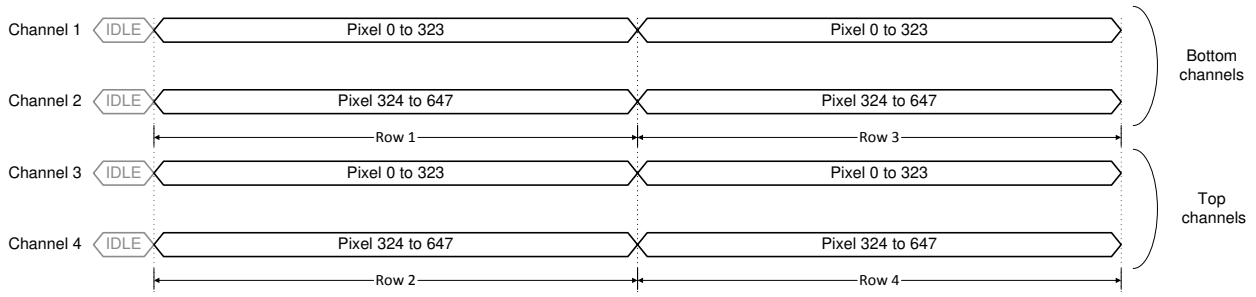


FIGURE 20: PIXEL REMAPPING FOR 4 OUTPUT CHANNELS

4 bursts (2 x 2) of 324 pixels happen in parallel on the data outputs. This means that two complete rows are read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 488 rows being read out.

4.1.3.2 2 OUTPUTS

When only 2 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 2 bursts of 324 pixels happen in parallel on the data outputs. This means that one complete row is read out in one burst. The time needed to read out two rows is doubled compared to when 4 outputs are used. The top LVDS channels are not being used in this mode, so they can be turned off by setting the correct bits in the register with address 81. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 488 rows being read out.

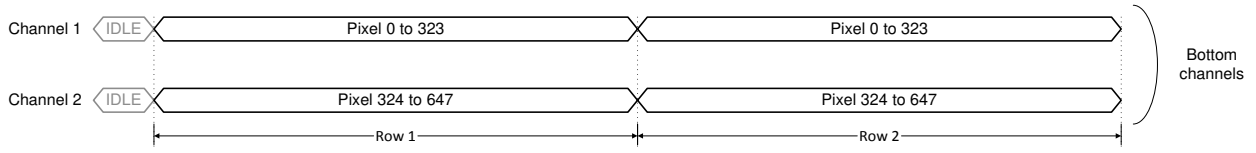


FIGURE 21: PIXEL REMAPPING FOR 2 OUTPUT CHANNELS

4.1.3.3 1 OUTPUT

When only 1 output is used, 1 burst of 324 pixels happens on the data outputs. This means that one complete row is read out in 2 bursts. The time needed to read out one row is 2x longer compared to when 2 outputs are used. The top LVDS channels are not being used in this mode, so these and the remaining bottom channel can be turned off by setting the correct bits in the register with address 81. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be readout depends on the value in the corresponding register. By default there are 488 rows being read out

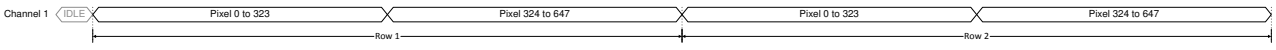


FIGURE 22: PIXEL REMAPPING FOR 1 OUTPUT CHANNEL

4.1.4 CONTROL CHANNEL

The CMV300 has one LVDS output channel dedicated for the valid data synchronization and timing of the output channels. The end user must use this channel to know when valid image data or training data is available on the data output channels.

The control channel transfers status information in 12-bit word format. Every bit of the word has a specific function. Next table describes the function of the individual bits.

Bit	Function	Description
[0]	DVAL	Indicates valid pixel data on the outputs
[1]	LVAL	Indicates validity of the readout of a row
[2]	FVAL	Indicates the validity of the readout of a frame
[3]	FOT	Indicates when the sensor is in FOT (sampling of image data in pixels) (*)
[4]	INTE1	Indicates when pixels of integration block 1 are integrating (*)
[5]	INTE2	Indicates when pixels of integration block 2 are integrating (*)
[6]	'0'	Constant zero
[7]	'1'	Constant one
[8]	'0'	Constant zero
[9]	'0'	Constant zero
[10]	'0'	Constant zero
[11]	'0'	Constant zero

(*)Note: The status bits are purely informational. These bits are not required to know when the data is valid. The DVAL, LVAL and FVAL signals are sufficient to know when to sample the image data.

Pin C6 (Test3 / CLK_OUT) can be programmed to map some control bits for easy measurement. Register 69 is used for this programming:

Register 69 Value	T_dig1
0	DVAL
1	LVAL
2	FVAL
6	FOT
7	INTE1
8	INTE2
9	CLK_OUT

4.1.4.1 DVAL, LVAL, FVAL

The first three bits of the control word must be used to identify valid data and the readout status. Next figure shows the timing of the DVAL, LVAL and FVAL bits of the control channel with an example of the readout of a frame of 3 rows (default is 488 rows). This example uses the default mode of 4 outputs (2 outputs on each side).

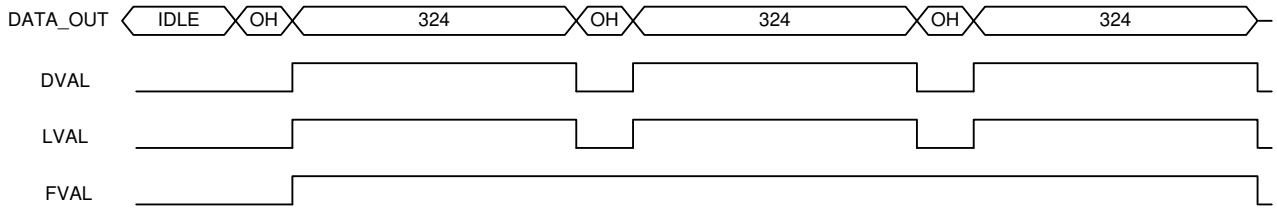


FIGURE 23: DVAL, LVAL AND FVAL TIMING IN 4 OUTPUT MODE

When only 1 output (on one side) is used, the line read-out time is 2x longer. The control channel takes this into account and the timing in this mode looks like the diagram below.

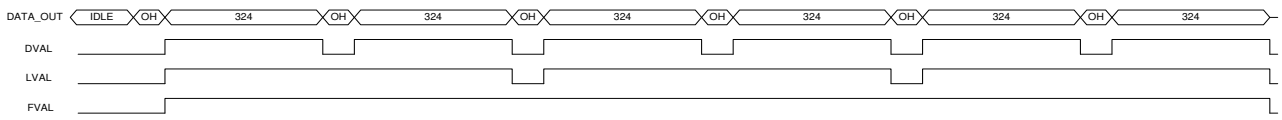


FIGURE 24: DVAL, LVAL AND FVAL TIMING IN 1 OUTPUT MODE

4.1.5 TRAINING DATA

The LVDS outputs are not perfectly edge aligned. This alignment has to be done in the receiving system. You can see the typical output skew in Figure 25. This skew is independent of the clock speed used. To synchronize the receiving