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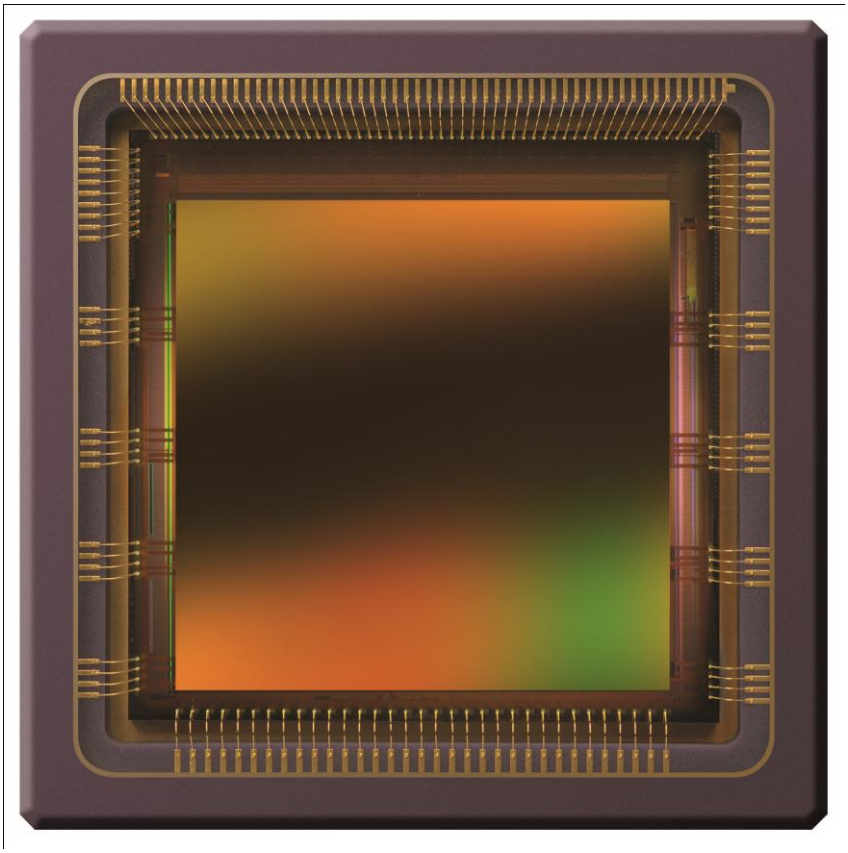
4.2 Megapixel machine vision CMOS image sensor

Datasheet



Change record

Issue	Date	Modification
1	06/05/09	Origination
1.1	12/11/09	- Corrected register address of sub_s[7:0] to '35' (p 29/30/33)
1.2	11/01/10	Adjusted min input frequency (section 3.3) Changed 3.0V to 2.8V for Vpix
1.3	14/01/10	Adjusted pin width in package drawing
2	29/03/10	Added spectral response Added spectral response for color devices Updated specifications for version 2 devices Changed VDD18 to VDD20 Added ordering info Added handling and soldering procedures Removed "confidential" in footer Added recommended and adjustabel register settings
2.1	22/7/10	Frame rate calculation added
2.2	2/8/10	Read-out in 12 bit mode added
2.3	1/9/10	Added exposure time offset (0.65 x register73 x clk_per x 129)
2.4	17/9/10	Added Vtf_l1 to GND remark
2.5	19/10/10	Added E12 spectral response curve and part numbers

Disclaimer

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Table of Contents

1 INTRODUCTION

1.1 OVERVIEW

The CMV4000 is a high speed CMOS image sensor with 2048 by 2048 pixels (1 optical inch) developed for machine vision applications. The image array consists of 5.5µm x 5.5µm pipelined global shutter pixels which allow exposure during read out, while performing CDS operation. The image sensor has sixteen 10- or 12-bit digital LVDS outputs (serial). The image sensor also integrates a programmable gain amplifier and offset regulation. Each channel runs at 480 Mbps maximum which results in 180 fps frame rate at full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes.

1.2 FEATURES

- 2048 * 2048 active pixels on a 5.5µm pitch
- frame rate 180 Frames/sec
- row windowing capability
- X-Y mirroring function
- Master clocks: 5-48MHz and 50-480MHz (LVDS)
- 16 LVDS-outputs @480MHz multiplexable to 8, 4 and 2 at reduced frame rate
- LVDS control line with frame and line information
- LVDS DDR output clock to sample data on the receiving end
- 10 bit ADC output at maximum frame rate, 12 bit ADC at reduced frame rate
- Multiple High Dynamic Range modes supported
- On chip temperature sensor
- On chip timing generation
- SPI-control
- Ceramic µPGA package (95 pins)
- 3.3V signaling
- Available in panchromatic and Bayer (RGB)

1.3 SPECIFICATIONS

- Full well charge: 13.5Ke$^-$
- Sensitivity: 4.64 V/lux.s (with microlenses)
- Dark noise: 13e$^-$ RMS
- Conversion factor: 0.075LSB/e$^-$ (10 bit mode) at unity gain
- SNR: 60 dB
- Extended dynamic range: Piecewise linear response or interleaved read-out
- Parasitic light sensitivity: 1/50 000
- Dark current: 125 e/s (@ 25C die temp)
- Fixed pattern noise: <1 LSB (10 bit mode, <0.1% of full swing, standard deviation on full image)
- Power consumption: 600mW

1.4 CONNECTION DIAGRAM

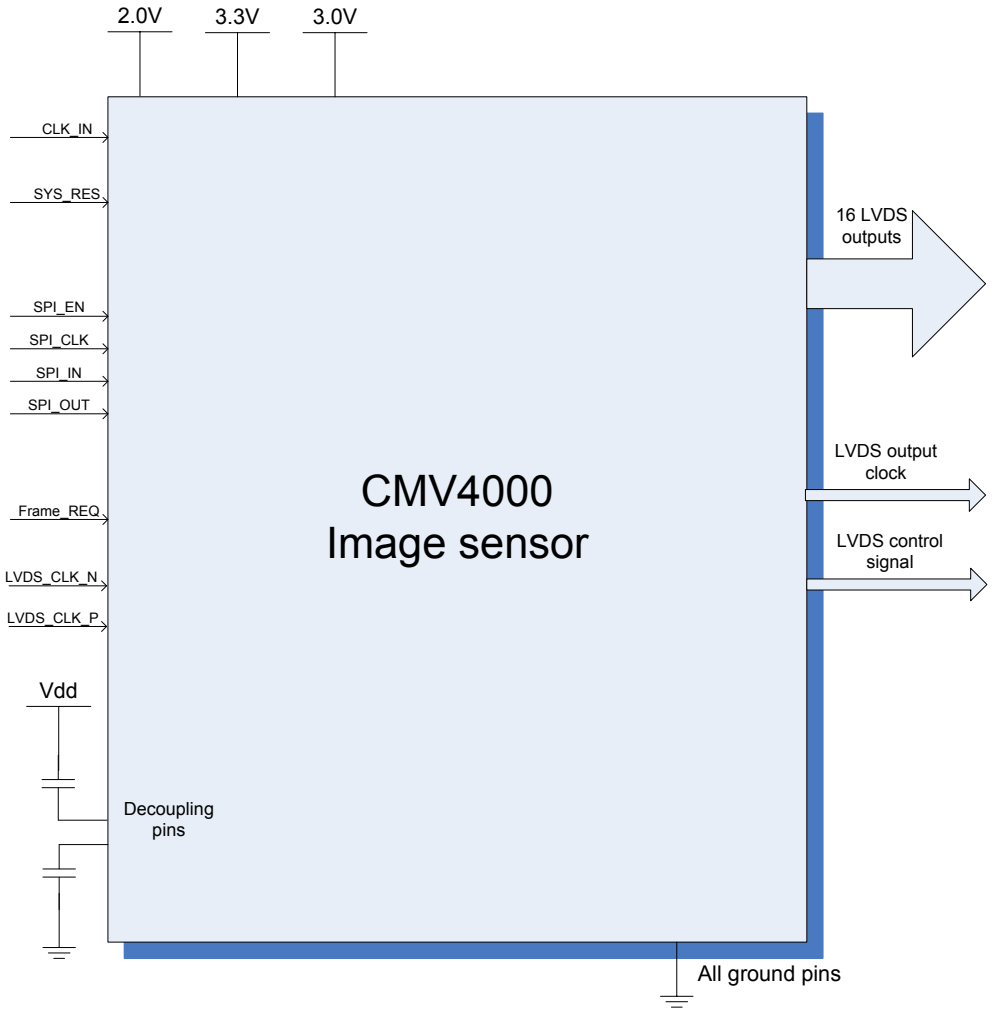

Figure 1: Connection diagram for the CMV4000 image sensor

Please look at the pin list for a detailed description of all pins and their proper connections. Some optional pins are not displayed on the figure above. The exact pin numbers can be found in the pin list and on the package drawing.

2 SENSOR ARCHITECTURE

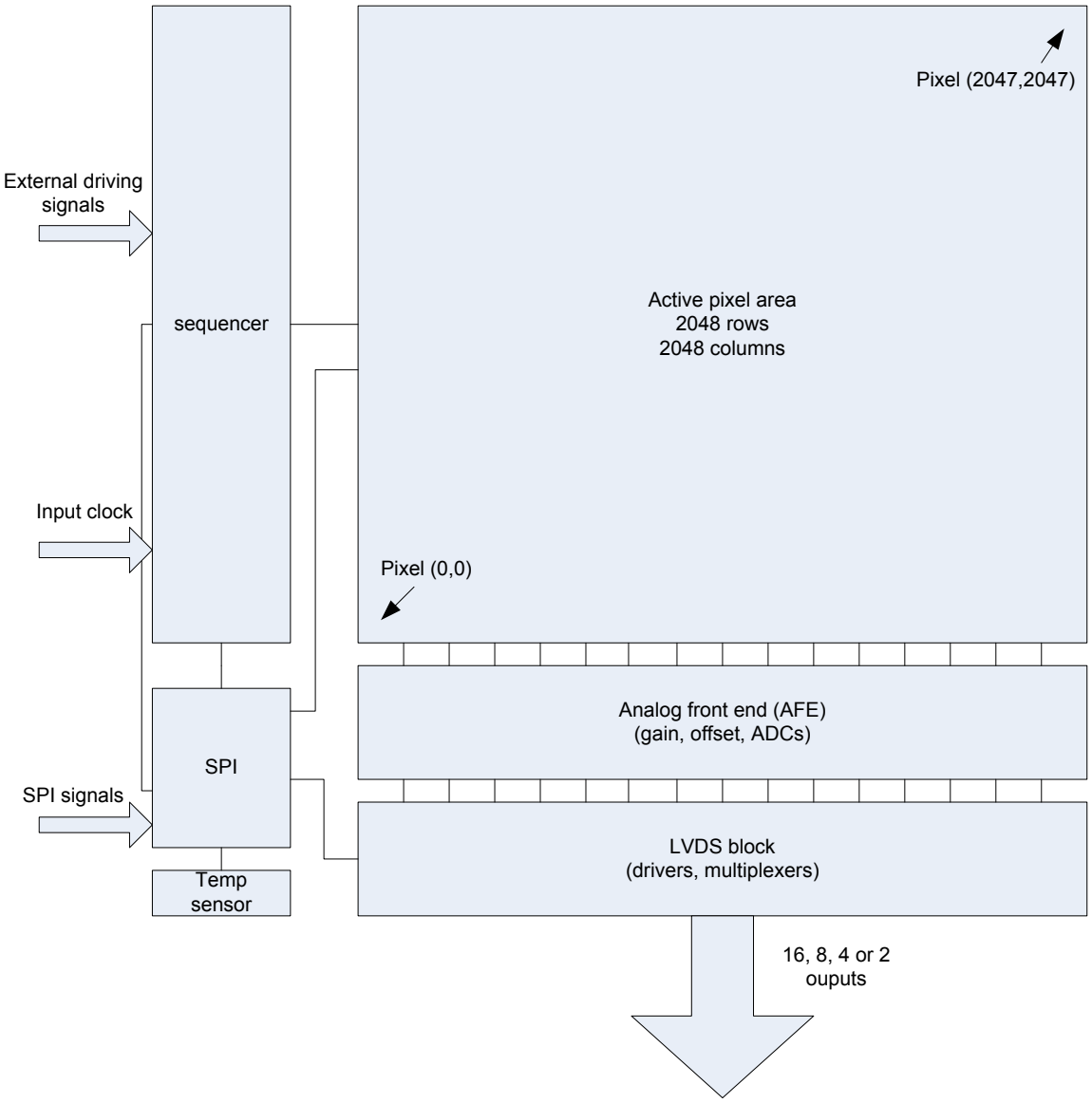

Figure 2: Sensor block diagram

Figure 2 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and is then read out sequentially, row-by-row. On the pixel output, an analog gain of x1, x1.2, x1.4 and x1.6 is possible. The pixel values then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels. Each LVDS channel reads out 128 adjacent columns of the array. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface. A temperature sensor which can be read out over the SPI interface is also included.

2.1 PIXEL ARRAY

The pixel array consists of 2048 x 2048 square global shutter pixels with a pitch of 5.5µm (5.5µm x 5.5µm). This results in an optical area of close to 1 optical inch (16mm). This means that off-the-shelve C-mount lenses can be used.

The pixels are designed to achieve maximum sensitivity with low noise and low PLS specifications. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency (>50%).

2.2 ANALOG FRONT END

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface). The column ADC converts the analog pixel value to a 10 or 12 bit value. A digital offset can also be applied to the output of the column ADC's. All gain and offset settings can be programmed using the SPI interface.

2.3 LVDS BLOCK

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at maximum 480Mbps. The sensor has 18 LVDS output pairs:

- 16 Data channels
- 1 Control channel
- 1 Clock channel

The 16 data channels are used to transfer 10-bit or 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels, among other useful sensor status information. Details on the LVDS timing and format can be found in section 4 of this document.

2.4 SEQUENCER

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control clocks. This sequencer can be activated and programmed through the SPI interface. A detailed description of the SPI registers and sensor (sequencer) programming can be found in section 5 of this document.

2.5 SPI INTERFACE

The SPI interface is used to load the sequencer registers with data. The data in these registers is used by the sequencer while driving and reading out the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system. Section 5 contains more details on register programming and SPI timing.

2.6 TEMPERATURE SENSOR

A 16-bit digital temperature sensor is included in the image sensor and can be controlled by the SPI-interface. The on-chip temperature can be obtained by reading out the registers with address 126 and 127 (in burst mode, see section 3.7.2 for more details on this mode).

A calibration of the temperature sensor is needed for absolute temperature measurements. A typical temperature sensor output vs temperature curve can be found below. The temperature sensor requires a running input clock (CLK_IN), the other functions of the image sensor can be operational or in standby mode.

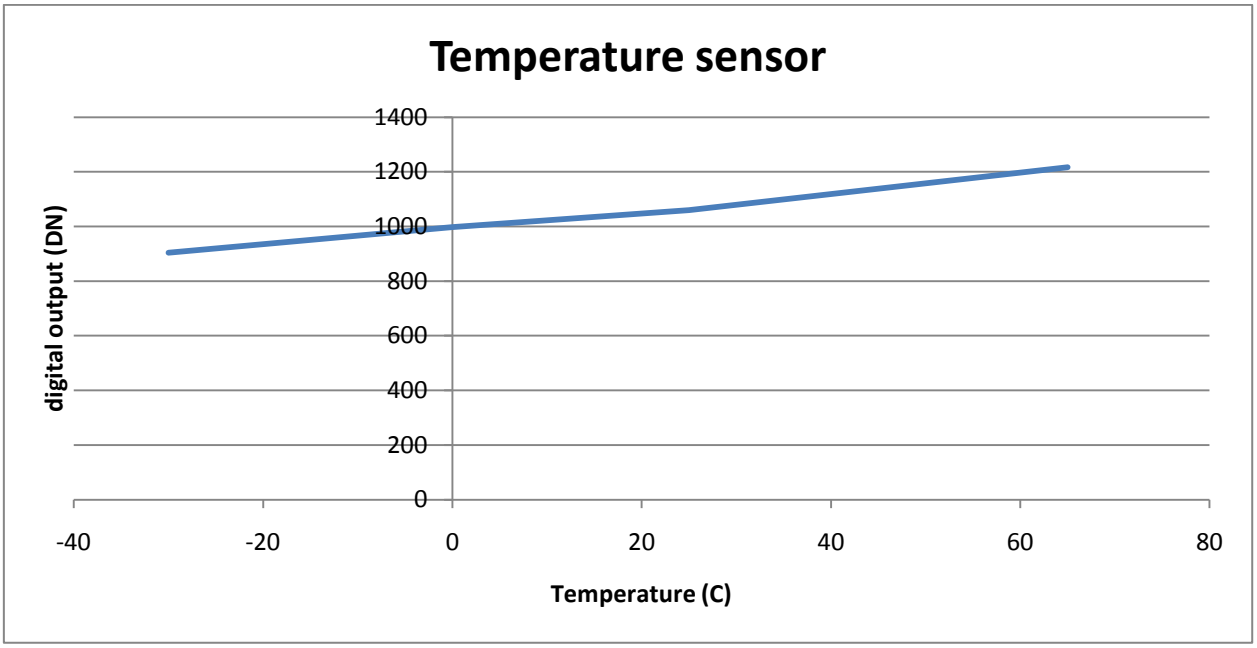

Figure 3: Typical output of the temperature sensor of the CMV4000

3 DRIVING THE CMV4000

3.1 SUPPLY SETTINGS

The CMV4000 image sensor has the following supply settings:

Supply name	Typical value	Range	Current nominal	Current peak
VDD20	2.0V	1.6V-2.1V	200mA	1A
VDD33	3.3V	3V-3.6V	100mA	0.5A
VDDpix	3.0V	2.3V-3.6V	20mA	0.6A
Vres_h	3.3V	3.0V-3.6V	NA	0.5A

See pin list for exact pin numbers for every supply.

3.2 BIASING

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

3.3 DIGITAL INPUT PINS

The table below gives an overview of the external pins used to drive the sensor

Pin name	Description
CLK_IN	Master input clock, frequency range between 5 and 48 MHz
LVDS_CLK_N/P	High speed LVDS input clock, frequency range between 50 and 480 MHz
SYS_RES_N	System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up
FRAME_REQ	Frame request pin. When a rising edge is detected on this pin the programmed number of frames is captured and sent by the sensor
SPI_IN	Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
SPI_EN	SPI enable pin. When this pin is high the data should be written/read on the SPI
SPI_CLK	SPI clock. This is the clock on which the SPI runs (max 48Mz)
T_EXP1	Input pin which can be used to program the exposure time externally. Optional
T_EXP2	Input pin which can be used to program the exposure time externally in interleaved high dynamic range mode. Optional

V_{IH}= 3.0V-3.3V
V_{IL}= 0.0V-0.3V

3.4 INPUT CLOCK

The high speed LVDS input clock (LVDS_CLK_N/P) defines the output data rate of the CMV4000. The mastclock (CLK_IN) must be 10 or 12 times slower depending on the programmed bit mode setting. The maximum data rate of the output is 480Mbps which results in a LVDS_CLK_N/P of 480MHz and a CLK_IN of 48MHz in 10-bit mode and 40MHz in 12-bit mode. The minimum frequencies are 5MHz for CLK_IN and 50MHz for LVDS_CLK_N/P. Any frequency between the minimum and maximum can be applied by the user and will result in a corresponding output data rate.

3.5 FRAME RATE CALCULATION

The frame rate of the CMV4000 is defined by 2 main factors.

1. Exposure time
2. Read out time

For ease of use we will assume that the exposure time is not longer than the read out time. By assuming this the frame rate is completely defined by the read out time (because the exposure time happens in parallel with the read-out time). The read-out time (and thus the frame rate) is defined by:

1. Output clock speed: max 480Mbps
2. ADC mode: 10 or 12 bit
3. Number of lines read-out
4. Number of LVDS outputs used: max 16 outputs

This means that if any of the parameters above is changed, it will have an impact on the frame rate of the CMV4000. In normal operation (16 outputs @ 480Mbps, 10 bit and full resolution) this will result in 180 fps.

Total readout time is composed of two parts: FOT (frame overhead time) + image readout time

FOT = (FOT_REG_VALUE + (2 x 16/#outputs used)) x 129 x master clock period
==> When running the CMV4000 sensor at 48MHz with 16 outputs and default FOT settings this results in: 59us

Image read-out time = (129 x master clock period x 16/#outputs used) * nr_lines
==> When running the CMV4000 sensor at 48MHz with 16 outputs and reading 2048 lines this results in: 5.495ms

This results in a total read-out time of 59us + 5.495ms = 5.554ms ==> 180fps.

3.6 START-UP SEQUENCE

The following sequence should be followed when the CMV4000 is started up in default output mode (480Mbps, 10bit resolution).

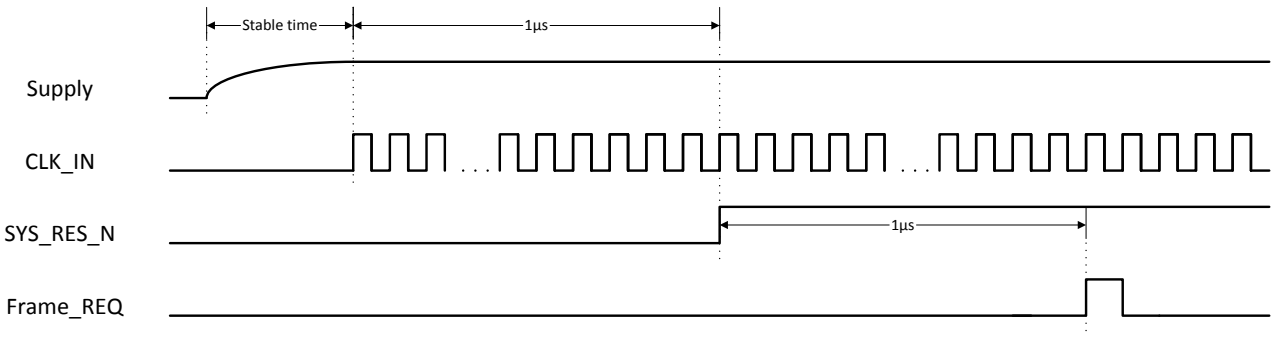

Figure 4: Start-up sequence for 480Mbps @ 10-bit

The masterclock (48MHz in for 480Mbps in 10-bit mode) should only start after the rise time of the supplies. The external reset pin should be released at least 1µs after the supplies have become stable. The first frame can be requested 1µs after the reset pin has been released. An optional SPI upload (to program the sequencer) is possible 1µs after the reset pin has been released. In this case the Frame_REQ pulse must be postponed until after the SPI upload has been completed.

When the CMV4000 will be used in 12-bit mode, an SPI upload is necessary to program the ADC and LVDS. In this case the start-up sequence looks like the diagram below.

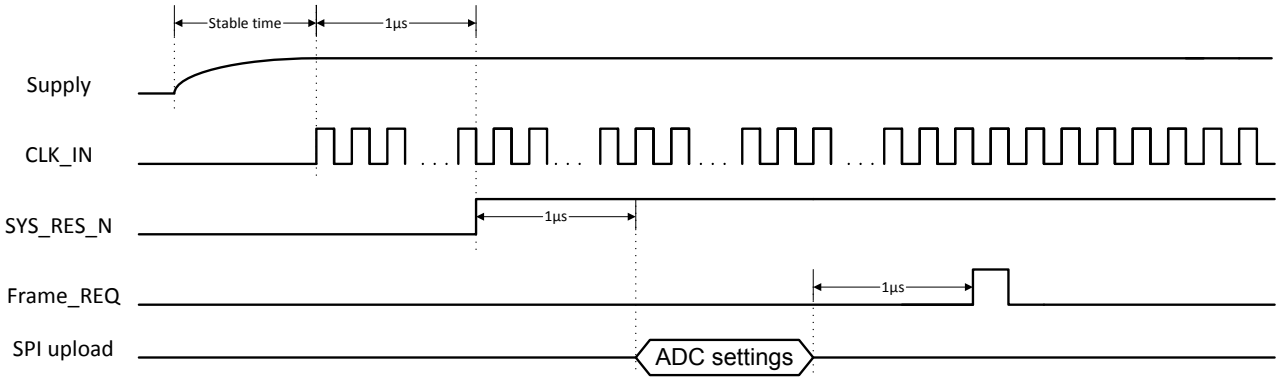

Figure 5: Start-up sequence for 12-bit mode

The following SPI registers (ADC and LVDS settings) should be uploaded in this mode:

1. LVDS settings (address 111) : set to 12 bit mode
2. ADC bit mode (address 112): set to 12 bit resolution

Note: As mentioned in section 3.3, for a lower output data rate only the input clocks need to be lowered.

3.7 RESET SEQUENCE

If a sensor reset is necessary while the sensor is running the following sequence should be followed.

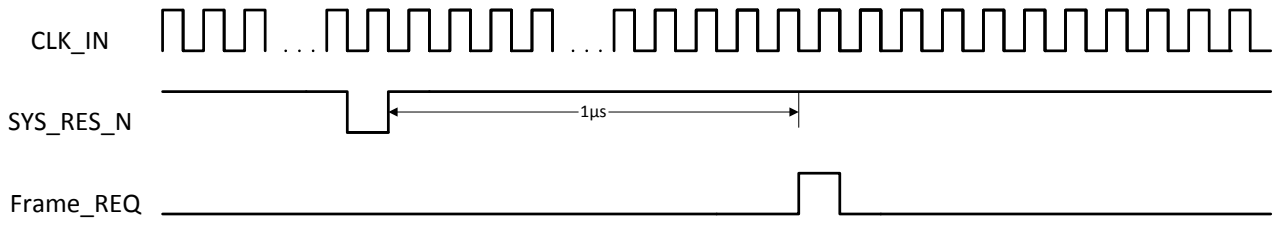

Figure 6: Reset sequence

The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RES_N pin. After the reset there is a minimum time of 1µs needed before a FRAME_REQ pulse can be sent.

When a switch from 10-bit to 12-bit mode (or vice versa) is necessary, the following sequence should be followed.

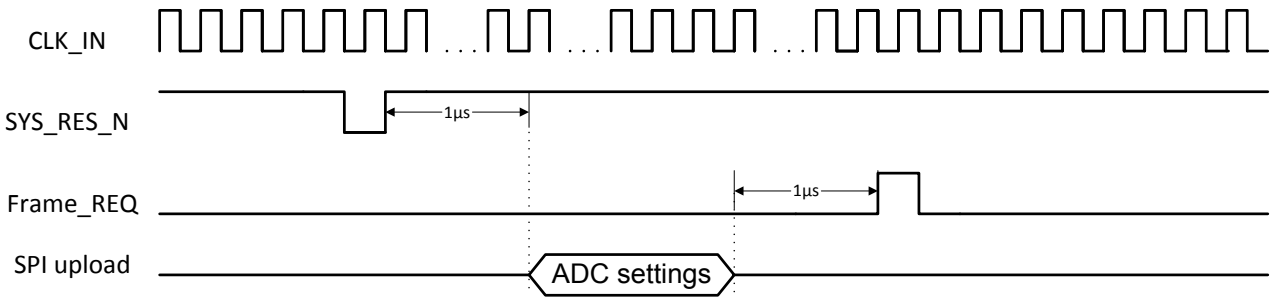

Figure 7: Reset sequence when changing bit mode

The following SPI registers (ADC settings) should be uploaded in this mode:

1. LVDS setting (address 111): set to desired bit resolution
2. ADC bit mode (address 112): set to desired bit resolution mode

Note: As mentioned in section 3.3, for a lower output data rate only the input clocks need to be lowered.

3.8 SPI PROGRAMMING

Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

3.8.1 SPI WRITE

The timing to write data over the SPI interface can be found below.

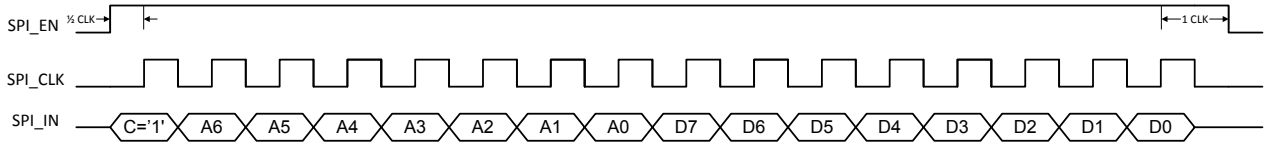

Figure 8: SPI write timing

The data is sampled by the CMV4000 on the rising edge of the SPI_CLK. The SPI_CLK has a maximum frequency of 48MHz. The SPI_EN signal has to be high for half a clock period before the first databit is sampled. SPI_EN has to remain high for 1 clock period after the last databit is sampled.

One write action contains 16 databits:

- One control bit: First bit to be sent, indicates whether a read (‘0’) or write (‘1’) will occur on the SPI interface.
- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 8 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the figure below for an example of 2 registers being written in burst.

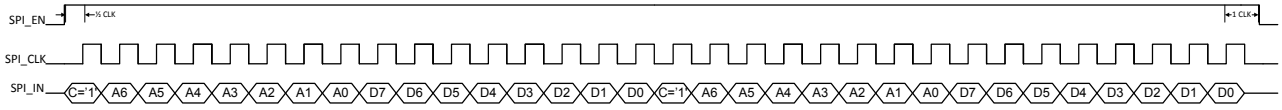

Figure 9: SPI write timing for 2 registersin burst

3.8.2 SPI READ

The timing to read data from the registers over the SPI interface can be found below.

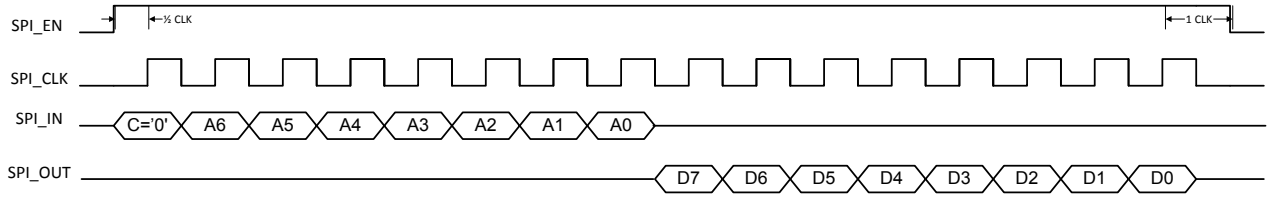

Figure 10: SPI read timing

To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made '0'. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK. This means that the data should be sampled by the receiving system on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first. When reading out the temperature sensor over the SPI, addresses 126 and 127 should de read-out in burst mode (keep SPI_EN high)

3.9 REQUESTING A FRAME

After starting up the sensor (see section 3.5), a number of frames can be requested by sending a FRAME_REQ pulse. The number of frames can be set by programming the appropriate register (addresses 70 and 71). The default number of frames to be grabbed is 1.

In internal-exposure-time mode, the exposure time will start after this FRAME_REQ pulse. In the external-exposure-time mode, the read-out will start after the FRAME_REQ pulse. Both modes are explained into detail in the sections below.

3.9.1 INTERNAL EXPOSURE CONTROL

In this mode, the exposure time is set by programming the appropriate registers (address 42-44) of the CMV4000.After the high state of the FRAME_REQ pin is detected, the exposure time will start immediately. When the exposure time ends (as programmed in the registers), the pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). Immediately after the FOT, the frame is read-out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one. See the diagram below for more details.

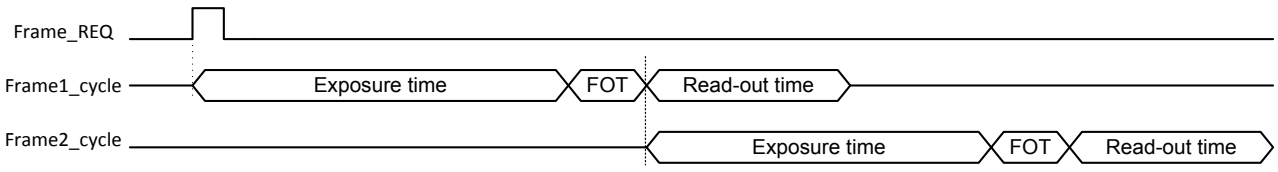

Figure 11: request for 2 frames in internal- exposure-time mode

When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame.

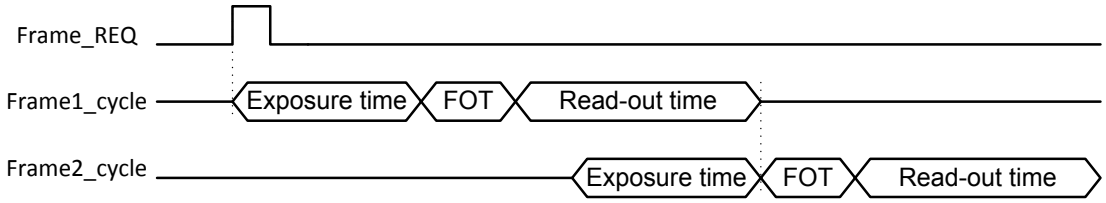

Figure 12: Request for 2 frames in internal exposure mode with exposure time < read-out time

3.9.2 EXTERNAL EXPOSURE TIME

The exposure time can also be programmed externally by using the T_EXP1 input pin. This mode needs to be enabled by setting the appropriate register (address 41). In this case, the exposure starts when a high state is detected on the T_EXP1 pin. When a high state is detected on the FRAME_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the T_EXP1 pin during or after the read-out of the previous frame.

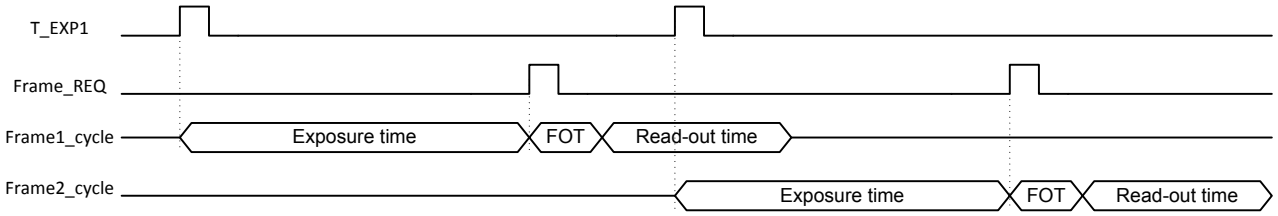

Figure 13: request for 2 frames using external-exposure-time mode

4 READING OUT THE SENSOR

4.1 LVDS DATA OUTPUTS

The CMV4000 has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 16 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 18 LVDS output pairs (2 pins for each LVDS channel):

- 16 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 36 pins of the CMV4000 are used for the LVDS outputs (32 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs.

The 16 data channels are used to transfer the 10-bit or 12-bit pixel data from the sensor to the receiver in the surrounding system.

The output clock channel transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 480Mbps output data rate is used, the LVDS output clock will be 240MHz.

The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 10-bit or 12-bit words that are transferred synchronous to the 16 data channels.

4.2 LOW-LEVEL PIXEL TIMING

The figures below show the timing for transfer of 10-bit and 12-bit pixel data over one LVDS output. To make the timing more clear, the figures show only the p-channel of each LVDS pair. The data is transferred LSB first, with the transfer of bit D[0] during the high phase of the DDR output clock.

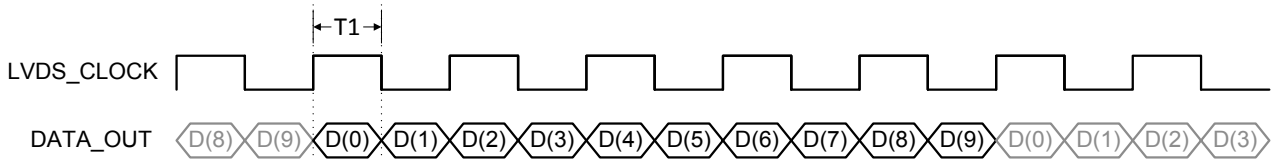

Figure 14: 10-bit pixel data on an LVDS channel

The time 'T1' in the diagram above is 1/10th of the period of the input clock (CLK_IN) of the CMV4000. When a frequency of 48MHz is used for CLK_IN (max in 10-bit mode) and 480MHz for LVDS_CLK_N/P, this results in a 240MHz LVDS_CLOCK.

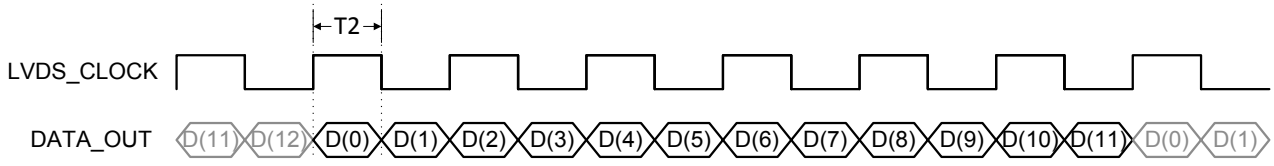

Figure 15: 12-bit pixel data on an LVDS channel

The time 'T2' in figure 14 is 1/12th of the period of the input clock (CLK_IN) of the CMV4000. When a frequency of 40MHz is used for CLK_IN (max in 12-bit mode) and 480MHz for LVDS_CLK_N/P, this results in a 240MHz LVDS_CLOCK.

4.3 READOUT TIMING

The readout of image data is grouped in bursts of 128 pixels per channel. Each pixel is either 10 or 12 bits of data (see section 4.2). One complete pixel period equals one period of the master clock input. For details on pixel remapping and pixel vs channel location please see section 4.4 of this document. An overhead time exists between two bursts of 128 pixels. This overhead time has the same length of one pixel read-out (i.e. the length of 10 or 12 bits at the selected data rate).

4.3.1 10 BIT MODE

In this section, the readout timing for the default 10 bit mode is explained. In this mode the maximum framerate of 180 fps can be reached.

4.3.1.1 16 OUTPUT CHANNELS

By default, all 16 data output channels are used to transmit the image data. This means that an entire row of image data is transferred in one slot of 128 pixel periods (16 x 128 = 2048). Next figure shows the timing for one LVDS channel.

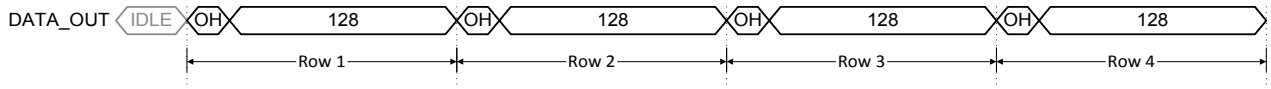

Figure 16: Output timing in default 16 channel mode

Only when 10 bit mode and 16 data outputs, running at 480Mbps, are used, the frame rate of 180fps can be achieved (default).

4.3.1.2 8 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 8 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (2*128) + (2*1) master clock periods. Next figure shows the timing for one LVDS channel.

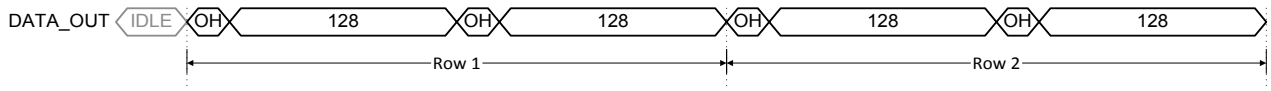

Figure 17: Output timing in 8 channel mode

In this 8 channel mode, the frame rate is reduced with factor of 2 compared to 16 channel mode.

4.3.1.3 4 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 4 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (4*128) + (4*1) master clock periods. Next figure shows the timing for one LVDS channel.

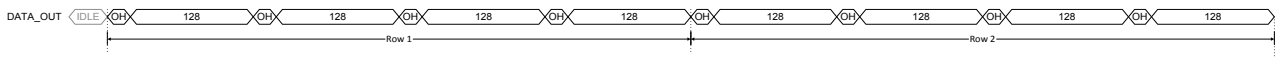

Figure 18: Output timing in of 4 channel mode

In this 4 channel mode, the frame rate is reduced with factor 4 compared to 16 channel mode.

4.3.1.4 2 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 2 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (8*128) + (8*1) master clock periods. Next figure shows the timing for one LVDS channel.

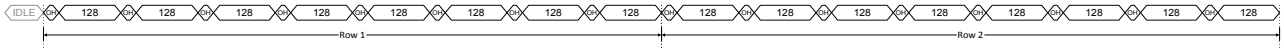

Figure 19: Output timing in 2 channel mode

In this 2 channel mode, the frame rate is reduced with factor of 8 compared to 16 channel mode.

4.3.2 12 BIT MODE

In 12 bit mode, the analog-to-digital conversion takes 4x longer to complete. This causes the framerate to drop to 70 fps when 480Mhz is used for LVDS_CLK_N/P. Due to this extra conversion time, the framerate in 16 channel mode is the same as in 8 and 4 channel mode.

4.3.2.1 16 OUTPUT CHANNELS

By default, all 16 data output channels are used to transmit the image data. This means that an entire row of image data is transferred in one slot of 128 pixel periods (16 x 128 = 2048). Next figure shows the timing for one LVDS channel.

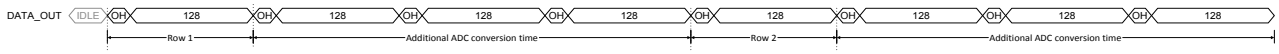

Figure 20: Output timing in default 16 channel mode

4.3.2.2 8 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 8 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (2*128) + (2*1) master clock periods. Next figure shows the timing for one LVDS channel.

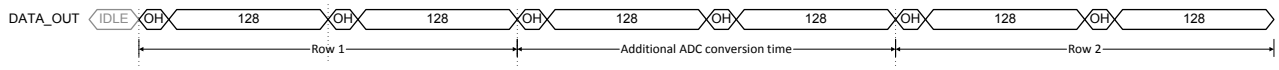

Figure 21: Output timing in 8 channel mode

4.3.2.3 4 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 4 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (4*128) + (4*1) master clock periods. Next figure shows the timing for one LVDS channel.

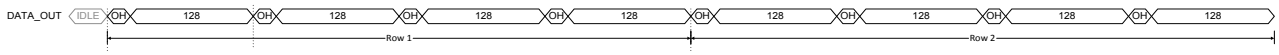

Figure 22: Output timing in of 4 channel mode

4.3.2.4 2 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 2 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (8*128) + (8*1) master clock periods. Next figure shows the timing for one LVDS channel.

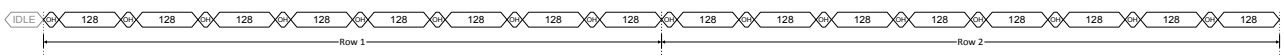

Figure 23: Output timing in 2 channel mode

In this 2 channel mode, the frame rate is reduced with factor of 2 compared to 16, 8 and 4 channel mode.

4.4 PIXEL REMAPPING

Depending on the number of output channels, the pixels are read out by different channels and come out at a different moment in time. With the details from the next sections, the end user is able to remap the pixel values at the output to their correct image array location.

4.4.1 16 OUTPUTS

The figure below shows the location of the image pixels versus the output channel of the image sensor.

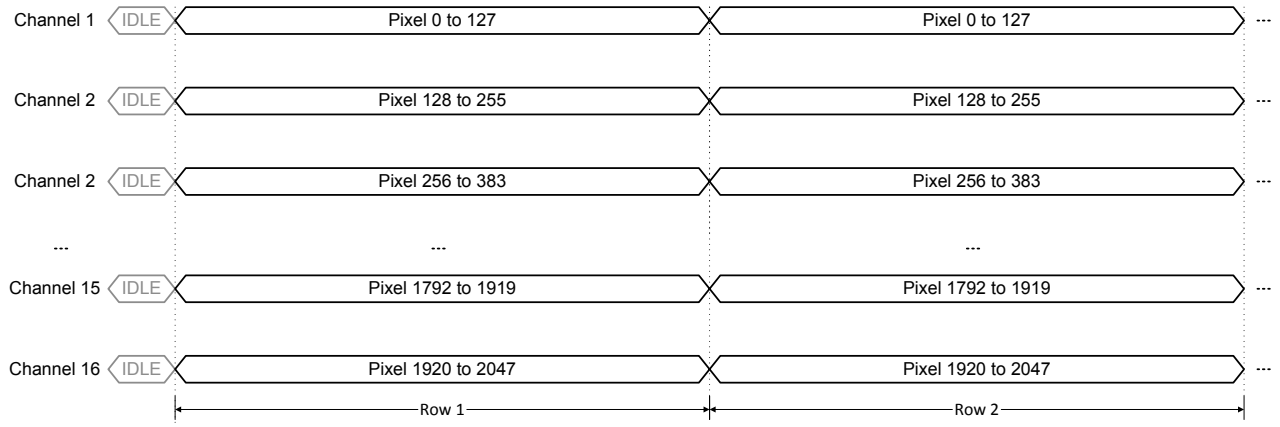

Figure 24: Pixel remapping for 16 output channels

16 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 2048 rows being read out.

4.4.2 8 OUTPUTS

When only 8 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 8 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in two bursts. The time needed to read out one row is doubled compared to when 16 outputs are used. Channel 2, 4, 6…16 are not being used in this mode, so they can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be read out depends on the value in the corresponding register. By default there are 2048 rows being read out.

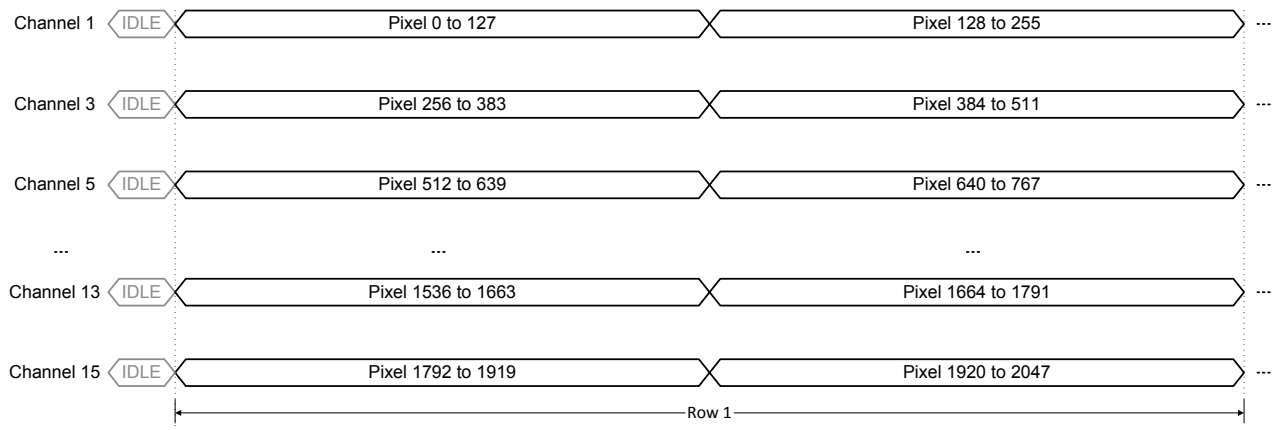

Figure 25: Pixel remapping for 8 output channels

4.4.3 4 OUTPUTS

When only 4 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 4 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in four bursts. The time needed to read out one row is 4x longer compared to when 16 outputs are used. Only channel 1, 5, 9 and 13 are being used in this mode, so the remaining channels can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be read out depends on the value in the corresponding register. By default there are 2048 rows being read out.

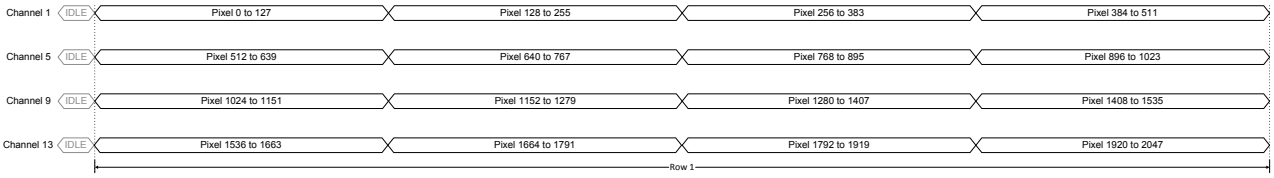

Figure 26: Pixel remapping for 4 output channels

4.4.4 2 OUTPUTS

When only 2 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 2 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in 8 bursts. The time needed to read out one row is 8x longer compared to when 16 outputs are used. Only channel 1 and 9 are being used in this mode, so the remaining channels can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be readout depends on the value in the corresponding register. By default there are 2048 rows being read out.

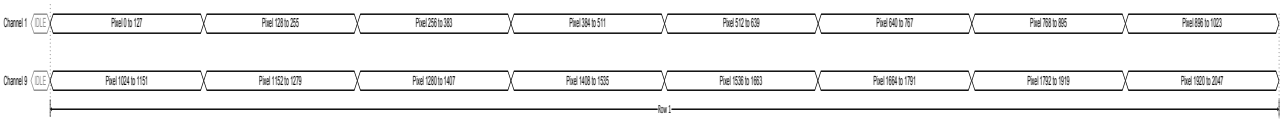

Figure 27: Pixel remapping for 2 output channels

4.5 CONTROL CHANNEL

The CMV4000 has one LVDS output channel dedicated for the valid data synchronization and timing of the output channels. The end user must use this channel to know when valid image data or training data is available on the data output channels.

The control channel transfers status information in 10-bit or 12-bit word format. Every bit of the word has a specific function. Next table describes the function of the individual bits.

Bit	Function	Description
[0]	DVAL	Indicates valid pixel data on the outputs
[1]	LVAL	Indicates validity of the readout of a row
[2]	FVAL	Indicates the validity of the readout of a frame
[3]	SLOT	Indicates the overhead period before 128-pixel bursts (*)
[4]	ROW	Indicates the overhead period before the readout of a row (*)
[5]	FOT	Indicates when the sensor is in FOT (sampling of image data in pixels) (*)
[6]	INTE1	Indicates when pixels of integration block 1 are integrating (*)
[7]	INTE2	Indicates when pixels of integration block 2 are integrating (*)
[8]	'0'	Constant zero
[9]	'1'	Constant one
[10]	'0'	Constant zero
[11]	'0'	Constant zero

(*)Note: The status bits are purely informational. These bits are not required to know when the data is valid. The DVAL, LVAL and FVAL signals are sufficient to know when to sample the image data.

4.5.1 DVAL, LVAL, FVAL

The first three bits of the control word must be used to identify valid data and the readout status.

Next figure shows the timing of the DVAL, LVAL and FVAL bits of the control channel with an example of the readout of a frame of 3 rows (default is 2048 rows). This example uses the default mode of 16 outputs in 10 bit mode.

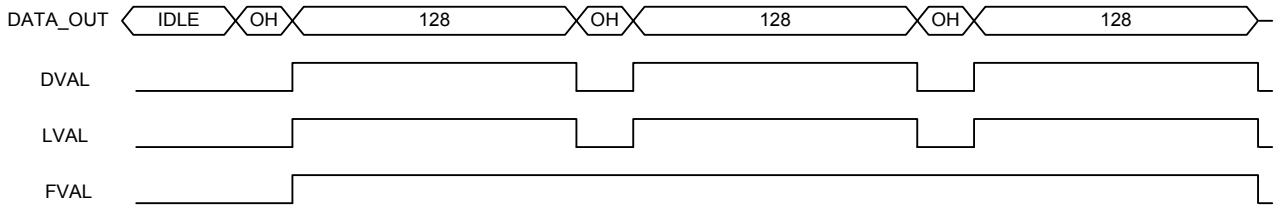

Figure 28: DVAL, LVAL and FVAL timing in 16 output mode

When only 8 outputs are used, the line read-out time is 2x longer. The control channel takes this into account and the timing in this mode looks like the diagram below. The timing extrapolates identically for 4 and 2 outputs.

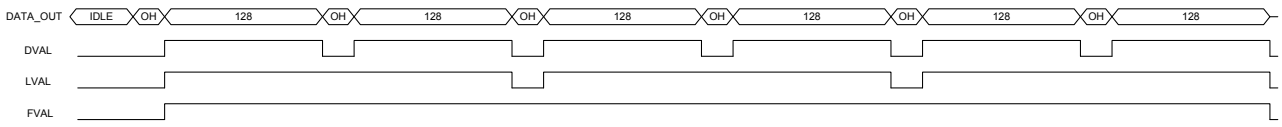

Figure 29: DVAL, LVAL and FVAL timing in 8 output mode

4.6 TRAINING DATA

To synchronize the receiving side with the LVDS outputs of the CMV4000, a known data pattern can be put on the output channels. This pattern can be used to “train” the LVDS receiver of the surrounding system to achieve correct word alignment of the image data. Such a training pattern is put on all 16 data channel outputs when there is no valid image data to be sent (so, also in between bursts of 128 pixels). The training pattern is a 10-bit or 12-bit data word that replaces the pixel data. The sensor has a 12-bit sequencer register (address 78-79) that can be loaded through the SPI to change the contents of the 12-bit training pattern.

The control channel does not send a training pattern, because it is used to send control information at all time. Word alignment can be done on this channel when the sensor is idle (not exposing or sending image data). In this case all bits of the control word are zero, except for bit [9].

The figure below shows the location of the training pattern (TP) on the data channels and control channels when the sensor is in idle mode and when a frame of 3 rows is read-out. The default mode of 16 outputs is selected.

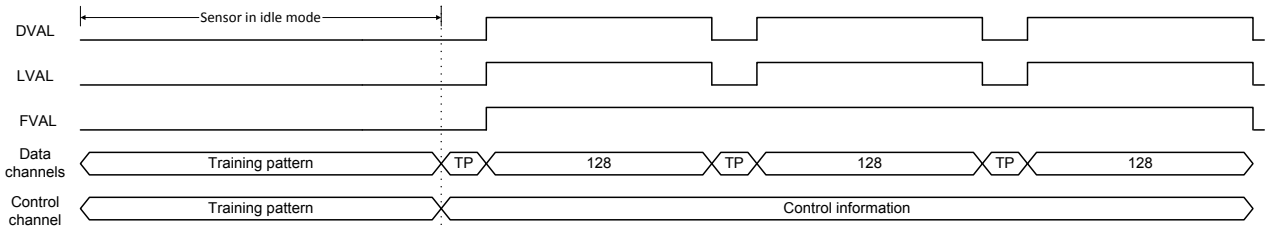

Figure 30: Training pattern location in the data and control channels.

5 IMAGE SENSOR PROGRAMMING

This section explains how the CMV4000 can be programmed using the on-board sequencer registers.

5.1 EXPOSURE MODES

The exposure time can be programmed in two ways, externally or internally. Externally, the exposure time is defined as the time between the rising edge of T_EXP1 and the rising edge of FRAME_REQ (see section 3.8.2 for more details). Internally, the exposure time is set by uploading the desired value to the corresponding sequencer register.

The table below gives an overview of the registers involved in the exposure mode.

Exposure time settings			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_ext	41 bit[0]	0	0: Exposure time is defined by the value uploaded in the sequencer register (42-44) 1: Exposure time is defined by the pulses applied to the TEXP1 and FRAME_REQ pins.
Exp_time	42-44	2048	When the Exp_ext register is set to '0', the value in this register defines the exposure time according to the following formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the period of the master input clock.

5.2 HIGH DYNAMIC RANGE MODES

The sensor has different ways to achieve high optical dynamic range in the grabbed image.

- Interleaved read-out: the odd and even rows have a different exposure time
- Piecewise linear response: pixels respond to light with a piecewise linear response curve.
- Multi-frame readout: Different frames are read-out with increasing exposure time

All the HDR modes mentioned above can be used in both the internal and external exposure time mode.

5.2.1 INTERLEAVED READ-OUT

In this HDR mode, the odd and even rows of the image sensors will have a different exposure time. This mode can be enabled by setting the register in the table below.

HDR settings – interleaved read-out			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_dual	41 bit[1]	0	0: interleaved exposure mode disabled 1: interleaved exposure mode enabled

The surrounding system can combine the image of the odd rows with the image of the even rows which can result in a high dynamic range image. In such an image very bright and very dark objects are made visible without clipping. The table below gives an overview of the registers involved in the interleaved read-out when the internal exposure mode is selected.

HDR settings – interleaved read-out			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_time	42-44	2048	When the Exp_dual register is set to '1', the value in this register defines the exposure time for the even rows according following formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the

			period of the master input clock.
Exp_time2	56-58	2048	When the Exp_dual register is set to '1', the value in this register defines the exposure time for the odd rows according following formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the period of the master input clock.

When the external exposure mode and interleaved read-out are selected, the different exposure times are achieved by using the T_EXP1 and T_EXP2 input pins. TEXP1 defines the exposure time for the even lines, while TEXP2 defines the exposure time for the odd lines. See the figure below for more details.

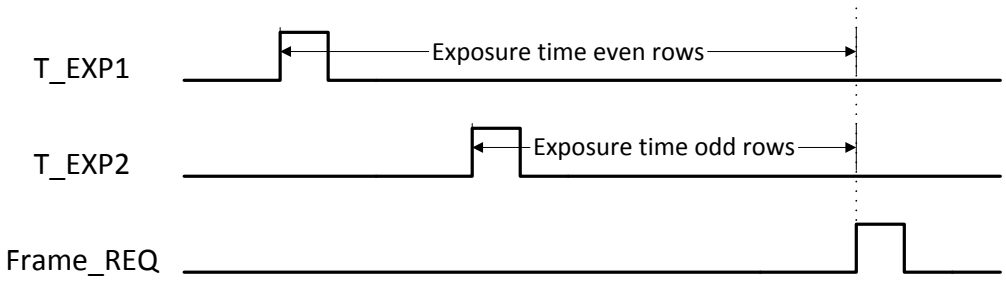

Figure 31: Interleaved read-out in external exposure mode

When a color sensor is used, the sequencer should be programmed to make sure it takes the Bayer pattern into account when doing interleaved read-out. This can be done by setting the appropriate register to '0'.

Color/mono			
Register name	**Register address**	**Default value**	**Description of the value**
Color	39	1	0: color sensor is used 1: monochrome sensor is used

5.2.2 PIECEWISE LINEAR RESPONSE

The CMV4000 has the possibility to achieve a high optical dynamic range by using a piecewise linear response. This feature will clip illuminated pixels which reach a programmable voltage, while leaving the darker pixels untouched. The clipping level can be adjusted 2 times within one exposure time to achieve a maximum of 3 slopes in the response curve. More details can be found in the figure below.

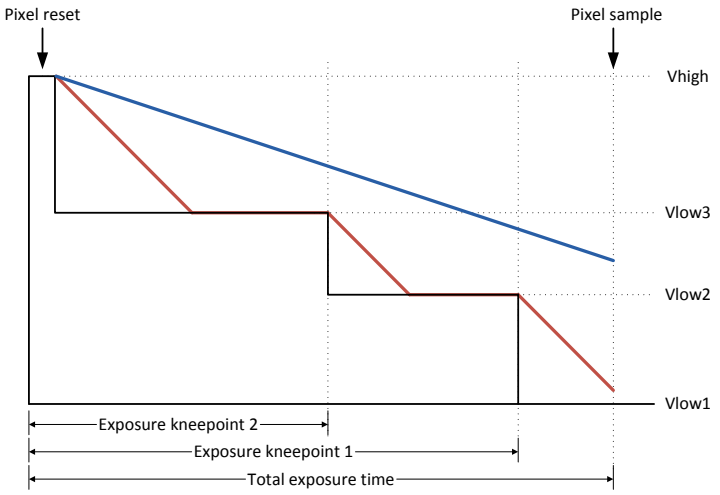

Figure 32: Piecewise linear response details