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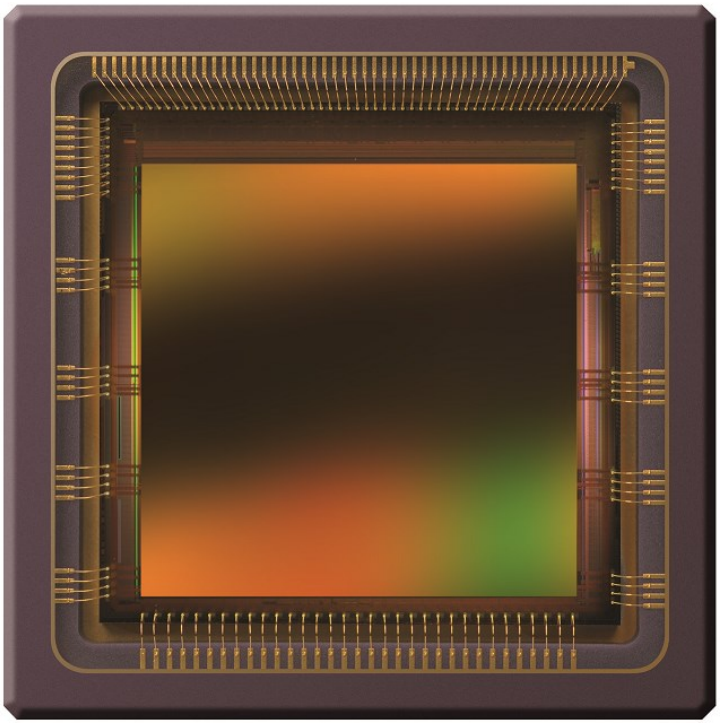
4.2 Megapixel machine vision CMOS image sensor



Datasheet

Change record

Issue	Date	Modification
1	06/05/2009	Origination
1.1	12/11/2009	Corrected register address of sub_s[7:0] to '35' (p 29/30/33)
1.2	11/01/2010	Adjusted min input frequency (section 3.3)
1.3	14/01/2010	Adjusted pin width in package drawing
2	29/03/2010	Added spectral response Added spectral response for color devices Updated specifications for version 2 devices Changed VDD18 to VDD20 Added ordering info Added handling and soldering procedures Removed "confidential" in footer Added recommended and adjustable register settings
2.1	22/7/2010	Frame rate calculation added
2.2	2/8/2010	Read-out in 12 bit mode added
2.3	1/9/2010	Added exposure time offset (0.65 x register73 x clk_per x 129)
2.4	17/9/2010	Added Vtf_l1 to GND remark
2.5	19/10/2010	Added E12 spectral response curve and part numbers
2.6	11/01/2011	Added RGB Bayer pattern details
2.7	1/2/2011	Added electrical IO specifications
2.8	25/3/2011	Updated reflow soldering profile
2.9	13/4/2011	Changed tilt to 0.2 degrees, updated spectral response, changed exposure time formula
2.9.1	20/5/2011	Changed 12 bit read-out mode (removed 16 and 8 outputs)
3	1/9/2011	Complete revision for version 3 sensor
3.1	24/05/2012	Line up with v2.9.5 datasheet
3.2	30/07/2012	Added: - PLR Vlow2/3 enable bit - Sampling of digital inputs on rising CLK_IN - Details on LVDS data out in multiplex modes - CTR channel bits on Tdig1/2 pins - Evaluation kit available - Minimum time between FRAME_REQ pulses in internal mode - Temperature sensor calibration example Updated: - Bayer pattern figure (pixel(0,0) green → red). No actual device change compared to previous devices. - Supply noise influence - Control bit INTE1/2 (no FOT overlap) - FOT and Read-out time rounding - Detailed timing of control channel figure - LVDS clock delay figure (CLK_IN period) - SPI timing from SPI upload to FRAME_REQ (1µs → 1ms) - Total power use (600mW → 650mW) - VDD33 power use (165mW → 200mW) - VDD supplies internal PLL - Register 77 recommended to set to 0 Removed: - Reference errors

Issue	Date	Modification
3.3	01/08/2013	Added: - Pin head dimensions to package drawing - Tdig1 and Tdig2 addresses to register overview - Recommended FOT register settings to register overview - Angular response curve - Minimum exposure value Updated: - Training pattern of control channel - Text and figure of Image flipping chapter - Text and figure of Color filter chapter - Assembly drawing: now refers to pixel (0,0), added dimensions, transparent view, pin numbers and corrected tilt of die - Supply settings table: peak current calculation, typical values to recommended values, supply voltage range - Connection diagram: changed 1.8V to 2.1V - Response curve: replaced figure - Temperature sensor figure now refers to pixel (0,0) - Expanded PLL settings table - Ordering information: part numbers - New table for PLL range in Data rate chapter, corrected frequency range - Start-up sequence: time after SPI upload described more accurately - LVDS driver specification: Voc dependency Removed: - Input clock skew limits
3.4	27/09/2013	Added: - Settling time to reset sequence (Figure 9) - Recommended register setting for PGA register Updated: - Recommended register settings and register overview - Dimensions in assembly drawing: 0.76mm to 1.76mm - LVDS clock enable address from 82[3] to 82[2] - Corrected Figure 19 - SPI_OUT is now an output on the connection diagram
3.5	28/11/2013	Updated: - Reset sequence figure: added settling time - Assembly drawing: corrected location of pixel(0,0) - Mechanical drawing: new version has correct cavity dimensions; higher resolution - Temperature sensor location figure - Added description of recommended settings registers to register overview - Figure 29 now has proper aspect ratio - Correct offset register, is now a 14bit value - Some layout improvements

Issue	Date	Modification
3.6	1/04/2014	Added: - Register addresses now show bit location in Chapter 5 - All PLL registers are now in the register overview - Recommendation for unused pins - Note that fot_length register can be lowered for shorter integration times - Note that LVDS output current can be lowered for meeting EMC standards - Ordering information now includes part numbers for all packages - Reg73 is now called fot_length, to clarify the function of this register - SPI write operation: added requirement of a final falling edge on SPI_CLK Updated: - Corrected some register addresses in the register overview - Description of settling time should be more clear now, added typical values - Description of start-up and reset sequence - Description of PGA settings should be more clear now - Description of register optimization is now more complete - Improved some layout issues - Corrected table in Chapter 5.2.2.1: Vlow3 wrongly referred to Vlow2 - PLL registers in register overview: bit locations are clarified - Pin list table is now sorted on function, rather than pin coordinate - New figures for glass transmittance, QE and response - “color” register is now called “mono” because it better fits the functionality - Power figures are now more accurate, and tested under default configuration Removed: - Recommended setting of “0” for i_lvds_rec was causing confusion - Pixel coordinates on block diagram
3.7	28/01/2015	Added: - Part numbers and specifications for the new LCC package Updated - The power figure in the Specification Overview is now more accurate; it considers the sensor configuration - The exposure time is shortest in external exposure mode, so this mode is added to the calculation. - FRAME_REQ pin is level sensitive, not edge sensitive - Maximum number of frames is 65535, not 65548 - Default value of register 125 was listed as 35, should be 67 - Corrected note that said that the exposure starts directly after F_REQ, there is a delay between the two - Corrected calibration procedure, step 2 should be repeated, not step 1. Removed - Nr_slopes2 register from overview, this is an unused register. - Scratch/dig/bubble spec for cover glass
3.8	18/06/2015	Updated: - LCC pin layout now correctly says it’s the bottom view, not the top - LCC Product number now for AR coated glass only Added - Transmittance curve for AR coated glass

Disclaimer

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Table of Contents

1 INTRODUCTION

1.1 OVERVIEW

The CMV4000 is a high speed CMOS image sensor with 2048 by 2048 pixels (1 optical inch) developed for machine vision applications. The image array consists of 5.5µm x 5.5µm pipelined global shutter pixels which allow exposure during read-out, while performing CDS operation. The image sensor has sixteen 10- or 12-bit digital LVDS outputs (serial). The image sensor also integrates a programmable gain amplifier and offset regulation. Each channel runs at 480 Mbps maximum which results in 180 fps frame rate at full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read-out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes.

1.2 FEATURES

- Capability to define up to 8 different windows
- Horizontal and vertical mirroring function
- Multiplexable output channels: 16, 8, 4 or 2 channel output possible
- LVDS control channel with read-out and frame information
- DDR LVDS output clock to sample data on the receiving end
- Selectable ADC Resolution: choose between maximum frame rate (10bit) or better image quality (12bit)
- Multiple High Dynamic Range options
- Configurable subsampling modes
- On-chip temperature sensor
- On-chip timing generation
- Sensor controllable via SPI-interface
- Available as panchromatic or with RGB Bayer-filter
- Programmable on-chip PLL that can generate all high speed clocks internally.

1.3 SPECIFICATIONS

- Full well charge: 13.5Ke$^-$
- Sensitivity: 5.56 V/lux.s (with microlenses @ 550nm)
- Dark noise: 13e$^-$ RMS
- Conversion gain: 0.075LSB/e$^-$ (10 bit mode) at unity gain
- Dynamic range: 60dB
- Parasitic light sensitivity: 1/50000
- Dark current: 125 e$^-$/s (@ 25°C die temperature)
- Fixed pattern noise: <1 LSB (10 bit mode, <0.1% of full swing, standard deviation on full image)
- Power consumption: 550mW to 1200mW
- 3.3V signaling
- 2048 by 2048 active pixels on a 5.5µm pitch
- Maximum frame rate of 180FPS
- Range of input clocks is 5 to 48MHz (Master clock to PLL) and 50 to 480MHz (LVDS clock)
- Range of custom ceramic packages available: 95 pins µPGA or LGA, or 92 pins LCC

1.4 CONNECTION DIAGRAM

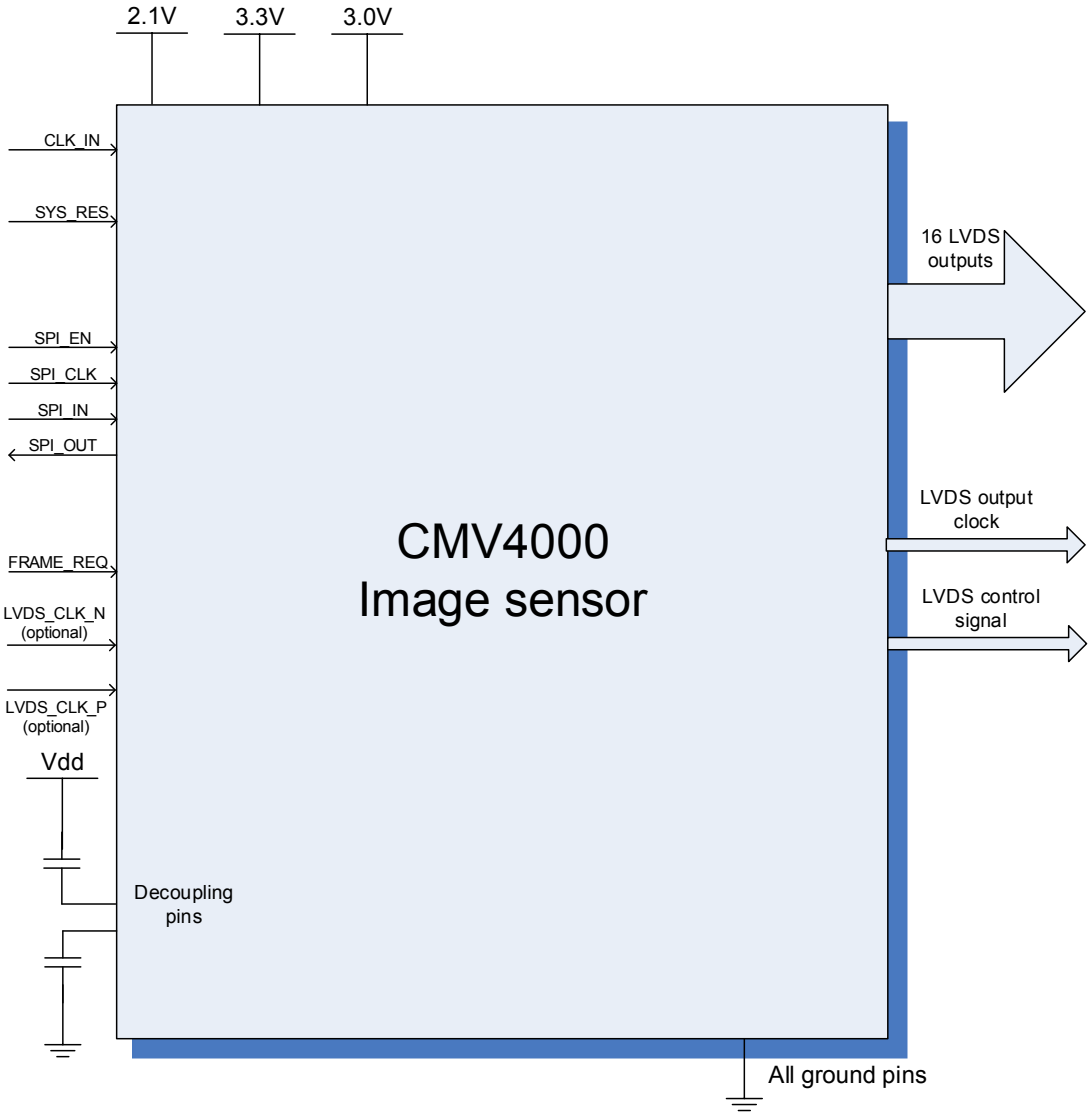

Figure 1: Connection diagram for the CMV4000 image sensor

Please look at the pin list for a detailed description of all pins and their proper connections. Some optional pins are not displayed on the figure above. The exact pin numbers can be found in the pin list and on the package drawing.

2 SENSOR ARCHITECTURE

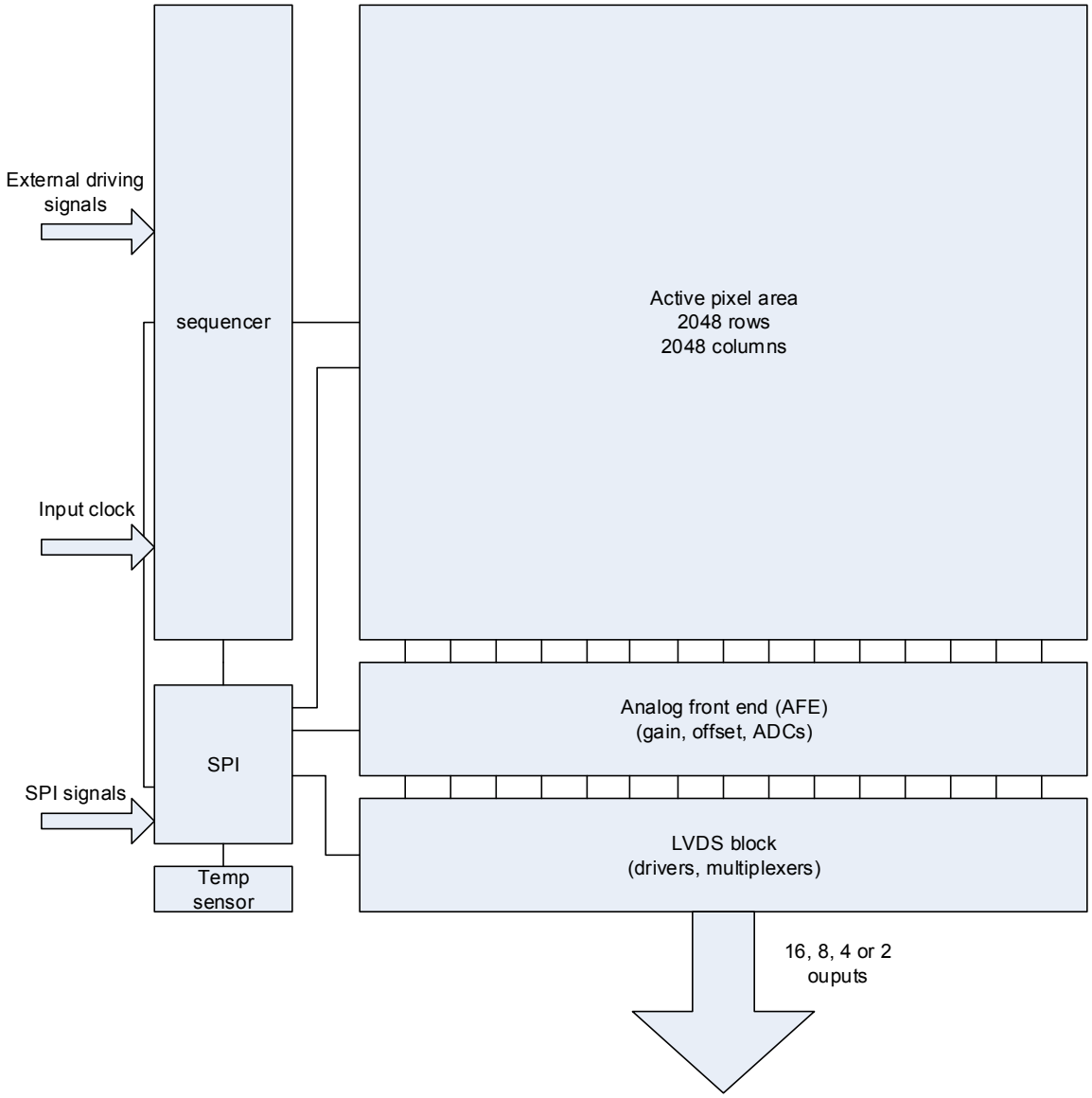

Figure 2: Sensor block diagram

Figure 2 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and is then read out sequentially, row-by-row. On the pixel output, an analog gain can be applied. The pixel values then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels. Each LVDS channel reads out 128 adjacent columns of the array. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface. A temperature sensor which can be read out over the SPI interface is also included.

2.1 PIXEL ARRAY

The pixel array consists of 2048 x 2048 square global shutter pixels with a pitch of 5.5µm (5.5µm x 5.5µm). This results in an optical area of close to 1 optical inch (16mm). This means that off-the-shelve C-mount lenses can be used.

The pixels are designed to achieve maximum sensitivity with low noise and low PLS specifications. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency (>50%).

2.2 ANALOG FRONT END

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface). The column ADC converts the analog pixel value to a 10 or 12 bit value. A digital offset can also be applied to the output of the column ADC's. All gain and offset settings can be programmed using the SPI interface.

2.3 LVDS BLOCK

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at maximum 480Mbps. The sensor has 18 LVDS output pairs:

- 16 Data channels
- 1 Control channel
- 1 Clock channel

The 16 data channels are used to transfer 10-bit or 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels, among other useful sensor status information. Details on the LVDS timing and format can be found in Chapter 4 of this document.

LVDS requires parallel termination at the receiver side (if used). So between LVDS_CLK_P (pin D1) and LVDS_CLK_N (pin D2) should be an external 100Ω resistor. Also all the LVDS outputs should all be externally terminated at the receiver side. See the TIA/EIA-644A standard for details.

2.4 SEQUENCER

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control clocks. This sequencer can be activated and programmed through the SPI interface. A detailed description of the SPI registers and sensor (sequencer) programming can be found in Chapter 5 of this document.

2.5 SPI INTERFACE

The SPI interface is used to load the sequencer registers with data. The data in these registers is used by the sequencer while driving and reading out the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system. Chapter 3.9 contains more details on register programming and SPI timing.

2.6 TEMPERATURE SENSOR

A 16-bit digital temperature sensor is included in the image sensor and can be controlled by the SPI-interface. The on-chip temperature can be obtained by reading out the registers with address 126 and 127 (in burst mode, see Chapter 3.9.2 for more details on this mode).

A calibration of the temperature sensor is needed for absolute temperature measurements per device because the offset differs from device to device. The temperature sensor requires a running input clock (CLK_IN), the other functions of the image sensor can be operational or in standby mode. The output value of the sensor is dependent on the input clock. A typical temperature sensor output vs. temperature curve at 40MHz can be found below. The die temperature will be about 10°C~15°C higher than ambient temperature. The ceramic package has about the same temperature as the die.

The typical (offset) value of the temperature sensor at 0°C would be: $1000 * \frac{f\,[MHz]}{40}$ DN. This offset can differ per device. A typical slope would be around $0.3 * \frac{40}{f[MHz]}$ °C/DN.

For example, for the calibration of a sensor you're reading out a temperature register value of 1066 at 35°C die temperature and an input frequency of 40MHz. If later you read out the temperature register value and it is 1184. You can calculate the ambient temperature back from that.

Ambient temperature = [(1184-1066)*0.3*40/40Mhz] + 35°C = 70.4°C die temperature.

Or vice versa, if you want to know the temperature register value for a die temperature of -10°C at 40MHz:

Register value = (-10°C -35°C) * 40MHz/40 * (1/0.3) +1066 = 916 DN

If you want a more accurate calibration you can calibrate the sensor at multiple temperatures, so you will have the exact value of the slope also. For most devices this should be around 0.29 ~0.31.

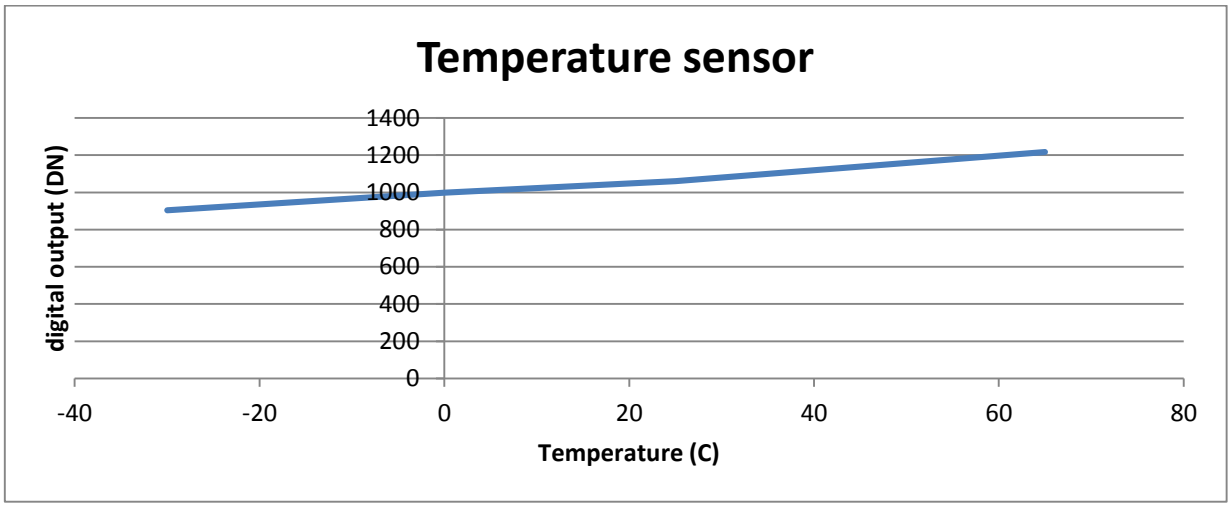

Figure 3: Typical output of the temperature sensor of the CMV4000

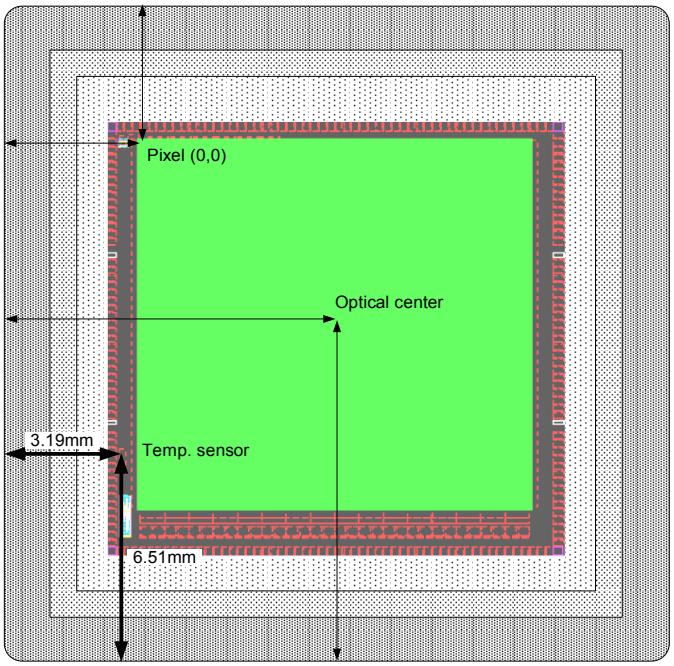

Figure 4: Location of the temperature sensor

3 DRIVING THE CMV4000

3.1 SUPPLY SETTINGS

Supply name	Usage	Recommended value [V]	Range [V]	DC power nominal [mW]	DC current nominal [mA]	DC current peak [mA]
VDD20	LVDS, ADC	2.1	2.0 - 2.2	750	360	360
VDD33	Dig. I\O, PGA, SPI, ADC	3.3	3.0 - 3.6	300	90	90
VDDPIX	Pixel array power supply	3.0	2.3 - 3.6	60	20	218
Vres_h	Pixel reset pulse	3.3	3.0 - 3.6	50	15	15

The power figures are measured at 48MHz CLK_IN speed in 16 channel mode while constantly grabbing images. When idle, the sensor will consume about 25% less energy. Reducing the amount of output channels will reduce power consumption of the VDD20 supply and will have the biggest impact on the power consumption.

All variations on the VDD33 and VDDPIX can contribute to variations (noise) on the analog pixel signal, which is seen as noise in the image. During the camera design precautions have to be taken to supply the sensor with very stable supply voltages to avoid this additional noise.

Because of the peak currents, decoupling is advised. Place large decoupling capacitors directly at the output of the voltage regulator to filter low noise and improve peak current supply. We advise 1x 330µF electrolytic, 1x 33µF tantalum and a 10µF ceramic capacitor per supply, directly at the output of the regulator.

Place small decoupling capacitors as close as possible to the sensor between supply pins and ground. We advise 1x 4.7µF and 1x 100nF ceramic capacitor per power supply pin (see pin list) and 1x 100µF ceramic capacitor per power supply plane (VDD20, VDDPIX, VDD33). Vres_h doesn't need a 100µF capacitor. See pin list for exact pin numbers for every supply. Analog and digital ground can be tied together.

3.2 BIASING

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

3.3 DIGITAL INPUT PINS

The table below gives an overview of the external pins used to drive the sensor. The digital signals are sampled on the rising edge of the CLK_IN, therefor the length of the signal applied to an input should be at least 1 CLK_IN period to assure it has been detected. All digital I/O's have a capacitance of 2pF max.

Pin name	Description
CLK_IN	Master input clock, frequency range between 5 and 48 MHz
LVDS_CLK_N/P	High speed LVDS input clock, frequency range between 50 and 480 MHz. Should not be used if PLL is enabled (default).
SYS_RES_N	System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up. This signal should be at least one period of CLK_IN long to assure detection on the rising edge of CLK_IN.
FRAME_REQ	Frame request pin. When a high level is detected on this pin the programmed number of frames is captured and sent by the sensor. This signal should be at least one period of CLK_IN long to assure detection on the rising edge of CLK_IN.
SPI_IN	Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
SPI_EN	SPI enable pin. When this pin is high the data should be written/read on the SPI
SPI_CLK	SPI clock. This is the clock on which the SPI runs (max 48Mz)
T_EXP1	Input pin to program the exposure time externally. Optional
T_EXP2	Input pin to program the exposure time externally in HDR mode. Optional

3.4 ELECTRICAL I/O SPECIFICATIONS

3.4.1 DIGITAL I/O CMOS/TTL DC SPECIFICATIONS (SEE PIN LIST FOR SPECIFIC PINS)

Parameter	Description	Conditions	min	typ	max	Units
V_{IH}	High level input voltage		2.0		VDD33	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	VDD=3.3V I_{OH}=-2mA	2.4			V
V_{OL}	Low level output voltage	VDD=3.3V I_{OL}=2mA			0.4	V

3.4.2 TIA/EIA-644A[1] LVDS DRIVER SPECIFICATIONS (OUTX_N/P, OUTCLK_N/P, OUTCTR_N/P)

Parameter	Description	Conditions	min	typ	max	Units
V_{OD}	Differential output voltage	Steady State, RL = 100Ω	247	350	454	mV
ΔV_{OD}	Difference in V_{OD} between complementary output states	Steady State, RL = 100Ω			50	mV
V_{OC}	Common mode voltage	Steady State, RL = 100Ω	1.26	1.37	1.50	V
ΔV_{OC}	Difference in V_{OC} between complementary output states	Steady State, RL = 100Ω			50	mV
$I_{OS,GND}$	Output short circuit current to ground	V_{OUTP}=V_{OUTN}=GND			24	mA
$I_{OS,PN}$	Output short circuit current	V_{OUTP}=V_{OUTN}			12	mA

3.4.3 TIA/EIA-644A LVDS RECEIVER SPECIFICATIONS (LVDS_CLK_N/P)

Parameter	Description	Conditions	min	typ	max	Units
V_{ID}	Differential input voltage	Steady state	100	350	600	mV
V_{IC}	Receiver input range	Steady state	0.0		2.4	V
I_{ID}	Receiver input current	$V_{INP\|INN}$=1.2V±50mV, 0≤ $V_{INP\|INN}$≤2.4V			20	µA
ΔI_{ID}	Receiver input current difference	$\|I_{INP} - I_{INN}\|$			6	µA

[1] V_{oc} is dependent on the 2.1V supply voltage, therefore these values differ from the TIA/EIA-644A spec.

3.5 INPUT CLOCK

The input clock (CLK_IN) defines the output data rate of the CMV4000. The master clock (CLK_IN) is 10 or 12 times slower than the output data rate, depending on the programmed bit mode setting. The maximum data rate of the output is 480Mbps which results in CLK_IN of 48MHz in 10-bit mode and 40MHz in 12-bit mode. The minimum frequency for CLK_IN is 5MHz. Any frequency between the minimum and maximum can be applied by the user and will result in a corresponding output data rate. The SPI registers with address 114 and 116 must be programmed to the correct frequency range when the CLK_IN frequency is changed.

CLK_IN	LVDS_CLK 10bit	LVDS_CLK 12bit
5 MHz	50 MHz	60 MHz
40 MHz	400 MHz	480 MHz
48 MHz	480 MHz	n/a

There is no maximum skew for the LVDS input clock (if used) for every frequency used.

3.6 FRAME RATE CALCULATION

The frame rate of the CMV4000 is defined by 2 main factors.

1. Exposure time
2. Read-out time

To simplify the calculation, we will assume that the exposure time is shorter than the read-out time and that the sensor is operating at default settings, taking a full resolution 10-bit image at 48MHz through 16 outputs. This means that the frame rate will be defined only by the read-out time because the exposure time happens in parallel with the read-out time. The read-out time is defined by:

1. Output clock speed: max 240MHz
2. ADC mode: 10 or 12 bit
3. Number of lines read-out
4. Number of LVDS outputs used: max 16 outputs

If any of these parameters is changed, it will have an impact on the frame rate. In default operation this will result in 180FPS. The total read-out time is composed of two parts: FOT (frame overhead time) and the image read-out time.

The FOT is defined as:

$$FOT = \left(fot\_length + \left(2 * \frac{16}{\#outputs\ used} \right) \right) * 129 * master\ clock\ period$$

With fot_length (register 73) at its default value of 20, this results in 59.125µs frame overhead time.

The image read-out time is defined as:

$$Image\ read\text{-}out\ time = (129 * master\ clock\ period * \frac{16}{\#outputs\ used}) * nr\_lines$$

Reading out a full resolution image, this results in 5.504ms image read-out time.

The total read-out time is now the sum of the FOT and the image read-out time, which results in 59.125µs + 5.504ms or 5.563125ms to read-out a single full resolution image. The frame rate is thus 180FPS.

The table below gives some examples of how the frame rate increases when reading out a smaller frame in 10-bit mode.

Number of columns	Number of lines	Frame rate (fps)
2048	2048	180
2048	1024	356
2048	70	4044

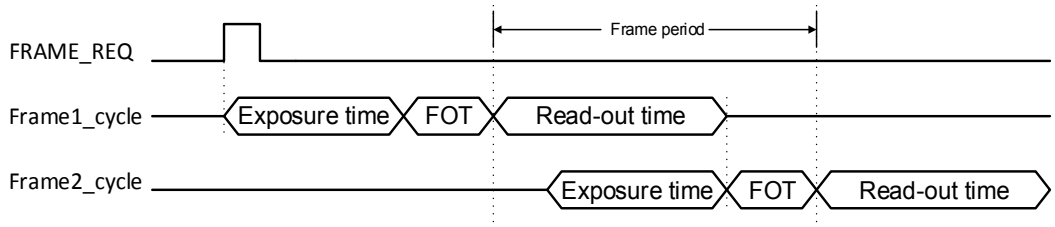

Figure 5: Frame period

When the exposure time is greater than the read-out time, the frame rate is mostly defined by the exposure time itself (because the exposure time would be much longer than the FOT).

3.7 START-UP SEQUENCE

The following sequence should be followed when the CMV4000 is started up in default output mode (480Mbps, 10bit resolution). There is no specific startup sequence for the power supplies needed.

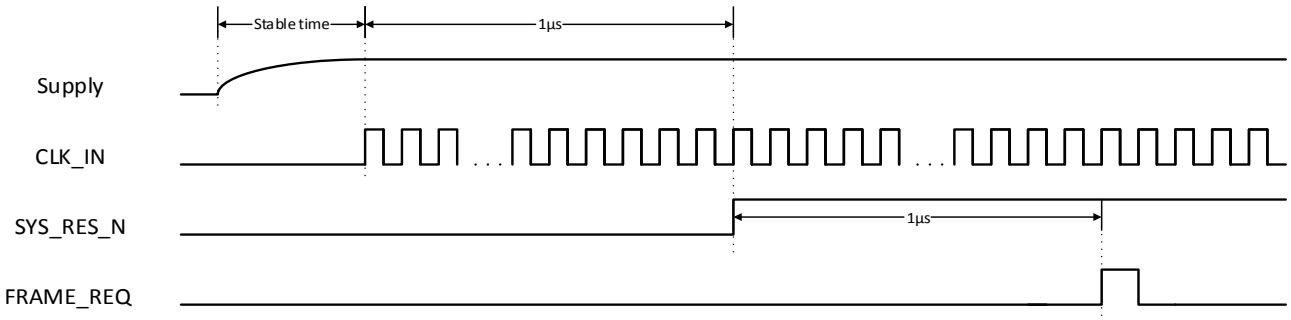

Figure 6: Start-up sequence for 480Mbps @ 10-bit

The master clock CLK_IN (48MHz for 480Mbps in 10-bit mode) should start after the rise time of the supplies. The external reset pin should be released at least 1µs after the supplies are stable. The first frame can be requested 1µs after the reset pin has been released.

If the register settings need to be changed (e.g. when using 12-bit mode), this can be done through an SPI upload 1µs after the rising edge on the SYS_RES_N pin, as described in Figure 7. In this case the FRAME_REQ pulse must not be sent until after the SPI upload is completed, plus a settling time. This settling time is to ensure that the changes programmed in the SPI upload have taken effect before an image is captured. The main factor that determines this settling time is a change in ADC gain, because the voltage over the ramp capacitor has to settle. For typical applications, where the ADC gain is changed from the default value of 32 to a value that saturates the ADC output (40 to 45 at 48MHz), the settling time is 7ms. In extreme cases, when the ADC gain is changed from default to maximum, the settling time can increase to 20ms.

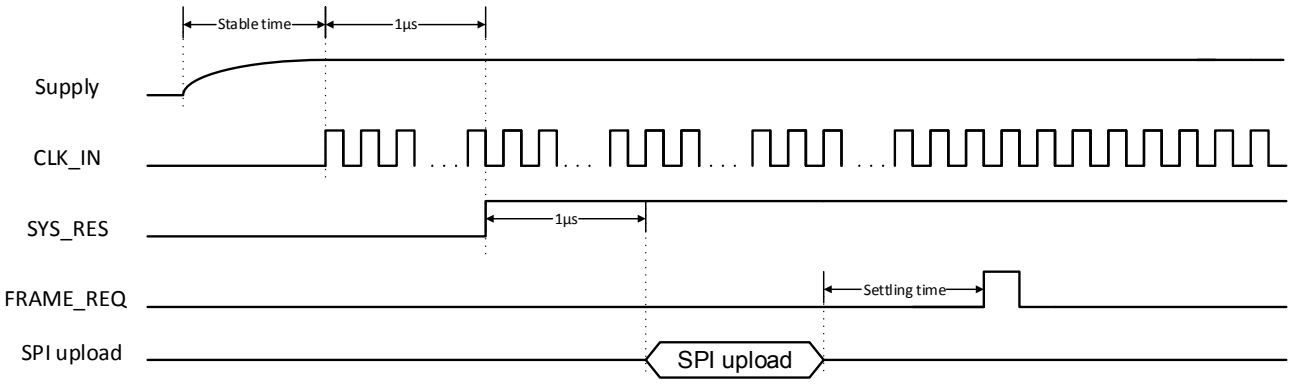

Figure 7: Start-up sequence for 12-bit mode

3.8 RESET SEQUENCE

If a sensor reset is necessary while the sensor is running the following sequence should be followed. The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RES_N pin. As with the start-up sequence, there is a minimum time of 1µs plus a settling time needed before a FRAME_REQ pulse can be sent, to allow the gain settings to settle at their default value.

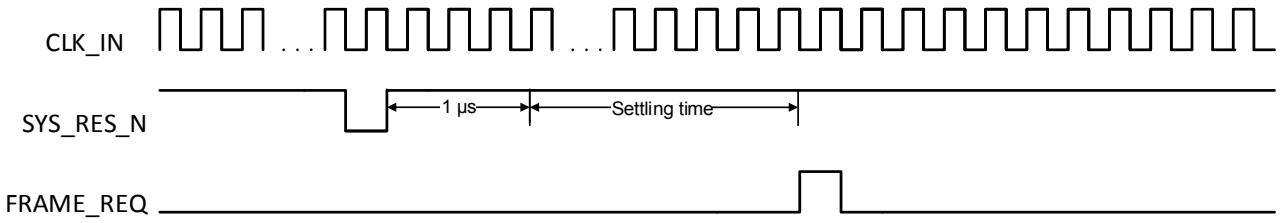

Figure 8: Reset sequence

When register settings are uploaded after the reset (e.g. when changing the bit mode), the following sequence should be followed.

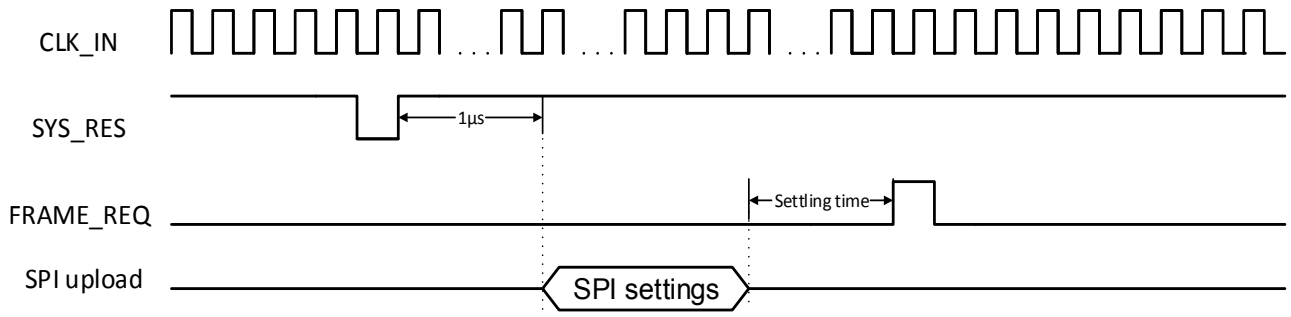

Figure 9: Reset sequence when changing bit mode

3.9 SPI PROGRAMMING

Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

3.9.1 SPI WRITE

The timing to write data over the SPI interface can be found below.

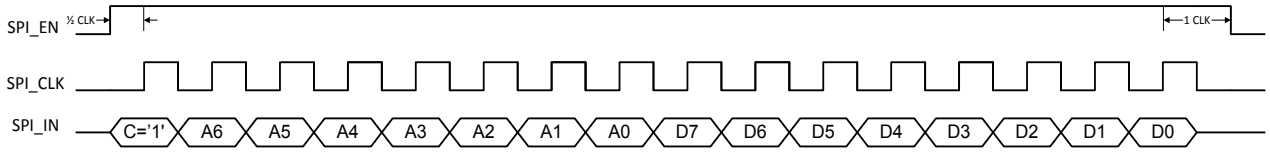

Figure 10: SPI write timing

The data is sampled by the CMV4000 on the rising edge of the SPI_CLK. The SPI_CLK has a maximum frequency of 48MHz. The SPI_EN signal has to be high for half a clock period before the first data bit is sampled. After the last databit is sent, SPI_EN has to remain high for 1 clock period and SPI_CLK has to receive a final falling edge to complete the write operation.

One write action contains 16 bits:

- One control bit: First bit to be sent, indicates whether a read (‘0’) or write (‘1’) will occur on the SPI interface.
- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 8 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the figure below for an example of 2 registers being written in burst.

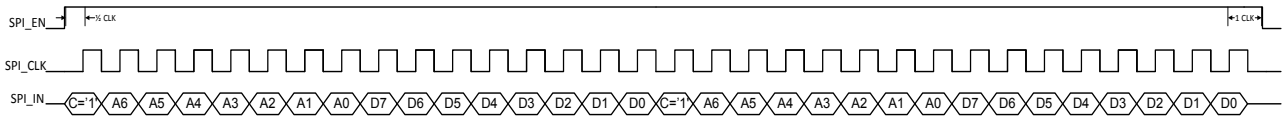

Figure 11: SPI write timing for 2 registers in burst

All registers should be updated during IDLE time. The sensor is not IDLE during a frame burst (between start of integration of first frame and read-out of last pixel of last frame).

Registers 35-38, 40-69, 100-103 can be updated during IDLE or FOT. Registers 1-34 and 70-71 can always be updated but it is recommended to update these during IDLE or FOT to minimize image effects. Registers 78-79 can always be updated without disrupting the imaging process.

3.9.2 SPI READ

The timing to read data from the registers over the SPI interface can be found below.

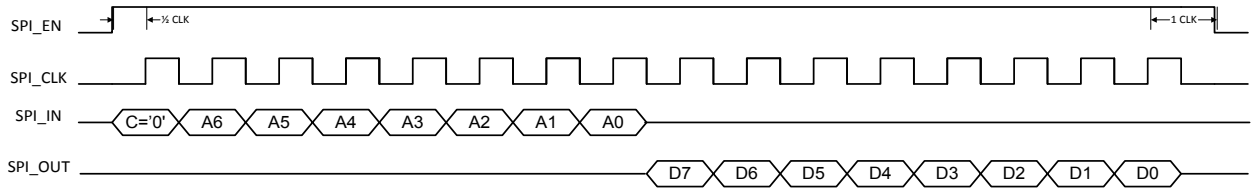

Figure 12: SPI read timing

To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made '0'. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK. This means that the data should be sampled by the receiving system on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first. When reading out the temperature sensor over the SPI, addresses 126 and 127 should de read-out in burst mode (keep SPI_EN high)

3.10 REQUESTING A FRAME

After starting up the sensor (see 3.7), a number of frames can be requested by sending a FRAME_REQ pulse. The number of frames can be set by programming the appropriate register (addresses 70 and 71). The default number of frames to be grabbed is 1.

In internal-exposure-time mode, the exposure time will start after this FRAME_REQ pulse. In the external-exposure-time mode, the read-out will start after the FRAME_REQ pulse. Both modes are explained into detail in the chapters below.

3.10.1 INTERNAL EXPOSURE CONTROL

In this mode, the exposure time is set by programming the appropriate registers (address 42-44) of the CMV4000.

After the high state of the FRAME_REQ pulse is detected, the exposure time will start after a delay of 133 clock cycles, see AN16 – Exposure Timings for all the timing details. When the exposure time ends (as programmed in the registers), the pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). Immediately after the FOT, the frame is read-out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one.

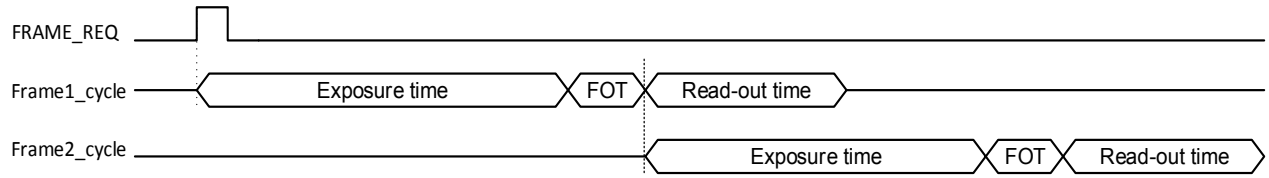

Figure 13: request for 2 frames in internal- exposure-time mode

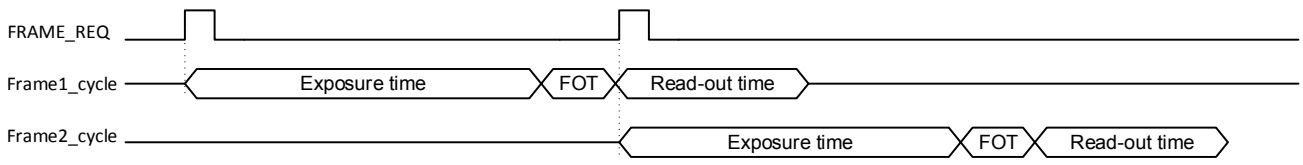

Figure 14: Two requests for 1 frame in internal exposure mode

When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame. Keep in mind that the next FRAME_REQ pulse has to occur after the FOT of

the current frame. For an exact calculation of the exposure time see Chapter 5.1. When a new FRAME_REQ is applied, the exposure of the next frame will be delayed so that the FOT begins right after the read-out time of the current frame.

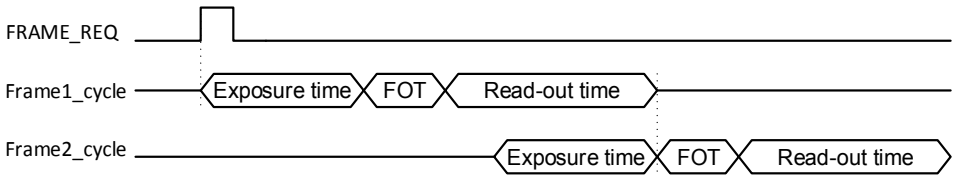

Figure 15: Request for 2 frames in internal exposure mode with exposure time < read-out time

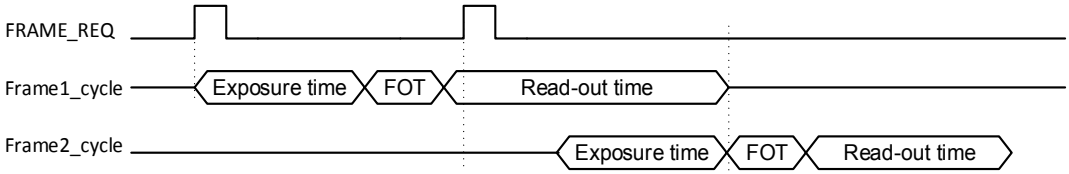

Figure 16: Two requests for 1 frame in internal exposure mode

3.10.2 EXTERNAL EXPOSURE TIME

The exposure time can also be programmed externally by using the T_EXP1 input pin. This mode needs to be enabled by setting the appropriate register (address 41). In this case, the exposure starts when a high state is detected on the T_EXP1 pin. When a high state is detected on the FRAME_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the T_EXP1 pin during or after the read-out of the previous frame. The minimum time between T_EXP1 and FRAME_REQ is 1 master clock cycle, the minimum time between FRAME_REQ and T_EXP1 pulse is FOT. For an exact calculation of the exposure time see Chapter 5.1.

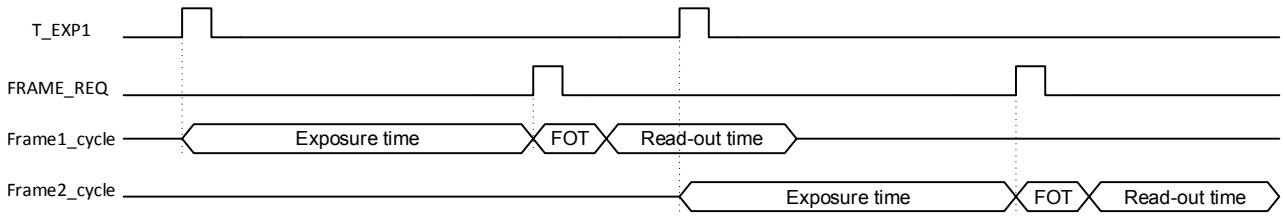

Figure 17: request for 2 frames using external-exposure-time mode

4 READING OUT THE SENSOR

4.1 LVDS DATA OUTPUTS

The CMV4000 has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 16 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 18 LVDS output pairs (2 pins for each LVDS channel):

- 16 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 36 pins of the CMV4000 are used for the LVDS outputs (32 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs.

The 16 data channels are used to transfer the 10-bit or 12-bit pixel data from the sensor to the receiver in the surrounding system.

The output clock channel transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 480Mbps output data rate is used, the LVDS output clock will be 240MHz.

The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 10-bit or 12-bit words that are transferred synchronous to the 16 data channels.

4.2 LOW-LEVEL PIXEL TIMING

Figure 18 and Figure 19 show the timing for transfer of 10-bit and 12-bit pixel data over one LVDS output. To make the timing more clear, the figures show only the p-channel of each LVDS pair. The data is transferred LSB first, with the transfer of bit D0 during the high phase of the DDR output clock OUTCLK.

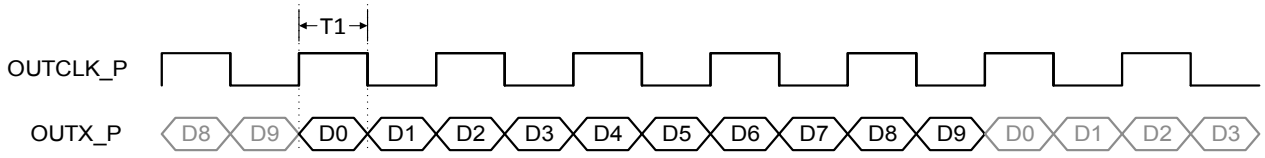

Figure 18: 10-bit pixel data on an LVDS channel

The time 'T1' in Figure 18 is 1/10th of the period of the CLK_IN input clock. If a frequency of 48MHz is used for CLK_IN (max in 10-bit mode), this results in a 240MHz OUTCLK frequency.

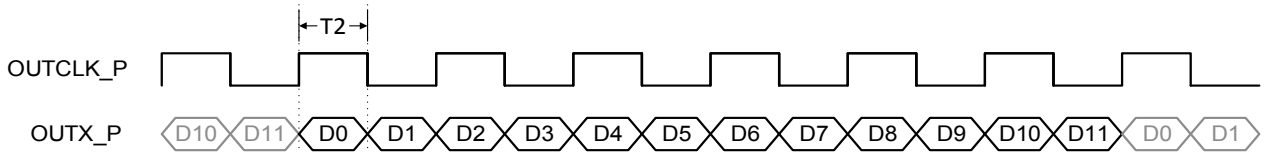

Figure 19: 12-bit pixel data on an LVDS channel

The time 'T2' in Figure 19 is 1/12th of the period of the CLK_IN input clock. If a frequency of 40MHz is used for CLK_IN (max in 12-bit mode), this results in a 240MHz OUTCLK frequency.

4.3 READ-OUT TIMING

The read-out of image data is grouped in bursts of 128 pixels per channel. Each pixel is either 10 or 12 bits of data (see Chapter 4.2). One complete pixel period equals one period of the master clock input. For details on pixel remapping and pixel vs. channel location please see Chapter 4.4 of this document. An overhead time exists between two bursts of 128 pixels. This overhead time has the same length of one pixel read-out (i.e. the length of 10 or 12 bits at the selected data rate or one master clock period). For details on how to program the sequencer for different output modes, see Chapter 5.7.

4.3.1 10 BIT MODE

In this section, the read-out timing for the default 10 bit mode is explained. In this mode the maximum frame rate of 180FPS can be reached. To simplify the figures below, the timing for only one LVDS channel is shown in every case.

4.3.1.1 16 OUTPUT CHANNELS

By default, all 16 data output channels are used to transmit the image data. This means that an entire row of image data is transferred in one slot of 128 pixel periods (16 x 128 = 2048). This results in a maximum frame rate of 180FPS.

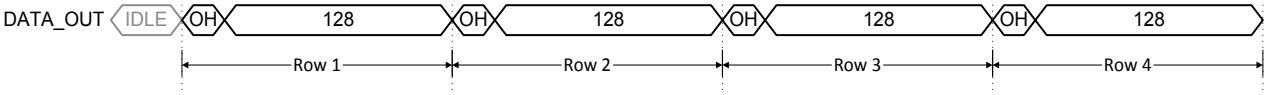

Figure 20: Output timing in default 16 channel mode

4.3.1.2 8 OUTPUT CHANNELS

When only 8 LVDS output channels are used, the read-out of one row takes (2 x 128) + (2 x 1) master clock periods. The maximum frame rate is reduced with a factor of 2 compared to 16 channel mode.

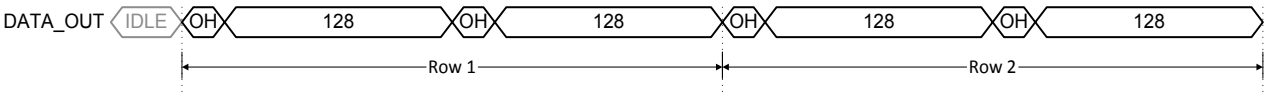

Figure 21: Output timing in 8 channel mode

4.3.1.3 4 OUTPUT CHANNELS

When only 4 LVDS output channels are used, the read-out of one row takes (4 x 128) + (4 x 1) master clock periods. The maximum frame rate is reduce with a factor of 4 compared to 16 channel mode.

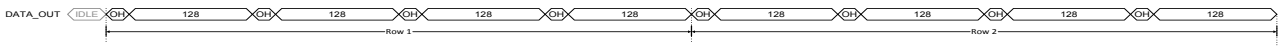

Figure 22: Output timing in 4 channel mode

4.3.1.4 2 OUTPUT CHANNELS

When only 2 LVDS output channels are used, the read-out of one row takes (8 x 128) + (8 x 1) master clock periods. The maximum frame rate is reduced with a factor of 8 compared to 16 channel mode.

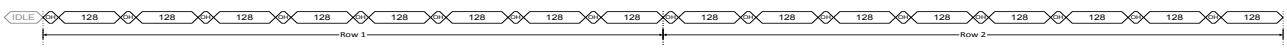

Figure 23: Output timing in 2 channel mode

4.3.2 12 BIT MODE

In 12 bit mode, the analog-to-digital conversion takes 4x longer to complete. This causes the frame rate to drop to 37.5 fps when 40MHz is used for CLK_IN. Due to this extra conversion time, the sensor automatically multiplexes to 4 outputs when 12 bit is used. To simplify the figures below, the timing for only one LVDS channel is shown in every case.

4.3.2.1 4 OUTPUT CHANNELS

By default, the CMV4000 uses only 4 LVDS output channels in 12 bit mode. This means that the read-out of one row takes (4 x 128) + (4 x 1) master clock periods.

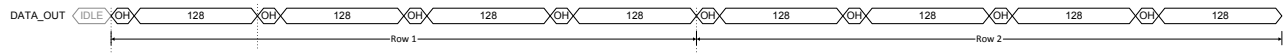

Figure 24: Output timing in 4 channel mode

4.3.2.2 2 OUTPUT CHANNELS

When only 2 LVDS output channels are used, the read-out of one row takes (8 x 128) + (8 x 1) master clock periods. The maximum frame rate is reduced with a factor of 2 compared to 4-channel mode.

Figure 25: Output timing in 2 channel mode

4.4 PIXEL REMAPPING

Depending on the number of output channels, the pixels are read out by different channels and come out at a different moment in time. With the details from the next sections, the end user is able to remap the pixel values at the output to their correct image array location.

4.4.1 16 OUTPUTS

Figure 26 shows the location of the image pixels versus the output channel of the image sensor.

16 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 2048 rows being read out.

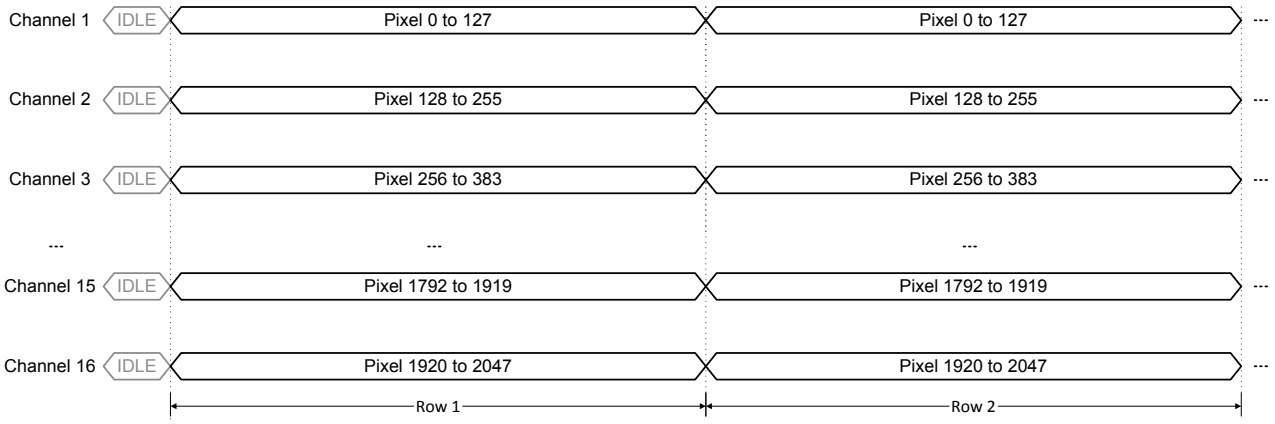

Figure 26: Pixel remapping for 16 output channels

4.4.2 8 OUTPUTS

When only 8 outputs are used, the pixel data is placed on the outputs as detailed in Figure 27. 8 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in two bursts. The time needed to read out one row is doubled compared to when 16 outputs are used. Channel 2, 4, 6…16 are not being used in this mode, so they can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be read out can be set in the register. By default 2048 rows are read out.

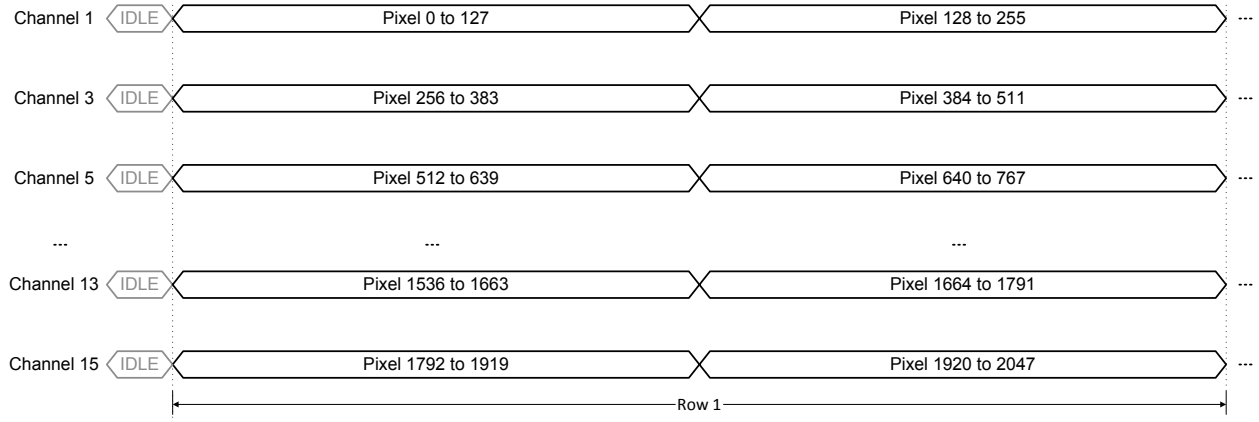

Figure 27: Pixel remapping for 8 output channels

4.4.3 4 OUTPUTS

When only 4 outputs are used, the pixel data is placed on the outputs as detailed in Figure 28. 4 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in four bursts. The time needed to read out one row is 4x longer compared to when 16 outputs are used. Only channel 1, 5, 9 and 13 are being used in this mode, so the remaining channels can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be read out can be set in the register. By default 2048 rows are read out.

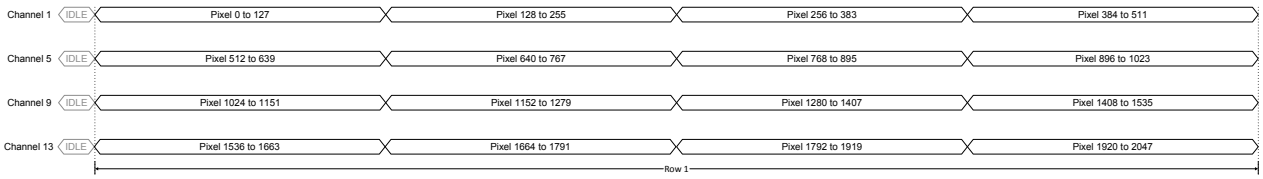

Figure 28: Pixel remapping for 4 output channels

4.4.4 2 OUTPUTS

When only 2 outputs are used, the pixel data is placed on the outputs as detailed in Figure 29. 2 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in 8 bursts. The time needed to read out one row is 8x longer compared to when 16 outputs are used. Only channel 1 and 9 are being used in this mode, so the remaining channels can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be read out can be set in the register. By default 2048 rows are read out.

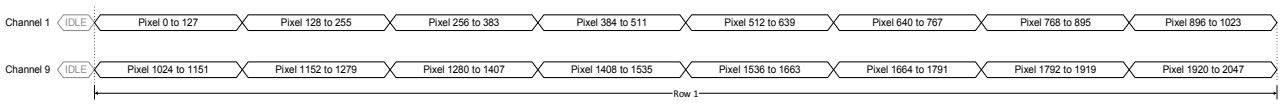

Figure 29: Pixel remapping for 2 output channels