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Datasheet

DS000522

CMV50000

47.5MP CMOS Machine Vision Image Sensor

v1-00 • 2018-Feb-23

Content Guide

1 General Description

The CMV50000 is a high speed CMOS image sensor with 7920 × 6004 effective pixels (47.5Mp) developed for machine vision and video applications. The image array consists of 4.6µm pipelined 8T global shutter pixels which allow exposure during read out, while performing true CDS (Correlated Double Sampling) operation. The image sensor also integrates a programmable analog gain amplifier and offset regulation. The image sensor has 22 digital sub-LVDS data output channels. Each output channel runs up to 830 Mbit/s, which results in a frame rate of 30 fps at full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read out timings are generated by a programmable on-chip sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by a dual exposure HDR mode.

1.1 Key Benefits & Features

The benefits and features of CMV50000, 47.5MP CMOS Machine Vision Image Sensor, are listed below:

Figure 1:
Added Value of Using CMV50000

Benefits	Features
Designed for high performance applications	Resolution of 7920x6004 at 30 frames per second
Capture fast moving objects	8T global shutter pixel with true Correlated Double Sampling (true-CDS)
Use in low light conditions	Low noise (8.8e) and high sensitivity (QE=60%), with on-chip noise reduction.
Use in bright light conditions	In binning mode the full well capacity reaches 58000e^- with an SNR of 47.6dB and DR=68dB
Standard optics can be used	35mm Full Frame optical format
Easy to operate	On-chip digital sequencer which handles all the sensor controls, over SPI

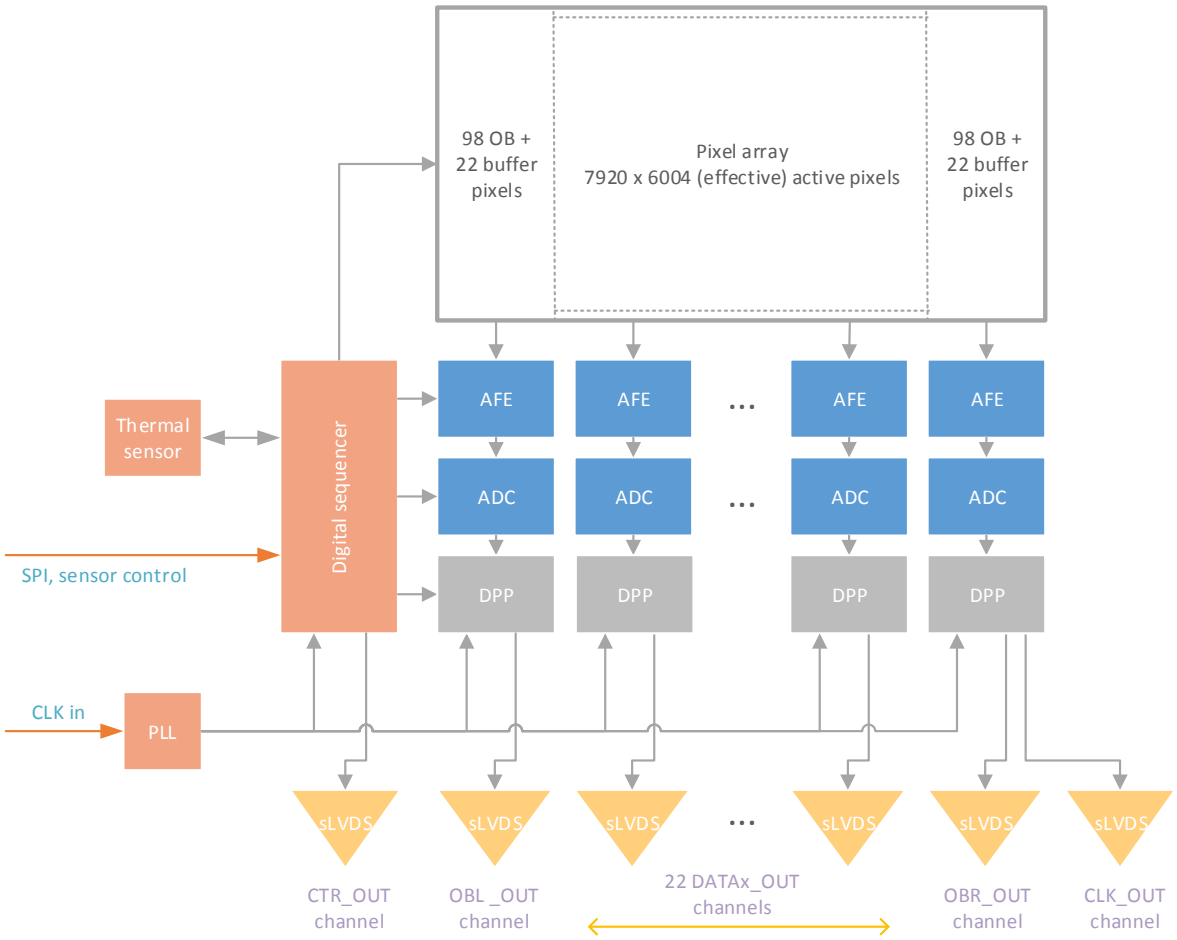
1.2 Applications

- Machine vision
- Video/Broadcast
- Security
- High-end inspection
- Aerial mapping
- Document scanning
- ITS
- Scientific
- 3D imaging

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2 :
Functional Blocks of CMV50000



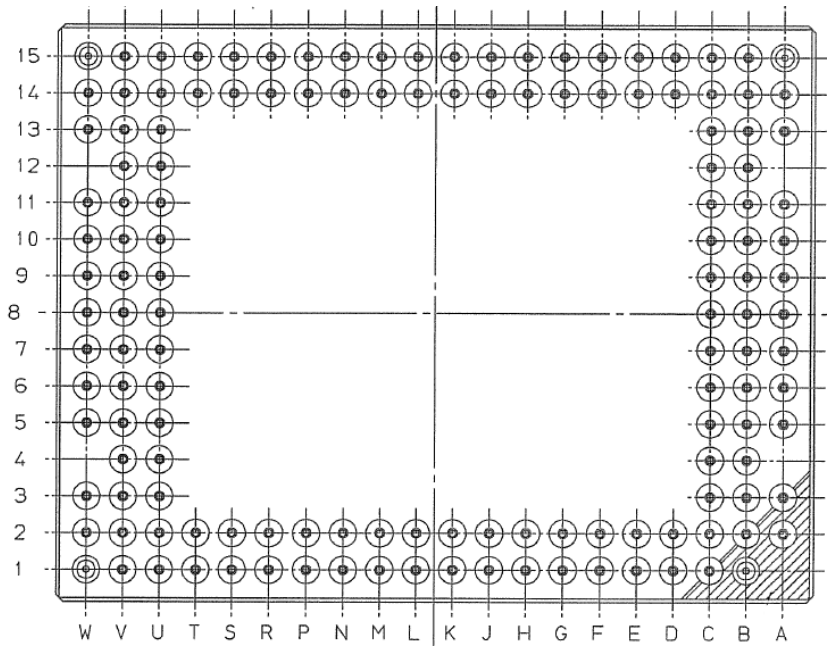
2 Ordering Information

Ordering Code	Package	Chroma	Options	Delivery Quantity
CMV50000ES-1E3M1PA	PGA	Mono		10 Pcs / Tray
CMV50000ES-1E3C1PA	PGA	Color		10 Pcs / Tray

3 Pin Assignment

3.1 Pin Diagram

Figure 3 :
Pin Numbering (bottom view)



3.2 Pin Description

Figure 4:
Pin Description of CMV50000

Pin Number	Pin Name	Pin Type	Description
A2	SPI_CSN	Digital input	SPI Chip Select
A3	VSSA	Analog ground	Analog ground
A5	REQ_FRAME	Digital input	Request frame (stop exposure)
A6	VDDARRAY	Analog supply	Pixel array supply
A7	VDDARRAY	Analog supply	Pixel array supply
A8	NC1	Analog	Do Not Connect
A9	NC2	Analog	Do Not Connect

Pin Number	Pin Name	Pin Type	Description
A10	CTRL_P	sub-LVDS	Control channel output
A11	CTRL_N	sub-LVDS	Control channel output
A13	VSSA	Analog ground	Main analog ground
A14	DOBL_P	sub-LVDS	Left Optical Black output
A15	DOBL_N	sub-LVDS	Left Optical Black output
B1	SPI_MISO	Digital output	SPI Master In/Slave Out data
B2	SPI_MOSI	Digital input	SPI Master Out/Slave In data
B3	SPI_CLK	Digital input	SPI clock
B4	CLK_IN	Digital input	Sensor input clock
B5	RST_N	Digital input	Asynchronous hard reset input pin
B6	VDD33	Analog supply	On-chip regulators supply
B7	VSELHREG	Analog	On-chip regulator output
B8	VS2HREG	Analog	On-chip regulator output
B9	VS1HREG	Analog	On-chip regulator output
B10	VTXHREG	Analog	On-chip regulator output
B11	VRESHREG	Analog	On-chip regulator output
B12	VDD27	Analog supply	Main analog supply
B13	D00_P	sub-LVDS	Channel 0 output
B14	D00_N	sub-LVDS	Channel 0 output
B15	D02_P	sub-LVDS	Channel 2 output
C1	VDDD12PLL1	Digital supply	Digital supply for PLL1
C2	VDDD12PLL2	Digital supply	Digital supply for PLL2
C3	REQ_EXP	Digital input	Request exposure (start exposure)
C4	VDD27	Analog supply	Main analog supply
C5	VSSD	Digital ground	Digital ground
C6	VSSD	Digital ground	Digital ground
C7	VSELH	Analog	Bias
C8	VS2H	Analog	Bias
C9	VS1H	Analog	Bias
C10	VTXH	Analog	Bias
C11	VRESH	Analog	Bias
C12	D01_P	sub-LVDS	Channel 1 output
C13	D01_N	sub-LVDS	Channel 1 output
C14	D03_P	sub-LVDS	Channel 3 output
C15	D02_N	sub-LVDS	Channel 2 output

Pin Number	Pin Name	Pin Type	Description
D1	VDD12C	Digital supply	Logic supply for ADC
D2	VSSD	Digital ground	Main digital ground
D14	D03_N	sub-LVDS	Channel 3 output
D15	D04_P	sub-LVDS	Channel 4 output
E1	VSSDPLL1	Digital ground	Digital ground for PLL1
E2	VSSDPLL2	Digital ground	Digital ground for PLL2
E14	D05_P	sub-LVDS	Channel 0 output
E15	D04_N	sub-LVDS	Channel 0 output
F1	VSSAPLL1	Analog ground	Analog ground for PLL1
F2	VSSAPLL2	Analog ground	Analog ground for PLL2
F14	D05_N	sub-LVDS	Channel 5 output
F15	D06_P	sub-LVDS	Channel 6 output
G1	VDDA12PLL1	Analog supply	Analog supply for PLL1
G2	VDDA12PLL2	Analog supply	Analog supply for PLL2
G14	D07_P	sub-LVDS	Channel 7 output
G15	D06_N	sub-LVDS	Channel 6 output
H1	VDD12	Digital supply	Logic supply for core logic
H2	VSSD	Digital ground	Main digital ground
H14	D07_N	sub-LVDS	Channel 7 output
H15	D08_P	sub-LVDS	Channel 8 output
J1	VDD12	Digital supply	Logic supply for core logic
J2	VSSA	Analog ground	Main analog ground
J14	D09_P	sub-LVDS	Channel 9 output
J15	D08_N	sub-LVDS	Channel 8 output
K1	VDD12C	Digital supply	Logic supply for ADC
K2	VSSA	Analog ground	Main analog ground
K14	D09_N	sub-LVDS	Channel 9 output
K15	D10_P	sub-LVDS	Channel 10 output
L1	VSSDC	Digital ground	Digital ground for ADC
L2	VDDARRAY	Analog supply	Pixel array supply
L14	D11_P	sub-LVDS	Channel 11 output
L15	D10_N	sub-LVDS	Channel 10 output
M1	VSSDC	Digital ground	Digital ground for ADC
M2	VDDARRAY	Analog supply	Pixel array supply
M14	D11_N	sub-LVDS	Channel 11 output

Pin Number	Pin Name	Pin Type	Description
M15	D12_P	sub-LVDS	Channel 12 output
N1	VSSDC	Digital ground	Digital ground
N2	VSSD	Digital ground	Digital ground
N14	D13_P	sub-LVDS	Channel 13 output
N15	D12_N	sub-LVDS	Channel 12 output
P1	VDD18	Digital supply	I/O supply for CMOS and I/O's
P2	VDD27	Analog supply	Main analog supply
P14	D13_N	sub-LVDS	Channel 13 output
P15	D14_P	sub-LVDS	Channel 14 output
R1	VDD18	Digital supply	I/O supply for CMOS and I/O's
R2	VDD27	Analog supply	Main analog supply
R14	D15_P	sub-LVDS	Channel 15 output
R15	D14_N	sub-LVDS	Channel 14 output
S1	VDD27CP	Analog supply	Connect to VDD27
S2	VSSACP	Analog ground	Analog ground
S14	D15_N	sub-LVDS	Channel 15 output
S15	D16_P	sub-LVDS	Channel 16 output
T1	VDD12C	Digital supply	Logic supply for ADC
T2	VSSD	Digital ground	Main digital ground
T14	D17_P	sub-LVDS	Channel 17 output
T15	D16_N	sub-LVDS	Channel 16 output
U1	EXTRA1	Analog ground	Connect to analog ground
U2	TDIGO1	Digital output	Digital test output
U3	TANAI1	Analog	Do Not Connect
U4	TANAI2	Analog	Do Not Connect
U5	VSELLNEG12	Analog	On-chip regulator output
U6	VS2LNEG12	Analog	On-chip regulator output
U7	VPCLNEG12	Analog	On-chip regulator output
U8	VS1LNEG12	Analog	On-chip regulator output
U9	VABNEG12	Analog	On-chip regulator output
U10	VRESLNEG12	Analog	On-chip regulator output
U11	VRESL	Analog	Bias
U12	D19_N	sub-LVDS	Channel 19 output
U13	D19_P	sub-LVDS	Channel 19 output
U14	D17_N	sub-LVDS	Channel 17 output

Pin Number	Pin Name	Pin Type	Description
U15	D18_P	sub-LVDS	Channel 18 output
V1	REF2	Analog	Do Not Connect
V2	JTAG_MODE	Digital input	JTAG Mode select. Connect to VSSD if JTAG is not used.
V3	REF3	Analog	Bias
V4	TANAO	Analog	Do Not Connect
V5	VSELL	Analog	Bias
V6	VS2L	Analog	Bias
V7	VPCL	Analog	Bias
V8	VS1L	Analog	Bias
V9	VABREG	Analog	On-chip regulator output
V10	VRESLREG	Analog	On-chip regulator output
V11	DOBR_P	sub-LVDS	Right Optical Black output
V12	DOBR_N	sub-LVDS	Right Optical Black output
V13	D20_N	sub-LVDS	Channel 20 output
V14	D20_P	sub-LVDS	Channel 20 output
V15	D18_N	sub-LVDS	Channel 18 output
W1	REF1	Analog	Do Not Connect
W2	REF0	Analog	Bias
W3	VSSA	Analog ground	Analog ground
W5	VSELLREG	Analog	On-chip regulator output
W6	VS2LREG	Analog	On-chip regulator output
W7	VPCLREG	Analog	On-chip regulator output
W8	VS1LREG	Analog	On-chip regulator output
W9	VAB	Analog	Bias
W10	CLK_N	sub-LVDS	Clock output
W11	CLK_P	sub-LVDS	Clock output
W13	VSSA	Analog ground	Main analog ground
W14	D21_N	sub-LVDS	Channel 21 output
W15	D21_P	sub-LVDS	Channel 21 output

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings of CMV50000

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
I_{SCR}	Input Current (latch-up immunity)	±100		mA	JEDEC JESD78D Nov 2011
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±2000		V	JEDEC JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	±250		V	JEDEC JS-002-2014
Temperature Ranges and Storage Conditions					
T_J	Operating Junction Temperature	-30	70	°C	
T_{STRG}	Storage Temperature Range	-30	70	°C	
R_{HNC}	Relative Humidity (non-condensing)	30	60	%	Storage condition

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics of CMV50000

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supplies						
VDD12	Logic Supply Voltage of digital core, PLL		1.10	1.20	1.30	V
VDD12C	Logic Supply Voltage of ADC		1.10	1.20	1.30	V
VDD18	I/O Supply Voltage for sub-LVDS, CMOS I/O's		1.70	1.80	1.90	V
VDD27	Main Analog Supply Voltage; Supply Voltage for negative regulators		2.60	2.70	2.80	V
VDDARRAY	Pixel Array Supply Voltage		2.60	2.70	2.80	V
VDD33	Internal Regulator Supply Voltage		3.20	3.30	3.40	V
IDD12	Supply Current	Idle Running		350 375		mA
IDD12C	Supply Current	Idle Running		10 410		mA
IDD18	Supply Current	Idle Running		130 115		mA
IDD27	Supply Current	Idle Running		550 550		mA
IDDARRAY	Supply Current	Idle Running		130 130 (1)		mA
IDD33	Supply Current	Idle Running		20 20		mA
Ptot	Total Power Consumption	Idle Running		2.5 3.0		W
Digital I/O						
V_{IH}	High level input voltage		0.7 × VDD18		VDD18 +0.5	V
V_{IL}	Low level input voltage		-0.5		0.3 × VDD18	V
V_{OH}	High level output voltage	I_{OH}=4mA	VDD18 -0.15		-	V
V_{OL}	Low level output voltage	I_{OL}=4mA	-		0.15	V
C_I	Input load		-		10	pF
C_O	Output load		-		20	pF
T_{tran}	Input transition time		0.1		5.0	ns
f_{CLK_IN}	CLK_IN frequency		6		96	MHz
DC_{CLK_IN}	CLK_IN duty cycle		40		60	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SPI_CLK}	SPI input clock frequency		-		10	MHz
t_{setup}	SPI setup time		0.25 × T_{SPI_CLK}		-	ns
t_{hold}	SPI hold time		0		-	ns
t_{REQ}	REQ_FRAME/EXP pulse width		2 × T_{CLK_PIX}		-	ns
Sub-LVDS Interface						
V_{CM}	Common mode voltage		0.8	0.9	1.0	V
V_{OD}	Differential voltage swing		100	150	200	mV
R_O	Output impedance (2)		40		240	Ohm
D_{R0}	Impedance mismatch				10	%
DC	Clock duty cycle		45	50	55	%
f	Operating frequency		60		415	MHz
I_{OD}	Drive current		1	1.5	2	mA
ΔIOD	IOD variation over Temp.				15	%
I_{DC}	DC current consumption			3.7		mA
I_{AC}	AC current consumption			7.2		µA/MHz

(1) VDDARRAY draws high peak currents (>1A) during GLOB. Enough decoupling is needed to suppress these peaks.
(2) Unused sub-LVDS channels must be terminated the same way as the used channels.

6 Typical Operating Characteristics

6.1 Electro-Optical Characteristics

Below are the typical electro-optical specifications of the CMV50000. These are typical values for the whole operating temperature range.

Figure 7:
Electro-Optical Characteristics of CMV50000

Parameter	Value	Remark
Effective pixels	7920 × 6004	
Pixel pitch	4.6 × 4.6 µm^2	
Optical format	35mm full frame	
Pixel type	Global shutter with true CDS	Allows fixed pattern noise correction and reset (kTC) noise canceling by true correlated double sampling (true-CDS).
Shutter type	Pipelined global shutter	Exposure of next image during readout of the previous image.
Full well charge	14500 e$^-$ 58000 e$^-$	Normal mode Binning mode
Conversion gain	0.27 DN/e$^-$ 0.068 DN/ e$^-$	Normal mode, unity gain Binning mode, unity gain
Responsivity	0.16 DN/photon 0.25 A/W	@ 510nm (with micro-lenses)
Temporal noise	8.8 e$^-$ 22 e$^-$	Normal mode Binning mode
Dynamic range	64 dB 68 dB	Normal mode Binning mode
SNR_{MAX}	41.6 dB 47.6dB	Normal mode Binning mode
Shutter efficiency 1/PLS	1/18000	At 520nm, f/8.
DC	0.24 e$^-$/s 66.2 e$^-$/s	@ 20°C sensor temperature @ 60°C sensor temperature Dark Current doubles every 5.1°C increase
DCNU	0.72 e$^-$/s 14.2 e$^-$/s	@ 20°C sensor temperature @ 60°C sensor temperature DC Non-Uniformity doubles every 10°C increase
DSNU	24.5 e$^-$	Dark Signal Non Uniformity (FPN) <0.2%rms of saturation
PRNU	< 1.0% RMS	Photo Response Non Uniformity RMS of signal

Parameter	Value	Remark
Color filters	Optional	RGB Bayer pattern
QE	58 / 61 / 53 / 14.5 % 49 / 55 / 45 %	Quantum Efficiency (with micro-lenses) @ 450 / 510 / 600 / 850nm (mono device) @ 450 / 510 / 600nm (color device)
Sub-LVDS outputs	22 Data 1 Control 1 Clock	Each data output running @ 830 Mbit/s. Less outputs selectable at reduced frame rate
Frame rate	30 fps	Using 830 Mbit/s sub-LVDS in pixel-based output Higher frame rate possible in row windowing mode.
Timing generation	On-chip	Possibility to control exposure time through external pin.
PGA	Yes	x1, x1.33, x2, x4 analog gain settings
Programmable registers	Sensor parameters	Window coordinates, Timing parameters, Gain & offset, Exposure time,
HDR mode	Interleaved	2 exposure times for odd/even columns
ADC	12 bit	Column ADC
Interface	sub-LVDS; 830 Mbit/s	Serial output data + synchronization signals
I/O logic levels	sub-LVDS = 1.2 V Dig. I/O = 1.8 V	
Cover glass	D263T eco	Double sided AR coating R<1.5 % abs, 400 - 900nm, per surface, AOI=15°
Mass	20gr	

6.2 Spectral Characteristics

Figure 8 :
Quantum Efficiency

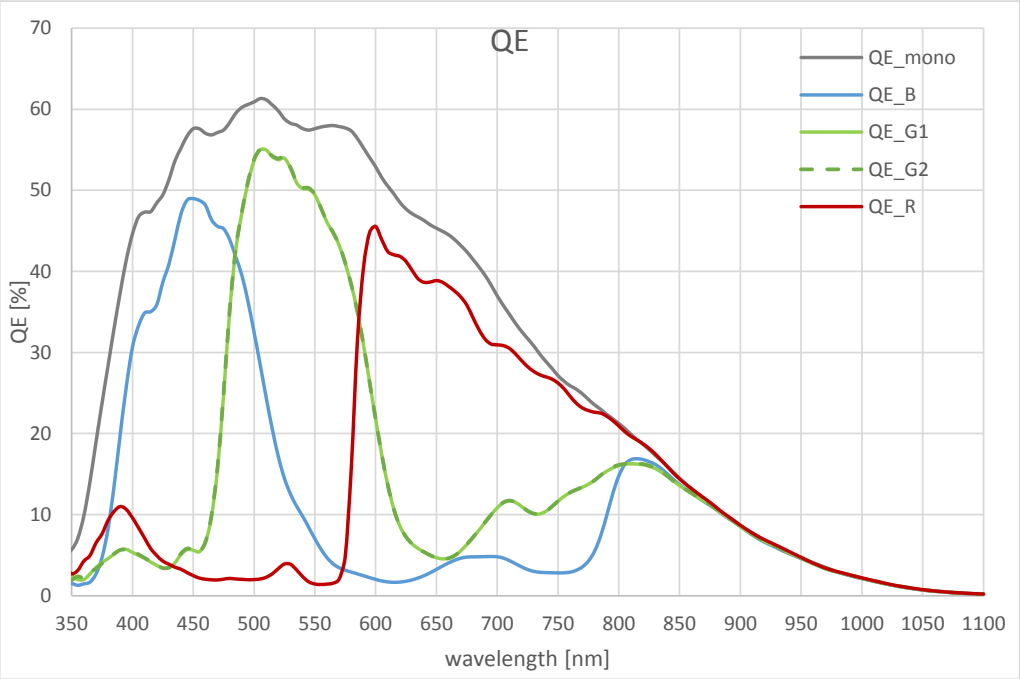


Figure 9 :
Responsivity (Analog Gain x4)

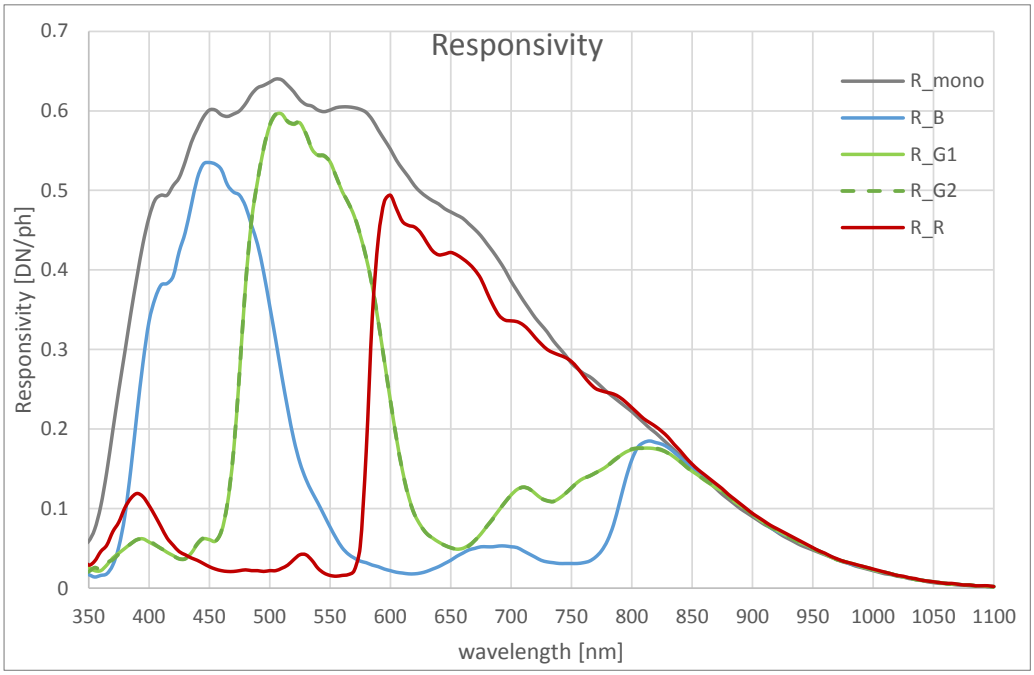


Figure 10 :
Spectral Response

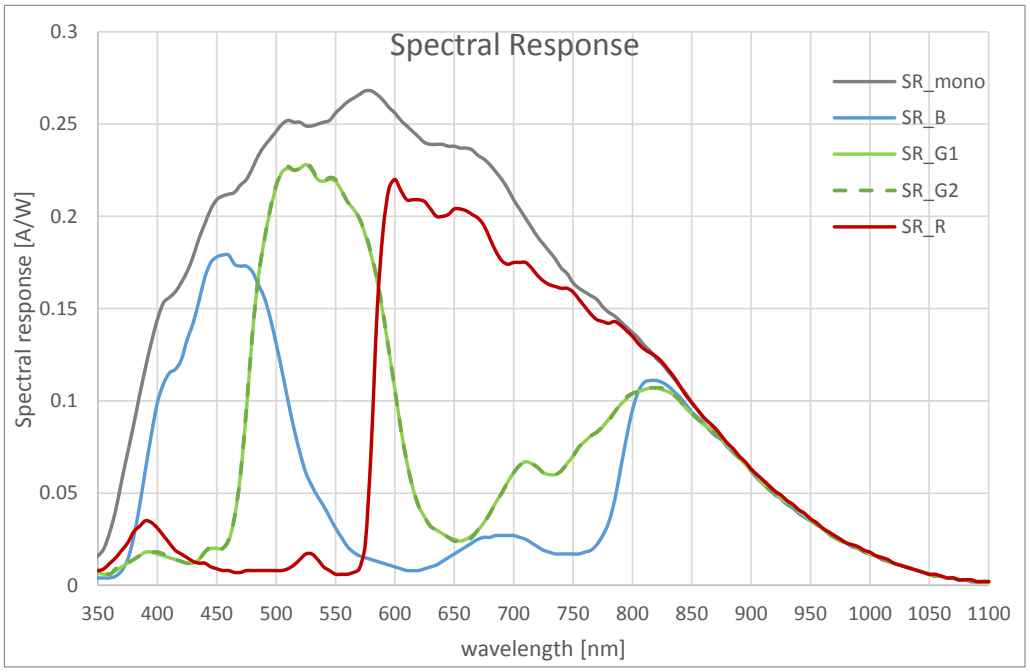


Figure 11 :
Responsivity (Analog Gain x4)

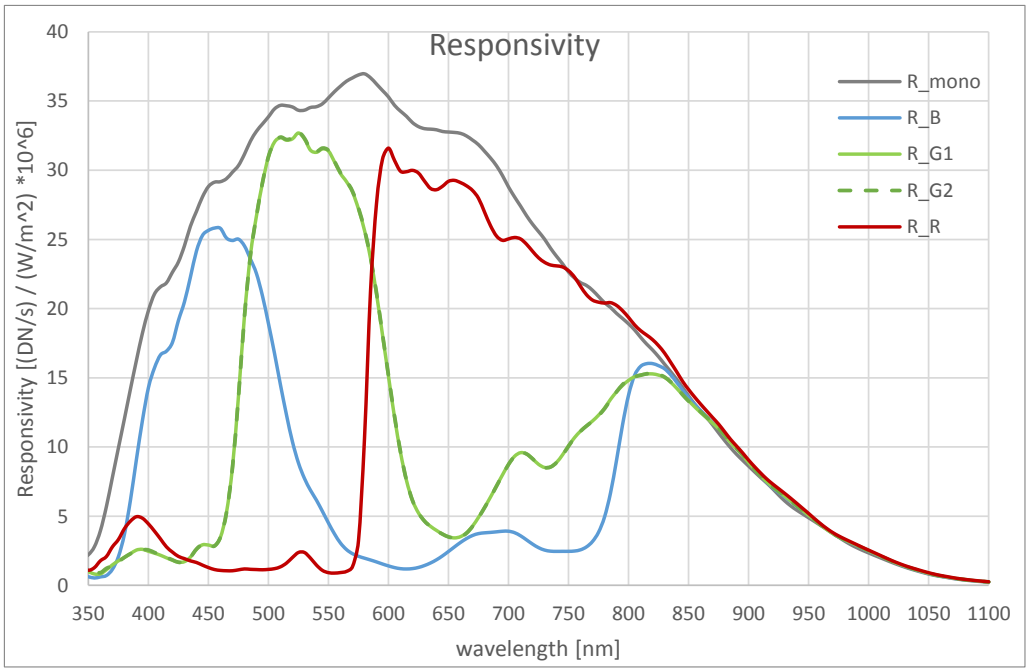


Figure 12 :
MTF

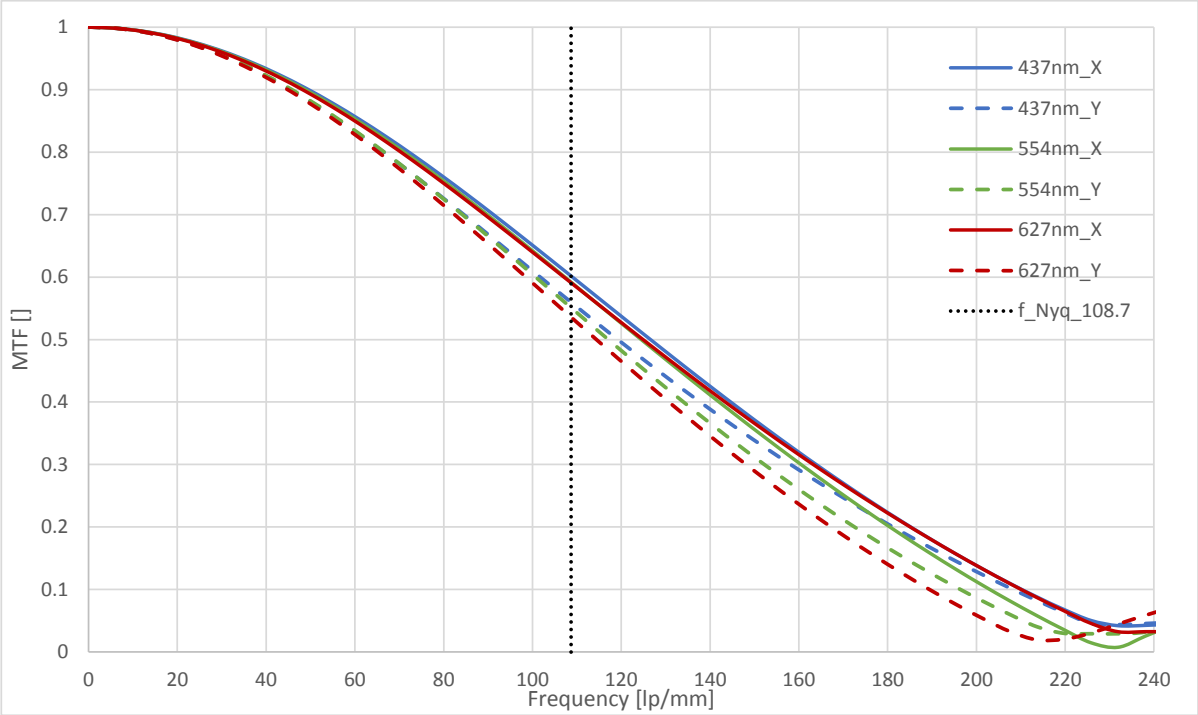
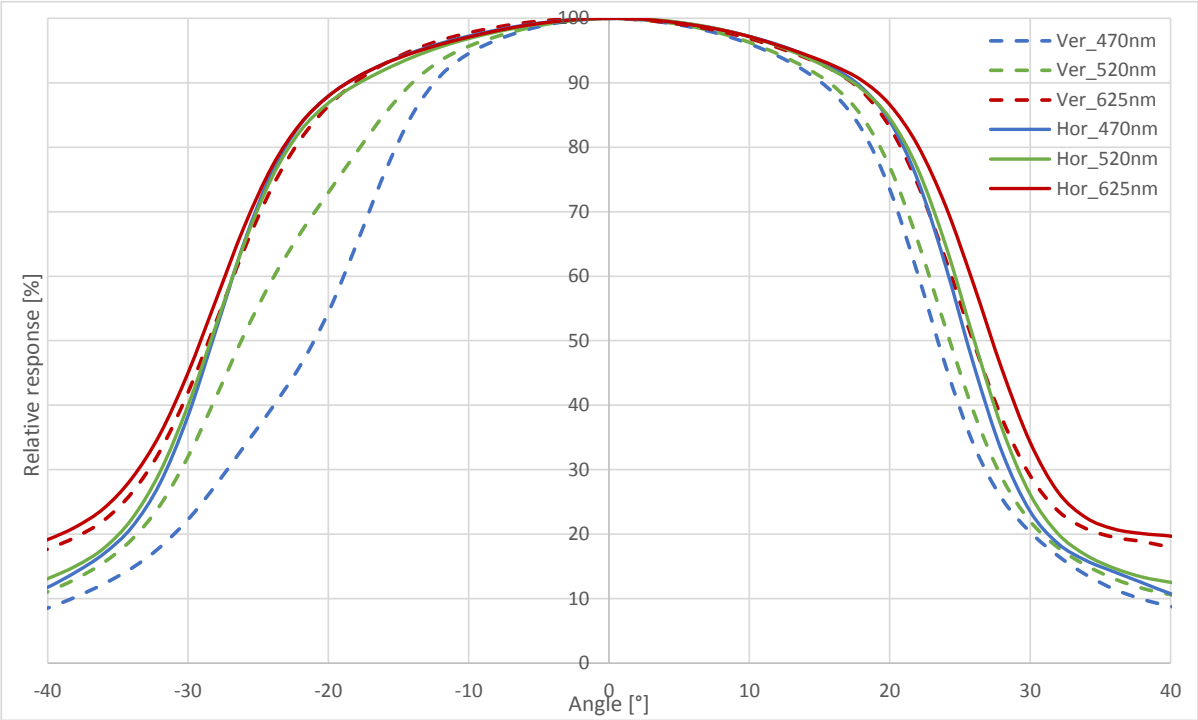


Figure 13 :
Angular Response



7 Functional Description

7.1 Sensor Architecture

Figure 2 shows a high-level representation of the chip architecture for the CMV50000 sensor. The drawing shows the active pixel array and the periphery around it that enables the control and readout of the pixels.

The core of the image sensor is made up from the pixel array, which is driven from two sides by 2 instances of the row logic and drivers. The pixel control signals are created globally by the global drivers and distributed to the sides of the sensor. The pixel data is read out row by row using a data path consisting of an analog front-end (AFE), analog-to-digital converter (ADC) and a digital data post-processing (DPP) block.

The converted data is sent, pixel by pixel, to a set of sub-LVDS drivers. An additional control (CTR) channel provides synchronization information about the data on the data channels, while a specific CLK channel can be used to sample the data channels.

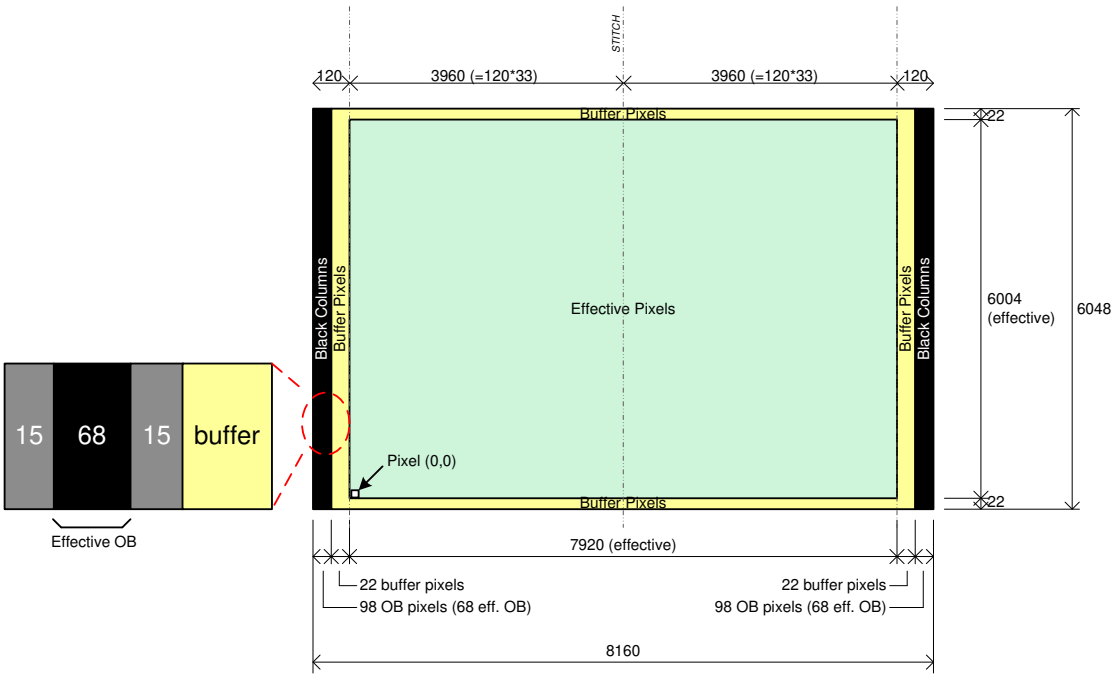
The data path is organized in kernels of 360 columns. Between kernels, control signals are repeated. There is one sub-LVDS driver for every kernel. At the left and right side of the pixel array, an additional kernel of OB pixels is added.

An on-chip sequencer controls the sensor operation and contains a register bank that is programmable over an SPI interface. There is also an on-chip temperature sensor available. A low-frequency CMOS input clock is transformed using an on-chip PLL to a set of high-frequency signals used in the sensor.

7.1.1 Pixel Array

Figure 14 shows the complete pixel array.

Figure 14:
Pixel Array



The pixel array can be split up in 3 parts: Optical black (OB) pixels (left and right side), buffer pixels (around effective array perimeter) and effective pixels. Only the 68 effective OB pixels are used for internal row clamping, which improves row noise and allows setting a pre-defined black level. The buffer pixels form a guard ring around the effective pixels. The buffer pixels are optically active, but are not guaranteed to meet the optical specifications. The 98 OB and 22 buffer pixels are read out via the sub-LVDS OB-L/R outputs.

The full resolution of the pixel array is 8160 × 6048 pixels. This results in an effective resolution of 7920 × 6004 pixels or 47.5Mpixels. The effective array is 36.4mm × 27.6mm which is slightly larger than the 35mm full frame optical format (= 36mm × 24mm; which would correspond to a window of 7826 × 5217).

Because of the large sensor area, a wafer process called mask stitching is done. The vertical stitch line is located exactly in the middle of the array. Therefor a small offset between the pixels left and right of the stitch line might be present.

Micro-lenses are placed on the pixels for improved quantum efficiency and fill factor.

7.1.2 Analog Front End

The analog front end consists of the PGA (programmable gain amplifier) and circuitry to prepare the signal for ADC conversion

7.1.3 ADC

The column ADC converts the analog pixel value to a 12-bit value.

7.1.4 DPP

The DPP blocks perform digital operations on the visible pixel data: digital offset, digital gain, row noise correction.

7.1.5 Sub-LVDS Outputs

The sensor has 22 sub-LVDS data channels to output the processed data. Each data channel outputs the data of 360 columns. Readout modes using less parallel channels at reduced framerate are supported as well.

7.1.6 Sequencer

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control clocks. This sequencer can be activated and programmed through the SPI interface.

- Among the different features that the sequencer has implemented are the following:
- SPI protocol and register banks management.
- Exposure and frame timing generation based on external inputs or internal settings.
- Dual exposure HDR mode.
- Y-windowing, subsampling and binning

7.1.7 SPI Interface

The SPI interface is used to load the sequencer registers with settings to configure the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The settings in the on-chip registers can also be read back for test and debug of the surrounding system.

7.1.8 Temperature Sensor

An on-chip thermal sensor is included. The temperature data is read out through the SPI interface.

7.1.9 PLL

Various clock frequencies are required internally to operate the sensor. These are derived from a single input frequency using an on-chip PLL. Through configuration over SPI, a range of input clock frequencies is supported.

The 3 main internal clocks are CLK_ADC, CLK_SER and CLK_PIX:

- CLK_ADC is the PLL output clock and is equal to the data rate (830MHz for 830Mbit/s).
- CLK_SER is 1:2 of CLK_ADC and equal to the sub-LVDS output clock.
- CLK_PIX is the pixel clock and has a ratio of 1:12 of CLK_ADC.

7.1.10 OTP Memory

A non-volatile, one time programmable memory is included on-chip. This is programmed with unique device ID and temperature sensor calibration data which the user can use.

7.2 Operating the Sensor

This section explains how to connect and power the sensor, as well as basic recipes of how to configure the sensor in a certain operation mode.

7.2.1 Power Supplies

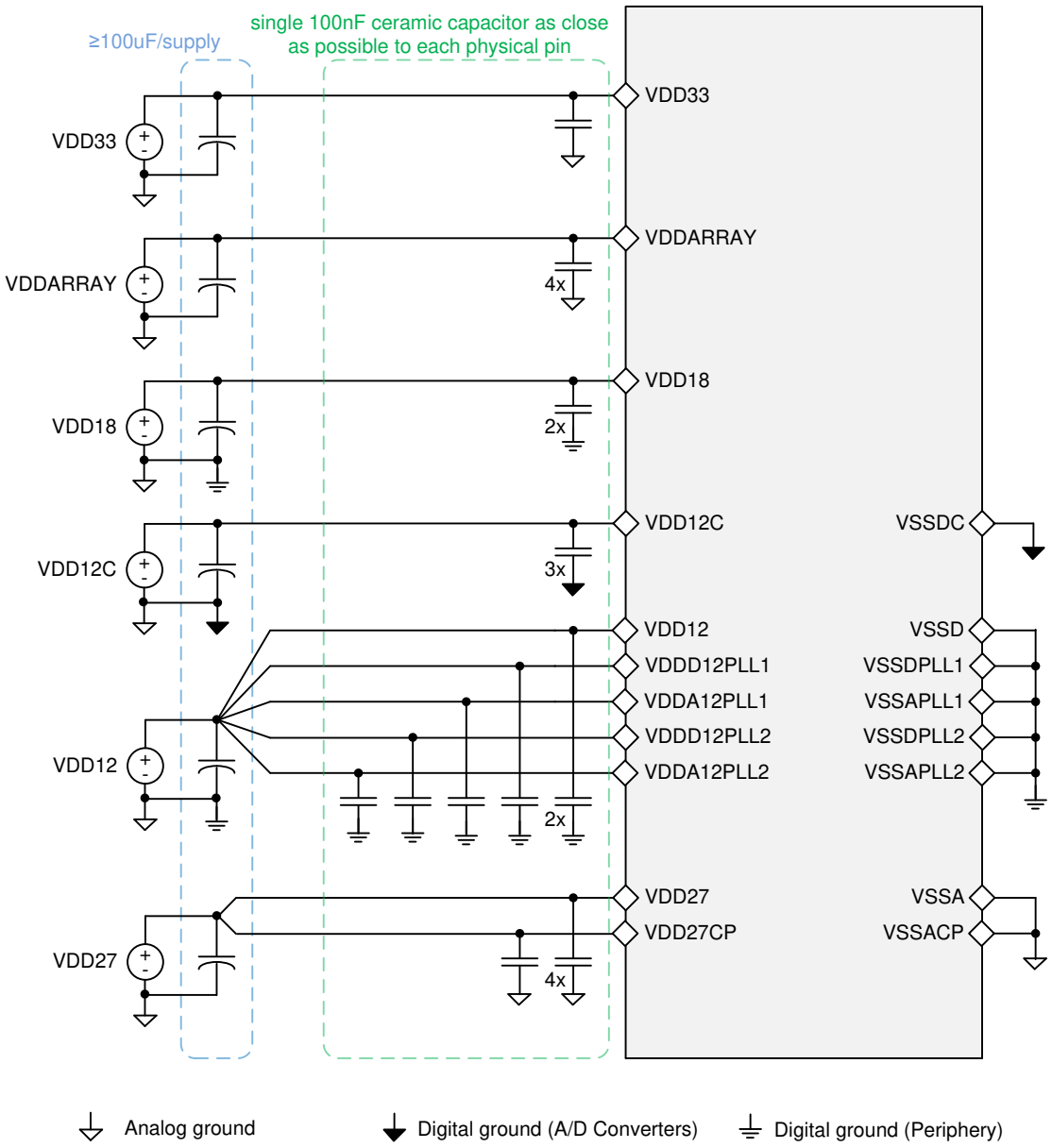
External Power Supplies

To power the sensor, six externally generated supplies are required as listed in Figure 6. A distinction is made between digital supplies (VDD12, VDD12C, VDD18) and analog supplies (VDD27, VDDARRAY, VDD33). Avoid using switching power supplies when possible, especially for the analog supplies.

Sufficient bulk (at the regulators) and local (at the sensor pins) decoupling is needed. In case of multiple pins for the same supply, local decoupling must be foreseen for each pin (e.g. four capacitors for the four VDDARRAY pins). Separate ground planes must be provided to minimize coupling.

For optimal noise performance, it is advised to keep the analog and digital ground nets separated and connect them together as close as possible to the external supply regulators.

Figure 15:
Power Supply Decoupling and Grounding Diagram



Biasing (on-chip regulators)

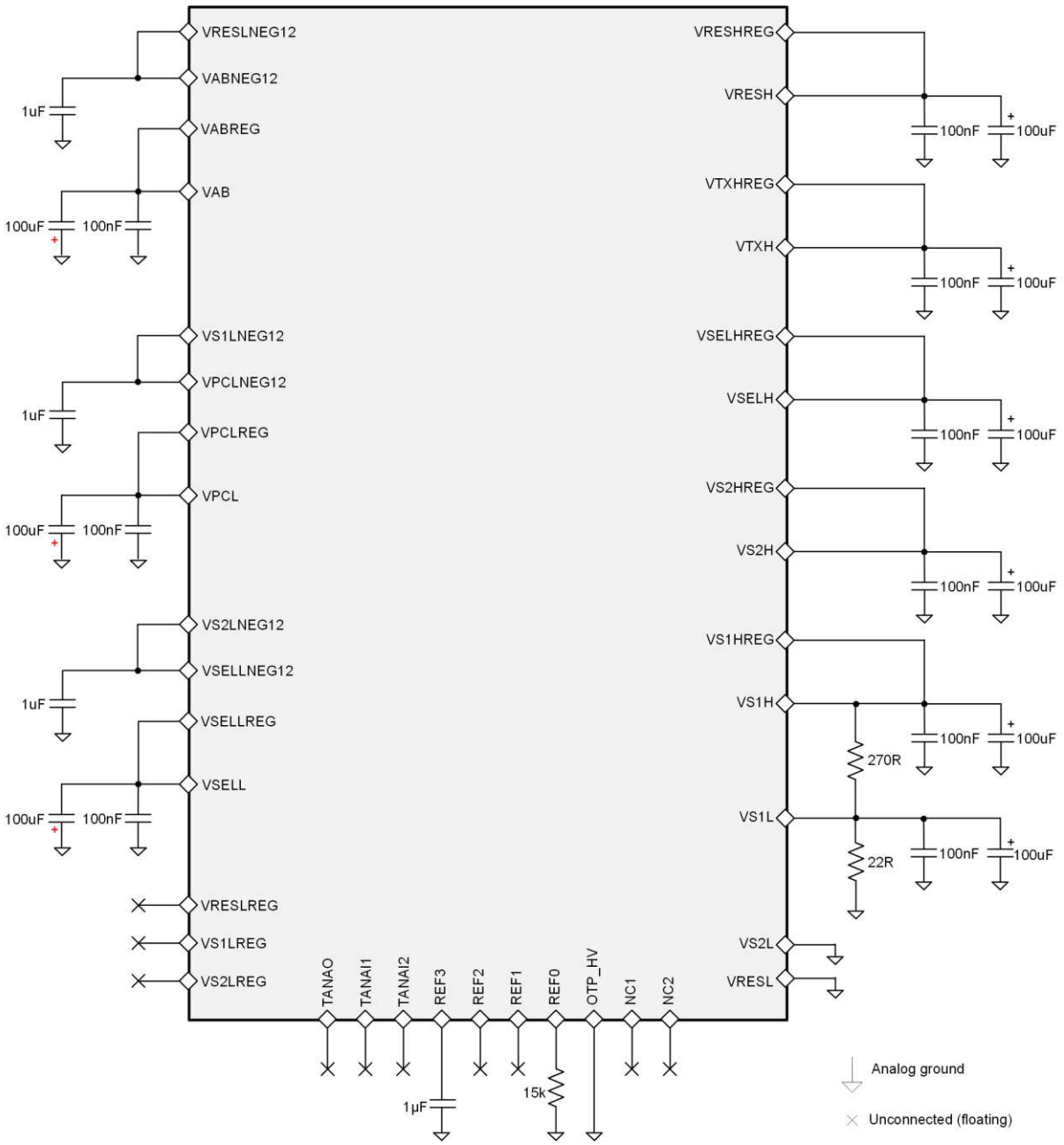
Operating the pixel array requires multiple different biasing supply levels. These supply levels can be generated using on-chip regulators. The chip contains 2 types of regulators, for positive supply levels and negative supply levels. The regulator output voltages are controlled using the SPI interface.

The supply regulators are internally not connected to the actual image sensor. Connections have to be made on PCB level (from a VxxREG pin to a Vyy pin). Also, each supply regulator requires to be

decoupled by a 100µF and 100nF capacitor. The negative supply regulators also require a decoupling of 1µF on a separate output pin (which will settle to -1.2V).

Next figure shows the positive and negative voltage regulator as well as the bias connections.

Figure 16:
On-Chip Regulators Connection Diagram



For the 100nF and 1µF capacitors, ceramic types can be used. Capacitances of 100µF can be electrolytic types (beware of the polarity on the negative supplies!). The maximal specified ESR and ESL of these 100µF capacitors are 0.1Ω and 10nH respectively.

A resistor network is necessary between VS1H and VS1L (±5% tolerance).

To obtain an accurate current bias reference in the sensor, an external bias resistor of 15kOhm (±5%) must be placed between REF0 and ground. No decoupling is required in parallel with this resistor. A maximal capacitance of 1nF on this node is allowed.

After power-up of the sensor, the recommended register settings will set the correct supply levels for these regulators (see section 7.4). Next table gives an overview of the available supply regulators, the connection to the bias pin and the required voltage on that pin.

Figure 17:
Bias Voltages

Regulator Pin	Type	Bias Pin	Voltage (V)
VRESHREG	Positive	VRESH	3.2
VTXHREG	Positive	VTXH	3.0
VS1HREG	Positive	VS1H	3.0
VS2HREG	Positive	VS2H	3.0
VSELHREG	Positive	VSELH	3.0
VABREG	Negative	VAB	-0.8
VPCLREG	Negative	VPCL	-0.3
VSELLREG	Negative	VSELL	-0.6
-	Positive	VS1L	0.25
-	Ground	VS2L	0
-	Ground	VRESL	0
VRESLREG	Negative	-	0
VS1LREG	Negative	-	0
VS2LREG	Negative	-	0
VRESLNEG12	Negative	VABNEG12	-1.2
VS1LNEG12	Negative	VPCLNEG12	-1.2
VS2LNEG12	Negative	VSELLNEG12	-1.2

7.2.2 Power-Up/Down Sequence

To avoid peak currents and guarantee a proper power-up/down of the sensor, following supply order and timing must be applied.