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RFM69HCW ISM TRANSCEIVER MODULE V1.1

GENERAL DESCRIPTION

TAL
ND

The RFM69HCW is a transceiver module capable of operation over a wide frequency range, including the 315,433,868 and 915MHz license-free ISM (Industry Scientific and Medical) frequency bands. All major RF communication parameters are programmable and most of them can be dynamically set. The RFM69HCW offers the unique advantage of programmable narrow-band and wide- band communication modes. The RFM69HCW is optimized for low power consumption while offering high RF output power and channelized operation. Compliance ETSI and FCC regulations.

In order to better use RFM69HCW modules, this specification also involves a large number of the parameters and functions of its core chip RF69H's,including those IC pins which are not leaded out. All of these can help customers gain a better understanding of the performance of RFM69HCW modules, and enhance the application skills.

KEY PRODUCT FEATURES

- +20 dBm - 100 mW Power Output Capability
- High Sensitivity: down to -120 dBm at 1.2 kbps
- High Selectivity: 16-tap FIR Channel Filter
- Bullet-proof front end: IIP3 = -18 dBm, IIP2 = +35 dBm,80 dB Blocking Immunity, no Image Frequency response
- Low current: Rx = 16 mA, 100nA register retention
- Programmable Pout: -18 to +20 dBm in 1dB steps
- Constant RF performance over voltage range of module
- FSK Bit rates up to 300 kb/s
- Fully integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK modulations
- Built-in Bit Synchronizer performing Clock Recovery
- Incoming Sync Word Recognition
- 115 dB+ Dynamic Range RSSI
- Automatic RF Sense with ultra-fast AFC
- Packet engine with CRC-16, AES-128, 66-byte FIFO
  Built-in temperature sensor
- Module Size:16X16mm

RFM69HCW

APPLICATIONS

- Automated Meter Reading
- Wireless Sensor Networks
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Wireless M-BUS

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Acronyms

BOM	Bill Of Materials
BR	Bit Rate
BW	Bandwidth
CCITT	Comité Consultatif International Téléphonique et Télégraphique - ITU
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
Fdev	Frequency Deviation
FIFO	First In First Out
FIR	Finite Impulse Response
FS	Frequency Synthesizer
FSK	Frequency Shift Keying
GUI	Graphical User Interface
IC	Integrated Circuit
ID	IDentificator
IF	Intermediate Frequency
IRQ	Interrupt ReQuest
ITU	International Telecommunication Union
LFSR	Linear Feedback Shift Register
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MSB	Most Significant Bit
NRZ	Non Return to Zero
OOK	On Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
POR	Power On Reset
RBW	Resolution BandWidth
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
Rx	Receiver
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
SR	Shift Register
Stby	Standby
Tx	Transmitter
uC	Microcontroller
VCO	Voltage Controlled Oscillator
XO	Crystal Oscillator
XOR	eXclusive OR

This product datasheet contains a detailed description of the RFM69HCW performance and functionality.

1. General Description

The RFM69HCW is a transceiver module ideally suited for today's high performance ISM band RF applications. It is intended for use as high-performance, low-cost FSK and OOK RF transceiver for robust frequency agile, half-duplex bi-directional RF links, and where stable and constant RF performance is required over the full operating range of the device down to 1.8V.

The RFM69HCW is intended for applications over a wide frequency range, including the 315MHz,433 MHz,868 MHz and 915MHz ISM bands. Coupled with a link budget in excess of 140 dB, the advanced system features of the RFM69HCW include a 66 byte TX/RX FIFO, configurable automatic packet handler, listen mode, temperature sensor and configurable DIOs which greatly enhance system flexibility whilst at the same time significantly reducing MCU requirements.

The RFM69HCW complies with both ETSI and FCC regulatory requirements and is available

1.1. Simplified Block Diagram

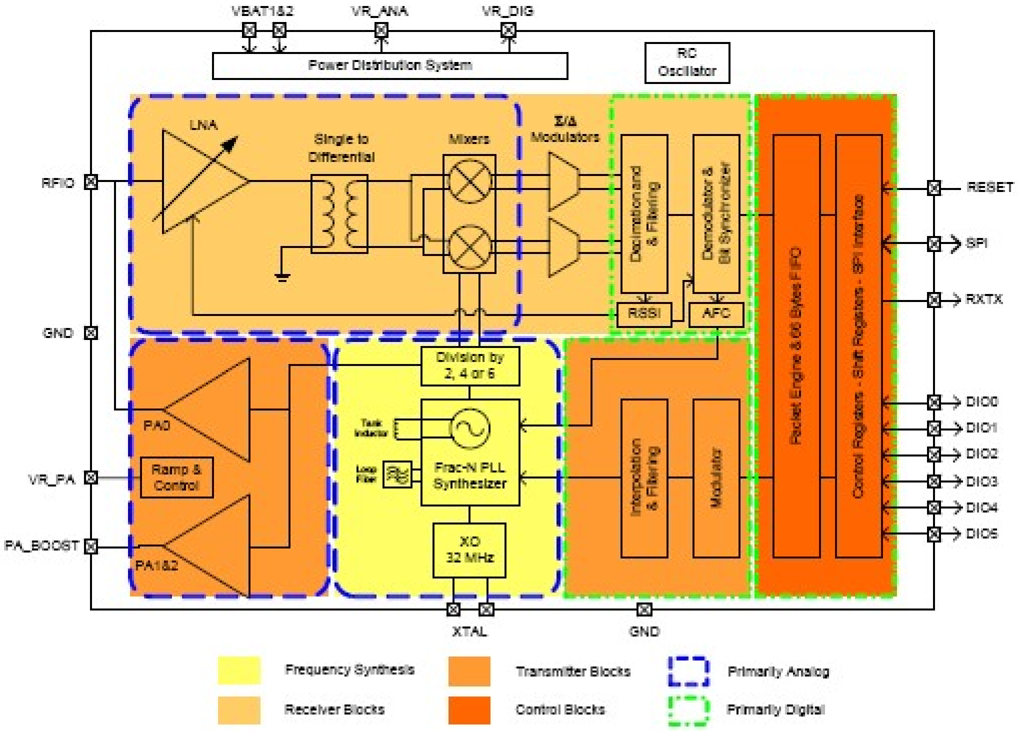

Figure 1. Block Diagram

1.2. Pin and Marking Diagram

The following diagram shows the pin arrangement of the top view.

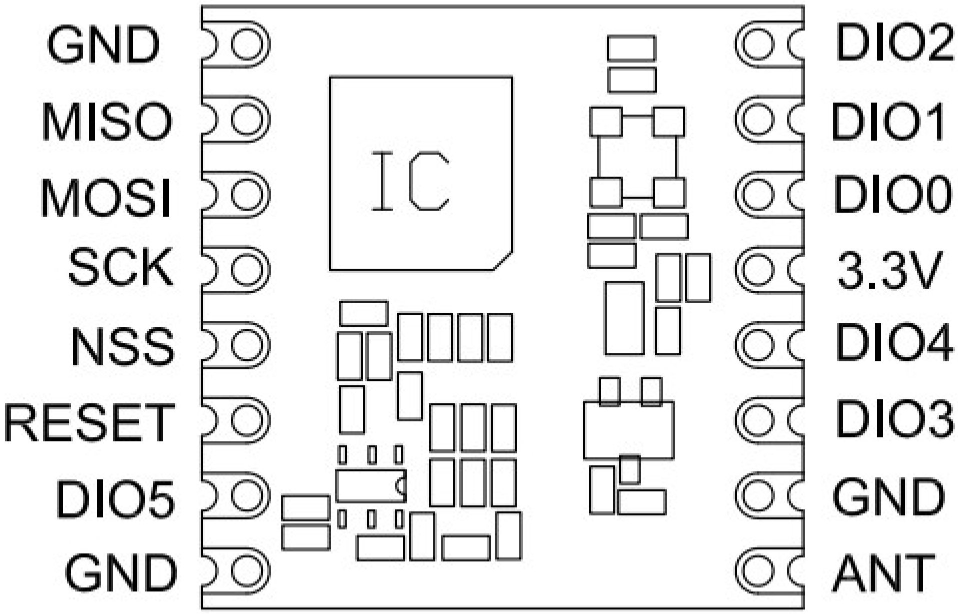

Figure 3. Marking Diagram

1.3. Pin Description

Table 1 RFM69HCW Pinouts

Number	Name	Type	Description
1	GND	-	Ground
2	MISO	I	SPI Data output
3	MOSI	O	SPI Data input
4	SCK	I	SPI Clock input
5	NSS	I	SPI Chip select input
6	RESET	I/O	Reset trigger input
7	DIO5	I/O	Digital I/O, software configured
8	GND	-	Ground
9	ANT	-	RF signal output/input.
10	GND	-	Ground
11	DIO3	I/O	Digital I/O, software configured
12	DIO4	I/O	Digital I/O, software configured
13	3.3V	-	Supply voltage
14	DIO0	I/O	Digital I/O, software configured
15	DIO1	I/O	Digital I/O, software configured
16	DIO2	I/O	Digital I/O, software configured

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Temperature	-55	+115	° C
Tj	Junction temperature	-	+125	° C
Pmr	RF Input Level	-	+6	dBm
DC_20dBm	Duty Cycle of transmission at +20dBm output	-	1	%
VSWR_20dBm	Maximum VSWR at antenna port	-	3:1	-

2.2. Operating Range

Table 3 Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply voltage(1.8V-2.4V 17dBm, 2.4V- 3.6V 20dBm)	1.8	3.6	V
Top	Operational temperature range	-40	+85	°C
Clop	Load capacitance on digital ports	-	25	pF
ML	RF Input Level	-	0	dBm

2.3 Module Specification

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VBAT1= VBAT2=VDD=3.3 V, temperature = 25 °C, F_{RF} = 915 MHz, Pout = +20dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified.

Note Unless otherwise specified, the performances in the other frequency bands are similar or better.

2.3.1. Power Consumption

Table 4 Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in Sleep mode		-	0.1	1	uA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	-	1.2	-	uA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	-	1.25	1.5	mA
IDDFS	Supply current in Synthesizer mode		-	9	-	mA
IDDR	Supply current in Receive mode		-	16	-	mA
IDDT	Supply current in Transmit mode with appropriate matching, stable across VDD range	RFOP = +20 dBm, on PA_BOOST RFOP = +17 dBm, on PA_BOOST RFOP = +13 dBm, on RFIO pin RFOP = +10 dBm, on RFIO pin RFOP = 0 dBm, on RFIO pin RFOP = -1 dBm, on RFIO pin	- - - - - -	130 95 45 33 20 16	- - - - - -	mA mA mA mA mA mA

2.3.2. Frequency Synthesis

Table 5 Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer Frequency Range	315MHz Module 433MHz Module 868MHz Module 915MHz Module	290 424 862 890		340 510 890 1020	MHz MHz MHz MHz
FXOSC	Crystal oscillator frequency	For All Module	-	32	-	MHz
TS_OSC	Crystal oscillator wake-up time		-	250	500	us
TS_FS	Frequency synthesizer wake-up time to PllLock signal	From Standby mode	-	80	150	us
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	- - - - - - -	20 20 50 50 80 80 80	- - - - - - -	us us us us us us us

FSTEP	Frequency synthesizer step	FSTEP = FXOSC/2^{19}	-	61.0	-	Hz
FRC	RC Oscillator frequency	After calibration	-	62.5	-	kHz
BRF	Bit rate, FSK	Programmable	1.2	-	300	kbps
BRO	Bit rate, OOK	Programmable	1.2	-	32.768	kbps
FDA	Frequency deviation, FSK	Programmable FDA + BRF/2 =< 500 kHz	0.6	-	300	kHz

2.3.3. Receiver

All receiver tests are performed with *RxBw* = 10 kHz (Single Side Bandwidth) as programmed in *RegRxBw*, receiving a PN15 sequence with a BER of 0.1% (Bit Synchronizer is enabled), unless otherwise specified. The LNA impedance is set to 200 Ohms, by setting bit *LnaZin* in *RegLna* to 1. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the nominal sensitivity level.

Table 6 Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	FSK sensitivity, highest LNA gain	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s	- - -	-118 -114 -105	- - -	dBm dBm dBm
		FDA = 5 kHz, BR = 1.2 kb/s *	-	-120	-	dBm
RFS_O	OOK sensitivity, highest LNA gain	BR = 4.8 kb/s	-	-112	-109	dBm
CCR	Co-Channel Rejection		-13	-10	-	dB
ACR	Adjacent Channel Rejection	Offset = +/- 25 kHz Offset = +/- 50 kHz	- 37	42 42	- -	dB dB
BI	Blocking Immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	66 71 79	- - -	dB dB dB
	Blocking Immunity Wanted signal at sensitivity +16dB	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	62 65 73	- - -	dB dB dB
AMR	AM Rejection , AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	66 71 79	- - -	dB dB dB
IIP2	2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Lowest LNA gain Highest LNA gain	- -	+75 +35	- -	dBm dBm

IIP3	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Lowest LNA gain Highest LNA gain	- -23	+20 -18	- -	dBm dBm
BW_SSB	Single Side channel filter BW	Programmable	2.6	-	500	kHz
IMR_OOK	Image rejection in OOK mode	Wanted signal level = -106 dBm	27	30	-	dB
TS_RE	Receiver wake-up time, from PLL locked state to *RxReady*	RxBw = 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	- -	1.7 96	- -	ms us
TS_RE_AGC	Receiver wake-up time, from PLL locked state, AGC enabled	RxBw = 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	-	3.0 163		ms us
TS_RE_AGC &AFC	Receiver wake-up time, from PLL lock state, AGC and AFC enabled	RxBw = 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s		4.8 265		ms us
TS_FEI	FEI sampling time	Receiver is ready	-	$4.T_{bit}$	-	-
TS_AFC	AFC Response Time	Receiver is ready	-	$4.T_{bit}$	-	-
TS_RSSI	RSSI Response Time	Receiver is ready	-	$2.T_{bit}$	-	-
DR_RSSI	RSSI Dynamic Range	AGC enabled Min Max	- -	-115 0	- -	dBm dBm

* *Set SensitivityBoost in RegTestLna to 0x2D to reduce the noise floor in the receiver*

2.3.4. Transmitter

Table 7 Transmitter Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RF_OP	RF output power in 50 ohms On RFIO pin	Programmable with 1dB steps Max Min	- -	+20 -18	- -	dBm dBm
RF_OPH	Max RF output power, on PA_BOOST pin	With external match to 50 ohms	-	+20	-	dBm
ΔRF_OP	RF output power stability	From VDD=2.4V to 3.6V	-	+/-0.3	-	dB
PHN	Transmitter Phase Noise	50 kHz Offset from carrier 868 / 915 MHz bands 434 / 315 MHz bands	- -	-95 -99	- -	dBc/ Hz
ACP	Transmitter adjacent channel power (measured at 25 kHz offset)	BT=0.5 . Measurement conditions as defined by EN 300 220-1 V2.1.1	-	-	-37	dBm
TS_TR	Transmitter wake up time, to the first rising edge of DCLK	Frequency Synthesizer enabled, *PaRamp* = 10 us, BR = 4.8 kb/s.	-	120	-	us

2.3.5. Digital Specification

Conditions: Temp = 25°C, VDD = 3.3V, unless otherwise specified.

Table 8 Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Digital input level high		0.8	-	-	VDD
V_{IL}	Digital input level low		-	-	0.2	VDD
V_{OH}	Digital output level high	Imax = 1 mA	0.9	-	-	VDD
V_{OL}	Digital output level low	Imax = -1 mA	-	-	0.1	VDD
F_{SCK}	SCK frequency		-	-	10	MHz
t_{ch}	SCK high time		50	-	-	ns
t_{cl}	SCK low time		50	-	-	ns
t_{rise}	SCK rise time		-	5	-	ns
t_{fall}	SCK fall time		-	5	-	ns
t_{setup}	MOSI setup time	from MOSI change to SCK rising edge	30	-	-	ns
t_{hold}	MOSI hold time	from SCK rising edge to MOSI change	60	-	-	ns
t_{nsetup}	NSS setup time	from NSS falling edge to SCK rising edge	30	-	-	ns
t_{nhold}	NSS hold time	from SCK falling edge to NSS rising edge, normal mode	30	-	-	ns
t_{nhigh}	NSS high time between SPI accesses		20	-	-	ns
T_DATA	DATA hold and setup time		250	-	-	ns

3. Module Description

This section describes in depth the architecture of the RFM69HCW low-power, highly integrated transceiver.

3.1. Power Supply Strategy

The RFM69HCW employs an advanced power supply scheme, which provides stable operating characteristics over the full temperature and voltage range of operation. This includes the full output power of +20dBm maintained from 2.4 to 3.6V.

The RFM69HCW can be powered from any low-noise voltage source via pins VBAT1 and VBAT2. Decoupling capacitors should be connected, as suggested in the reference design, on VR_PA, VR_DIG and VR_ANA pins to ensure a correct operation of the built-in voltage regulators.

3.2. Frequency Synthesis

The LO generation on the RFM69HCW is based on a state-of-the-art fractional-N PLL. The PLL is fully integrated with automatic calibration.

3.2.1. Reference Oscillator

The crystal oscillator is the main timing reference of the RFM69HCW. It is used as a reference for the frequency synthesizer and as a clock for the digital processing.

The XO startup time, TS_OSC, depends on the actual XTAL being connected on pins XTA and XTB. When using the built-in sequencer, the RFM69HCW optimizes the startup time and automatically triggers the PLL when the XO signal is stable. To manually control the startup time, the user should either wait for TS_OSC max, or monitor the signal CLKOUT which will only be made available on the output buffer when a stable XO oscillation is achieved.

3.2.2. CLKOUT Output

The reference frequency, or a fraction of it, can be provided on DIO5 by modifying bits *ClkOut* in *RegDioMapping2*. Two typical applications of the CLKOUT output include:

- To provide a clock output for a companion processor, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode except Sleep mode and is automatically enabled at power on reset.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note to minimize the current consumption of the RFM69HCW, please ensure that the CLKOUT signal is disabled when not required.

3.2.3. PLL Architecture

The frequency synthesizer generating the LO frequency for both the receiver and the transmitter is a fractional-N sigma-delta PLL. The PLL incorporates a third order loop capable of fast auto-calibration, and it has a fast switching-time. The VCO and the loop filter are both fully integrated, removing the need for an external tight-tolerance, high-Q inductor in the VCO tank circuit.

3.2.3.1. VCO

The VCO runs at 2, 4 or 6 times the RF frequency (respectively in the 915, 434 and 315 MHz bands) to reduce any LO leakage in receiver mode, to improve the quadrature precision of the receiver, and to reduce the pulling effects on the VCO during transmission.

The VCO calibration is fully automated. A coarse adjustment is carried out at power on reset, and a fine tuning is performed each time the RFM69HCW PLL is activated. Automatic calibration times are fully transparent to the end-user, as their processing time is included in the *TS_TE* and *TS_RE* specifications.

3.2.3.2. PLL Bandwidth

The bandwidth of the RFM69HCW Fractional-N PLL is wide enough to allow for:

- High speed FSK modulation, up to 300 kb/s, inside the PLL bandwidth
- Very fast PLL lock times, enabling both short startup and fast hop times required for frequency agile applications

3.2.3.3. Carrier Frequency and Resolution

The RFM69HCW PLL embeds a 19-bit sigma-delta modulator and its frequency resolution, constant over the whole frequency range, and is given by:

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

The carrier frequency is programmed through *RegFrf*, split across addresses 0x07 to 0x09:

$$F_{RF} = F_{STEP} \cdot Frf(23,0)$$

Note The Frf setting is split across 3 bytes. A change in the center frequency will only be taken into account when the least significant byte FrfLsb in RegFrfLsb is written. This allows for more complex modulation schemes such as m-ary FSK, where frequency modulation is achieved by changing the programmed RF frequency.

3.2.4. Lock Time

PLL lock time *TS_FS* is a function of a number of technical factors, such as synthesized frequency, frequency step, etc. When using the built-in sequencer, the RFM69HCW optimizes the startup time and automatically starts the receiver or the transmitter when the PLL has locked. To manually control the startup time, the user should either wait for *TS_FS* max given in the specification, or monitor the signal PLL lock detect indicator, which is set when the PLL has is within its locking range.

When performing an AFC, which usually corrects very small frequency errors, the PLL response time is approximately:

$$T_{PLLAFC} = \frac{5}{PLLBW}$$

In a frequency hopping scheme, the timings *TS_HOP* given in the table of specifications give an order of magnitude for the expected lock times.

3.2.5. Lock Detect Indicator

A lock indication signal can be made available on some of the DIO pins, and is toggled high when the PLL reaches its locking range. Please refer to Table 21 and Table 22 to map this interrupt to the desired pins.

Note *The lock detect block may indicate an unlock condition (signal toggling low) when the transmitter is FSK modulated with large frequency deviation settings.*

3.3. Transmitter Description

The transmitter of RFM69HCW comprises the frequency synthesizer, modulator and power amplifier blocks.

3.3.1. Architecture Description

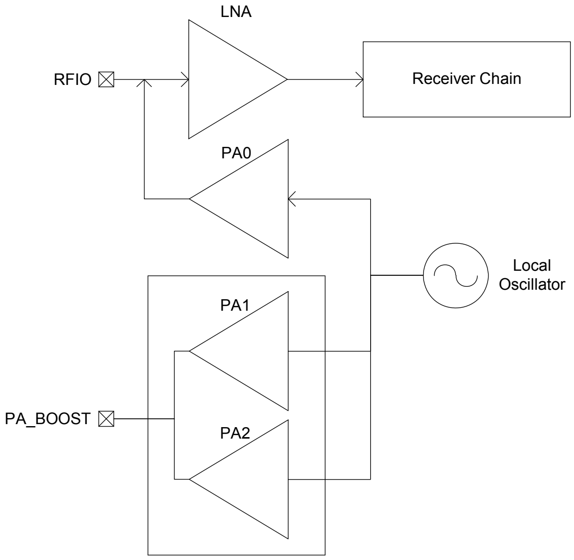

Figure 4. Transmitter Block Diagram

3.3.2. Bit Rate Setting

When using the RFM69HCW in Continuous mode, the data stream to be transmitted can be input directly to the modulator via pin DIO2/DATA in an asynchronous manner, unless Gaussian filtering is used, in which case the DCLK signal on pin DIO1/DCLK is used to synchronize the data stream. See section 3.3.5 for details on the Gaussian filter.

In Packet mode or in Continuous mode with Gaussian filtering enabled (refer to section 5.5 for details), the Bit Rate (BR) is controlled by bits *BitRate* in *RegBitrate*:

$$BR = \frac{F_{XOSC}}{BitRate}$$

Amongst others, the following Bit Rates are accessible:

Table 9 Bit Rate Examples

Type	BitRate (15:8)	BitRate (7:0)	(G)FSK (G)MSK	OOK	Actual BR (b/s)
Classical modem baud rates (multiples of 1.2 kbps)	0x68	0x2B	1.2 kbps	1.2 kbps	1200.015
	0x34	0x15	2.4 kbps	2.4 kbps	2400.060
	0x1A	0x0B	4.8 kbps	4.8 kbps	4799.760
	0x0D	0x05	9.6 kbps	9.6 kbps	9600.960
	0x06	0x83	19.2 kbps	19.2 kbps	19196.16
	0x03	0x41	38.4 kbps		38415.36
	0x01	0xA1	76.8 kbps		76738.60
	0x00	0xD0	153.6 kbps		153846.1
Classical modem baud rates (multiples of 0.9 kbps)	0x02	0x2C	57.6 kbps		57553.95
	0x01	0x16	115.2 kbps		115107.9
Round bit rates (multiples of 12.5, 25 and 50 kbps)	0x0A	0x00	12.5 kbps	12.5 kbps	12500.00
	0x05	0x00	25 kbps	25 kbps	25000.00
	0x02	0x80	50 kbps		50000.00
	0x01	0x40	100 kbps		100000.0
	0x00	0xD5	150 kbps		150234.7
	0x00	0xA0	200 kbps		200000.0
	0x00	0x80	250 kbps		250000.0
	0x00	0x6B	300 kbps		299065.4
Watch Xtal frequency	0x03	0xD1	32.768 kbps	32.768 kbps	32753.32

3.3.3. FSK Modulation

FSK modulation is performed inside the PLL bandwidth, by changing the fractional divider ratio in the feedback loop of the PLL. The large resolution of the sigma-delta modulator, allows for very narrow frequency deviation. The frequency deviation FDEV is given by:

$$F_{DEV} = F_{STEP} \times Fdev(13,0)$$

To ensure a proper modulation, the following limit applies:

$$F_{DEV} + \frac{BR}{2} \le 500kHz$$

Note no constraint applies to the modulation index of the transmitter, but the frequency deviation must exceed 600 Hz.

3.3.4. OOK Modulation

OOK modulation is applied by switching on and off the Power Amplifier. Digital control and smoothing are available to improve the transient power response of the OOK transmitter.

3.3.5. Modulation Shaping

Modulation shaping can be applied in both OOK and FSK modulation modes, to improve the narrowband response of the transmitter. Both shaping features are controlled with *PaRamp* bits in *RegPaRamp*.

- In FSK mode, a Gaussian filter with BT = 0.3, 0.5 or 1 is used to filter the modulation stream, at the input of the sigma-delta modulator. If the Gaussian filter is enabled when the RFM69HCW is in Continuous mode, DCLK signal on pin DIO1/DCLK will trigger an interrupt on the uC each time a new bit has to be transmitted. Please refer to section 5.4.2 for details.
- When OOK modulation is used, the PA bias voltages are ramped up and down smoothly when the PA is turned on and off, to reduce spectral splatter.

Note the transmitter must be restarted if the PaRamp setting is changed, in order to recalibrate the built-in filter.

3.3.6. Power Amplifiers

- ◆ A higher power mode, when PA1 and PA2 are combined, providing up to +20 dBm to a matched load.

When PA1 and PA2 are combined to deliver +20 dBm to the antenna, a specific impedance matching / harmonic filtering design is required to ensure impedance transformation and regulatory compliance.

All PA settings are controlled by *RegPaLevel*, and the truth table of settings is given in Table 10.

Table 10 Power Amplifier Mode Selection Truth Table

Pa0On	*Pa1On*	*Pa2On*	Mode	Power Range	Pout Formula
1	0	0	PA0 output on pin RFIO	-18 to +13 dBm	-18 dBm + *OutputPower*
0	1	0	PA1 enabled on pin PA_BOOST	-2 to +13 dBm	-18 dBm + *OutputPower*
0	1	1	PA1 and PA2 combined on pin PA_BOOST	+2 to +17 dBm	-14 dBm + *OutputPower*
0	1	1	PA1+PA2 on PA_BOOST with high output power +20dBm settings (see 3.3.7)	+5 to +20 dBm	-11 dBm + *OutputPower*
Other combinations			Reserved		

Notes - To ensure correct operation at the highest power levels, please make sure to adjust the Over Current Protection Limit accordingly in RegOcp, except above +18dBm where it must be disabled

- If PA_BOOST pin is not used (+20dBm applications and less), the pin can be left floating.

3.3.7. High Power Settings

The RFM69HCW has a high power +20 dBm capability on PA_BOOST pin, with the following settings:

Table 11 High Power Settings

Register	***Address***	***Value for High Power***	***Value for Rx or PA0 use***	**Description**
RegOcp	0x13	0x0F	0x1x	OCP control
RegTestPa1	0x5A	0x5D	0x55	High power PA control
RegTestPa2	0x5C	0x7C	0x70	High power PA control

Note High Power settings MUST be turned off when using PA0, and in Receive mode

The Duty Cycle of transmission at +20dBm is limited to 1%, with a maximum VSWR of 3:1 at antenna port, over the standard operating range [-40;+85°C].

3.3.8. Output Power Summary

The curves below summarize the possible PA options on the RFM69HCW:

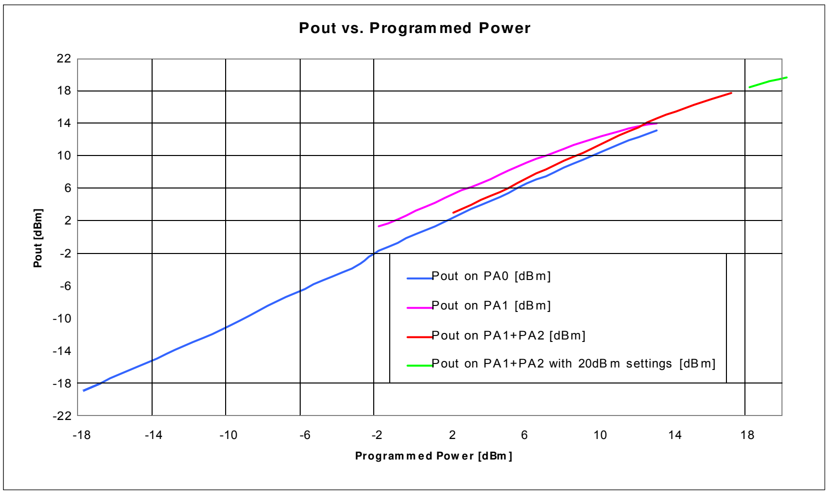

Figure 5. Output Power Curves

3.3.9. Over Current Protection

An over current protection block is built-in the module. It helps preventing surge currents required when the transmitter is used at its highest power levels, thus protecting the battery that may power the application. The current clamping value is controlled by *OcpTrim* bits in *RegOcp*, and is calculated with the following formula:

$$Imax = 45 + 5 - OcpTrim \quad mA$$

Note Imax sets a limit on the current drain of the Power Amplifier only, hence the maximum current drain of the RFM69HCW is equal to Imax + I_{FS}

3.4. Receiver Description

The RFM69HCW features a digital receiver with the analog to digital conversion process being performed directly following the LNA-Mixers block. The zero-IF receiver is able to handle (G)FSK and (G)MSK modulation. ASK and OOK modulation is, however, demodulated by a low-IF architecture. All the filtering, demodulation, gain control, synchronization and packet handling is performed digitally, which allows a very wide range of bit rates and frequency deviations to be selected. The receiver is also capable of automatic gain calibration in order to improve precision on RSSI measurements.

3.4.1. Block Diagram

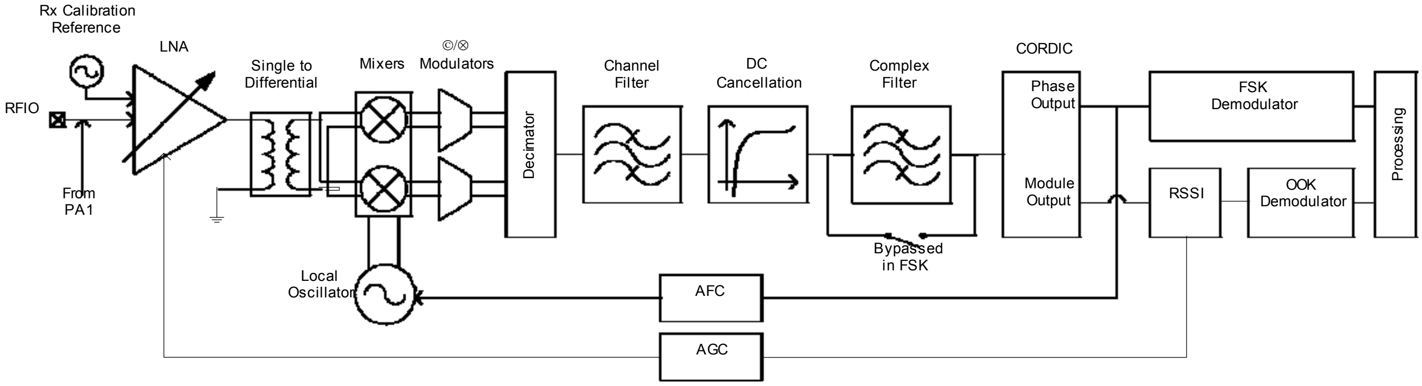

Figure 6. Receiver Block Diagram

The following sections give a brief description of each of the receiver blocks.

3.4.2. LNA - Single to Differential Buffer

The LNA uses a common-gate topology, which allows for a flat characteristic over the whole frequency range. It is designed to have an input impedance of 50 Ohms or 200 Ohms (as selected with bit *LnaZin* in *RegLna)*, and the parasitic capacitance at the LNA input port is cancelled with the external RF choke. A single to differential buffer is implemented to improve the second order linearity of the receiver.

The LNA gain, including the single-to-differential buffer, is programmable over a 48 dB dynamic range, and control is either manual or automatic with the embedded AGC function.

Note In the specific case where the LNA gain is manually set by the user, the receiver will not be able to properly handle FSK signals with a modulation index smaller than 2 at an input power greater than the 1dB compression point, tabulated in section 3.4.3.

Table 12 LNA Gain Settings

LnaGainSelect	**LNA Gain**	**Gain Setting**
000	Any of the below, set by the AGC loop	-
001	Max gain	G1
010	Max gain - 6 dB	G2
011	Max gain - 12 dB	G3
100	Max gain - 24 dB	G4
101	Max gain - 36 dB	G5
110	Max gain - 48 dB	G6
111	Reserved	-

3.4.3. Automatic Gain Control

By default (*LnaGainSelect = 000*), the LNA gain is controlled by a digital AGC loop in order to obtain the optimal sensitivity/ linearity trade-off.

Regardless of the data transfer mode (Packet or Continuous), the following series of events takes place when the receiver is enabled:

- The receiver stays in WAIT mode, until *RssiValue* exceeds *RssiThreshold* for two consecutive samples. Its power consumption is the receiver power consumption.
- When this condition is satisfied, the receiver automatically selects the most suitable LNA gain, optimizing the sensitivity/linearity trade-off.
- The programmed LNA gain, read-accessible with *LnaCurrentGain* in *RegLna*, is carried on for the whole duration of the packet, until one of the following conditions is fulfilled:
- Packet mode: if *AutoRxRestartOn = 0,* the LNA gain will remain the same for the reception of the following packet. If *AutoRxRestartOn = 1*, after the controller has emptied the FIFO the receiver will re-enter the WAIT mode described above, after a delay of *InterPacketRxDelay*, allowing for the distant transmitter to ramp down, hence avoiding a false RSSI detection. In both cases (AutoRxRestartOn=0 or AutoRxRestartOn=1), the receiver can also re-enter the WAIT mode by setting *RestartRx* bit to 1. The user can decide to do so, to manually launch a new AGC procedure.
- Continuous mode: upon reception of valid data, the user can decide to either leave the receiver enabled with the same LNA gain, or to restart the procedure, by setting *RestartRx* bit to 1, resuming the WAIT mode of the receiver, described above.

Notes - the AGC procedure must be performed while receiving preamble in FSK mode

- in OOK mode, the AGC will give better results if performed while receiving a constant “1” sequence

The following figure illustrates the AGC behavior:

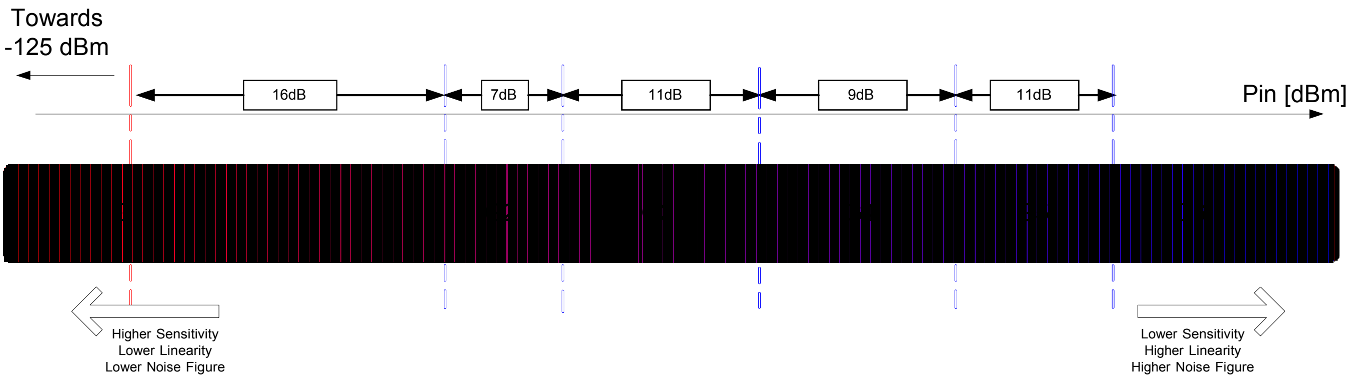

Figure 7. AGC Thresholds Settings

The following table summarizes the performance (typical figures) of the complete receiver:

Table 13 Receiver Performance Summary

Input Power Pin	Gain Setting	Receiver Performance (typ)			
		P_{-1dB} [dBm]	NF [dB]	IIP3 [dBm]	IIP2 [dBm]
Pin < AgcThresh1	G1	-37	7	-18	+35
AgcThresh1 < Pin < AgcThresh2	G2	-31	13	-15	+40
AgcThresh2 < Pin < AgcThresh3	G3	-26	18	-8	+48
AgcThresh3 < Pin < AgcThresh4	G4	-14	27	-1	+62
AgcThresh4 < Pin < AgcThresh5	G5	>-6	36	+13	+68
AgcThresh5 < Pin	G6	>0	44	+20	+75

3.4.3.1. RssiThreshold Setting

For correct operation of the AGC, *RssiThreshold* in *RegRssiThresh* must be set to the sensitivity of the receiver. The receiver will remain in WAIT mode until *RssiThreshold* is exceeded.

Note *When AFC is enabled and performed automatically at the receiver startup, the channel filter used by the receiver during the AFC and the AGC is RxBwAfc instead of the standard RxBw setting. This may impact the sensitivity of the receiver, and the setting of RssiThreshold accordingly*

3.4.3.2. AGC Reference

The AGC reference level is automatically computed in the RFM69HCW, according to:

AGC Reference [dBm] = -174 + NF + DemodSnr +10.log(2**RxBw***) + FadingMargin [dBm]**

With:

- *NF* = 7dB : LNA's Noise Figure at maximum gain
- *DemodSnr* = 8 dB : SNR needed by the demodulator
- *RxBw* : Single sideband channel filter bandwidth
- *FadingMargin = 5 dB* : Fading margin

3.4.4. Continuous-Time DAGC

In addition to the automatic gain control described in section 3.4.3, the RFM69HCW is capable of continuously adjusting its gain in the digital domain, after the analog to digital conversion has occured. This feature, named DAGC, is fully transparent to the end user. The digital gain adjustment is repeated every 2 bits, and has the following benefits:

- Fully transparent to the end user
- Improves the fading margin of the receiver during the reception of a packet, even if the gain of the LNA is frozen
- Improves the receiver robustness in fast fading signal conditions, by quickly adjusting the receiver gain (every 2 bits)
- Works in Continuous, Packet, and unlimited length Packet modes

The DAGC is enabled by setting *RegTestDagc* to 0x20 for low modulation index systems (i.e. when *AfcLowBetaOn*=1, refer to section 3.4.16), and 0x30 for other systems. It is recommended to always enable the DAGC.