Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

COM20019i 3.3V Rev. C

Cost Competitive ARCNET (ANSI 878.1) Controller with 2K x 8 On-Chip RAM

Highlights

- Data Rates up to 312.5 Kbps
- Programmable Reconfiguration Times
- 28-Pin PLCC and 48-Pin TQFP RoHS Compliant packages
- Ideal for Industrial/Factory/Building Automation and Transportation Applications
- Deterministic, (ANSI 878.1), Token Passing ARCNET Protocol
- Minimal Microcontroller and Media Interface Logic Required
- Flexible Interface For Use With All Microcontrollers or Microprocessors
- Automatically Detects Type of Microcontroller Interface
- 2Kx8 On-Chip Dual Port RAM
- Command Chaining for Packet Queuing
- Sequential Access to Internal RAM
- Software Programmable Node ID
- Eight, 256 Byte Pages Allow Four Pages TX and RX Plus Scratch-Pad Memory
- Next ID Readable
- Internal Clock Scaler for Adjusting Network Speed
- Operating Temperature Range of -40°C to +85°C
- 3.3V power supply with 5V tolerant I/O
- Self-Reconfiguration Protocol
- Supports up to 255 Nodes
- Supports Various Network Topologies (Star, Tree, Bus...)
- CMOS, Single +3.3V Supply
- Duplicate Node ID Detection
- Powerful Diagnostics
- Receive All Packets Mode
- Flexible Media Interface:
  - RS485 Differential Driver Interface For Cost Competitive, Low Power, High Reliability

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Table of Contents

1.0 GENERAL DESCRIPTION

Microchip's COM20019i 3V is a member of the family of Embedded ARCNET Controllers. The device is a general purpose communications controller for networking microcontrollers and intelligent peripherals in industrial and embedded control environments using an ARCNET protocol engine. The flexible microcontroller and media interfaces, eight-page message support, and extended temperature range of the COM20019i 3V make it the only true network controller optimized for use in industrial and embedded applications. Using an ARCNET protocol engine is the ideal solution for embedded control applications because it provides a deterministic token-passing protocol, a highly reliable and proven networking scheme, and a data rate of up to 312.5 Kbps when using the COM20019i 3V.

A token-passing protocol provides predictable response times because each network event occurs within a predetermined time interval, based upon the number of nodes on the network. The deterministic nature of ARCNET is essential in real time applications. The integration of the 2Kx8 RAM buffer on-chip, the Command Chaining feature, the maximum data rate, and the internal diagnostics make the COM20019i 3V the highest performance embedded communications device available. With only one COM20019i 3V and one microcontroller, a complete communications node may be implemented.

For more details on the ARCNET protocol engine and traditional dipulse signaling schemes, please refer to the ARCNET Local Area Network Standard, available from Microchip or the ARCNET Designer's Handbook, available from Datapoint Corporation.

For more detailed information on cabling options including RS485, transformer-coupled RS-485 and Fiber Optic interfaces, please refer to the following technical note which is available from Microchip: Technical Note 7-5 - Cabling Guidelines for the COM20020 ULANC.

2.0 PIN CONFIGURATION

FIGURE 2-1: COM20019I 3V 28-PIN PLCC PACKAGE

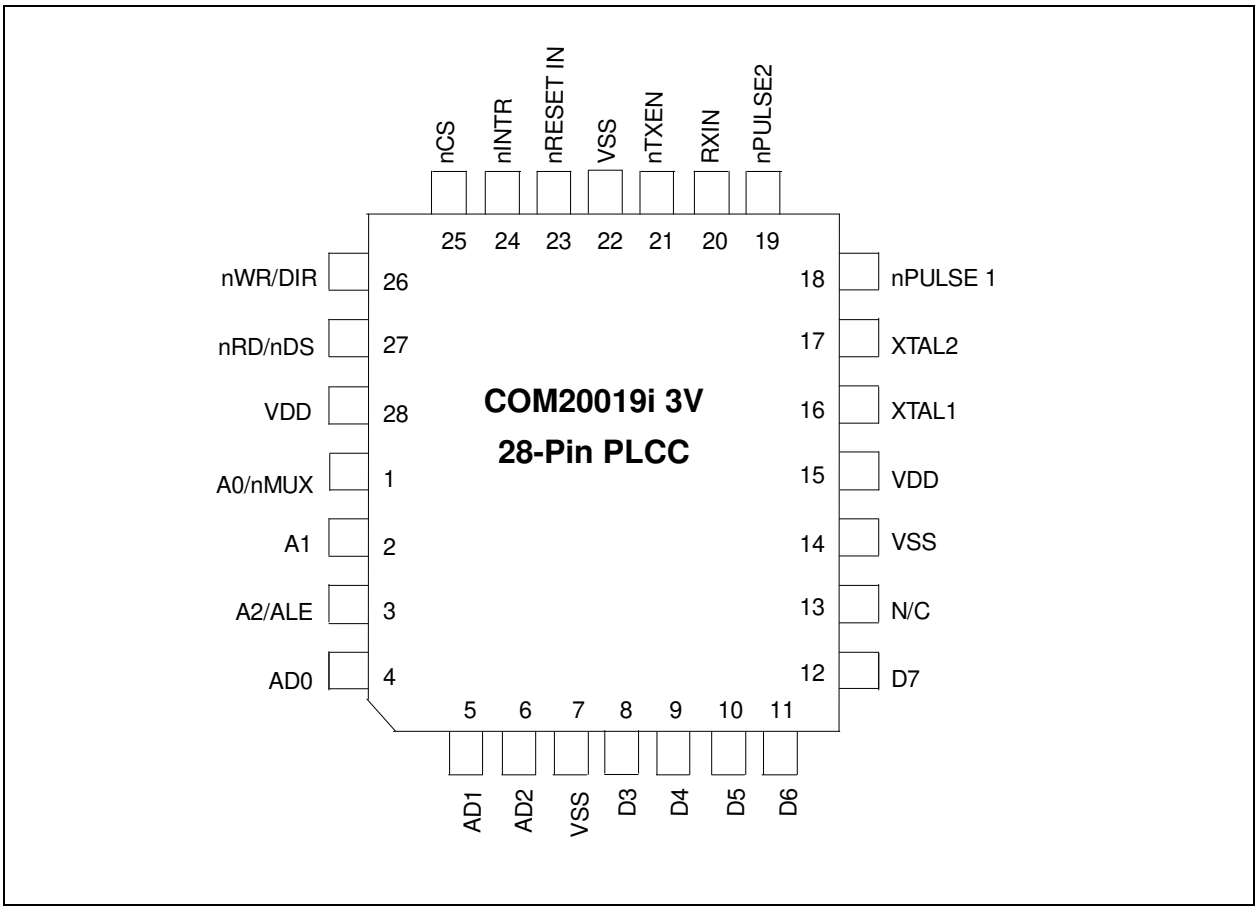
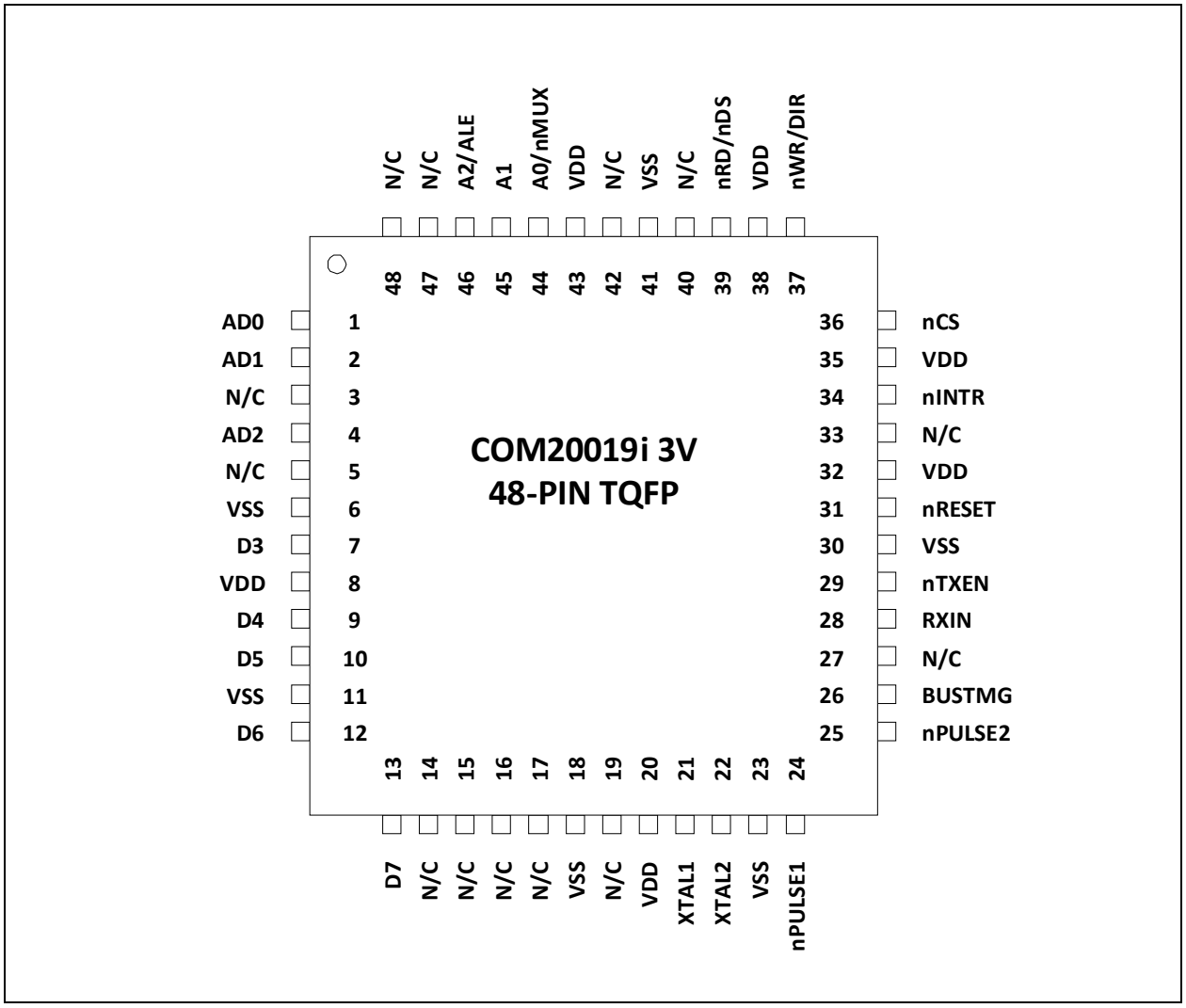


FIGURE 2-2: COM20019I 3V 48-PIN TQFP



Note: BUSTMG pin is only TQFP package.

3.0 DESCRIPTION OF PIN FUNCTIONS

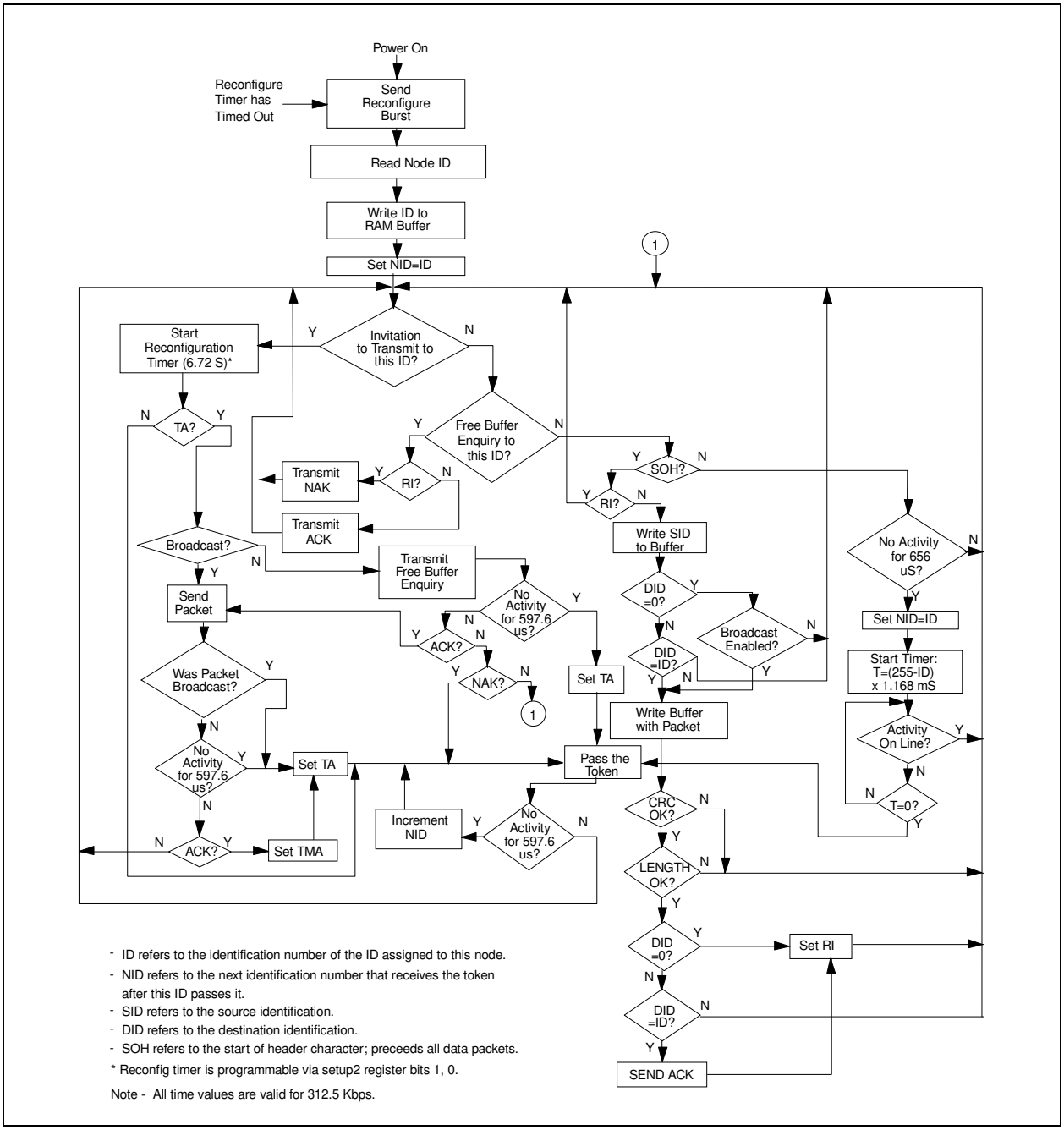
TABLE 3-1: COM20019I 3V PIN FUNCTIONS

Pin Number		Name	Symbol	I/O	Description
PLCC	**TQFP**	**MICROCONTROLLER INTERFACE**			
1, 2, 3	44, 45, 46	Address 0-2	A0/nMUX A1 A2/ALE	IN IN IN	On a non-multiplexed mode, A0-A2 are address input bits (A0 is the LSB). On a multiplexed address/data bus, nMUX tied Low, A1 is left open, and ALE is tied to the Address Latch Enable signal. A1 is connected to an internal pull-up resistor.
4, 5, 6, 8, 9, 10, 11, 12	1, 2, 4, 7, 9, 10, 12, 13	Data 0-7	AD0-AD2, D3-D7	I/O	On a non-multiplexed bus, these signals are used as the lower byte data bus lines. On a multiplexed address/data bus, AD0-AD2 act as the address lines (latched by ALE) and as the low data lines. D3-D7 are always used for data only. These signals are connected to internal pull-up resistors.
26	37	nWrite/ Direction	nWR/DIR	IN	nWR is for 80xx CPU, nWR is Write signal input. Active Low. DIR is for 68xx CPU, DIR is Bus Direction signal input. (Low: Write, High: Read.)
27	39	nRead/ nData Strobe	nRD/nDS	IN	nRD is for 80xx CPU, nRD is Read signal input. Active Low. nDS is for 68xx CPU, nDS is Data Strobe signal input. Active Low.
23	31	nReset In	nRESET	IN	Hardware reset signal. Active Low.
24	34	nInterrupt	nINTR	OUT	Interrupt signal output. Active Low.
25	36	nChip Select	nCS	IN	Chip Select input. Active Low.
-	26	Read/Write Bus Timing Select	BUSTMG	IN	Read and Write Bus Access Timing mode selecting signal. Status of this signal effects CPU Timing. L: High speed timing mode (only for non-multiplexed bus) H: Normal timing mode This signal is connected to internal pull-up registers. **Note:** BUSTMG pin does not exist in PLCC package.

TABLE 3-1: COM20019I 3V PIN FUNCTIONS (CONTINUED)

Pin Number		Name	Symbol	I/O	Description
PLCC	TQFP	TRANSMISSION MEDIA INTERFACE			
18 19	24 25	nPulse 1 nPulse 2	nPULSE1 nPULSE2	OUT I/O	In Normal Mode, these active low signals carry the transmit data information, encoded in pulse format as DIPULSE waveform. In Backplane Mode, the nPULSE1 signal driver is programmable (push/pull or open-drain), while the nPULSE2 signal provides a clock with frequency of doubled data rate. nPULSE1 is connected to a weak internal pull-up resistor on the open/drain driver in backplane mode.
20	28	Receive In	RXIN	IN	This signal carries the receive data information from the line transceiver.
21	29	nTransmit Enable	nTXEN	OUT	Transmission Enable signal. Active polarity is programmable through the nPULSE2 pin. nPULSE2 floating before power-up; nTXEN active low nPULSE2 grounded before power-up; nTXEN active high (this option is only available in Back Plane mode)
16 17	21 22	Crystal Oscillator	XTAL1 XTAL2	IN OUT	An external crystal should be connected to these pins. Oscillation frequency range is from 10 MHz to 20 MHz. If an external TTL clock is used instead, it must be connected to XTAL1 with a 390ohm pull-up resistor, and XTAL2 should be left floating.
15, 28	8, 20, 32, 43	Power Supply	VDD	PWR	+3.3 Volt power supply pins.
7, 14, 22	6, 11, 18, 23, 30, 41	Ground	VSS	PWR	Ground pins.
13	3, 5, 14-17, 19, 27, 33, 35, 38, 40, 42, 47, 48	N/C	N/C		Non-connection

FIGURE 3-1: COM20019I 3V OPERATION



- ID refers to the identification number of the ID assigned to this node.
- NID refers to the next identification number that receives the token after this ID passes it.
- SID refers to the source identification.
- DID refers to the destination identification.
- SOH refers to the start of header character; preceeds all data packets.

* Reconfig timer is programmable via setup2 register bits 1, 0.

Note - All time values are valid for 312.5 Kbps.

4.0 PROTOCOL DESCRIPTION

4.1 Network Protocol

Communication on the network is based on a token passing protocol. Establishment of the network configuration and management of the network protocol are handled entirely by the COM20019i 3V's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the COM20019i 3V's internal RAM buffer, and issuing a command to enable the transmitter. When the COM20019i 3V next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16-bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative ACKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node verifies the packet. If the packet is received successfully,

the receiving node transmits an ACKnowledge message (or nothing if it is not received successfully) allowing the transmitter to set the appropriate status bits to indicate successful or unsuccessful delivery of the packet. An interrupt mask permits the COM20019i 3V to generate an interrupt to the processor when selected status bits become true. FIGURE 3-1: COM20019i 3V Operation on page 9 is a flow chart illustrating the internal operation of the COM20019i 3V connected to a 20 MHz crystal oscillator.

4.2 Data Rates

The COM20019i 3V is capable of supporting data rates from 156.25 Kbps to 312.5 Kbps. The following protocol description assumes a 312.5 Kbps data rate. For slower data rates, an internal clock divider scales down the clock frequency. Thus all timeout values are scaled as shown in the following table:

Example: IDLE LINE Timeout @ 312.5 Kbps = 656 μs. IDLE LINE Timeout for 156.2 Kbps is 656 μs * 2 = 1.3 ms

Internal Clock Frequency	Clock Prescaler	Data Rate	Timeout Scaling Factor (Multiply By)
20 MHz	Div. by 64 Div. by 128	312.5 Kbps 156.25 Kbps	1 2

4.3 Network Reconfiguration

A significant advantage of the COM20019i 3V is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated, a NETWORK RECONFIGURATION is performed. When a new COM20019i 3V is turned on (creating a new active node on the network), or if the COM20019i 3V has not received an INVITATION TO TRANSMIT for 6.72S, or if a software reset occurs, the COM20019i 3V causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line.

When any COM20019i 3V senses an idle line for greater than 656μS, which occurs only when the token Is lost, each COM20019i 3V starts an internal timeout equal to 1.168mS times the quantity 255 minus its own ID. The COM20019i 3V starts network reconfiguration by sending an invitation to transmit first to itself and then to all other nodes by decrementing the destination Node ID. If the timeout expires with no line activity, the COM20019i 3V starts sending INVITATION TO TRANSMIT with the Destination ID (DID) equal to the currently stored NID. Within a given network, only one COM20019i 3V will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM20019i 3V waits for activity on the line. If there is no activity for 597.6uS, the COM20019i 3V increments the NID value and transmits another INVITATION TO TRANSMIT using the NID equal to the DID. If activity appears before the 597.6?S timeout expires, the COM20019i 3V releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT are sent to all NIDs (1-255).

Each COM20019i 3V on the network will finally have saved a NID value equal to the ID of the COM20019i 3V that it released control to. At this point, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT being sent to ID's not on the network, until the next NETWORK RECONFIGURATION occurs. When a node is powered off, the previous node attempts to pass the token to it by issuing an INVITATION TO TRANSMIT. Since this node does not respond, the previous node times out and transmits another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The NETWORK RECONFIGURATION time depends on the number of nodes in the network, the propagation delay between nodes, and the highest ID number on the network, but is typically within the range of 192 to 488 mS.

4.4 Broadcast Messages

Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the DID equal to zero. Figure 4 illustrates the position of each byte in the packet with the DID residing at address 0X01 or 1 Hex of the current page selected in the "Enable Transmit from Page fnn" command. Each individual node has the ability to ignore broadcast messages by setting the most significant bit of the "Enable Receive to Page fnn" command to a logic "0".

4.5 Extended Timeout Function

There are three timeouts associated with the COM20019i 3V operation. The values of these timeouts are controlled by bits 3 and 4 of the Configuration Register and bit 5 of the Setup 1 Register.

4.5.1 RESPONSE TIME

The Response Time determines the maximum propagation delay allowed between any two nodes, and should be chosen to be larger than the round trip propagation delay between the two furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM20019i 3V to start sending a message in response to a received message) which is approximately 101.6 μS. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 248 μS translates to a distance of about 32 miles. The flow chart in FIGURE 3-1: COM20019i 3V Operation on page 9 uses a value of 597.6 μS (248 + 248 + 101.6) to determine if any node will respond.

4.5.2 IDLE TIME

The Idle Time is associated with a NETWORK RECONFIGURATION. Figure 3-1 illustrates that during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. All other nodes on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 656 μS. This 656 μS is equal to the Response Time of 597.6 μS plus the time it takes the COM20019i 3V to start retransmitting another message (usually another INVITATION TO TRANSMIT).

4.5.3 RECONFIGURATION TIME

If any node does not receive the token within the Reconfiguration Time, the node will initiate a NETWORK RECONFIGURATION. The ET2 and ET1 bits of the Configuration Register allow the network to operate over longer distances than the 32 miles stated earlier. The logic levels on these bits control the maximum distances over which the COM20019i 3V can operate by controlling the three timeout values described above. For proper network operation, all COM20019i 3V's connected to the same network must have the same Response Time, Idle Time, and Reconfiguration Time.

4.6 Line Protocol

The ARCNET line protocol is considered isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. *On a 312.5 Kbps network,* each byte takes exactly 11 clock intervals of 3.2 μS each. As a result, one byte is transmitted every 35.2 μS and the time to transmit a message can be precisely determined. The line idles in a spacing (logic "0") condition. A logic "0" is defined as no line activity and a logic "1" is defined as a negative pulse of 1.6 uS duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic "1"). Eight bit data characters are then sent, with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be performed as described below:

4.6.1 INVITATIONS TO TRANSMIT

An Invitation To Transmit is used to pass the token from one node to another and is sent by the following sequence:

- An ALERT BURST
- An EOT (End Of Transmission: ASCII code 04H)
- Two (repeated) DID (Destination ID) characters

ALERT BURST	EOT	DID	DID

4.6.2 FREE BUFFER ENQUIRIES

A Free Buffer Enquiry is used to ask another node if it is able to accept a packet of data. It is sent by the following sequence:

- An ALERT BURST
- An ENQ (ENQuiry: ASCII code 85H)
- Two (repeated) DID (Destination ID) characters

ALERT BURST	ENQ	DID	DID

4.6.3 DATA PACKETS

A Data Packet consists of the actual data being sent to another node. It is sent by the following sequence:

- An ALERT BURST
- An SOH (Start Of Header--ASCII code 01H)
- An SID (Source ID) character
- Two (repeated) DID (Destination ID) characters
- A single COUNT character which is the 2's complement of the number of data bytes to follow if a short packet is sent, or 00H followed by a COUNT character if a long packet is sent.
- N data bytes where COUNT = 256-N (or 512-N for a long packet)

Two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is: $X^{16} + X^{15} + X^2 + 1$.

ALERT BURST	SOH	SID	DID	DID	COUNT	data	data	CRC	CRC

4.6.4 ACKNOWLEDGEMENTS

An Acknowledgement is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- An ACK (ACKnowledgement--ASCII code 86H) character

ALERT BURST	ACK

4.6.5 NEGATIVE ACKNOWLEDGEMENTS

A Negative Acknowledgement is used as a negative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- A NAK (Negative Acknowledgement--ASCII code 15H) character

ALERT BURST	NAK

5.0 SYSTEM DESCRIPTION

5.1 Microcontroller Interface

The top halves of Figure 5-1 and Figure 5-2 illustrate typical COM20019i 3V interfaces to the microcontrollers. The interfaces consist of a 8-bit data bus, an address bus and a control bus. In order to support a wide range of microcontrollers without requiring glue logic and without increasing the number of pins, the COM20019i 3V automatically detects and adapts to the type of microcontroller being used. Upon hardware reset, the COM20019i 3V first determines whether the read and write control signals are separate READ and WRITE signals (like the 80XX) or DIRECTION and DATA STROBE (like the 68XX). To determine the type of control signals, the device requires the software to execute at least one write access to external memory before attempting to access the COM20019i 3V. The device defaults to 80XX-like signals. Once the type of control signals are determined, the COM20019i 3V remains in this interface mode until the next hardware reset occurs. The second determination the COM20019i 3V makes is whether the bus is multiplexed or non-multiplexed. To determine the type of bus, the device requires the software to write to an odd memory location followed by a read from an odd location before attempting to access the COM20019i 3V. The signal on the A0 pin during the odd location access tells the COM20019i 3V the type of bus. Since multiplexed operation requires A0 to be active low, activity on the A0 line tells the COM20019i 3V that the bus is non-multiplexed. The device defaults to multiplexed operation. Both determinations may be made simultaneously by performing a WRITE followed by a READ operation to an odd location within the COM20019i 3V Address space 20019 registers. Once the type of bus is determined, the COM20019i 3V remains in this interface mode until hardware reset occurs.

Whenever nCS and nRD are activated, the preset determinations are assumed as final and will not be changed until hardware reset. Refer to Description of Pin Functions section for details on the related signals. All accesses to the internal RAM and the internal registers are controlled by the COM20019i 3V. The internal RAM is accessed via a pointer-based scheme (refer to the Sequential Access Memory section), and the internal registers are accessed via direct addressing. Many peripherals are not fast enough to take advantage of high-speed microcontrollers. Since microcontrollers do not typically have READY inputs, standard peripherals cannot extend cycles to extend the access time. The access time of the COM20019i 3V, on the other hand, is so fast that it does not need to limit the speed of the microcontroller. The COM20019i 3V is designed to be flexible so that it is independent of the microcontroller speed.

The COM20019i 3V provides for no wait state arbitration via direct addressing to its internal registers and a pointer based addressing scheme to access its internal RAM. The pointer may be used in auto-increment mode for typical sequential buffer emptying or loading, or it can be taken out of auto-increment mode to perform random accesses to the RAM. The data within the RAM is accessed through the data register. Data being read is prefetched from memory and placed into the data register for the microcontroller to read. It is important to notice that only by writing a new address pointer (writing to an address pointer low), one obtains the contents of COM20019i 3V internal RAM. Performing only read from the Data Register does not load new data from the internal RAM. During a write operation, the data is stored in the data register and then written into memory. Whenever the pointer is loaded for reads with a new value, data is immediately prefetched to prepare for the first read operation.

FIGURE 5-1: MULTIPLEXED, 8051-LIKE BUS INTERFACE WITH RS-485 INTERFACE

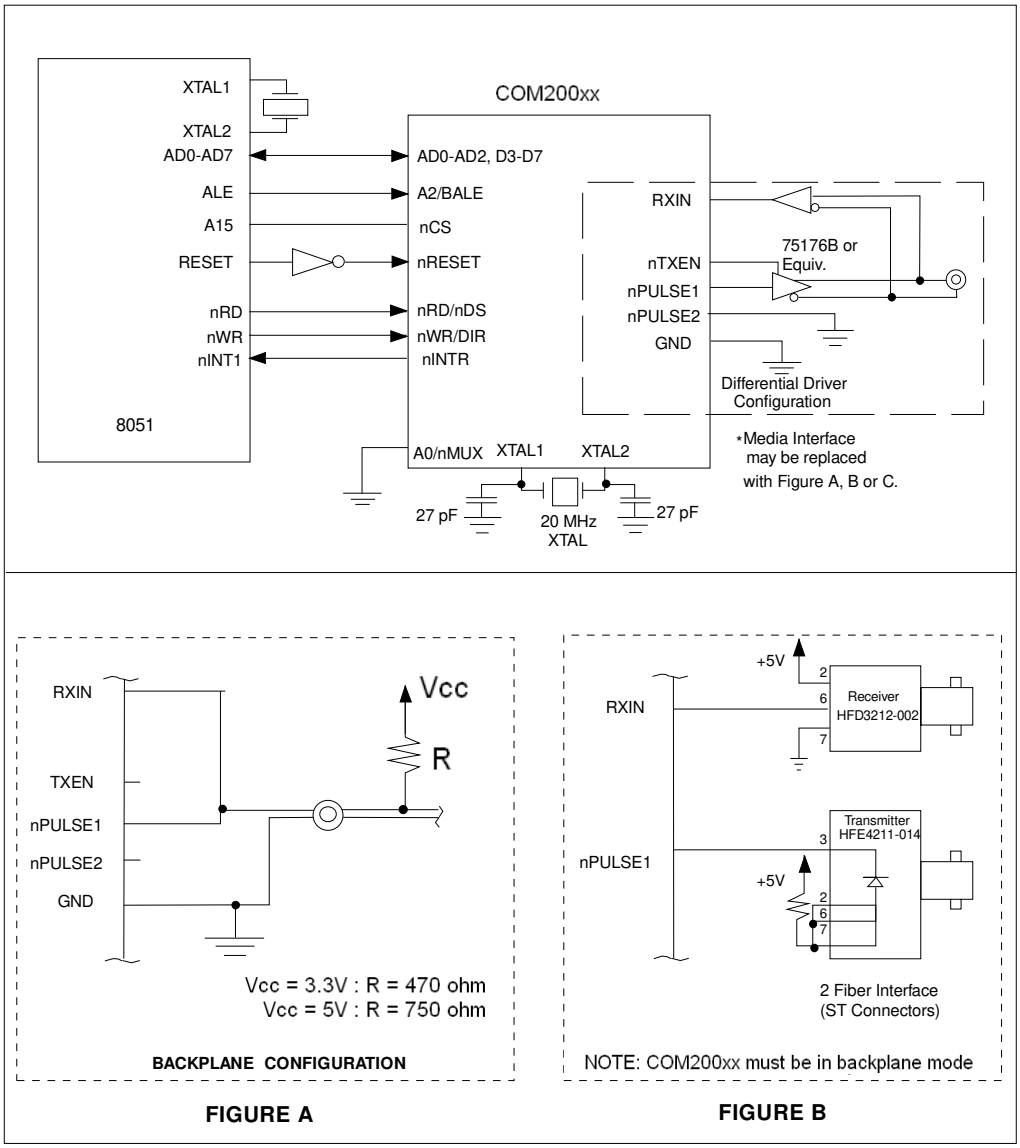
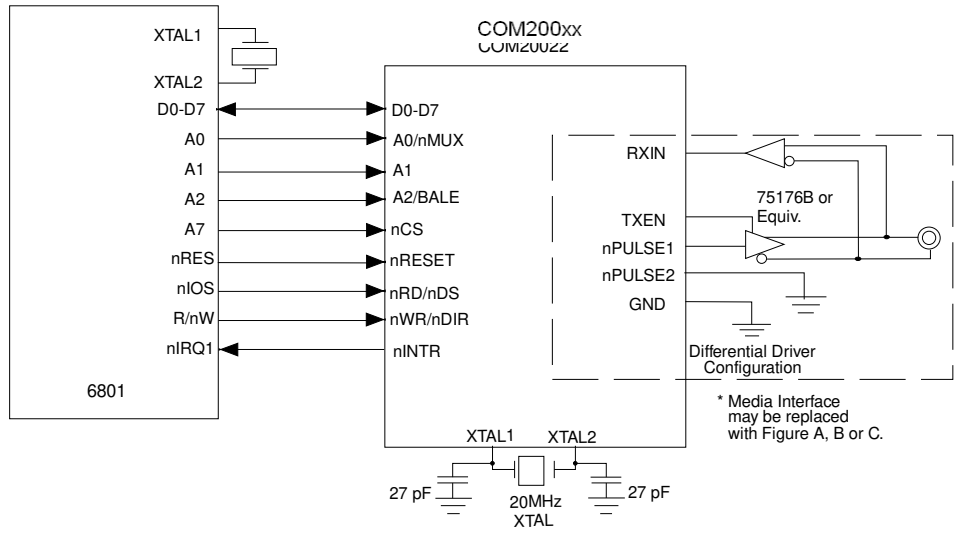


FIGURE A **FIGURE B**

FIGURE 5-2: NON-MULTIPLEXED, 6801-LIKE BUS INTERFACE WITH RS-485 INTERFACE



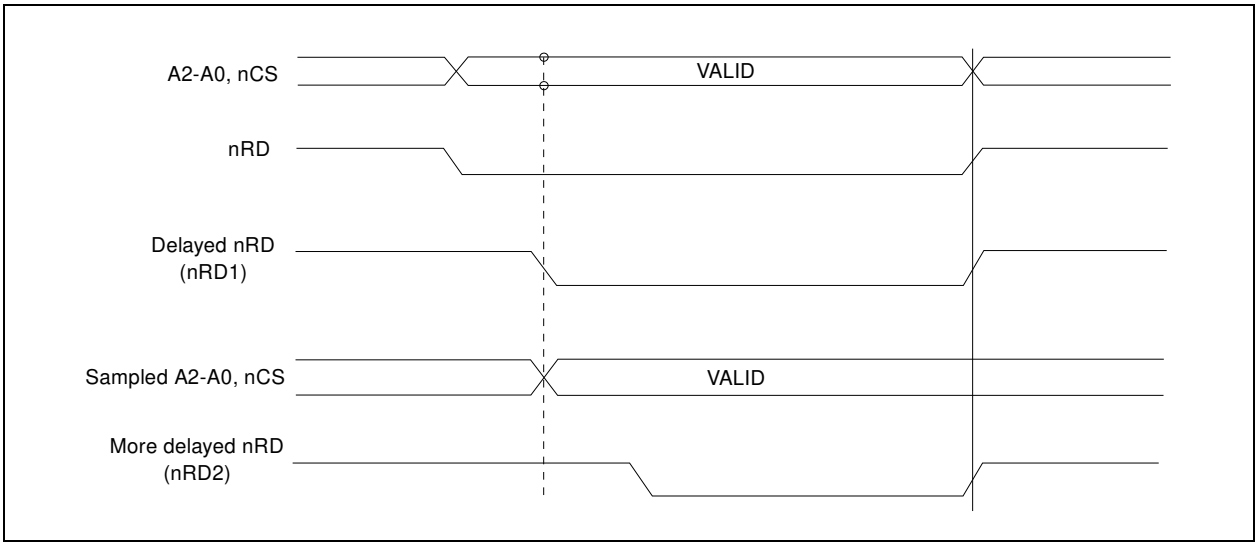
5.1.1 HIGH SPEED CPU BUS TIMING SUPPORT

High speed CPU bus support was added to the COM20019i 3V. The reasoning behind this is as follows: With the Host interface in Non-multiplexed Bus mode, I/O address and Chip Select signals must be stable before the read signal is active and remain after the read signal is inactive. But the High Speed CPU bus timing doesn't adhere to these timings. For example, a RISC type single chip microcontroller (like the HITACHI SH-1 series) changes I/O address at the same time as the read signal. Therefore, several external logic ICs would be required to connect to this microcontroller.

In addition, the Diagnostic Status (DIAG) register is cleared automatically by reading itself. The internal DIAG register read signal is generated by decoding the Address (A2-A0), Chip Select (nCS) and Read (nRD) signals. The decoder will generate a noise spike at the above tight timing. The DIAG register is cleared by the spike signal without reading itself. This is unexpected operation. Reading the internal RAM and Next Id Register have the same mechanism as reading the DIAG register.

Therefore, the address decode and host interface mode blocks were modified to fit the above CPU interface to support high speed CPU bus timing. In Intel CPU mode (nRD, nWR mode), 3 bit I/O address (A2-A0) and Chip Select (nCS) are sampled internally by Flip-Flops on the falling edge of the internal delayed nRD signal. The internal real read signal is the more delayed nRD signal. But the rising edge of nRD doesn't delay. By this modification, the internal real address and Chip Select are stable while the internal real read signal is active. Refer to Figure 5-3 following.

FIGURE 5-3: HIGH SPEED CPU BUS TIMING - INTEL CPU MODE



The I/O address and Chip Select signals, which are supplied to the data output logic, are not sampled. Also, the nRD signal is not delayed, because the above sampling and delaying paths decrease the data access time of the read cycle.

The above sampling and delaying signals are supplied to the Read Pulse Generation logic which generates the clearing pulse for the Diagnostic register and generates the starting pulse of the RAM Arbitration. Typical delay time between nRD and nRD1 is around 15nS and between nRD1 and nRD2 is around 10nS.

Longer pulse widths are needed due to these delays on nRD signal. However, the CPU can insert some wait cycles to extend the width without any impact on performance.

The BUSTMG pin (TQFP package only) is used to support this function. It is used to Enable/Disable the High Speed CPU Read and Write function. It is defined as: BUSTMG = 0, the High Speed CPU Read and Write operations are enabled; BUSTMG = 1, the High Speed CPU Read and Write operations are disabled if the RBUSTMG bit is 0. If BUSTMG = 1 and RBUSTMG = 1, High Speed CPU Read operations are enabled (see definition of RBUSTMG bit below).

In the MOTOROLA CPU mode (DIR, nDS mode), the same modifications apply.

- **For 28-Pin PLCC package** (BUSTMG is tied to 1 internally)

RBUSTMG Bit	Bus Timing Mode
0	Normal Speed CPU Read and Write
1	High Speed CPU Read and Normal Speed CPU Write

- For 48-Pin TQFP package

BUSTMG Pin	RBUSTMG Bit	Bus Timing Mode
0	X	High Speed CPU Read and Write
1	0	Normal Speed CPU Read and Write
1	1	High Speed CPU Read and Normal Speed CPU Write

5.2 Transmission Media Interface

The bottom halves of Figures 2 and 3 illustrate the COM20019i 3V interface to the transmission media used to connect the node to the network. Table 1 lists different types of cable which are suitable for ARCNET applications. (Refer to Note 5-1)

The user may interface to the cable of choice in one of three ways:

Note 5-1 Please refer to TN7-5 – Cabling Guidelines for the COM20020 ULANC, available from Microchip, for recommended cabling distance, termination, and node count for ARCNET nodes.

5.2.1 BACKPLANE CONFIGURATION

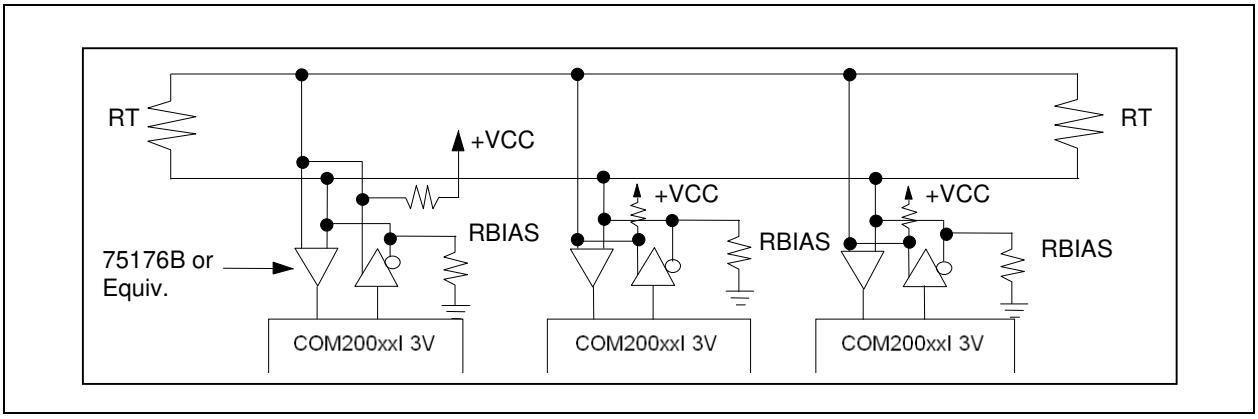
The Backplane Open Drain Configuration is recommended for cost-sensitive, short-distance applications like backplanes and instrumentation. This mode is advantageous because it saves components, cost, and power.

Since the Backplane Configuration encodes data differently than the traditional Hybrid Configuration, nodes utilizing the Backplane Configuration cannot communicate directly with nodes utilizing the Traditional Hybrid Configuration. The Backplane Configuration does not isolate the node from the media nor protects it from Common Mode noise, but Common Mode Noise is less of a problem in short distances.

The COM20019i 3V supplies a programmable output driver for Backplane Mode operation. A push/pull or open drain driver can be selected by programming the P1MODE bit of the Setup 1 Register (see register descriptions for details). The COM20019i 3V defaults to an open drain output.

The Backplane Configuration provides for direct connection between the COM20019i 3V and the media. Only one pull-up resistor (in open drain configuration of the output driver) is required somewhere on the media (not on each individual node). The nPULSE1 signal, in this mode, is an open drain or push/pull driver and is used to directly drive the media. It issues a 1.6µS negative pulse to transmit a logic "1". Note that when used in the open-drain mode, the COM20019i 3V does not have a fail/safe input on the RXIN pin. The nPULSE1 signal actually contains a weak pull-up resistor. This pull-up should not take the place of the resistor required on the media for open drain mode.

FIGURE 5-4: COM20019I 3V NETWORK USING RS-485 DIFFERENTIAL TRANSCEIVERS



In typical applications, the serial backplane is terminated at both ends and a bias is provided by the external pull-up resistor.

The RXIN signal is directly connected to the cable via an internal Schmitt trigger. A negative pulse on this input indicates a logic "1". Lack of pulse indicates a logic "0". For typical single-ended backplane applications, RXIN is connected to nPULSE1 to make the serial backplane data line. A ground line (from the coax or twisted pair) should run in parallel with the signal. For applications requiring different treatment of the receive signal (like filtering or squelching), nPULSE1 and RXIN remain as independent pins. External differential drivers/receivers for increased range and common mode noise rejection, for example, would require the signals to be independent of one another. When the device is in Backplane Mode, the clock provided by the nPULSE2 signal may be used for encoding the data into a different encoding scheme or other synchronous operations needed on the serial data stream.

5.2.2 DIFFERENTIAL DRIVER CONFIGURATION

The Differential Driver Configuration is a special case of the Backplane Mode. It is a dc coupled configuration recommended for applications like car-area networks or other cost-sensitive applications which do not require direct compatibility with existing ARCNET nodes and do not require isolation.

The Differential Driver Configuration cannot communicate directly with nodes utilizing the Traditional Hybrid Configuration. Like the Backplane Configuration, the Differential Driver Configuration does not isolate the node from the media.

The Differential Driver interface includes a RS485 Driver/Receiver to transfer the data between the cable and the COM20019i 3V. The nPULSE1 signal transmits the data, provided the Transmit Enable signal is active. The nPULSE1 signal issues a 1.6µS negative pulse to transmit a logic "1". Lack of pulse indicates a logic "0". The RXIN signal receives the data, the transmitter portion of the COM20019i 3V is disabled during reset and the nPULSE1, nPULSE2 and nTXEN pins are inactive.

5.2.3 PROGRAMMABLE TXEN POLARITY

To accommodate transceivers with active high ENABLE pins, the COM20019i 3V contains a programmable TXEN output. To program the TXEN pin for an active high pulse, the nPULSE2 pin should be connected to ground. To retain the normal active low polarity, nPULSE2 should be left open. The polarity determination is made at power on reset and is valid only for Backplane Mode operation. The nPULSE2 pin should remain grounded at all times if an active high polarity is desired.

FIGURE 5-5: INTERNAL BLOCK DIAGRAM

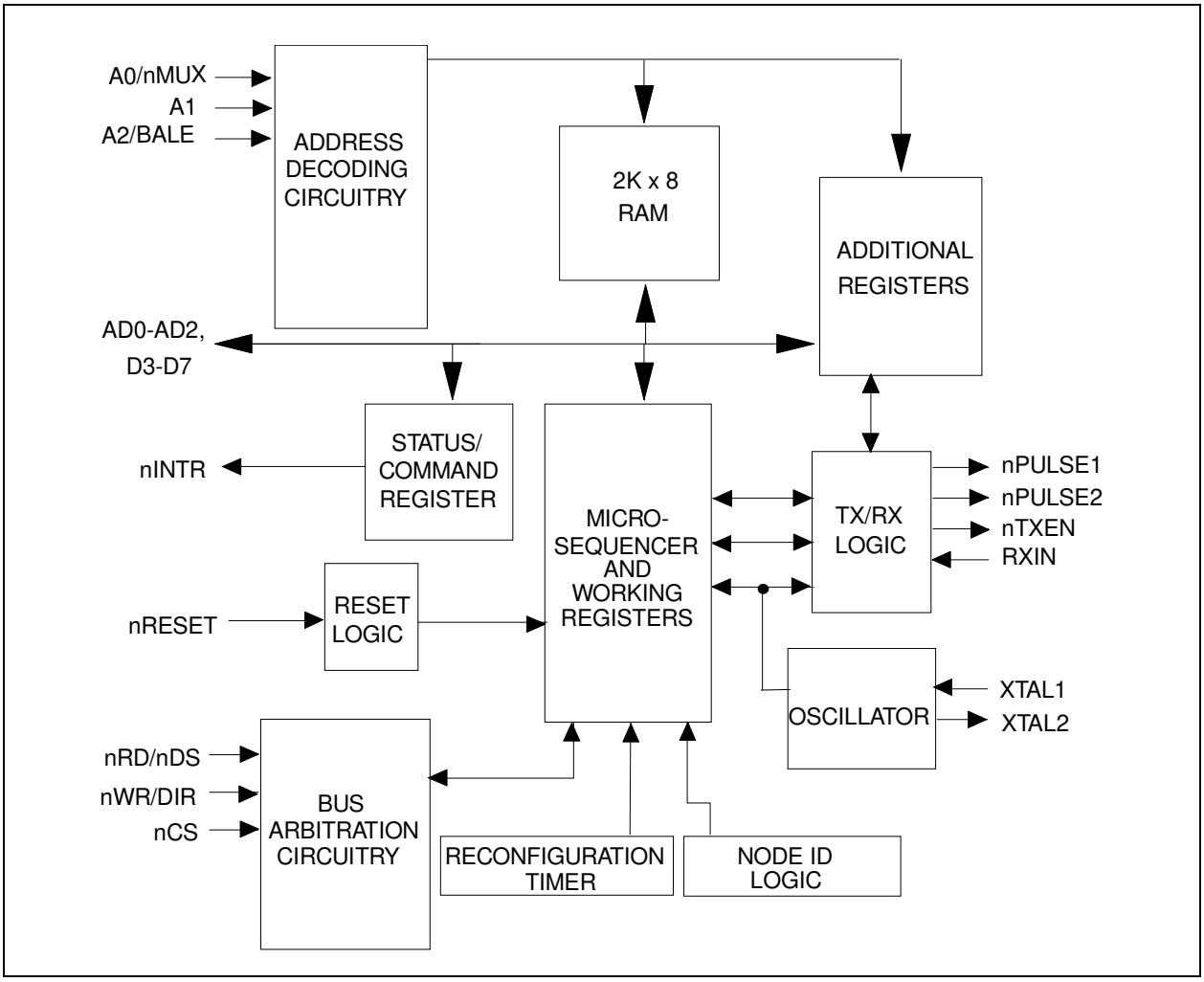


TABLE 5-1: TYPICAL MEDIA

Cable Type	Nominal Impedance	Attenuation per 1000 Ft. at 5 MHz
RG-62 Belden #86262	93Ω	5.5dB
RG-59/U Belden #89108	75Ω	7.0dB
RG-11/U Belden #89108	75Ω	5.5dB
IBM Type 1 (See Note 5-2) Belden #89688	150Ω	7.0dB
IBM Type 3 (See Note 5-2) Telephone Twisted Pair Belden #1155A	100Ω	17.9dB
COMCODE 26 AWG Twisted Pair Part #105-064-703	105Ω	16.0dB

Note 5-2 Non-plenum-rated cables of this type are also available.

Note: For more detailed information on Cabling options including RS-485, transformer-coupled RS-485 and Fiber Optic interfaces, please refer to TN7-5 – Cabling Guidelines for the COM20020 ULANC, available from Microchip.

6.0 FUNCTIONAL DESCRIPTION

6.1 Microsequencer

The COM20019i 3V contains an internal microsequencer which performs all of the control operations necessary to carry out the ARCNET protocol. It consists of a clock generator, a 544 x 8 ROM, a program counter, two instruction registers, an instruction decoder, a no-op generator, jump logic, and reconfiguration logic.

The COM20019i 3V derives a 625 kHz and a 312.5 kHz clock from the output clock of the Clock Multiplier. These clocks provide the rate at which the instructions are executed within the COM20019i 3V. The 625 kHz clock is the rate at which the program counter operates, while the 312.5 kHz clock is the rate at which the instructions are executed. The micro-program is stored in the ROM and the instructions are fetched and then placed into the instruction registers. One register holds the opcode, while the other holds the immediate data. Once the instruction is fetched, it is decoded by the internal instruction decoder, at which point the COM20019i 3V proceeds to execute the instruction. When a no-op instruction is encountered, the microsequencer enters a timed loop and the program counter is temporarily stopped until the loop is complete. When a jump instruction is encountered, the program counter is loaded with the jump address from the ROM. The COM20019i 3V contains an internal reconfiguration timer which interrupts the microsequencer if it has timed out. At this point the program counter is cleared and the MYRECON bit of the Diagnostic Status Register is set.

TABLE 6-1: READ REGISTER SUMMARY

Register	MSB	Read						LSB	ADDR
STATUS	RI/TRI	X/RI	X/TA	POR	TEST	RECON	TMA	TA/ TTA	00
DIAG. STATUS	MY-RECON	DUPID	RCV-ACT	TOKEN	EXC-NAK	TENTID	NEW NEXTID	X	01
ADDRESS PTR HIGH	RD-DATA	AUTO-INC	X	X	X	A10	A9	A8	02
ADDRESS PTR LOW	A7	A6	A5	A4	A3	A2	A1	A0	03
DATA	D7	D6	D5	D4	D3	D2	D1	D0	04
SUB ADR	(R/W) (Note 6-1)	(R/W) (Note 6-1)	X	X	X	SUB-AD2	SUB-AD1	SUB-AD0	05
CONFIG-URATION	RESET	CCHEN	TXEN	ET1	ET2	BACK-PLANE	SUB-AD1	SUB-AD0	06
TENTID	TID7	TID6	TID5	TID4	TID3	TID2	TID1	TID0	07-0
NODE ID	NID7	NID6	NID5	NID4	NID3	NID2	NID1	NID0	07-1
SETUP1	P1 MODE	FOUR NAKS	X	RCV- ALL	CKP3	CKP2	CKP1	SLOW-ARB	07-2
NEXT ID	NXT ID7	NXT ID6	NXT ID5	NXT ID4	NXT ID3	NXT ID2	NXT ID1	NXT ID0	07-3
SETUP2	RBUS-TMG	X	X	X	EF	NO-SYNC	RCN-TM1	RCM-TM2	07-4

Note 6-1 (R/W) These bits can be Written or Read. For more information see Appendix C.

TABLE 6-2: WRITE REGISTER SUMMARY

ADDR	MSB	Write						LSB	Register
00	RI/TR1	0	0	0	EXCNAK	RECON	NEW NEXTID	TA/ TTA	INTERRUPT MASK
01	C7	C6	C5	C4	C3	C2	C1	C0	COMMAND
02	RD-DATA	AUTO-INC	0	0	0	A10	A9	A8	ADDRESS PTR HIGH
03	A7	A6	A5	A4	A3	A2	A1	A0	ADDRESS PTR LOW
04	D7	D6	D5	D4	D3	D2	D1	D0	DATA
05	(R/W) (Note 6-2)	(R/W) (Note 6-2)	0	0	0	SUB-AD2	SUB- AD1	SUB-AD0	SUBADR
06	RESET	CCHEN	TXEN	ET1	ET2	BACK-PLANE	SUB-AD1	SUB-AD0	CONFIG-URATION
07-0	TID7	TID6	TID5	TID4	TID3	TID2	TID1	TID0	TENTID
07-1	NID7	NID6	NID5	NID4	NID3	NID2	NID1	NID0	NODEID
07-2	P1-MODE	FOUR NAKS	0	RCV-ALL	CKP3	CKP2	CKP1	SLOW-ARB	SETUP1
07-3	0	0	0	0	0	0	0	0	TEST
07-4	RBUS-TMG	0	0	0	EF	NO-SYNC	RCN-TM1	RCN-TM0	SETUP2

Note 6-2 (R/W) These bits can be Written or Read. For more information see Appendix C.

6.2 Internal Registers

The COM20019i 3V contains 14 internal registers. Tables 2 and 3 illustrate the COM20019i 3V register map. All undefined bits are read as undefined and must be written as logic "0".

6.2.1 INTERRUPT MASK REGISTER (IMR)

The COM20019i 3V is capable of generating an interrupt signal when certain status bits become true. A write to the IMR specifies which status bits will be enabled to generate an interrupt. The bit positions in the IMR are in the same position as their corresponding status bits in the Status Register and Diagnostic Status Register. A logic "1" in a particular position enables the corresponding interrupt. The Status bits capable of generating an interrupt include the Receiver Inhibited bit, New Next ID bit, Excessive NAK bit, Reconfiguration Timer bit, and Transmitter Available bit. No other Status or Diagnostic Status bits can generate an interrupt.

The six maskable status bits are ANDed with their respective mask bits, and the results are ORed to produce the interrupt signal. An RI or TA interrupt is masked when the corresponding mask bit is reset to logic "0", but will reappear when the corresponding mask bit is set to logic "1" again, unless the interrupt status condition has been cleared by this time. A RECON interrupt is cleared when the "Clear Flags" command is issued. An EXCNAK interrupt is cleared when the "POR Clear Flags" command is issued. A New Next ID interrupt is cleared by reading the Next ID Register. The Interrupt Mask Register defaults to the value 0000 0000 upon hardware reset.

6.2.2 DATA REGISTER

This read/write 8-bit register is used as the channel through which the data to and from the RAM passes. The data is placed in or retrieved from the address location presently specified by the address pointer. The contents of the Data Register are undefined upon hardware reset. In case of READ operation, the Data Register is loaded with the contents of COM20019i 3V Internal Memory upon writing Address Pointer low only once.

6.2.3 TENTATIVE ID REGISTER

The Tentative ID Register is a read/write 8-bit register accessed when the Sub Address Bits are set up accordingly (please refer to the Configuration Register and SUB ADR Register). The Tentative ID Register can be used while the node is on-line to build a network map of those nodes existing on the network. It minimizes the need for operator inter-

action with the network. The node determines the existence of other nodes by placing a Node ID value in the Tentative ID Register and waiting to see if the Tentative ID bit of the Diagnostic Status Register gets set. The network map developed by this method is only valid for a short period of time, since nodes may join or depart from the network at any time. When using the Tentative ID feature, a node cannot detect the existence of the next logical node to which it passes the token. The Next ID Register will hold the ID value of that node. The Tentative ID Register defaults to the value 0000 0000 upon hardware reset only.

6.2.4 NODE ID REGISTER

The Node ID Register is a read/write 8-bit register accessed when the Sub Address Bits are set up accordingly (please refer to the Configuration Register and SUB ADR Register). The Node ID Register contains the unique value which identifies this particular node. Each node on the network must have a unique Node ID value at all times. The Duplicate ID bit of the Diagnostic Status Register helps the user find a unique Node ID. Refer to the Initialization Sequence section for further detail on the use of the DUPID bit. The core of the COM20019i 3V does not wake up until a Node ID other than zero is written into the Node ID Register. During this time, no microcode is executed, no tokens are passed by this node, and no reconfigurations are caused by this node. Once a non-zero NodeID is placed into the Node ID Register, the core wakes up but will not join the network until the TXEN bit of the Configuration Register is set. While the Transmitter is disabled, the Receiver portion of the device is still functional and will provide the user with useful information about the network. The Node ID Register defaults to the value 0000 0000 upon hardware reset only.

6.2.5 NEXT ID REGISTER

The Next ID Register is an 8-bit, read-only register, accessed when the sub-address bits are set up accordingly (please refer to the Configuration Register and SUB ADR Register). The Next ID Register holds the value of the Node ID to which the COM20019i 3V will pass the token. When used in conjunction with the Tentative ID Register, the Next ID Register can provide a complete network map. The Next ID Register is updated each time a node enters/leaves the network or when a network reconfiguration occurs. Each time the microsequencer updates the Next ID Register, a New Next ID interrupt is generated. This bit is cleared by reading the Next ID Register. Default value is 0000 0000 upon hardware or software reset.

6.2.6 STATUS REGISTER

The COM20019i 3V Status Register is an 8-bit read-only register. All of the bits, except for bits 5 and 6, are software compatible with previous Microchip ARCNET devices. In previous ARCNET devices the Extended Timeout status was provided in bits 5 and 6 of the Status Register. In the COM20019i 3V, the COM20020, the COM90C66, and the COM90C165, COM20020-5, COM20051 and COM20051+ these bits exist in and are controlled by the Configuration Register. The Status Register contents are defined as in Table 4, but are defined differently during the Command Chaining operation. Please refer to the Command Chaining section for the definition of the Status Register during Command Chaining operation. The Status Register defaults to the value 1XX1 0001 upon either hardware or software reset.

6.2.7 DIAGNOSTIC STATUS REGISTER

The Diagnostic Status Register contains seven read-only bits which help the user troubleshoot the network or node operation. Various combinations of these bits and the TXEN bit of the Configuration Register represent different situations. All of these bits, except the Excessive NAcK bit and the New Next ID bit, are reset to logic "0" upon reading the Diagnostic Status Register or upon software or hardware reset. The EXCNAK bit is reset by the "POR Clear Flags" command or upon software or hardware reset. The Diagnostic Status Register defaults to the value 0000 000X upon either hardware or software reset.

6.2.8 COMMAND REGISTER

Execution of commands are initiated by performing microcontroller writes to this register. Any combinations of written data other than those listed in Table 5 are not permitted and may result in incorrect chip and/or network operation.

6.2.9 ADDRESS POINTER REGISTERS

These read/write registers are each 8-bits wide and are used for addressing the internal RAM. New pointer addresses should be written by first writing to the High Register and then writing to the Low Register because writing to the Low Register loads the address. The contents of the Address Pointer High and Low Registers are undefined upon hardware reset. Writing to Address Pointer low loads the address.

6.2.10 CONFIGURATION REGISTER

The Configuration Register is a read/write register which is used to configure the different modes of the COM20019i 3V. The Configuration Register defaults to the value 0001 1000 upon hardware reset only. SUBAD0 and SUBAD1 point to the selection in Register 7.

6.2.11 SUB-ADDRESS REGISTER

The sub-address register is new to the COM20019i 3V, previously a reserved register. Bits 2, 1 and 0 are used to select one of the registers assigned to address 7h. SUBAD1 and SUBAD0 already exist in the Configuration register on the COM20020B. They are exactly same as those in the Sub-Address register. If the SUBAD1 and SUBAD0 bits in the Configuration register are changed, the SUBAD1and SUBAD0 in the Sub-Address register are also changed. SUBAD2 is a new sub-address bit. It is used to access the 1 new Set Up register, SETUP2. This register is selected by setting SUBAD2=1. The SUBAD2 bit is cleared automatically by writing the Configuration register.

6.2.12 SETUP 1 REGISTER

The Setup 1 Register is a read/write 8-bit register accessed when the Sub Address Bits are set up accordingly (see the bit definitions of the Configuration Register). The Setup 1 Register allows the user to change the network speed (data rate) or the arbitration speed independently, invoke the Receive All feature and change the nPULSE1 driver type. The data rate may be slowed to 156.25Kbps and/or the arbitration speed may be slowed by a factor of two. The Setup 1 Register defaults to the value 0000 0000 upon hardware reset only.

6.2.13 SETUP 2 REGISTER

The Setup 2 Register is new to the COM20019i 3V. It is an 8-bit read/write register accessed when the Sub Address Bits SUBAD[2:0] are set up accordingly (see the bit definitions of the Sub Address Register). This register contains bits for various functions. The RBUSTMG bit is used to Disable/Enable Fast Read function for High Speed CPU bus support. The EF bit is used to enable the new timing for certain functions in the COM20019i 3V (if EF = 0, the timing is the same as in the COM20020 Rev. B). See Appendix “A”. The NOSYNC bit is used to enable the NOSYNC function during initialization. If this bit is reset, the line has to be idle for the RAM initialization sequence to be written. If set, the line does not have to be idle for the initialization sequence to be written. See Appendix “A”.

The RCNTM[1,0] bits are used to set the time-out period of the recon timer. Programming this timer for shorter time periods has the benefit of shortened network reconfiguration periods. The time periods shown in the table on the following page are limited by a maximum number of nodes in the network. These time-out period values are for 312.5 Kbps. For other data rates, scale the time-out period time values accordingly; the maximum node count remains the same.

RCNTM1	RCNTM0	Time-Out Period	MAX Node Count
0	0	6.72 S	Up to 255 nodes
0	1	1.68 S	Up to 64 nodes
1	0	840 mS	Up to 32 nodes
1	1	420 mS	Up to 16 nodes (See Note 6-3)

Note 6-3 The node ID value 255 must exist in the network for the 420 mS time-out to be valid.

TABLE 6-3: STATUS REGISTER

Bit	Bit Name	Symbol	Description
7	Receiver Inhibited	RI	This bit, if high, indicates that the receiver is not enabled because either an "Enable Receive to Page fnn" command was never issued, or a packet has been deposited into the RAM buffer page fnn as specified by the last "Enable Receive to Page fnn" command. No messages will be received until this command is issued, and once the message has been received, the RI bit is set, thereby inhibiting the receiver. The RI bit is cleared by issuing an "Enable Receive to Page fnn" command. This bit, when set, will cause an interrupt if the corresponding bit of the Interrupt Mask Register (IMR) is also set. When this bit is set and another station attempts to send a packet to this station, this station will send a NAK.
6,5	(Reserved)		These bits are undefined.
4	Power On Reset	POR	This bit, if high, indicates that the COM20019i 3V has been reset by either a software reset, a hardware reset, or writing 00H to the Node ID Register. The POR bit is cleared by the "Clear Flags" command.
3	Test	TEST	This bit is intended for test and diagnostic purposes. It is a logic "0" under normal operating conditions.
2	Reconfiguration	RECON	This bit, if high, indicates that the Line Idle Timer has timed out because the RXIN pin was idle for 656mS. The RECON bit is cleared during a "Clear Flags" command. This bit, when set, will cause an interrupt if the corresponding bit in the IMR is also set. The interrupt service routine should consist of examining the MYRECON bit of the Diagnostic Status Register to determine whether there are consecutive reconfigurations caused by this node.
1	Transmitter Message Acknowledged	TMA	This bit, if high, indicates that the packet transmitted as a result of an "Enable Transmit from Page fnn" command has been acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast messages are never acknowledged. The TMA bit is cleared by issuing the "Enable Transmit from Page fnn" command.
0	Transmitter Available	TA	This bit, if high, indicates that the transmitter is available for transmitting. This bit is set when the last byte of scheduled packet has been transmitted out, or upon execution of a "Disable Transmitter" command. The TA bit is cleared by issuing the "Enable Transmit from Page fnn" command after the node next receives the token. This bit, when set, will cause an interrupt if the corresponding bit in the IMR is also set.

TABLE 6-4: DIAGNOSTIC STATUS REGISTER

Bit	Bit Name	Symbol	Description
7	My Reconfiguration	MY-RECON	This bit, if high, indicates that a past reconfiguration was caused by this node. It is set when the Lost Token Timer times out, and should be typically read following an interrupt caused by RECON. Refer to the Improved Diagnostics section for further detail.
6	Duplicate ID	DUPID	This bit, if high, indicates that the value in the Node ID Register matches both Destination ID characters of the token and a response to this token has occurred. Trailing zero's are also verified. A logic "1" on this bit indicates a duplicate Node ID, thus the user should write a new value into the Node ID Register. This bit is only useful for duplicate ID detection when the device is off line, that is, when the transmitter is disabled. When the device is on line this bit will be set every time the device gets the token. This bit is reset automatically upon reading the Diagnostic Status Register. Refer to the Improved Diagnostics section for further detail.
5	Receive Activity	RCVACT	This bit, if high, indicates that data activity (logic "1") was detected on the RXIN pin of the device. Refer to the Improved Diagnostics section for further detail.
4	Token Seen	TOKEN	This bit, if high, indicates that a token has been seen on the network, sent by a node other than this one. Refer to the Improved Diagnostic section for further detail.
3	Excessive NAK	EXCNAK	This bit, if high, indicates that either 128 or 4 Negative Acknowledgements have occurred in response to the Free Buffer Enquiry. This bit is cleared upon the "POR Clear Flags" command. Reading the Diagnostic Status Register does not clear this bit. This bit, when set, will cause an interrupt if the corresponding bit in the IMR is also set. Refer to the Improved Diagnostics section for further detail.
2	Tentative ID	TENTID	This bit, if high, indicates that a response to a token whose DID matches the value in the Tentative ID Register has occurred. The second DID and the trailing zero's are not checked. Since each node sees every token passed around the network, this feature can be used with the device on-line in order to build and update a network map. Refer to the Improved Diagnostics section for further detail.
1	New Next ID	NEW NXTID	This bit, if high, indicates that the Next ID Register has been updated and that a node has either joined or left the network. Reading the Diagnostic Status Register does not clear this bit. This bit, when set, will cause an interrupt if the corresponding bit in the IMR is also set. The bit is cleared by reading the Next ID Register.
0	(Reserved)		This bit is undefined.