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COM20020I 3.3V Rev.E

5Mbps ARCNET (ANSI 878.1) Controller with 2K x 8 On-Chip RAM

Datasheet

Product Features

- New Features:
  - Data Rates up to 5 Mbps
  - Programmable Reconfiguration Times
- 28 Pin PLCC and 48 Pin TQFP packages; Lead-Free RoHS Compliant packages also available
- Ideal for Industrial/Factory/Building Automation and Transportation Applications
- Deterministic, (ANSI 878.1), Token Passing ARCNET Protocol
- Minimal Microcontroller and Media Interface Logic Required
- Flexible Interface For Use With All Microcontrollers or Microprocessors
- Automatically Detects Type of Microcontroller Interface
- 2Kx8 On-Chip Dual Port RAM
- Command Chaining for Packet Queuing
- Sequential Access to Internal RAM
- Software Programmable Node ID
- Eight, 256 Byte Pages Allow Four Pages TX and RX Plus Scratch-Pad Memory
- Next ID Readable
- Internal Clock Scaler and Clock Multiplier for Adjusting Network Speed
- Operating Temperature Range of -40°C to +85°C
- 3.3V power supply with 5V tolerant I/O
- Self-Reconfiguration Protocol
- Supports up to 255 Nodes
- Supports Various Network Topologies (Star, Tree, Bus...)
- CMOS, Single +3.3V Supply
- Duplicate Node ID Detection
- Powerful Diagnostics
- Receive All Packets Mode
- Flexible Media Interface:
  - Traditional Hybrid Interface For Long Distances at 2.5Mbps
  - RS485 Differential Driver Interface For Low Cost, Low Power, High Reliability

ORDERING INFORMATION

Order Number(s):

COM20020I 3VLJP for 28 pin PLCC * package
COM20020I 3V-DZD for 28 pin PLCC * Lead-Free RoHS Compliant package

COM20020I 3V-HD for 48 pin TQFP package
COM20020I 3V-HT for 48 pin TQFP Lead-Free RoHS Compliant package

*** TQFP package is recommended for new design**

80 Arkay Drive
Hauppauge, NY 11788
(631) 435-6000
FAX (631) 273-3123

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Chapter 1 General Description

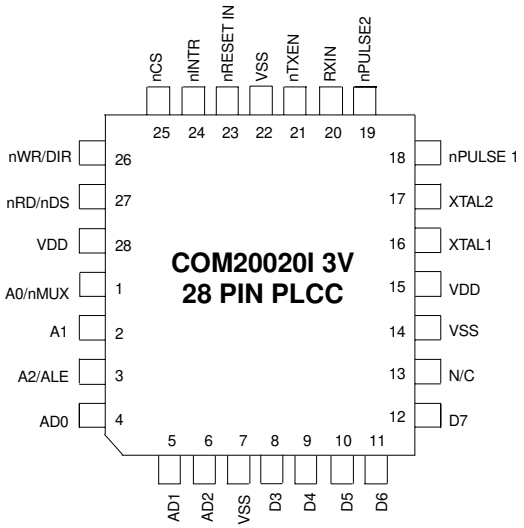
SMSC's COM20020I 3V is a member of the family of Embedded ARCNET Controllers from Standard Microsystems Corporation. The device is a general purpose communications controller for networking microcontrollers and intelligent peripherals in industrial and embedded control environments using an ARCNET protocol engine. The flexible microcontroller and media interfaces, eight-page message support, and extended temperature range of the COM20020I 3V make it the only true network controller optimized for use in industrial and embedded applications. Using an ARCNET protocol engine is the ideal solution for embedded control applications because it provides a deterministic token-passing protocol, a highly reliable and proven networking scheme, and a data rate of up to 5 Mbps when using the COM20020I 3V.

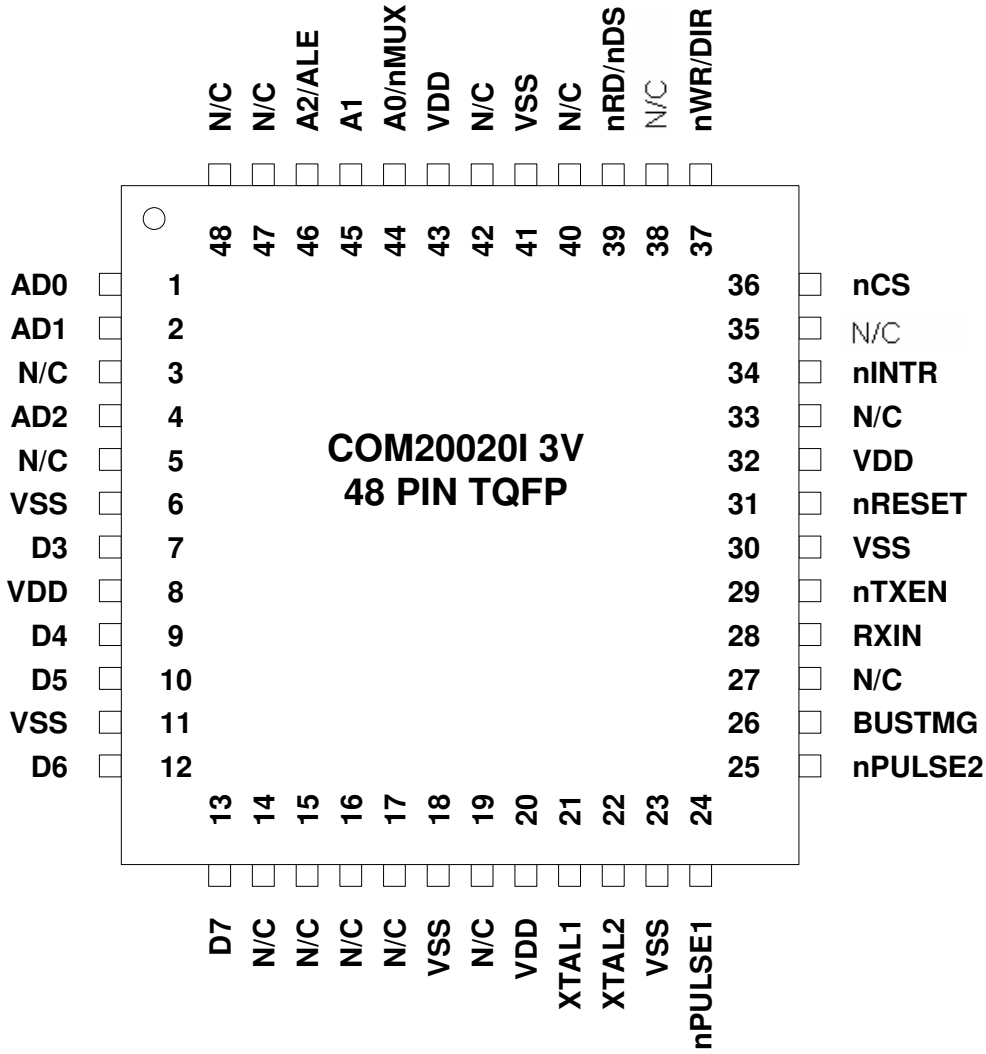
A token-passing protocol provides predictable response times because each network event occurs within a predetermined time interval, based upon the number of nodes on the network. The deterministic nature of ARCNET is essential in real time applications. The integration of the 2Kx8 RAM buffer on-chip, the Command Chaining feature, the 5 Mbps maximum data rate, and the internal diagnostics make the COM20020I 3V the highest performance embedded communications device available. With only one COM20020I 3V and one microcontroller, a complete communications node may be implemented.

For more details on the ARCNET protocol engine and traditional dipulse signaling schemes, please refer to the ARCNET Local Area Network Standard, available from Standard Microsystems Corporation or the ARCNET Designer's Handbook, available from Datapoint Corporation.

For more detailed information on cabling options including RS485, transformer-coupled RS-485 and Fiber Optic interfaces, please refer to the following technical note which is available from Standard Microsystems Corporation: Technical Note 7-5 - Cabling Guidelines for the COM20020I 3V ULANC.

Chapter 2 Pin Configurations





NOTE: BUSTMG pin is only TQFP package

Chapter 3 Description of Pin Functions

PIN NO		NAME	SYMBOL	I/O	DESCRIPTION
PLCC	TQFP	MICROCONTROLLER INTERFACE			
1, 2, 3	44, 45, 46	Address 0-2	A0/nMUX A1 A2/ALE	IN IN IN	On a non-multiplexed mode, A0-A2 are address input bits. (A0 is the LSB) On a multiplexed address/data bus, nMUX tied Low, A1 is left open, and ALE is tied to the Address Latch Enable signal. A1 is connected to an internal pull-up resistor.
4, 5, 6, 8, 9, 10, 11, 12	1, 2, 4, 7, 9, 10, 12, 13	Data 0-7	AD0-AD2, D3-D7	I/O	On a non-multiplexed bus, these signals are used as the lower byte data bus lines. On a multiplexed address/data bus, AD0-AD2 act as the address lines (latched by ALE) and as the low data lines. D3-D7 are always used for data only. These signals are connected to internal pull-up resistors.
26	37	nWrite/ Direction	nWR/DIR	IN	nWR is for 80xx CPU, nWR is Write signal input. Active Low. DIR is for 68xx CPU, DIR is Bus Direction signal input. (Low: Write, High: Read.)
27	39	nRead/ nData Strobe	nRD/nDS	IN	nRD is for 80xx CPU, nRD is Read signal input. Active Low. nDS is for 68xx CPU, nDS is Data Strobe signal input. Active Low.
23	31	nReset In	nRESET	IN	Hardware reset signal. Active Low.
24	34	nInterrupt	nINTR	OUT	Interrupt signal output. Active Low.
25	36	nChip Select	nCS	IN	Chip Select input. Active Low.
-	26	Read/Write Bus Timing Select	BUSTMG	IN	Read and Write Bus Access Timing mode selecting signal. Status of this signal effects CPU Timing. L: High speed timing mode (only for non-multiplexed bus) H: Normal timing mode This signal is connected to internal pull-up registers. **NOTE:** **BUSTMG pin does not exist in PLCC package.**

PIN NO		NAME	SYMBOL	I/O	DESCRIPTION
PLCC	TQFP	TRANSMISSION MEDIA INTERFACE			
18 19	24 25	nPulse 1 nPulse 2	nPULSE1 nPULSE2	OUT I/O	In Normal Mode, these active low signals carry the transmit data information, encoded in pulse format as DIPULSE waveform. In Backplane Mode, the nPULSE1 signal driver is programmable (push/pull or open-drain), while the nPULSE2 signal provides a clock with frequency of doubled data rate. nPULSE1 is connected to a weak internal pull-up resistor on the open/drain driver in backplane mode.
20	28	Receive In	RXIN	IN	This signal carries the receive data information from the line transceiver.
21	29	nTransmit Enable	nTXEN	OUT	Transmission Enable signal. Active polarity is programmable through the nPULSE2 pin. nPULSE2 floating before power-up; nTXEN active low nPULSE2 grounded before power-up; nTXEN active high (this option is only available in Back Plane mode)
16 17	21 22	Crystal Oscillator	XTAL1 XTAL2	IN OUT	An external crystal should be connected to these pins. Oscillation frequency range is from 10 MHz to 20 MHz. If an external TTL clock is used instead, it must be connected to XTAL1 with a 390ohm pull-up resistor, and XTAL2 should be left floating.
15, 28	8, 20, 32, 43	Power Supply	VDD	PWR	+3.3 Volt power supply pins.
7, 14, 22	6, 11, 18, 23, 30, 41	Ground	VSS	PWR	Ground pins.
13	3, 5, 14-17, 19, 27, 33, 35, 38, 40, 42, 47, 48	N/C	N/C		Non-connection

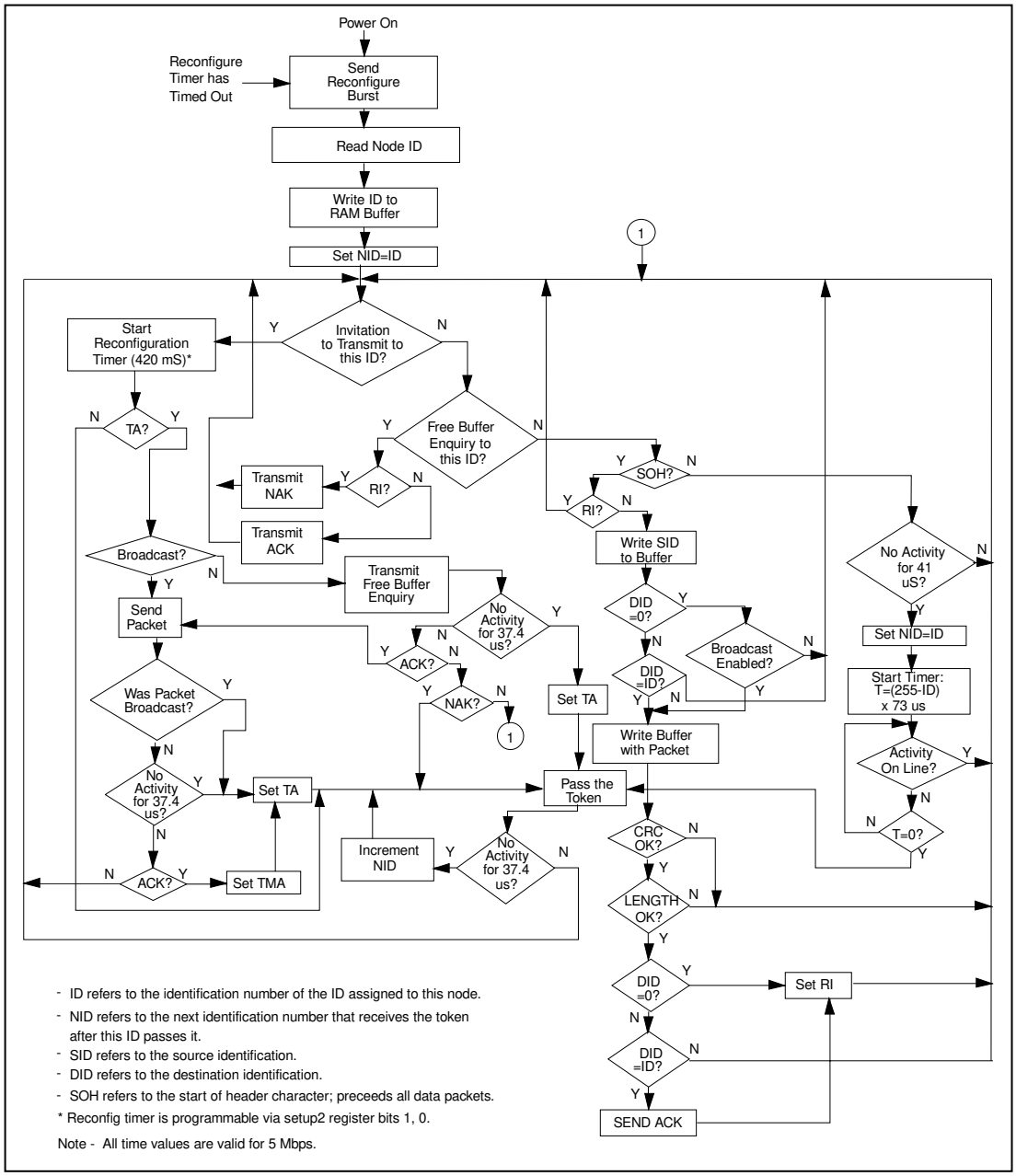


Figure 1 - COM20020I 3V Operation

Chapter 4 Protocol Description

4.1 Network Protocol

Communication on the network is based on a token passing protocol. Establishment of the network configuration and management of the network protocol are handled entirely by the COM20020I 3V's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the COM20020I 3V's internal RAM buffer, and issuing a command to enable the transmitter. When the COM20020I 3V next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16-bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node verifies the packet. If the packet is received successfully, the receiving node transmits an ACKnowledge message (or nothing if it is not received successfully) allowing the transmitter to set the appropriate status bits to indicate successful or unsuccessful delivery of the packet. An interrupt mask permits the COM20020I 3V to generate an interrupt to the processor when selected status bits become true. Figure 1 is a flow chart illustrating the internal operation of the COM20020I 3V connected to a 20 MHz crystal oscillator.

4.2 Data Rates

The COM20020I 3V is capable of supporting data rates from 156.25 Kbps to 5 Mbps. The following protocol description assumes a 5 Mbps data rate. To attain the faster data rates, the clock frequency may be doubled by the internal clock multiplier (see next section). For slower data rates, an internal clock divider scales down the clock frequency. Thus all timeout values are scaled as shown in the following table:

Example: IDLE LINE Timeout @ 5 Mbps = 41 μs. IDLE LINE Timeout for 156.2 Kbps is 41 μs * 32 = 1.3 ms

INTERNAL CLOCK FREQUENCY	CLOCK PRESCALER	DATA RATE	TIMEOUT SCALING FACTOR (MULTIPLY BY)
40 MHz	Div. by 8	5 Mbps	1
20 MHz	Div. by 8	2.5 Mbps	2
	Div. by 16	1.25 Mbps	4
	Div. by 32	625 Kbps	8
	Div. by 64	312.5 Kbps	16
	Div. by 128	156.25 Kbps	32

4.2.1 Selecting Clock Frequencies Above 2.5 Mbps

To realize a 5 Mbps network, an external 40 MHz clock must be input. However, since 40 MHz is near the frequency of FM radio band, it is not practical for use for noise emission reasons. Therefore, higher frequency clocks are generated from the 20 MHz crystal as selected through two bits in the Setup2 register, CKUP as shown below. The selected clock is supplied to the ARCNET controller.

CKUP	CLOCK FREQUENCY (DATA RATE)
0	20 MHz (Up to 2.5Mbps) Default (Bypass)
1	40 MHz (Up to 5Mbps)

This clock multiplier is powered-down (bypassed) on default. After changing the CKUP bit, the ARCNET core operation is stopped and the internal PLL in the clock generator is awakened and it starts to generate the 40 MHz. The lock out time of the internal PLL is 8uSec typically. After more than 8 μsec (this wait time is defined as 1 msec in this data sheet), it is necessary to write command data '18H' to the command register to re-start the ARCNET core operation. This clock generator is called “clock multiplier”.

Changing the CKUP bit must be one time or less after releasing hardware reset.

The EF bit in the SETUP2 register must be set when the data rate is over 5 Mbps.

4.3 Network Reconfiguration

A significant advantage of the COM20020I 3V is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated, a NETWORK RECONFIGURATION is performed. When a new COM20020I 3V is turned on (creating a new active node on the network), or if the COM20020I 3V has not received an INVITATION TO TRANSMIT for 420mS, or if a software reset occurs, the COM20020I 3V causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line.

When any COM20020I 3V senses an idle line for greater than 41μS, which occurs only when the token Is lost, each COM20020I 3V starts an internal timeout equal to 73μs times the quantity 255 minus its own ID. The COM20020I 3V starts network reconfiguration by sending an invitation to transmit first to itself and then to all other nodes by decrementing the destination Node ID. If the timeout expires with no line activity, the COM20020I 3V starts sending INVITATION TO TRANSMIT with the Destination ID (DID) equal to the currently stored NID. Within a given network, only one COM20020I 3V will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM20020I 3V waits for activity on the line. If there is no activity for 37.4μS, the COM20020I 3V increments the NID value and transmits another INVITATION TO TRANSMIT using the NID equal to the DID. If activity appears before the 37.4μS timeout expires, the COM20020I 3V releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT are sent to all NIDs *(1-255).*

Each COM20020I 3V on the network will finally have saved a NID value equal to the ID of the COM20020I 3V that it released control to. At this point, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT being sent to ID's not on the network, until the next NETWORK RECONFIGURATION occurs. When a node is powered off, the previous node attempts to pass the token to it by issuing an INVITATION TO TRANSMIT. Since this node does not respond, the previous node times out and transmits another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The NETWORK RECONFIGURATION time depends on the number of nodes in the network, the propagation delay between nodes, and the highest ID number on the network, but is typically within the range of 12 to 30.5 mS.

4.4 Broadcast Messages

Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the DID equal to zero. Figure 4 illustrates the position of each byte in the packet with the DID residing at address 0X01 or
Hex of the current page selected in the "Enable Transmit from Page fnn" command. Each individual node has the ability to ignore broadcast messages by setting the most significant bit of the "Enable Receive to Page fnn" command to a logic "0".

4.5 Extended Timeout Function

There are three timeouts associated with the COM20020I 3V operation. The values of these timeouts are controlled by bits 3 and 4 of the Configuration Register and bit 5 of the Setup 1 Register.

Response Time
The Response Time determines the maximum propagation delay allowed between any two nodes, and should be chosen to be larger than the round trip propagation delay between the two furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM20020I 3V to start sending a message in response to a received message) which is approximately 6.4 μS. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 15.5 μS translates to a distance of about 2 miles. The flow chart in Figure 1 uses a value of 37.4uS (15.5 + 15.5 + 6.4) to determine if any node will respond.

Idle Time
The Idle Time is associated with a NETWORK RECONFIGURATION. Figure 1 illustrates that during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. All other nodes on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 41 μS. This 41 μS is equal to the Response Time of 37.4 μS plus the time it takes the COM20020I 3V to start retransmitting another message (usually another INVITATION TO TRANSMIT).

Reconfiguration Time
If any node does not receive the token within the Reconfiguration Time, the node will initiate a NETWORK RECONFIGURATION. The ET2 and ET1 bits of the Configuration Register allow the network to operate over longer distances than the 2 miles stated earlier. The logic levels on these bits control the maximum distances over which the COM20020I 3V can operate by controlling the three timeout values described above. For proper network operation, all COM20020I 3V's connected to the same network must have the same Response Time, Idle Time, and Reconfiguration Time.

4.6 Line Protocol

The ARCNET line protocol is considered isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. *On a 5 Mbps network,* each byte takes exactly 11 clock intervals of 200ns each. As a result, one byte is transmitted every 2.2uS and the time to transmit a message can be precisely determined. The line idles in a spacing (logic "0") condition. A logic "0" is defined as no line activity and a logic "1" is defined as a negative pulse of 100nS duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic "1"). Eight bit data characters are then sent, with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be performed as described below:

Invitations To Transmit
An Invitation To Transmit is used to pass the token from one node to another and is sent by the following sequence:
- An ALERT BURST
- An EOT (End Of Transmission: ASCII code 04H)
- Two (repeated) DID (Destination ID) characters

ALERT BURST	EOT	DID	DID

Free Buffer Enquiries
A Free Buffer Enquiry is used to ask another node if it is able to accept a packet of data. It is sent by the following sequence:
- An ALERT BURST
- An ENQ (ENQuiry: ASCII code 85H)
- Two (repeated) DID (Destination ID) characters

ALERT BURST	ENQ	DID	DID

Data Packets
A Data Packet consists of the actual data being sent to another node. It is sent by the following sequence:

- An ALERT BURST
- An SOH (Start Of Header--ASCII code 01H)
- An SID (Source ID) character
- Two (repeated) DID (Destination ID) characters
- A single COUNT character which is the 2's complement of the number of data bytes to follow if a short packet is sent, or 00H followed by a COUNT character if a long packet is sent.

- N data bytes where COUNT = 256-N (or 512-N for a long packet)
- Two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is: $X^{16} + X^{15} + X^2 + 1$.

ALERT BURST	SOH	SID	DID	DID	COUNT	data	data	CRC	CRC

Acknowledgements

An Acknowledgement is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- An ACK (ACKnowledgement--ASCII code 86H) character

ALERT BURST	ACK

Negative Acknowledgements

A Negative Acknowledgement is used as a negative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- A NAK (Negative Acknowledgement--ASCII code 15H) character

ALERT BURST	NAK

Chapter 5 System Description

5.1 Microcontroller Interface

The top halves of Figure 2 and Figure 3 illustrate typical COM20020I 3V interfaces to the microcontrollers. The interfaces consist of a 8-bit data bus, an address bus and a control bus. In order to support a wide range of microcontrollers without requiring glue logic and without increasing the number of pins, the COM20020I 3V automatically detects and adapts to the type of microcontroller being used. Upon hardware reset, the COM20020I 3V first determines whether the read and write control signals are separate READ and WRITE signals (like the 80XX) or DIRECTION and DATA STROBE (like the 68XX). To determine the type of control signals, the device requires the software to execute at least one write access to external memory before attempting to access the COM20020I 3V. The device defaults to 80XX-like signals. Once the type of control signals are determined, the COM20020I 3V remains in this interface mode until the next hardware reset occurs. The second determination the COM20020I 3V makes is whether the bus is multiplexed or non-multiplexed. To determine the type of bus, the device requires the software to write to an odd memory location followed by a read from an odd location before attempting to access the COM20020I 3V. The signal on the A0 pin during the odd location access tells the COM20020I 3V the type of bus. Since multiplexed operation requires A0 to be active low, activity on the A0 line tells the COM20020I 3V that the bus is non-multiplexed. The device defaults to multiplexed operation. Both determinations may be made simultaneously by performing a WRITE followed by a READ operation to an odd location within the COM20020I 3V Address space 20020 registers. Once the type of bus is determined, the COM20020I 3V remains in this interface mode until hardware reset occurs.

Whenever nCS and nRD are activated, the preset determinations are assumed as final and will not be changed until hardware reset. Refer to Chapter 3 Description of Pin Functions for details on the related signals. All accesses to the internal RAM and the internal registers are controlled by the COM20020I 3V. The internal RAM is accessed via a pointer-based scheme (refer to the Sequential Access Memory section), and the internal registers are accessed via direct addressing. Many peripherals are not fast enough to take advantage of high-speed microcontrollers. Since microcontrollers do not typically have READY inputs, standard peripherals cannot extend cycles to extend the access time. The access time of the COM20020I 3V, on the other hand, is so fast that it does not need to limit the speed of the microcontroller. The COM20020I 3V is designed to be flexible so that it is independent of the microcontroller speed.

The COM20020I 3V provides for no wait state arbitration via direct addressing to its internal registers and a pointer based addressing scheme to access its internal RAM. The pointer may be used in auto-increment mode for typical sequential buffer emptying or loading, or it can be taken out of auto-increment mode to perform random accesses to the RAM. The data within the RAM is accessed through the data register. Data being read is prefetched from memory and placed into the data register for the microcontroller to read. It is important to notice that only by writing a new address pointer (writing to an address pointer low), one obtains the contents of COM20020I 3V internal RAM. Performing only read from the Data Register does not load new data from the internal RAM. During a write operation, the data is stored in the data register and then written into memory. Whenever the pointer is loaded for reads with a new value, data is immediately prefetched to prepare for the first read operation.

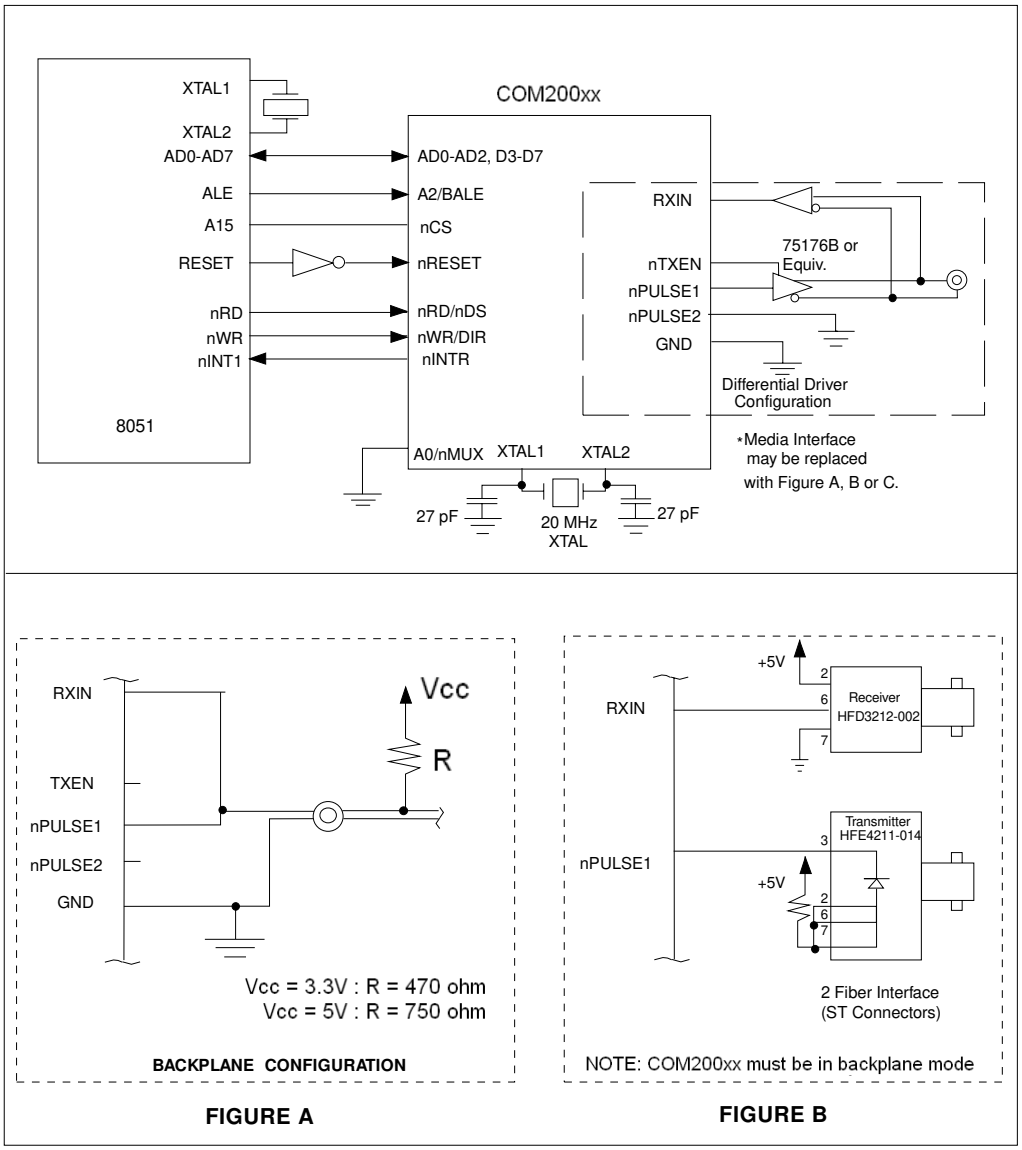
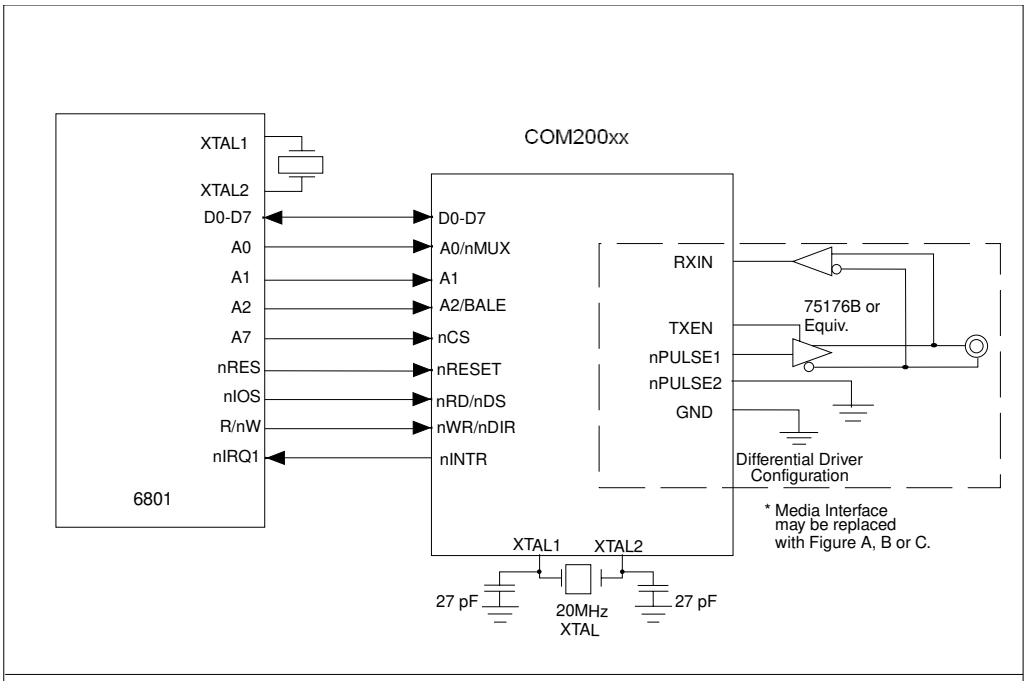


Figure 2 - Multiplexed, 8051-Like Bus Interface With RS-485 Interface



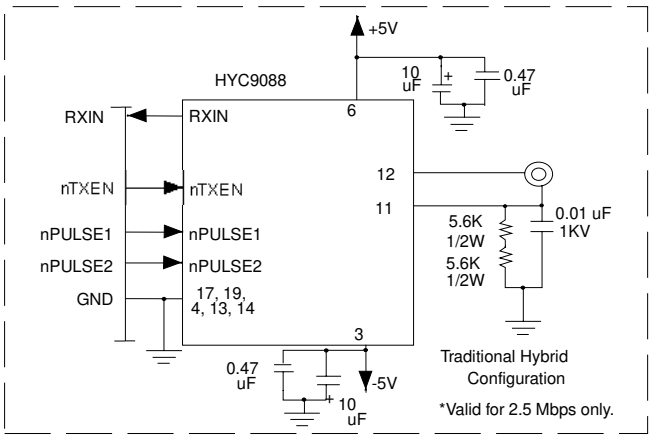


FIGURE C

Figure 3 - Non-Multiplexed, 6801-Like Bus Interface With RS-485 Interface

High Speed CPU Bus Timing Support

High speed CPU bus support was added to the COM20020I 3V. The reasoning behind this is as follows: With the Host interface in Non-multiplexed Bus mode, I/O address and Chip Select signals must be stable before the read signal is active and remain after the read signal is inactive. But the High Speed CPU bus timing doesn't adhere to these timings. For example, a RISC type single chip microcontroller (like the HITACHI SuperH series) changes I/O address at the same time as the read signal. Therefore, several external logic ICs would be required to connect to this microcontroller.

In addition, the Diagnostic Status (DIAG) register is cleared automatically by reading itself. The internal DIAG register read signal is generated by decoding the Address (A2-A0), Chip Select (nCS) and Read (nRD) signals. The decoder will generate a noise spike at the above tight timing. The DIAG register is cleared by the spike signal without reading itself. This is unexpected operation. Reading the internal RAM and Next Id Register have the same mechanism as reading the DIAG register.

Therefore, the address decode and host interface mode blocks were modified to fit the above CPU interface to support high speed CPU bus timing. In Intel CPU mode (nRD, nWR mode), 3 bit I/O address (A2-A0) and Chip Select (nCS) are sampled internally by Flip-Flops on the falling edge of the internal delayed nRD signal. The internal real read signal is the more delayed nRD signal. But the rising edge of nRD doesn't delay. By this modification, the internal real address and Chip Select are stable while the internal real read signal is active. Refer to Figure 4 below.

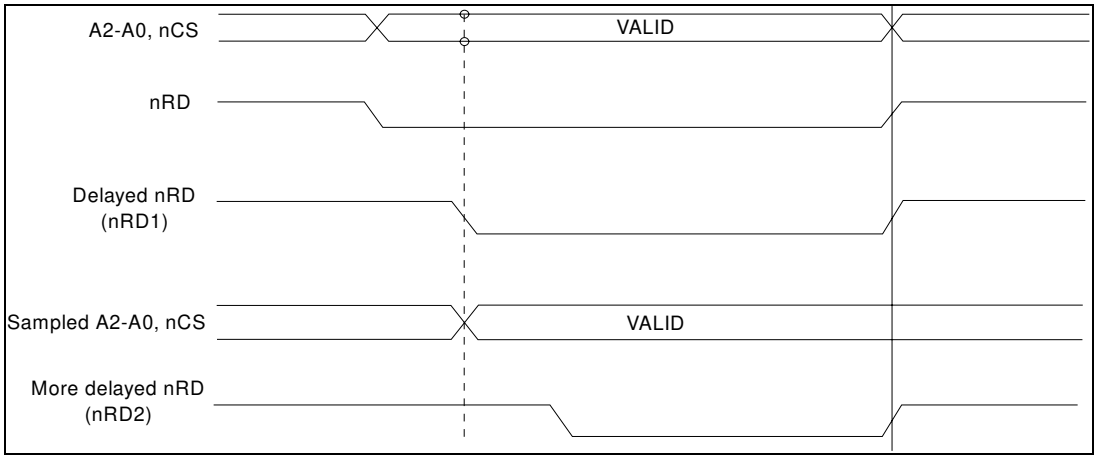


Figure 4 - High Speed Cpu Bus Timing - Intel CPU Mode

The I/O address and Chip Select signals, which are supplied to the data output logic, are not sampled. Also, the nRD signal is not delayed, because the above sampling and delaying paths decrease the data access time of the read cycle.

The above sampling and delaying signals are supplied to the Read Pulse Generation logic which generates the clearing pulse for the Diagnostic register and generates the starting pulse of the RAM Arbitration. Typical delay time between nRD and nRD1 is around 15nS and between nRD1 and nRD2 is around 10nS.

Longer pulse widths are needed due to these delays on nRD signal. However, the CPU can insert some wait cycles to extend the width without any impact on performance.
The RBUSTMG bit was added to Disable/Enable the High Speed CPU Read function. It is defined as: RBUSTMG=0, Disabled (Default); RBUSTMG=1, Enabled.

The BUSTMG pin (TQFP package only) is used to support this function. It is used to Enable/Disable the High Speed CPU Read and Write function. It is defined as: BUSTMG = 0, the High Speed CPU Read and Write operations are enabled; BUSTMG = 1, the High Speed CPU Read and Write operations are disabled if the RBUSTMG bit is 0. If BUSTMG = 1 and RBUSTMG = 1, High Speed CPU Read operations are enabled (see definition of RBUSTMG bit below).

In the MOTOROLA CPU mode (DIR, nDS mode), the same modifications apply.

- **For 28-Pin PLCC package** (BUSTMG is tied to 1 internally)

RBUSTMG BIT	BUS TIMING MODE
0	Normal Speed CPU Read and Write
1	High Speed CPU Read and Normal Speed CPU Write

- **For 48-Pin TQFP package**

BUSTMG PIN	RBUSTMG BIT	BUS TIMING MODE
0	X	High Speed CPU Read and Write
1	0	Normal Speed CPU Read and Write
1	1	High Speed CPU Read and Normal Speed CPU Write

5.2 Transmission Media Interface

The bottom halves of Figure 2 and Figure 3 illustrate the COM20020I 3V interface to the transmission media used to connect the node to the network. **Table** 1 **- Typical Media** lists different types of cable which are suitable for ARCNET applications. The user may interface to the cable of choice in one of three ways:

Traditional Hybrid Interface
The Traditional Hybrid Interface is that which is used with previous ARCNET devices. The Hybrid Interface is recommended if the node is to be placed in a network with other Hybrid-Interfaced nodes. The Traditional Hybrid Interface is for use with nodes operating at 2.5 Mbps only. The transformer coupling of the Hybrid offers isolation for the safety of the system and offers high Common Mode Rejection. The Traditional Hybrid Interface uses circuits like SMSC's HYC9068 or HYC9088 to transfer the pulse-encoded data between the cable and the COM20020I 3V. The COM20020I 3V transmits a logic "1" by generating two 100nS non-overlapping negative pulses, nPULSE1 and nPULSE2. Lack of pulses indicates a logic "0". The nPULSE1 and nPULSE2 signals are sent to the Hybrid, which creates a 200nS dipulse signal on the media.

A logic "0" is transmitted by the absence of the dipulse. During reception, the 200nS dipulse appearing on the media is coupled through the RF transformer of the LAN Driver, which produces a positive pulse at the RXIN pin of the COM20020I 3V. The pulse on the RXIN pin represents a logic "1". Lack of pulse represents a logic "0". Typically, RXIN pulses occur at multiples of 400nS. The COM20020I 3V can tolerate distortion of plus or minus 100nS and still correctly capture and convert the RXIN pulses to NRZ format. Figure 5 illustrates the events which occur in transmission or reception of data consisting of 1, 1, 0.

Please refer to TN7-5 – Cabling Guidelines for the COM20020I 3V ULANC, available from SMSC, for recommended cabling distance, termination, and node count for ARCNET nodes.

Backplane Configuration
The Backplane Open Drain Configuration is recommended for cost-sensitive, short-distance applications like backplanes and instrumentation. This mode is advantageous because it saves components, cost, and power.

Since the Backplane Configuration encodes data differently than the traditional Hybrid Configuration, nodes utilizing the Backplane Configuration cannot communicate directly with nodes utilizing the Traditional Hybrid Configuration. The Backplane Configuration does not isolate the node from the media nor protects it from Common Mode noise, but Common Mode Noise is less of a problem in short distances.

The COM20020I 3V supplies a programmable output driver for Backplane Mode operation. A push/pull or open drain driver can be selected by programming the P1MODE bit of the Setup 1 Register (see register descriptions for details). The COM20020I 3V defaults to an open drain output.

The Backplane Configuration provides for direct connection between the COM20020I 3V and the media. Only one pull-up resistor (in open drain configuration of the output driver) is required somewhere on the media (not on each individual node). The nPULSE1 signal, in this mode, is an open drain or push/pull driver and is used to directly drive the media. It issues a 200nS negative pulse to transmit a logic "1". Note that when used in the open-drain mode, the COM20020I 3V does not have a fail/safe input on the RXIN pin. The nPULSE1 signal actually contains a weak pull-up resistor. This pull-up should not take the place of the resistor required on the media for open drain mode.

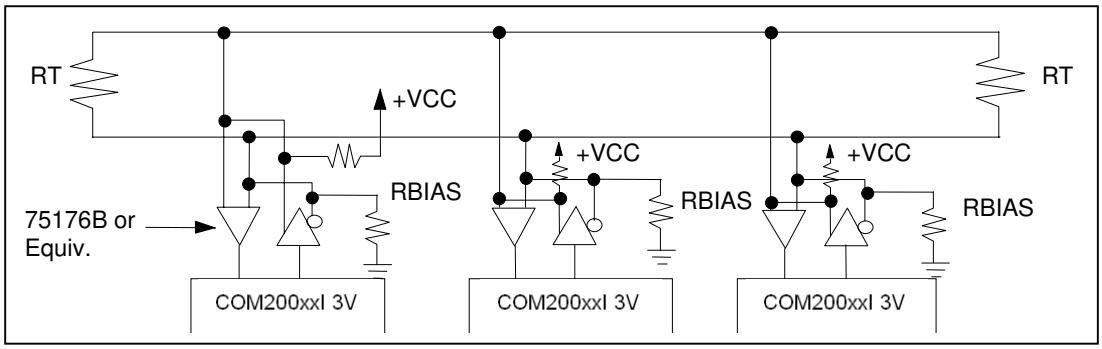


Figure 5 - COM20020I 3V Network Using RS-485 Differential Transceivers

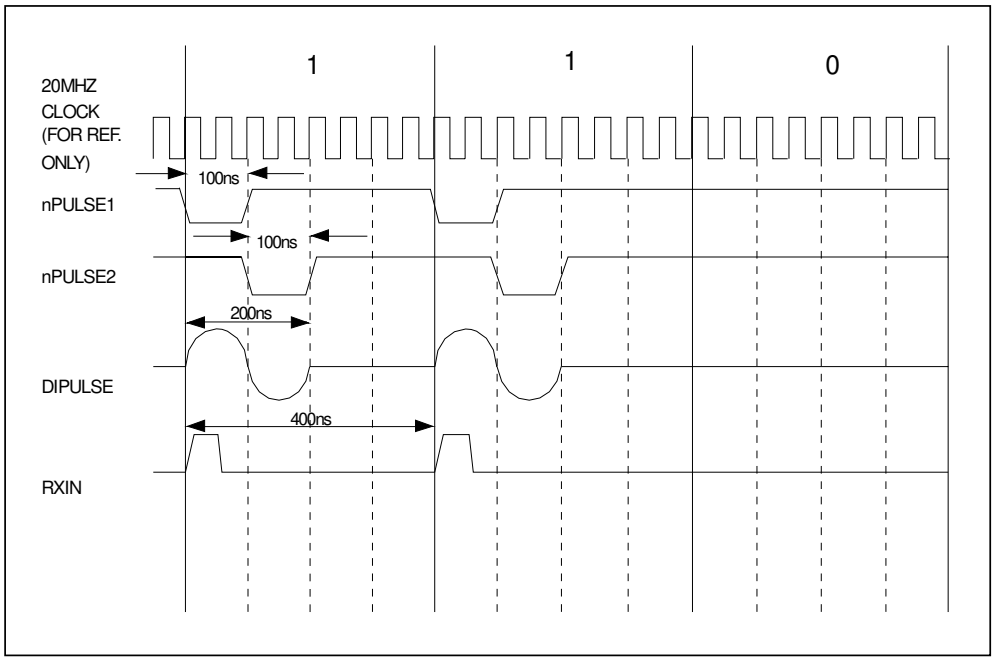


Figure 6 - Dipulse Waveform For Data Of 1-1-0

In typical applications, the serial backplane is terminated at both ends and a bias is provided by the external pull-up resistor.

The RXIN signal is directly connected to the cable via an internal Schmitt trigger. A negative pulse on this input indicates a logic "1". Lack of pulse indicates a logic "0". For typical single-ended backplane applications, RXIN is connected to nPULSE1 to make the serial backplane data line. A ground line (from the coax or twisted pair) should run in parallel with the signal. For applications requiring different treatment of the receive signal (like filtering or squelching), nPULSE1 and RXIN remain as independent pins. External differential drivers/receivers for increased range and common mode noise rejection, for example, would require the signals to be independent of one another.

When the device is in Backplane Mode, the clock provided by the nPULSE2 signal may be used for encoding the data into a different encoding scheme or other synchronous operations needed on the serial data stream.

Differential Driver Configuration

The Differential Driver Configuration is a special case of the Backplane Mode. It is a dc coupled configuration recommended for applications like car-area networks or other cost-sensitive applications which do not require direct compatibility with existing ARCNET nodes and do not require isolation.

The Differential Driver Configuration cannot communicate directly with nodes utilizing the Traditional Hybrid Configuration. Like the Backplane Configuration, the Differential Driver Configuration does not isolate the node from the media.

The Differential Driver interface includes a RS485 Driver/Receiver to transfer the data between the cable and the COM20020I 3V. The nPULSE1 signal transmits the data, provided the Transmit Enable signal is active. The nPULSE1 signal issues a 200nS (at 2.5Mbps) negative pulse to transmit a logic "1". Lack of pulse indicates a logic "0". The RXIN signal receives the data, the transmitter portion of the COM20020I 3V is disabled during reset and the nPULSE1, nPULSE2 and nTXEN pins are inactive.

Programmable TXEN Polarity

To accommodate transceivers with active high ENABLE pins, the COM20020I 3V contains a programmable TXEN output. To program the TXEN pin for an active high pulse, the nPULSE2 pin should be connected to ground. To retain the normal active low polarity, nPULSE2 should be left open. The polarity determination is made at power on reset and is valid only for Backplane Mode operation. The nPULSE2 pin should remain grounded at all times if an active high polarity is desired.

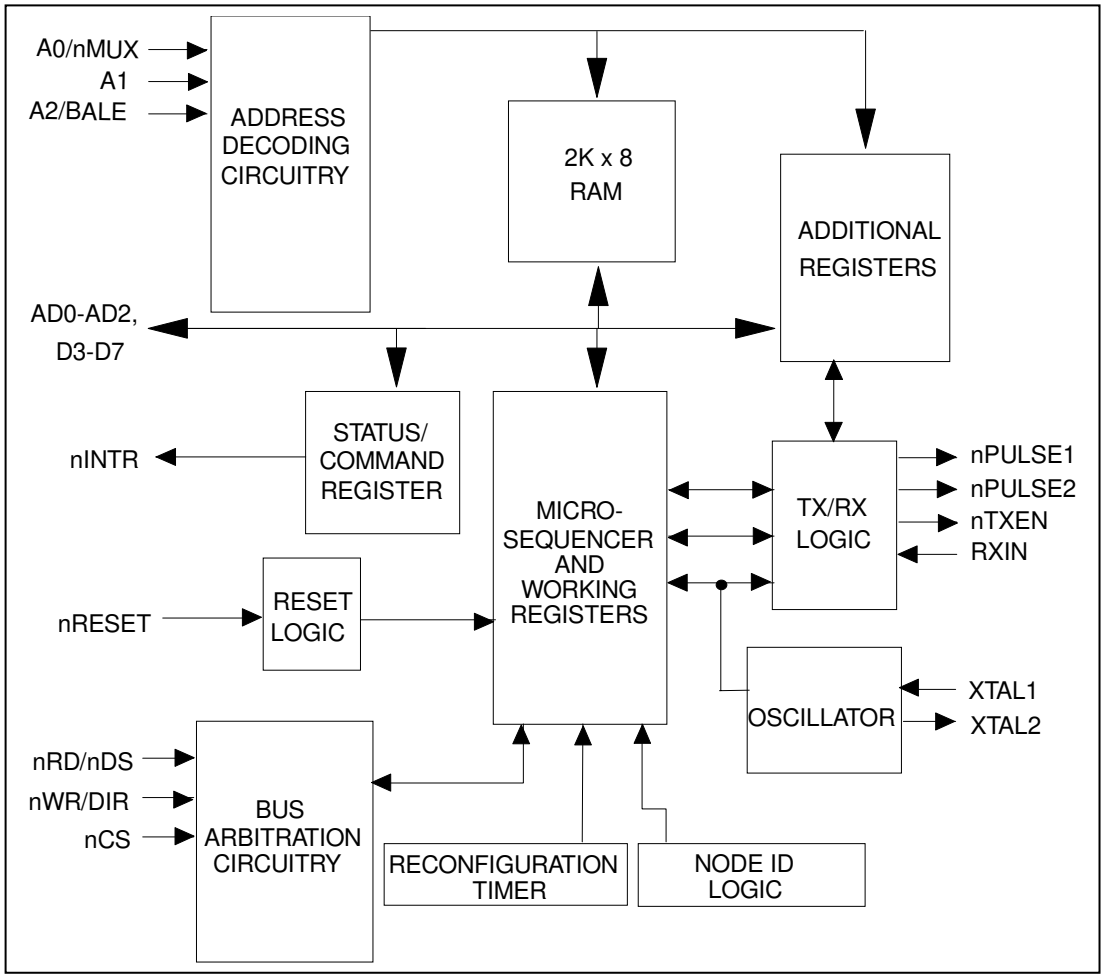


Figure 7 - Internal Block Diagram

Table 1 - Typical Media

CABLE TYPE	NOMINAL IMPEDANCE	ATTENUATION PER 1000 FT. AT 5 MHz
RG-62 Belden #86262	93Ω	5.5dB
RG-59/U Belden #89108	75Ω	7.0dB
RG-11/U Belden #89108	75Ω	5.5dB
IBM Type 1* Belden #89688	150Ω	7.0dB
IBM Type 3* Telephone Twisted Pair Belden #1155A	100Ω	17.9dB
COMCODE 26 AWG Twisted Pair Part #105-064-703	105Ω	16.0dB

*Non-plenum-rated cables of this type are also available.

Note: For more detailed information on Cabling options including RS-485, transformer-coupled RS-485 and Fiber Optic interfaces, please refer to TN7-5 – Cabling Guidelines for the COM20020I 3V ULANC, available from Standard Microsystems Corporation.

Chapter 6 Functional Description

6.1 Microsequencer

The COM20020I 3V contains an internal microsequencer which performs all of the control operations necessary to carry out the ARCNET protocol. It consists of a clock generator, a 544 x 8 ROM, a program counter, two instruction registers, an instruction decoder, a no-op generator, jump logic, and reconfiguration logic.

The COM20020I 3V derives a 10 MHz and a 5 MHz clock from the output clock of the Clock Multiplier. These clocks provide the rate at which the instructions are executed within the COM20020I 3V. The 10 MHz clock is the rate at which the program counter operates, while the 5 MHz clock is the rate at which the instructions are executed. The microprogram is stored in the ROM and the instructions are fetched and then placed into the instruction registers. One register holds the opcode, while the other holds the immediate data. Once the instruction is fetched, it is decoded by the internal instruction decoder, at which point the COM20020I 3V proceeds to execute the instruction. When a no-op instruction is encountered, the microsequencer enters a timed loop and the program counter is temporarily stopped until the loop is complete. When a jump instruction is encountered, the program counter is loaded with the jump address from the ROM. The COM20020I 3V contains an internal reconfiguration timer which interrupts the microsequencer if it has timed out. At this point the program counter is cleared and the MYRECON bit of the Diagnostic Status Register is set.

Table 2 - Read Register Summary

REGISTER	READ MSB							LSB	ADDR
STATUS	RI/TRI	X/RI	X/TA	POR	TEST	RECON	TMA	TA/ TTA	**00**
DIAG. STATUS	MY-RECON	DUPID	RCV-ACT	TOKEN	EXC-NAK	TENTID	NEW NEXT ID	X	**01**
ADDRESS PTR HIGH	RD-DATA	AUTO-INC	X	X	X	A10	A9	A8	**02**
ADDRESS PTR LOW	A7	A6	A5	A4	A3	A2	A1	A0	**03**
DATA	D7	D6	D5	D4	D3	D2	D1	D0	**04**
SUB ADR	(R/W)*	(R/W)*	X	X	X	SUB-AD2	SUB-AD1	SUB-AD0	**05**
CONFIG-URATION	RESET	CCHEN	TXEN	ET1	ET2	BACK-PLANE	SUB-AD1	SUB-AD0	**06**
TENTID	TID7	TID6	TID5	TID4	TID3	TID2	TID1	TID0	**07-0**
NODE ID	NID7	NID6	NID5	NID4	NID3	NID2	NID1	NID0	**07-1**
SETUP1	P1 MODE	FOUR NAKS	X	RCV-ALL	CKP3	CKP2	CKP1	SLOW-ARB	**07-2**
NEXT ID	NXT ID7	NXT ID6	NXT ID5	NXT ID4	NXT ID3	NXT ID2	NXT ID1	NXT ID0	**07-3**
SETUP2	RBUS-TMG	X	X	CKUP	EF	NO-SYNC	RCN-TM1	RCM-TM2	**07-4**

Note*: (R/W) These bits can be Written or Read. For more information see Appendix C.

Table 3 - Write Register Summary

ADDR	WRITE MSB							LSB	REGISTER
00	RI/TR1	0	0	0	EXCNAK	RECON	NEW NEXTID	TA/ TTA	**INTERRUPT MASK**
01	C7	C6	C5	C4	C3	C2	C1	C0	**COMMAND**
02	RD-DATA	AUTO-INC	0	0	0	A10	A9	A8	**ADDRESS PTR HIGH**
03	A7	A6	A5	A4	A3	A2	A1	A0	**ADDRESS PTR LOW**
04	D7	D6	D5	D4	D3	D2	D1	D0	**DATA**
05	(R/W)*	(R/W)*	0	0	0	SUB-AD2	SUB-AD1	SUB-AD0	**SUBADR**
06	RESET	CCHEN	TXEN	ET1	ET2	BACK-PLANE	SUB-AD1	SUB-AD0	**CONFIG-URATION**
07-0	TID7	TID6	TID5	TID4	TID3	TID2	TID1	TID0	**TENTID**
07-1	NID7	NID6	NID5	NID4	NID3	NID2	NID1	NID0	**NODEID**
07-2	P1-MODE	FOUR NAKS	0	RCV-ALL	CKP3	CKP2	CKP1	SLOW-ARB	**SETUP1**
07-3	0	0	0	0	0	0	0	0	**TEST**
07-4	RBUS-TMG	0	0	CKUP	EF	NO-SYNC	RCN-TM1	RCN-TM0	**SETUP2**

Note*:(R/W) These bits can be Written or Read. For more information see Appendix C.

6.2 INTERNAL REGISTERS

The COM20020I 3V contains 14 internal registers. **Table** 2 and **Table** 3 illustrate the COM20020I 3V register map. All undefined bits are read as undefined and must be written as logic "0".

Interrupt Mask Register (IMR)
The COM20020I 3V is capable of generating an interrupt signal when certain status bits become true. A write to the IMR specifies which status bits will be enabled to generate an interrupt. The bit positions in the IMR are in the same position as their corresponding status bits in the Status Register and Diagnostic Status Register. A logic "1" in a particular position enables the corresponding interrupt. The Status bits capable of generating an interrupt include the Receiver Inhibited bit, New Next ID bit, Excessive NAK bit, Reconfiguration Timer bit, and Transmitter Available bit. No other Status or Diagnostic Status bits can generate an interrupt.

The six maskable status bits are ANDed with their respective mask bits, and the results are ORed to produce the interrupt signal. An RI or TA interrupt is masked when the corresponding mask bit is reset to logic "0", but will reappear when the corresponding mask bit is set to logic "1" again, unless the interrupt status condition has been cleared by this time. A RECON interrupt is cleared when the "Clear Flags" command is issued. An EXCNAK interrupt is cleared when the "POR Clear Flags" command is issued. A New Next ID interrupt is cleared by reading the Next ID Register. The Interrupt Mask Register defaults to the value 0000 0000 upon hardware reset.

Data Register
This read/write 8-bit register is used as the channel through which the data to and from the RAM passes. The data is placed in or retrieved from the address location presently specified by the address pointer. The contents of the Data Register are undefined upon hardware reset. In case of READ operation, the Data Register is loaded with the contents of COM20020I 3V Internal Memory upon writing Address Pointer low only once.

Tentative ID Register
The Tentative ID Register is a read/write 8-bit register accessed when the Sub Address Bits are set up accordingly (please refer to the Configuration Register and SUB ADR Register). The Tentative ID Register can be used while the node is on-line to build a network map of those nodes existing on the network. It minimizes the need for operator