Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

COM20022I

10 Mbps ARCNET (ANSI 878.1) Controller with 2Kx8 On-Chip RAM

Datasheet

Product Features

- **New Features**
  - Data Rates up to 10 Mbps
  - Selectable 8/16 Bit Wide Bus With Data Swapper
  - Programmable DMA Channel
  - Programmable Reconfiguration Times
  - 48 Pin TQFP Package; Lead-Free RoHS Compliant Package also available
- Ideal for Industrial/Factory/Building Automation and Transportation Applications
- Deterministic, (ANSI 878.1), Token Passing ARCNET Protocol
- Minimal Microcontroller and Media Interface Logic Required
- Flexible Interface For Use With All Microcontrollers or Microprocessors
- Automatically Detects Type of Microcontroller Interface
- 2Kx8 On-Chip Dual Port RAM
- Command Chaining for Packet Queuing
- Sequential Access to Internal RAM
- Software Programmable Node ID
- Eight, 256 Byte Pages Allow Four Pages TX and RX Plus Scratch-Pad Memory
- Next ID Readable
- Internal Clock Scaler and Clock Multiplier for Adjusting Network Speed
- Operating Temperature Range of -40°C to +85°C
- Self-Reconfiguration Protocol
- Supports up to 255 Nodes
- Supports Various Network Topologies (Star, Tree, Bus...)
- CMOS, Single +5V Supply
- Duplicate Node ID Detection
- Powerful Diagnostics
- Receive All Packets Mode
- Flexible Media Interface:
  - Traditional Hybrid Interface For Long Distances up to Four Miles at 2.5Mbps
  - RS485 Differential Driver Interface For Low Cost, Low Power, High Reliability

DATASHEET

ORDERING INFORMATION

Order Numbers:

COM20022ITQFP for 48 pin TQFP package

COM20022I-HT for 48 pin, TQFP Lead-Free RoHS Compliant package

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Table of Contents

Chapter 1 General Description 6
Chapter 2 Pin Configuration 7
Chapter 3 Description of Pin Functions 8
Chapter 4 Protocol Description 11
4.1 Network Protocol 11
4.2 Data Rates 11
4.2.1 Selecting Clock Frequencies Above 2.5 Mbps 12
4.3 Network Reconfiguration 12
4.4 Broadcast Messages 13
4.5 Extended Timeout Function 13
4.5.1 Response Time 13
4.5.2 Idle Time 13
4.5.3 Reconfiguration Time 13
4.6 Line Protocol 14
4.6.1 Invitations To Transmit 14
4.6.2 Free Buffer Enquiries 14
4.6.3 Data Packets 14
4.6.4 Acknowledgements 15
4.6.5 Negative Acknowledgements 15
Chapter 5 System Description 16
5.1 Microcontroller Interface 16
5.1.1 Selection of 8/16-Bit Access 19
5.1.2 DMA Transfers To And From Internal RAM 19
5.1.3 DMA Operation 20
5.1.4 DMA Data Transfer Sequence (I/O to Memory: Read A Packet) 24
5.1.5 DMA Data Transfer Sequence (Memory to I/O: Write A Packet) 24
5.1.6 High Speed CPU Bus Timing Support 24
5.2 Transmission Media Interface 25
5.2.1 Traditional Hybrid Interface 26
5.2.2 Backplane Configuration 26
5.2.3 Differential Driver Configuration 28
5.2.4 Programmable TXEN Polarity 28
Chapter 6 Functional Description 30
6.1 Microsequencer 30
6.2 Internal Registers 32
6.2.1 Interrupt Mask Register (IMR) 32
6.2.2 Data Register 33
6.2.3 Tentative ID Register 33
6.2.4 Node ID Register 33
6.2.5 Next ID Register 34
6.2.6 Status Register 34
6.2.7 Diagnostic Status Register 34
6.2.8 Command Register 34
6.2.9 Address Pointer Registers 34
6.2.10 Configuration Register 35
6.2.11 Sub-Address Register 35
6.2.12 Setup 1 Register 35
6.2.13 Setup 2 Register 35
6.3 Bus Control Register 36
6.4 DMA Count Register 36
6.5 Internal RAM 47
6.5.1 Sequential Access Memory 47
6.5.2 Access Speed 47
6.6 Software Interface 47
6.6.1 Selecting RAM Page Size 48
6.6.2 Transmit Sequence 49
6.6.3 Receive Sequence 50

6.7 Command Chaining....51
6.7.1 Transmit Command Chaining 51
6.7.2 Receive Command Chaining 52
6.8 Reset Details....53
6.8.1 Internal Reset Logic 53
6.9 Initialization Sequence 53
6.9.1 Bus Determination....53
6.10 Improved Diagnostics 54
6.10.1 Normal Results:....54
6.10.2 Abnormal Results: 55
6.11 Oscillator....55
Chapter 7 Operational Description....56
7.1 Maximum Guaranteed Ratings* 56
7.2 DC Electrical Characteristics....56
Chapter 8 Timing Diagrams 59
Chapter 9 Package Outline 78
Chapter 10 Appendix A 79
10.1 NOSYNC Bit 79
10.2 EF Bit....79
Chapter 11 Appendix B: Example of Interface Circuit Diagram to ISA Bus....82

List of Figures

Figure 2.1 - COM20022I Pin Configuration 7
Figure 3.1 - COM20022I Operation....10
Figure 5.1 - Multiplexed, 8051-Like Bus Interface with RS-485 Interface....17
Figure 5.2 - Non-Multiplexed, 6801-Like Bus Interface with RS-485 Interface 18
Figure 5.3 - DREQ Pin First Assertion Timing for All DMA Modes 21
Figure 5.4 - Programmable Burst Mode DMA Transfer (Rough Timing) 22
Figure 5.5 - Non-Burst Mode DMA Data Transfer Rough Timing....23
Figure 5.6 - Burst Mode DMA Data Transfer Rough Timing 23
Figure 5.7 - High Speed CPU Bus Timing - Intel CPU Mode 25
Figure 5.8 - COM20022I Network Using RS-485 Differential Transceivers....27
Figure 5.9 - Dipulse Waveform for Data of 1-1-0 27
Figure 5.10 - Internal Block Diagram....28
Figure 6.1 - Illustration of the Effect of RTRG Bit on DMA Timing....36
Figure 6.2 - Sequential Access Operation....46
Figure 6.3 - RAM Buffer Packet Configuration 49
Figure 6.4 - Command Chaining Status Register Queue 51
Figure 8.1 - Multiplexed Bus, 68XX-Like Control Signals; Read Cycle 59
Figure 8.2 - Multiplexed Bus, 80XX-Like Control Signals; Read Cycle 60
Figure 8.3 - Multiplexed Bus, 68XX-Like Control Signals Write Cycle....61
Figure 8.4 - Multiplexed Bus, 80XX-Like Control Signals; Write Cycle....62
Figure 8.5 - Non-Multiplexed Bus, 80XX-Like Control Signals; Read Cycle....63
Figure 8.6 - Non-Multiplexed Bus, 80XX-Like Control Signals; Read Cycle....64
Figure 8.7 - Non-Multiplexed Bus, 68XX-Like Control Signals; Read Cycle....65
Figure 8.8 - Non-Multiplexed Bus, 68XX-Like Control Signals; Read Cycle....66
Figure 8.9 - Non-Multiplexed Bus, 80XX-Like Control Signals; Write Cycle....67
Figure 8.10 - Non-Multiplexed Bus, 80XX-Like Control Signals; Write Cycle....68
Figure 8.11 - Non-Multiplexed Bus, 68XX-Like Control Signals; Write Cycle....69
Figure 8.12 - Non-Multiplexed Bus, 68XX-Like Control Signals; Write Cycle....70
Figure 8.13 - Normal Mode Transmit or Receive Timing....71
Figure 8.14 - Backplane Mode Transmit or Receive Timing 72
Figure 8.15 - TTL Input Timing on XTAL1 Pin....73
Figure 8.16 - Reset and Interrupt Timing 73
Figure 8.17 - DMA Timing (Intel Mode 80XX) 74
Figure 8.18 - DMA Timing (Motorola Mode 68XX) 75
Figure 9.1 - COM20022I 48 Pin TQFP Package Outline....78

Figure 10.1 - Effect of the EF Bit on the TA/RI Bit....81

List of Tables

Table 5.1 - Typical Media 29
Table 6.1 - Read Register Summary....31
Table 6.2 - Write Register Summary 32
Table 6.3 - Status Register 37
Table 6.4 - Diagnostic Status Register....38
Table 6.5 - Command Register....39
Table 6.6 - Address Pointer High Register....40
Table 6.7 - Address Pointer Low Register....41
Table 6.8 - Sub Address Register....41
Table 6.9 - Configuration Register 42
Table 6.10 - Setup 1 Register....43
Table 6.11 - Setup 2 Register....44
Table 6.12 - Bus Control Register....45
Table 6.13 - DMA Count Register....46
Table 8.1 - DMA Timing....76
Table 9.1 - COM20022I 48 Pin TQFP Package Parameters....78

For more details on the ARCNET protocol engine and traditional dipulse signaling schemes, please refer to the ARCNET Local Area Network Standard, or the ARCNET Designer's Handbook, available from Datapoint Corporation.

Chapter 1 General Description

SMSC's COM20022I is a member of the family of Embedded ARCNET Controllers from Standard Microsystems Corporation. The device is a general purpose communications controller for networking microcontrollers and intelligent peripherals in industrial, automotive, and embedded control environments using an ARCNET protocol engine. The small 48 pin package, flexible microcontroller and media interfaces, eight- page message support, and extended temperature range of the COM20022I make it the only true network controller optimized for use in industrial, embedded, and automotive applications. Using an ARCNET protocol engine is the ideal solution for embedded control applications because it provides a deterministic token-passing protocol, a highly reliable and proven networking scheme, and a data rate of up to 10 Mbps when using the COM20022I. A token-passing protocol provides predictable response times because each network event occurs within a predetermined time interval, based upon the number of nodes on the network. The deterministic nature of ARCNET is essential in real time applications. The integration of the 2Kx8 RAM buffer on-chip, the Command Chaining feature, the 10 Mbps maximum data rate, and the internal diagnostics make the COM20022I the highest performance embedded communications device available. With only one COM20022I and one microcontroller, a complete communications node may be implemented.

Chapter 2 Pin Configuration

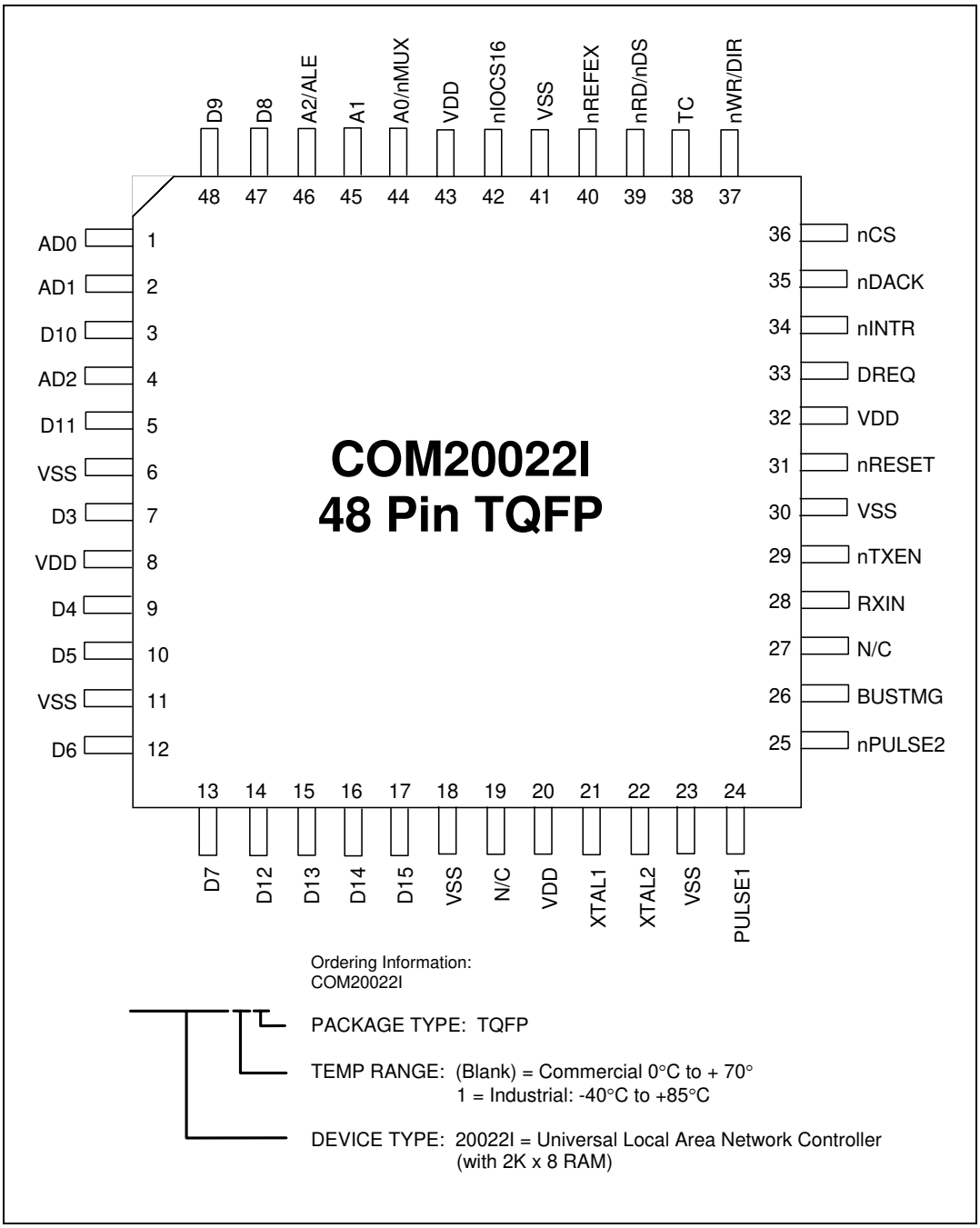


Figure 2.1 - COM20022I Pin Configuration

Chapter 3 Description of Pin Functions

PIN NO	NAME	SYMBOL	I/O	DESCRIPTION
MICROCONTROLLER INTERFACE				
44,45, 46	Address 0-2	A0/nMUX A1 A2/ALE	IN IN IN	On a non-multiplexed mode, A0-A2 are address input bits. (A0 is the LSB) On a multiplexed address/data bus, nMUX tied Low, A1 is left open, and ALE is tied to the Address Latch Enable signal. A1 is connected to an internal pull-up resistor.
1,2,4, 7,9, 10,12, 13	Data 0-7	AD0-AD2, D3-D7	I/O	On a non-multiplexed bus, these signals are used as the lower byte data bus lines. On a multiplexed address/data bus, AD0-AD2 act as the address lines (latched by ALE) and as the low data lines. D3-D7 are always used for data only. These signals are connected to internal pull-up resistors.
47, 48, 3,5, 14-17	Data 8-15	D8-D15	I/O	D8-D15 are always used as the higher byte data bus lines only for 16bit internal RAM access. When the 16bit access is disabled, these signals are always Hi-Z. Enabling or disabling the 16bit access is programmable. A data swapper is built in. These signals are connected to internal pull-up resistors.
37	nWrite/ Direction	nWR/DIR	IN	nWR is for 80xx CPU, nWR is Write signal input. Active Low. DIR is for 68xx CPU, DIR is Bus Direction signal input. (Low: Write, High: Read.)
39	nRead/ nData Strobe	nRD/nDS	IN	nRD is for 80xx CPU, nRD is Read signal input. Active Low. nDS is for 68xx CPU, nDS is Data Strobe signal input. Active Low.
31	nReset In	nRESET	IN	Hardware reset signal. Active Low.
34	nInterrupt	nINTR	OUT	Interrupt signal output. Active Low.
36	nChip Select	nCS	IN	Chip Select input. Active Low.
42	nI/O 16 Bit Indicator	nIOCS16	OUT	This signal is an active Low signal which indicates accessing 16bit data only by CPU. This signal becomes active when CPU accesses to data register only if W16 bit is 1. This signal is same as on ISA Bus signal, but it's not OPEN-DRAIN. An external OPEN-DRAIN Buffer is needed when this signal connects to the ISA Bus.
26	Read/Write Bus Timing Select	BUSTMG	IN	Read and Write Bus Access Timing mode selecting signal. Status of this signal effects CPU and DMA Timing. L: High speed timing mode (only for non-multiplexed bus) H: Normal timing mode This signal is connected to internal pull-up registers.
33	DMA Request	DREQ	OUT	DMA Request signal. Active polarity is programmable. Default is active high.
35	DMA Ack	nDACK	IN	DMA Acknowledge signal. Active Low. When BUSTMG is High, this signal is connected to internal pull-up registers
38	Terminal Count	TC	IN	Terminal Count signal. Active polarity is programmable. Default is active high. When BUSTMG is High, this signal is connected to the internal pull-up resistor.
40	Refresh Execution	nREFEX	IN	Refresh execution signal. Falling edge detection. This signal is connected to the internal pull-up resistor.

PIN NO	NAME	SYMBOL	I/O	DESCRIPTION
TRANSMISSION MEDIA INTERFACE				
24 25	nPulse 1 nPulse 2	nPULSE1 nPULSE2	OUT I/O	In Normal Mode, these active low signals carry the transmit data information, encoded in pulse format as DIPULSE waveform. In Backplane Mode, the nPULSE1 signal driver is programmable (push/pull or open-drain), while the nPULSE2 signal provides a clock with frequency of doubled data rate. nPULSE1 is connected to a weak internal pull-up resistor on the open/drain driver in backplane mode.
28	Receive In	RXIN	IN	This signal carries the receive data information from the line transceiver.
29	nTransmit Enable	nTXEN	OUT	Transmission Enable signal. Active polarity is programmable through the nPULSE2 pin. nPULSE2 floating before power-up; nTXEN active low nPULSE2 grounded before power-up; nTXEN active high (this option is only available in Back Plane mode)
21 22	Crystal Oscillator	XTAL1 XTAL2	IN OUT	An external crystal should be connected to these pins. Oscillation frequency range is from 10 MHz to 20 MHz. If an external TTL clock is used instead, it must be connected to XTAL1 with a 390ohm pull-up resistor, and XTAL2 should be left floating.
8,20, 32,43	Power Supply	VDD	PWR	+5 Volt power supply pins.
6,11, 18,23, 30,41	Ground	VSS	PWR	Ground pins.
19,27	N/C	N/C		Non-connection

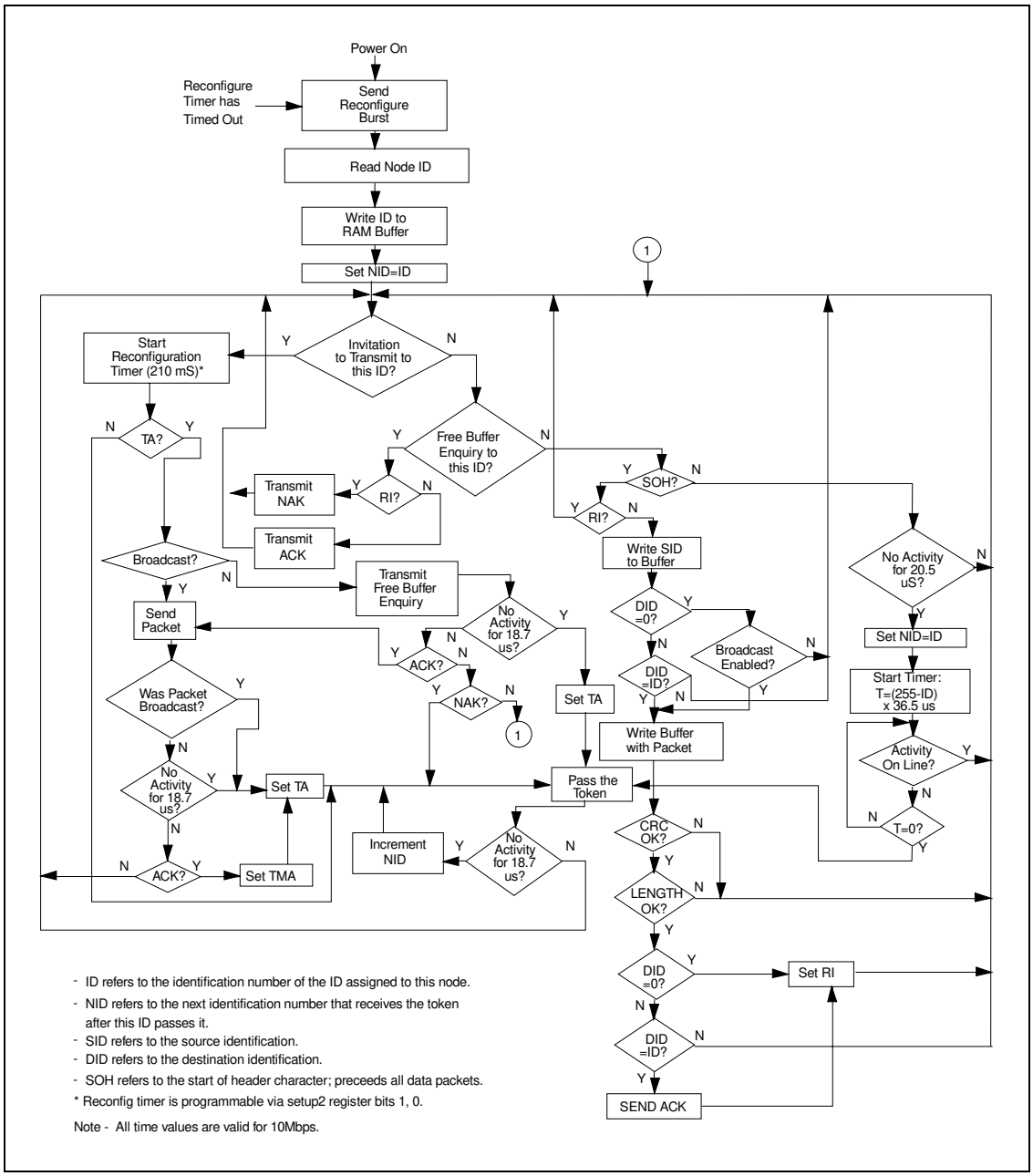


Figure 3.1 - COM20022I Operation

Chapter 4 Protocol Description

4.1 Network Protocol

Communication on the network is based on a token passing protocol. Establishment of the network configuration and management of the network protocol are handled entirely by the COM20022I's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the COM20022I's internal RAM buffer, and issuing a command to enable the transmitter. When the COM20022I next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16-bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node verifies the packet. If the packet is received successfully, the receiving node transmits an ACKnowledge message (or nothing if it is not received successfully) allowing the transmitter to set the appropriate status bits to indicate successful or unsuccessful delivery of the packet. An interrupt mask permits the COM20022I to generate an interrupt to the processor when selected status bits become true. Figure 2.1 is a flow chart illustrating the internal operation of the COM20022I connected to a 20 MHz crystal oscillator.

4.2 Data Rates

The COM20022I is capable of supporting data rates from 156.25 Kbps to 10 Mbps. The following protocol description assumes a 10 Mbps data rate. To attain the faster data rates, the clock frequency may be doubled or quadrupled by the internal clock multiplier (see next section). For slower data rates, an internal clock divider scales down the clock frequency. Thus all timeout values are scaled as shown in the following table:

Example:

IDLE LINE Timeout @ 10 Mbps = 20.5 μs. IDLE LINE Timeout for 156.2 Kbps is 20.5 μs * 64 = 1.3 ms

INTERNAL CLOCK FREQUENCY	CLOCK PRESCALER	DATA RATE	TIMEOUT SCALING FACTOR (MULTIPLY BY)
80 MHz	Div. by 8	10 Mbps	1
40 MHz	Div. by 8	5 Mbps	2
20 MHz	Div. by 8	2.5 Mbps	4
	Div. by 16	1.25 Mbps	8
	Div. by 32	625 Kbps	16
	Div. by 64	312.5 Kbps	32
	Div. by 128	156.25 Kbps	64

4.2.1 Selecting Clock Frequencies Above 2.5 Mbps

To realize a 10 Mbps network, an external 80 MHz clock must be input. However, since 80 MHz is the frequency of FM radio band, it is not practical for use for noise emission reasons. Therefore, higher frequency clocks are generated from the 20 MHz crystal as selected through two bits in the Setup2 register, CKUP[1,0] as shown below. The selected clock is supplied to the ARCNET controller.

CKUP1	CKUP0	CLOCK FREQUENCY (DATA RATE)
0	0	20 MHz (Up to 2.5Mbps) Default (Bypass)
0	1	40 MHz (Up to 5Mbps)
1	0	Reserved
1	1	80 MHz (Only 10Mbps)

This clock multiplier is powered-down (bypassed) on default. After changing the CKUP1 and CKUP0 bits, the ARCNET core operation is stopped and the internal PLL in the clock generator is awakened and it starts to generate the 40 MHz or 80 MHz. The lock out time of the internal PLL is 8uSec typically. After more than 8 μsec (this wait time is defined as 1 msec in this data sheet), it is necessary to write command data '18H' to the command register to re-start the ARCNET core operation. This clock generator is called “clock multiplier”.

Changing the CKUP1 and CKUP0 bits must be one time or less after releasing a hardware reset.

The EF bit in the SETUP2 register must be set when the data rate is over 5 Mbps.

4.3 Network Reconfiguration

A significant advantage of the COM20022I is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated, a NETWORK RECONFIGURATION is performed. When a new COM20022I is turned on (creating a new active node on the network), or if the COM20022I has not received an INVITATION TO TRANSMIT for 210mS, or if a software reset occurs, the COM20022I causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line.

When any COM20022I senses an idle line for greater than 20.5μS, which occurs only when the token Is lost, each COM20022I starts an internal timeout equal to 36.5μs times the quantity 255 minus its own ID. The COM20022I starts network reconfiguration by sending an invitation to transmit first to itself and then to all other nodes by decrementing the destination Node ID. If the timeout expires with no line activity, the COM20022I starts sending INVITATION TO TRANSMIT with the Destination ID (DID) equal to the currently stored NID. Within a given network, only one COM20022I will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM20022I waits for activity on the line. If there is no activity for 18.7μS, the COM20022I increments the NID value and transmits another INVITATION TO TRANSMIT using the NID equal to the DID. If activity appears before the 18.7μS timeout expires, the COM20022I releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT are sent to all NIDs *(1-255).*

Each COM20022I on the network will finally have saved a NID value equal to the ID of the COM20022I that it released control to. At this point, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT being sent to ID's not on the network, until the next NETWORK RECONFIGURATION occurs. When a node is powered off, the previous node attempts to pass the token to it by issuing an INVITATION TO TRANSMIT. Since this node does not respond, the previous node times out and transmits another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The NETWORK RECONFIGURATION time depends on the number of nodes in the network, the propagation delay between nodes, and the highest ID number on the network, but is typically within the range of 6 to 15.3 mS.

4.4 Broadcast Messages

Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the DID equal to zero. Figure 5.7 illustrates the position of each byte in the packet with the DID residing at address 0X01 or 1 Hex of the current page selected in the "Enable Transmit from Page fnn" command. Each individual node has the ability to ignore broadcast messages by setting the most significant bit of the "Enable Receive to Page fnn" command (see Table 6.5) to a logic "0".

4.5 Extended Timeout Function

There are three timeouts associated with the COM20022I operation. The values of these timeouts are controlled by bits 3 and 4 of the Configuration Register and bit 5 of the Setup 1 Register.

4.5.1 Response Time

The Response Time determines the maximum propagation delay allowed between any two nodes, and should be chosen to be larger than the round trip propagation delay between the two furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM20022I to start sending a message in response to a received message) which is approximately 3.2 µS. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 7.75 µS translates to a distance of about 1 mile. The flow chart in Figure 3.1Figure 2.1 uses a value of 18.7 µS (7.75 + 7.75 + 3.2) to determine if any node will respond.

4.5.2 Idle Time

The Idle Time is associated with a NETWORK RECONFIGURATION. Figure 3.1Figure 2.1 illustrates that during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. All other nodes on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 20.5 µS. This 20.5 µS is equal to the Response Time of 18.7 µS plus the time it takes the COM20022I to start retransmitting another message (usually another INVITATION TO TRANSMIT).

4.5.3 Reconfiguration Time

If any node does not receive the token within the Reconfiguration Time, the node will initiate a NETWORK RECONFIGURATION. The ET2 and ET1 bits of the Configuration Register allow the network to operate over longer distances than the 1 mile stated earlier. The logic levels on these bits control the maximum distances over which the COM20022I can operate by controlling the three timeout values described above. For proper network operation, all COM20022I's connected to the same network must have the same Response Time, Idle Time, and Reconfiguration Time.

4.6 Line Protocol

The ARCNET line protocol is considered isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. *On a 10 Mbps network,* each byte takes exactly 11 clock intervals of 100ns each. As a result, one byte is transmitted every 1.1 µS and the time to transmit a message can be precisely determined. The line idles in a spacing (logic "0") condition. A logic "0" is defined as no line activity and a logic "1" is defined as a negative pulse of 50nS duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic "1"). Eight bit data characters are then sent, with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be performed as described below:

4.6.1 Invitations To Transmit

An Invitation To Transmit is used to pass the token from one node to another and is sent by the following sequence:

- An ALERT BURST
- An EOT (End Of Transmission: ASCII code 04H)
- Two (repeated) DID (Destination ID) characters

ALERT BURST	EOT	DID	DID

4.6.2 Free Buffer Enquiries

A Free Buffer Enquiry is used to ask another node if it is able to accept a packet of data. It is sent by the following sequence:

- An ALERT BURST
- An ENQ (ENQuiry: ASCII code 85H)
- Two (repeated) DID (Destination ID) characters

ALERT BURST	ENQ	DID	DID

4.6.3 Data Packets

A Data Packet consists of the actual data being sent to another node. It is sent by the following sequence:

- An ALERT BURST
- An SOH (Start Of Header--ASCII code 01H)
- An SID (Source ID) character
- Two (repeated) DID (Destination ID) characters
- A single COUNT character which is the 2's complement of the number of data bytes to follow if a short packet is sent, or 00H followed by a COUNT character if a long packet is sent.
- N data bytes where COUNT = 256-N (or 512-N for a long packet)
- Two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is: $X^{16} + X^{15} + X^2 + 1$.

ALERT BURST	SOH	SID	DID	DID	COUNT	data	data	CRC	CRC

4.6.4 Acknowledgements

An Acknowledgement is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- An ACK (ACKnowledgement--ASCII code 86H) character

ALERT BURST	ACK

4.6.5 Negative Acknowledgements

A Negative Acknowledgement is used as a negative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- A NAK (Negative Acknowledgement--ASCII code 15H) character

ALERT BURST	NAK

Chapter 5 System Description

5.1 Microcontroller Interface

The top halves of Figure 5.1 and Figure 5.2 illustrate typical COM20022I interfaces to the microcontrollers. The interfaces consist of a 8-bit data bus, an address bus and a control bus. In order to support a wide range of microcontrollers without requiring glue logic and without increasing the number of pins, the COM20022I automatically detects and adapts to the type of microcontroller being used. Upon hardware reset, the COM20022I first determines whether the read and write control signals are separate READ and WRITE signals (like the 80XX) or DIRECTION and DATA STROBE (like the 68XX). To determine the type of control signals, the device requires the software to execute at least one write access to external memory before attempting to access the COM20022I. The device defaults to 80XX-like signals. Once the type of control signals are determined, the COM20022I remains in this interface mode until the next hardware reset occurs. The second determination the COM20022I makes is whether the bus is multiplexed or non-multiplexed. To determine the type of bus, the device requires the software to write to an odd memory location followed by a read from an odd location before attempting to access the COM20022I. The signal on the A0 pin during the odd location access tells the COM20022I the type of bus. Since multiplexed operation requires A0 to be active low, activity on the A0 line tells the COM20022I that the bus is non-multiplexed. The device defaults to multiplexed operation. Both determinations may be made simultaneously by performing a WRITE followed by a READ operation to an odd location within the COM20022I Address space 20022 registers. Once the type of bus is determined, the COM20022I remains in this interface mode until hardware reset occurs.

Whenever nCS and nRD are activated, the preset determinations are assumed as final and will not be changed until hardware reset. Refer to Description of Pin Functions section for details on the related signals. All accesses to the internal RAM and the internal registers are controlled by the COM20022I. The internal RAM is accessed via a pointer-based scheme (refer to the Sequential Access Memory section), and the internal registers are accessed via direct addressing. Many peripherals are not fast enough to take advantage of high-speed microcontrollers. Since microcontrollers do not typically have READY inputs, standard peripherals cannot extend cycles to extend the access time. The access time of the COM20022I, on the other hand, is so fast that it does not need to limit the speed of the microcontroller. The COM20022I is designed to be flexible so that it is independent of the microcontroller speed.

The COM20022I provides for no wait state arbitration via direct addressing to its internal registers and a pointer based addressing scheme to access its internal RAM. The pointer may be used in auto-increment mode for typical sequential buffer emptying or loading, or it can be taken out of auto-increment mode to perform random accesses to the RAM. The data within the RAM is accessed through the data register. Data being read is prefetched from memory and placed into the data register for the microcontroller to read. It is important to notice that only by writing a new address pointer (writing to an address pointer low), one obtains the contents of COM20022I internal RAM. Performing only read from the Data Register does not load new data from the internal RAM. During a write operation, the data is stored in the data register and then written into memory. Whenever the pointer is loaded for reads with a new value, data is immediately prefetched to prepare for the first read operation.

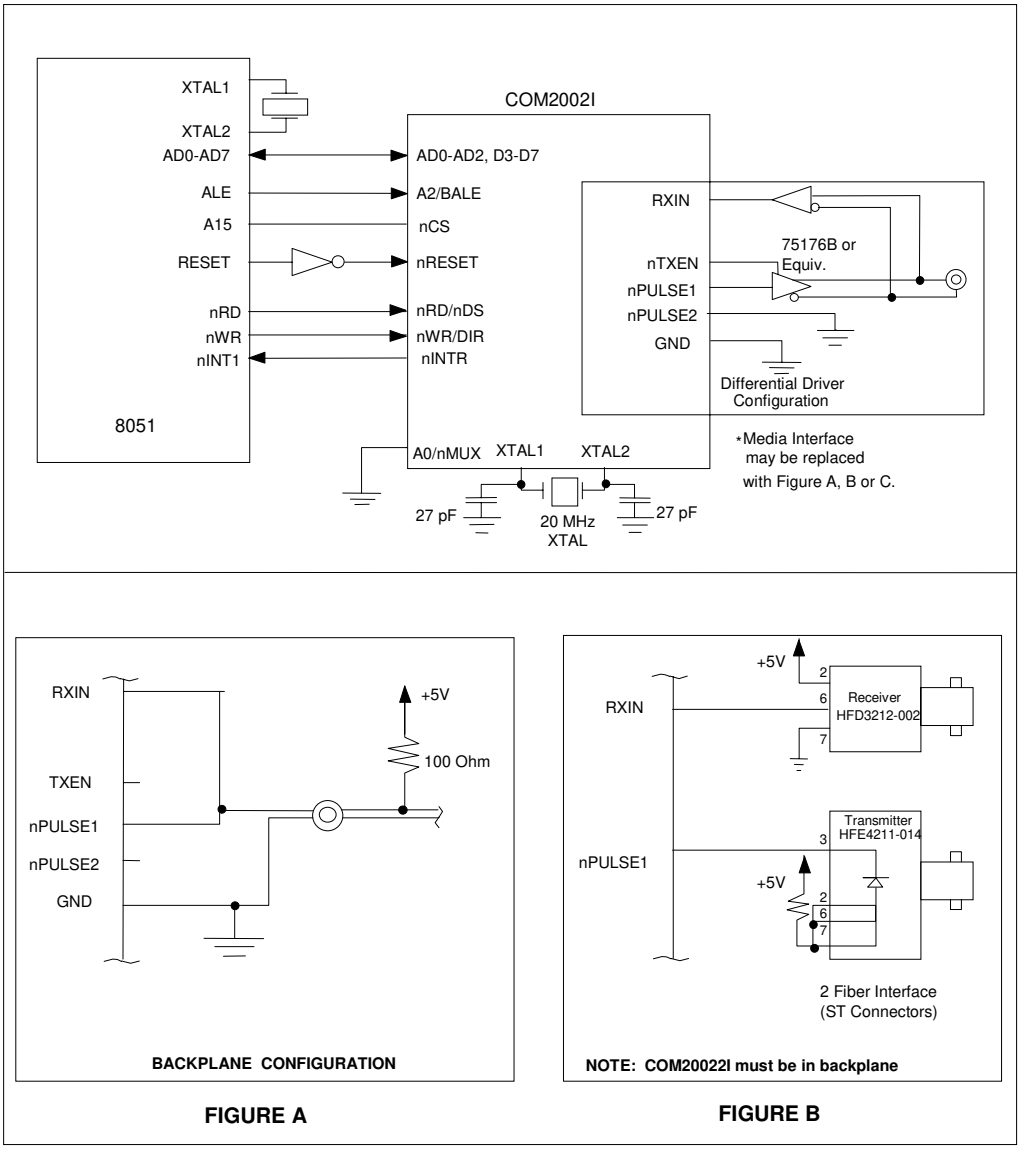


Figure 5.1 - Multiplexed, 8051-Like Bus Interface with RS-485 Interface

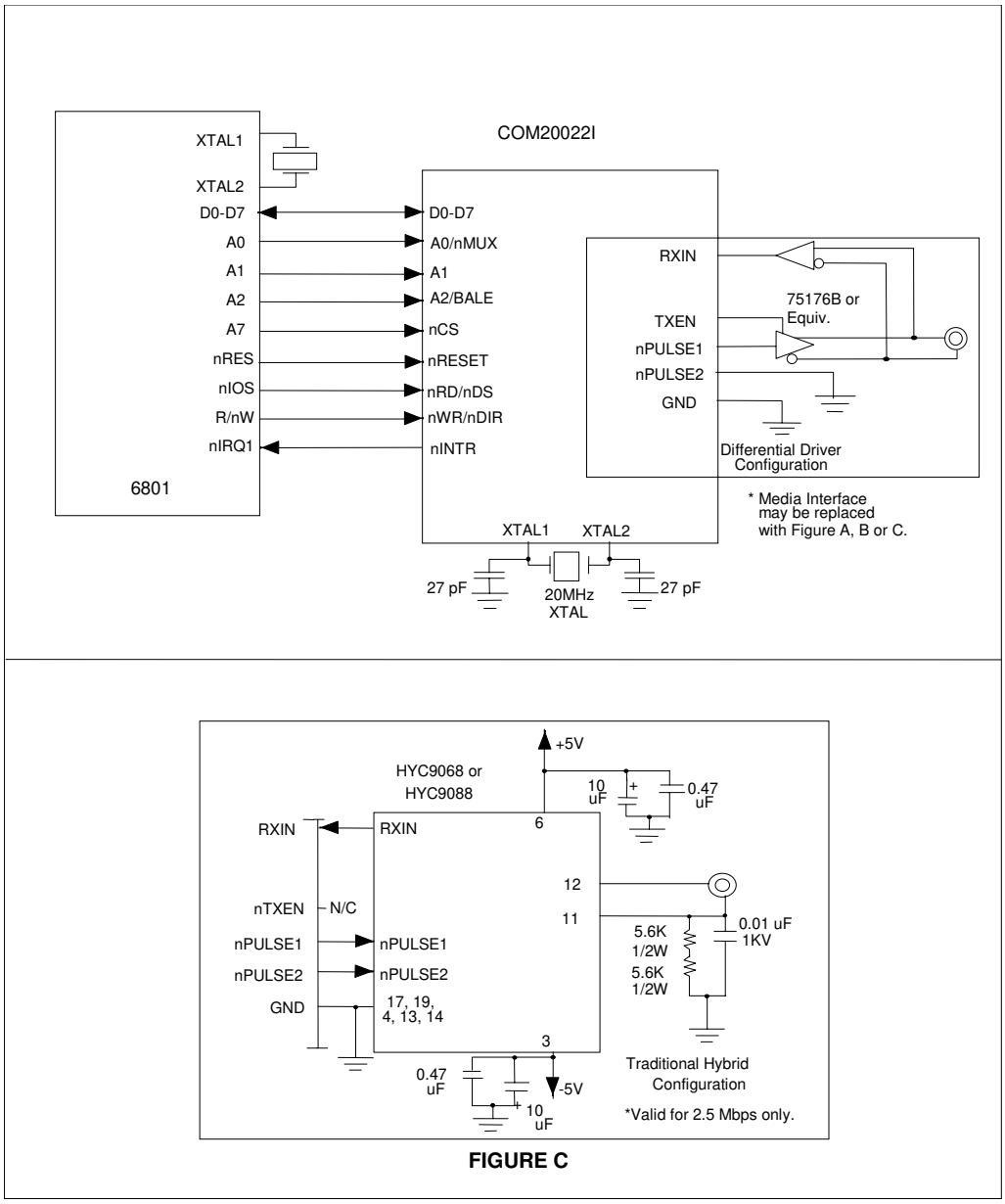


Figure 5.2 - Non-Multiplexed, 6801-Like Bus Interface with RS-485 Interface

5.1.1 Selection of 8/16-Bit Access

The interface to the internal RAM is software selectable as either 8 or 16-bit. This feature is new to the COM20022I. The D15-D8 pins are the upper-byte data bus pins. The nIOCS16 pin is the 16-bit I/O access enable output pin. This pin is active low for a 16-bit RAM access by the CPU (not a DMA access).

The 16-bit access mode is enabled and disabled through the W16 bit located in the Bus Control Register at bit 7. The SWAP bit is used to swap the upper and lower data bytes in 16-bit mode, as shown in the table below. The SWAP bit is located at bit 0 of Address Low Pointer. This location is same as the A0 bit; when 16 bit access is enabled (W16 =1), the A0 bit becomes the SWAP bit.

DETECTED HOST I/F MODE	SWAP BIT (NOTE)	D15-D8 PINS	D7-D0 PINS
Intel 80xx Mode	0	Odd	Even
(RD,WR Mode)	1	Even	Odd
Motorola 68xx Mode	0	Even	Odd
(DIR, DS Mode)	1	Odd	Even

Note: The SWAP bit is undefined after a hardware reset

As shown on the table above, even address data is to/from D7-D0 pins and odd address data is to/from D15-D8 pins when detected host interface mode is Intel 80xx mode and the SWAP bit is not set. The odd address data is to/from the D7-D0 pins and the even address data is to/from D15-D8 pins when detected host interface mode is Motorola 68xx mode and the SWAP bit is not set.

When disabling 16-bit access, the D15-D8 pins are always Hi-Z. The D15-D8 pins are Hi-Z when enabling 16-bit access except for internal RAM access.

W16 bit and SWAP bit influence both the CPU cycle and DMA cycle.

5.1.2 DMA Transfers To And From Internal RAM

The COM20022I supports DMA transfers to and from the internal RAM. This feature is new to the COM20022I. The software selectable 8/16 bit interface to the RAM pertains to DMA transfers. When the W16 bit=0, the microcontroller interface and DMA transfers are both 8-bit data transfers to/from internal RAM. When W16=1 they are both 16-bit data transfers. An 8-bit microcontroller interface and 16-bit DMA data transfer cannot be selected; they must be the same width data transfers to/from internal RAM.

The data swapping operation on 16-bit data transfers also pertains to both.

The DMA interface consists of several added pins. The DREQ pin is the DMA Request output pin. The active polarity of this pin is programmable; the default is active-high. The nDACK pin is the active-low DMA acknowledge input pin. The TC pin is the external terminal count input pin. This pin determines when the nDACK pin is active. It's active polarity is programmable; the default is active-high. The nREFEX pin is the active-low refresh execution pulse input pin.

The DMA interface is controlled by the following bits. The DMAEND bit selects whether or not to mask the interrupt upon finishing the DMA. This bit is located at bit 4 of the Mask register. The DMAEN bit is used to disable/enable the assertion of the DMA Request (DREQ pin) after writing the Address Pointer Low register. This bit is located in the Address Pointer High register, bit 3. The following bits are located in the Bus Control Register: DRPOL, TCPOL and DMAMD[1,0]. The DRQPOL bit sets the active polarity of the DREQ pin; the TCPOL bit sets the active polarity of the TC pin; the DMAMD[1,0] bits select the data transfer mode of the DMA.

The ITCEN/RTRG bit has one of two functions, depending on the DMA transfer mode selected. ITCEN is the Internal Terminal Counter Enable. It is used to select whether the DMA is terminated by external TC

only or by either internal or external TC. ITCEN is for Non-Burst or Burst mode. RTRG selects the re-trigger mode as either external or internal. It is for the two Programmable-Burst modes.

The TC8/RSYN/GTTM bit has one of three functions, depending on the DMA transfer mode selected. TC8 is bit 8 of the Terminal Count. It is the MSB of the 9 bit Terminal Count setting register (the other 8 bits are in the DMA Count register). TC8 is for Non-Burst or Burst mode. RSYN is the Refresh Synchronous bit. This bit is used to select whether the DMA is started immediately or after Refresh execution. GTTM is the Gate Time bit. This bit selects whether the Gate Time is 350nS (min) or 750nS (min). RSYN and GTTM are for the two Programmable-Burst modes. RSYN is for External Re-Trigger mode; GTTM is for internal Re-Trigger mode.

Located in the DMA Count Register, the TC7-TC0 /TIM7-TIM0 /CYC7-CYC0 bits have one of three functions depending on the DMA transfer mode. TC7-TC0 are for non-burst or burst mode. These are the lower 8 bits of the Terminal Count setting register (the MSB is in the Bus Control Register). The TIM7-TIM0 bits are for setting the time of the continuous DMA transfer in Programmable-Burst by Timer mode. The CYC7-CYC0 bits are for setting the time of the continuous DMA transfer in Programmable-Burst by Cycle mode.

5.1.3 DMA Operation

The DMA interface operates in one of four transfer modes: Non-Burst, Burst, Programmable-Burst (by timer) and Programmable-Burst (by cycle counter). The data transfer mode of the DMA is selected through the DMAMD[1,0] bits in the Bus Control register, bits [3,2]. These modes are described below.

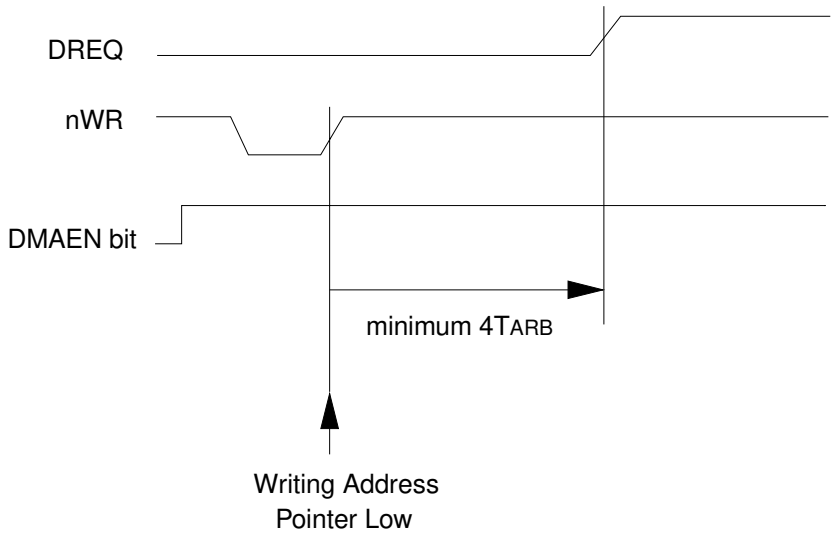
Non-Burst mode is a Single Transfer mode wherein, the DREQ pin is asserted after writing the Address Pointer Low Register when DMAEN=1. Actually, DREQ pin is asserted $4T_{ARB}$ time after writing the Address Pointer Low Register when DMAEN = 1 (refer to Figure 5.3). This mode operates as follows:

1. The nDACK pin is asserted by the DMA Controller detecting the DREQ pin asserted.
2. The DREQ pin is deasserted by the COM20022I detecting the nDACK pin asserted.
3. The nDACK pin is deasserted by the DMA Controller detecting the DREQ pin deasserted after executing the present read or write cycle.
4. The DREQ pin is asserted by the COM20022I detecting the DACK pin deasserted.

Repeat above 4 steps until the TC pin goes active. This mode is called "Cycle steal mode".

Burst mode is a Demand Transfer mode. In this mode, the DREQ pin is asserted after writing the Address Pointer Low Register when DMAEN=1. Actually, DREQ pin is asserted $4T_{ARB}$ time after writing the Address Pointer Low Register when DMAEN = 1 (refer to Figure 5.3). The DACK pin is asserted by the DMA Controller detecting the DREQ pin asserted. The DREQ pin stays asserted until the TC pin goes High.

Programmable-Burst mode is a Demand Transfer mode with temporary DREQ deassertion for a Refresh cycle. The DREQ pin is asserted after writing the Address Pointer Low Register when DMAEN=1 (refer to Figure 5.3). The DACK pin is asserted by the DMA Controller detecting the DREQ pin asserted. If the continuous DMA operation time is longer than the set Refresh period, then DREQ is deasserted. The DREQ is held deasserted after negating nDACK for the Gate time. After the Gate time, the DREQ pin is asserted again. The DREQ pin stays asserted until the TC pin goes High. In Programmable-Burst mode, the gating can be by timer or by cycle counter.



TARB is the ARBITRATION Clock Period. It depends on the TOPR and SLOW-ARB bit. TOPR is the period of operation clock frequency (output of the clock multiplier). It depends on the CKUP1 and CKUP0 bits.

TARB = TOPR @ SLOW-ARB = 0

TARB = 2 TOPR @ SLOW-ARB = 1

Figure 5.3 - DREQ Pin First Assertion Timing for All DMA Modes

As an example of gating by cycle, in an ISA bus system, the Refresh period is 15µS. Continuous transfer by DMA must be less than 15µS to prevent blocking by the Refresh cycle. A DMA cycle of consecutive DMA cycles is approximately 1uS. The DMA overhead time is approximately 2.5µS. The Refresh execution time is 500nS. This computes to 15µS - 2.5µS - 500nS = 12µS or 12 cycles. Therefore the DREQ pin must be negated every 12 cycles. Figure 5.4 illustrates the rough timing of the Programmable-Burst mode DMA transfer.

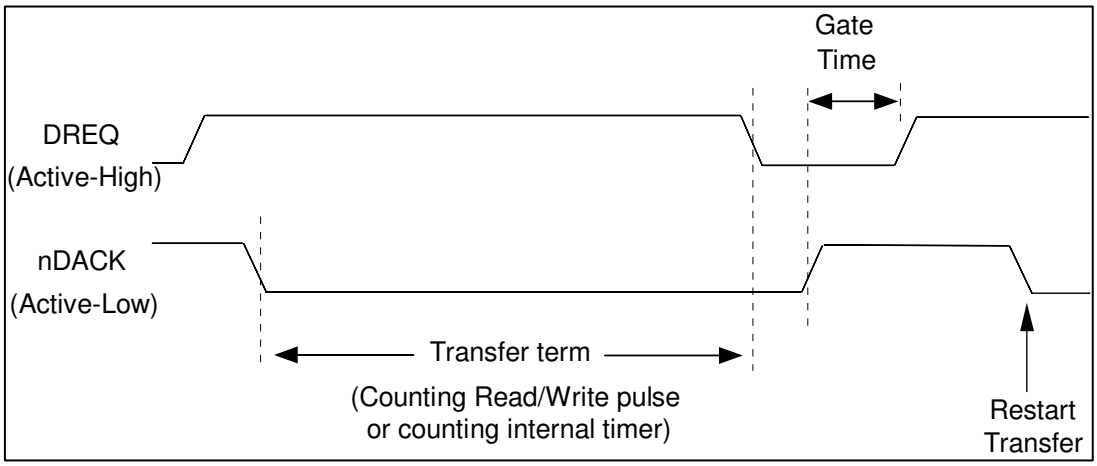


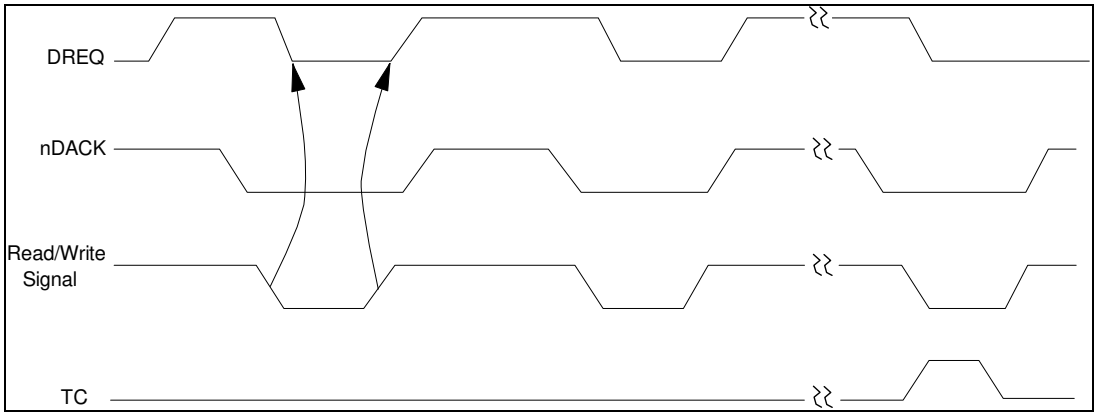
Figure 5.4 - Programmable Burst Mode DMA Transfer (Rough Timing)

The timing of the Non-Burst mode DMA data transfer is found in the Timing Diagrams section of this data sheet. The basic sequence of operation is as follows:

- nDACK becomes active (low) upon DREQ becoming active (high) and catching the host bus (AEN=1).
- DREQ becomes inactive after nDACK and read/write signal become active.
- DREQ becomes active after nDACK or read/write signal becomes inactive.
- DREQ becomes inactive after TC and the read/write signal assert (when nDACK=0). In this case, DREQ doesn't become active again after nDACK becomes inactive.
- nDACK becomes inactive after DREQ=0 and the present cycle finishes.

The following rough timing diagram of the non-burst mode DMA data transfer is included for illustration purposes.

Figure 5.5 - Non-Burst Mode DMA Data Transfer Rough Timing



The timing of the Burst mode DMA data transfer is found in the Timing Diagrams section of this data sheet. The basic sequence of operation is as follows:

- nDACK becomes active (low) upon DREQ becoming active (high) and catching the host bus (AEN= “1”).
- DREQ becomes inactive after TC asserts (when nDACK= “0”). In this case, DREQ doesn't become active again after nDACK becomes inactive.
- nDACK becomes inactive after DREQ= 0 and the present cycle finishes.

The following rough timing diagram of the non-burst mode DMA data transfer is included for illustration purposes.

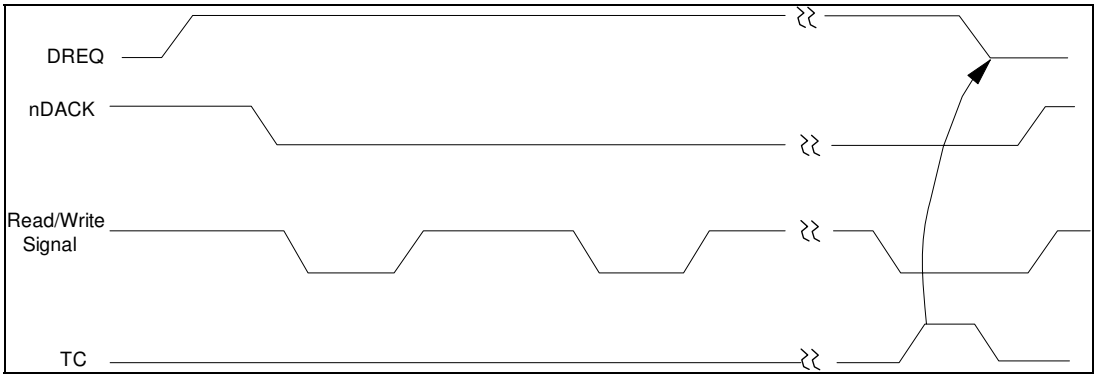


Figure 5.6 - Burst Mode DMA Data Transfer Rough Timing

The following sequences show the data transfer for a DMA read and a DMA write. The transfer of data between system memory and internal RAM functions as a memory to I/O DMA transfer. Since it is treated as an I/O device, the COM20022I has to create the RAM address. Therefore the COM20022I's address pointers must be programmed before starting the DMA transfers.

5.1.4 DMA Data Transfer Sequence (I/O to Memory: Read A Packet)

step1: Set DMA-controller (ex. 8237)
step2: Set DRQPOL, TCPOL, DMAMD1 and DMAMD0 bits
>>Finished DMA SETUP
>>A packet received
step3: Set address, byte count and etc. of DMA controller
step4: Set pointer High and Low (RDDATA=1,AUTOINC=1, DMAEN=0)
step5: Read SID, DID, CP in the received packet
step6: Set DMAEN=1 (RDDATA=1, AUTOINC=1)
step7: DMAEND=1 in Mask REG.
step8: Set pointer = CP
>>DREQ is asserted by step8
>>Interrupt occurs upon finishing DMA

5.1.5 DMA Data Transfer Sequence (Memory to I/O: Write A Packet)

step1: Set DMA-controller (ex. 8237)
step2: Set DRQPOL, TCPOL, DMAMD1 and DMAMD0 bits
>>Finished DMA SETUP
step3: Set address, byte count and etc. of DMA controller
step4: Set pointer High and Low (RDDATA=0,AUTOINC=1, DMAEN = 0)
step5: Write SID,DID,CP in the sending packet
step6: Set DMAEN=1 (RDDATA=0, AUTOINC=1)
step7: DMAEND=1 in Mask REG.
step8: Set pointer = CP
>>DREQ is asserted by step8
>>Interrupt occurs upon finishing DMA transfer
step9: Write Enable Transmit command to command register

5.1.6 High Speed CPU Bus Timing Support

High speed CPU bus support was added to the COM20022I. The reasoning behind this is as follows: With the Host interface in Non-multiplexed Bus mode, I/O address and Chip Select signals must be stable before the read signal is active and remain after the read signal is inactive. But the High Speed CPU bus timing doesn't adhere to these timings. For example, a RISC type single chip microcontroller (like the HITACHI SH-1 series) changes I/O address at the same time as the read signal. Therefore, several external logic ICs would be required to connect to this microcontroller.

In addition, the Diagnostic Status (DIAG) register is cleared automatically by reading itself. The internal DIAG register read signal is generated by decoding the Address (A2-A0), Chip Select (nCS) and Read (nRD) signals. The decoder will generate a noise spike at the above tight timing. The DIAG register is cleared by the spike signal without reading itself. This is unexpected operation. Reading the internal RAM and Next Id Register have the same mechanism as reading the DIAG register.

Therefore, the address decode and host interface mode blocks were modified to fit the above CPU interface to support high speed CPU bus timing. In Intel CPU mode (nRD, nWR mode), 3 bit I/O address (A2-A0) and Chip Select (nCS) are sampled internally by Flip-Flops on the falling edge of the internal delayed nRD signal. The internal real read signal is the more delayed nRD signal. But the rising edge of nRD doesn't delay. By this modification, the internal real address and Chip Select are stable while the internal real read signal is active. Refer to Figure 5.7 on the following page.

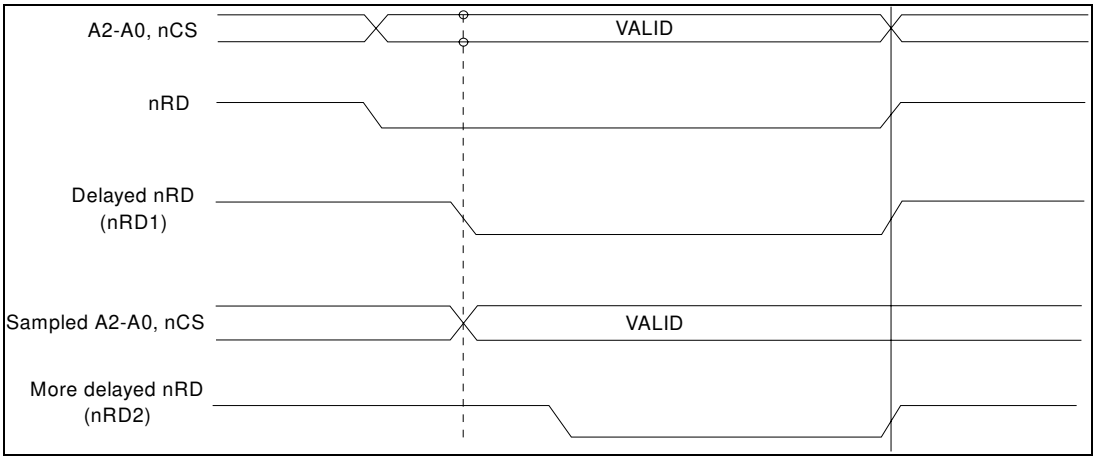


Figure 5.7 - High Speed CPU Bus Timing - Intel CPU Mode

The I/O address and Chip Select signals, which are supplied to the data output logic, are not sampled. Also, the nRD signal is not delayed, because the above sampling and delaying paths decrease the data access time of the read cycle.

The above sampling and delaying signals are supplied to the Read Pulse Generation logic which generates the clearing pulse for the Diagnostic register and generates the starting pulse of the RAM Arbitration. Typical delay time between nRD and nRD1 is around 15nS and between nRD1 and nRD2 is around 10nS.

Longer pulse widths are needed due to these delays on nRD signal. However, the CPU can insert some wait cycles to extend the width without any impact on performance.

The BUSTMG pin is used to support this function. It is used to Enable/Disable the High Speed CPU Read and Write function. It is defined as: BUSTMG = 0, the High Speed CPU Read and Write operations are enabled; BUSTMG = 1, the High Speed CPU Read and Write operations are disabled if the RBUSTMG bit is 0. If BUSTMG = 1 and RBUSTMG = 1, High Speed CPU Read operations are enabled (see definition of RBUSTMG bit below).

The RBUSTMG bit was added to Disable/Enable the High Speed CPU Read function. It is defined as: RBUSTMG=0, Disabled (Default); RBUSTMG=1, Enabled.

In the MOTOROLA CPU mode (DIR, nDS mode), the same modifications apply.

BUSTMG PIN	RBUSTMG BIT	BUS TIMING MODE
0	X	High Speed CPU Read and Write
1	0	Normal Speed CPU Read and Write
1	1	High Speed CPU Read and Normal Speed CPU Write

5.2 Transmission Media Interface

The bottom halves of Figure 5.1 and Figure 5.2 illustrate the COM20022I interface to the transmission media used to connect the node to the network. Table 5.1 lists different types of cable which are suitable for ARCNET applications. The user may interface to the cable of choice in one of three ways: