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Core10GMAC v2.0

Handbook

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Preface

About this Document

This handbook provides details about the Core10GMAC DirectCore module, and how to use it.

Intended Audience

FPGA designers using Libero® System-on-Chip (SoC).

References

Third Party Publications

- IEEE 802.3-2012

Introduction

Overview

The Core10GMAC is designed to the *IEEE 802.3-2012* specification and provides support for 10GBASE-R and 10GBASE-KR interfaces. This configurable core provides the complete MAC and PHY layer when used with a transceiver interface. The physical layer is designed to work seamlessly with the PolarFire transceiver using either the PMA or 64b/66b interface modes.

This handbook provides information on the Core10GMAC and the features it supports. This IP is part of the 10GbE subsystem which is defined in the PolarFire10GbE User Guide (link). This document provides information on how 10GbE can be implemented in PolarFire devices. For more information on the PolarFire transceivers please see the PolarFire Transceiver User Guide (link).

Key Features

The key features are listed below:

- Ethernet MAC / RS / PAUSE
- Link Training
- Auto-Negotiation

Core Version

This handbook is for Core10GMAC version 1.0

Supported Families

This version of Core10GMAC supports the following families:

- PolarFire

Utilization and Performance

Core10GMAC has been implemented in the following Microsemi device families. A summary of the implementation data for Core10GMAC configured for 10GBASE-R & 10GBASE-KR is listed in Table 1 & Table 2.

Table 1 Core10GMAC Utilization for 10GBASE-R Design

	Tiles			Utilization		Performance
Family	Sequential	Combinatorial	Total	Device	Total %	MHz
PolarFire	5209	5490	10699	MPF300TS	4.56	312.5

Note: 10G-BASE-R design connects to Microsemi's SERDES through the Gearbox Interface.

Table 2 Core10GMAC Utilization for 10GBASE-KR Design

	Tiles			Utilization		Performance
Family	Sequential	Combinatorial	Total	Device	Total %	MHz
PolarFire	5795	6596	12391	MPF300TS	4.13	312.5

Note: 10G-BASE-KR design connects to Microsemi's SERDES through the PMA Interface.

Functional Description

When Core10GMAC is configured for 10GBASE-R design the Transceiver 64b/66b Interface is used and it connects directly to the MAC. Supports 32bit or 64bit datapath configurationed. 10GBASE-R consists of onemain block: MAC. The MAC block supports Ethernet MAC RS/PAUSE. The Core10GMAC 10GBASE-R system level diagram is shown in **Error! Reference source not found.**.

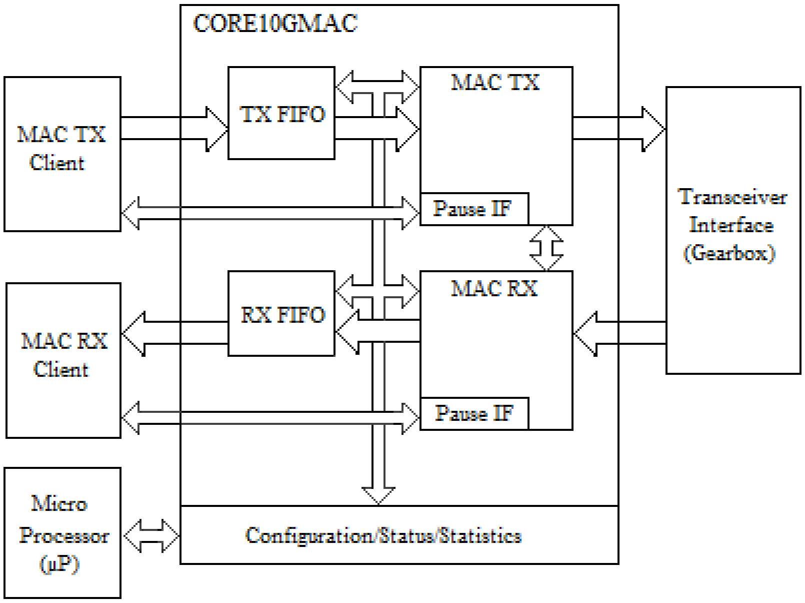

Figure 1 10GBASE-R Sysyem Level Diagram

When Core10GMAC is configured for 10GBASE-KR design the Transceiver PMA Interface is used and it connects to the Ethernet MAC through the PCS Interface. Supposts 32bit or 64bit datapath configuration. For 10GBASE-KR configuration the Link Training & Auto-Negotion Tx/Rx blocks are enable and they can be accessed from the 32-bit APB slave Interface. 10GBASE-KR consists of four main blocks: MAC PCS, Link Training and Auto-Negotion. The MAC PCS block supports Ethernet MAC RS/PAUSE.The Core10GMAC 10GBASE-KR system level diagram is shown in **Error! Reference source not found.**.

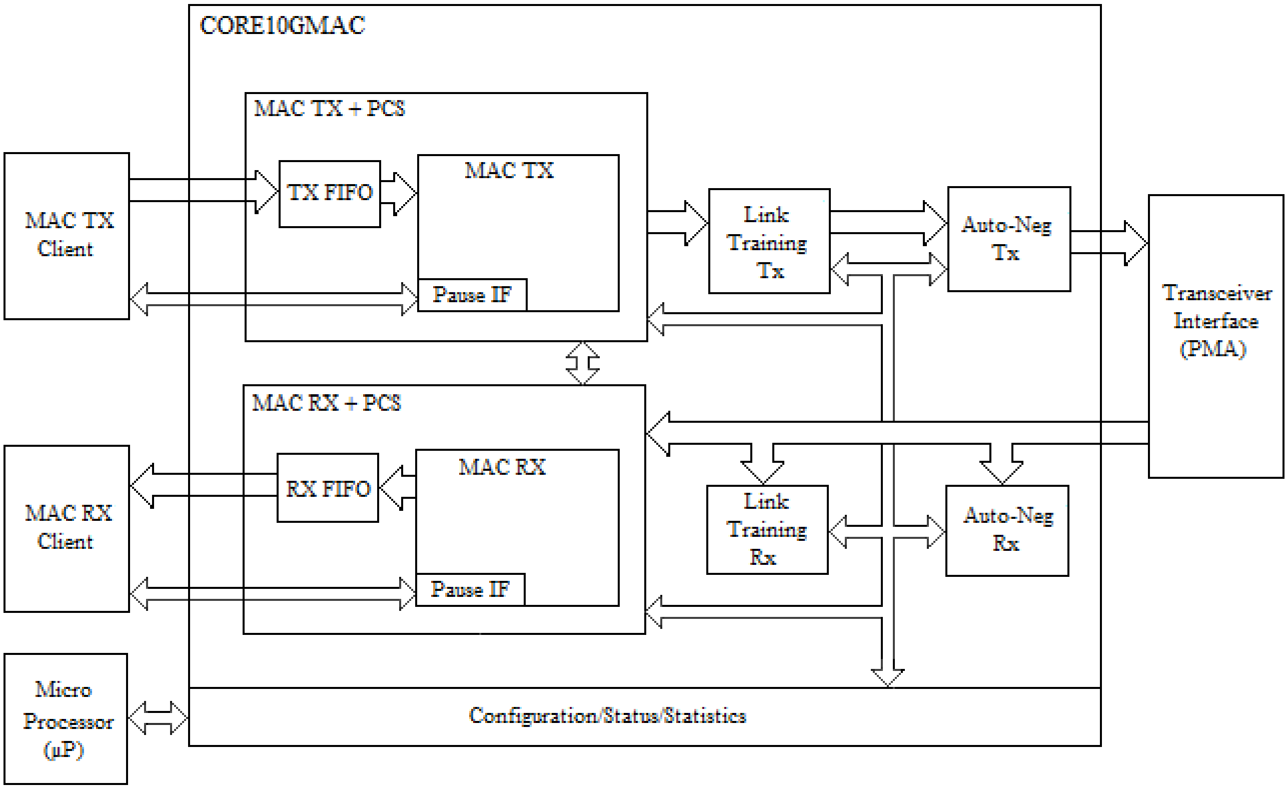

Figure 210GBASE-KR System Level Diagram

Core10GMAC Blocks

Core10GMAC blocks consists of the following:

ETHERNET MAC / RS / PAUSE

The MAC supports the following features:

- Configurable System Interface Bus Width which supports 32bit or 64bit.
- Synchronous or Asynchronous FIFO based transmit interface
- Synchronous or Asynchronous FIFO based receive interface
- FCS insertion on Transmit, and FCS checking on Receive
- Pad insertion on Transmit
- IFG insertion on Transmit, while complying with DIC, can be a fixed, static or dynamic value.
- User programmable IFG and DIC
- Configurable Preamble Size and Contents, normally 2 words for 10GE.
- Pause Frame Insertion on Transmit, and Flagging on receive
- Ethernet statistics on transmit and receive

Physical Coding Sub-layer

The PCS block supports the following features:

- Compliant with IEEE802.3 Clause 49, i.e. PCS Sublayer for 64B/66B.
- 32bit or 64bit datapath connection to the Transceiver Interface.
  Note: Support with IEEE802.3 Clause 36 to be added, i.e. PCS Sublayer for 8B/10B.

Link Training

The Link Training block is compliant with IEEE 802.3-Clause 72 and supports the following features:

- Transmit State-machine: Controls the transmittion of the training frame, which consists of the frame marker, coefficient update, status report and training pattern. The link training procedure is driven using a provided firmware driver which can be run on a local processor and accessed via the APB interface.
  Receive State-machine: Controls the receiption of the training frames by hunting for frame markers, performing bit slip and synchronizing to the frames. The received coefficient update and status report is handled by the firmware driver over the APB interface. The firmware driver will use this information to update transmitter emphasis as instructed by the Link partner.

Auto-Negotiation

The Auto-Negotiation block supports the ability to determine if the link is 10G KR, KX, or KX4. It is compliant with IEEE 802.3-Clause 73 and supports the following features:

- Transmit State-machine
- Receive State-machine
- Arbitration State-machine
- Next Page
- 32-bit APB slave interface to initialize and read results of negotiation.
- Default autonomous operation

A provided firmware driver handles the auto-negotiation process and the initialization and exchange of configuration pages.

Operation

APB Control Registers

Core10GMAC provides a 32-bit APB slave interface and operates with the following register map.

Address Map

Following is the detailed definition of PADDR[9:6] decoding and the explanation of the APB registers.

Address Map:

Address	Name
0x0	Auto-Negotiation Tx Register
0x1	Auto-Negotiation Rx Register
0x2	Link Training Tx Register
0x3	Link Training Rx Register
0x8	Tx Ctlr Register
0x9	Rx Ctlr Register
0xA	MAC Tx Config Register
0xB	MAC Rx Config Register
0xC	MAC Tx Static Register
0xD	MAC Rx Static Register

The following tables describes the APB registers functionality. The offset column represents PADDR[5:2]

Table 3 Auto-Negotiation Tx Register

Offset	Register Name	Bit(s) Name	Bit	Default	Action	Description
0	Main Control	Reset	7	0	RW	Dataplane Reset. APB interface is not influenced by this signal, i.e. apb can continue to read and write registers
			6	-	-	Reserved
			5	-	-	Reserved.
			4	-	-	Reserved
			[3:1]	-	-	Reserved.
		Page Ready	0	0	W1SC	Write a '1' to this bit to inform the transmitter that a new page is ready for transmission in the page registers. The bit will clear when the transmit dataplane has transferred the page to its internal register, and the apb can then start writing a new page.
1	ACK Control	ACK.on	4	0	RWSC	When asserted the transmitter will insert ACK into the outgoing frame for the next ACK.cnt frames, after which time it will send the value in the Page register. The bit clears when the cnt is done. This bit is sampled by the dataplane when a new page is transmitted, i.e. when Page.Ready goes from non-asserted to asserted.
		ACK.cnt	[3:0]	X	RW	The number of frames to send with ACK asserted. Count is minus 1, e.g. writing 1 will send 2 frames with ACK asserted.
2	External Cfg	Link Control	7	0	RW	When asserted all links are disconnected from the MDI
		C49	2	0	RW	Configures the transmitter to run as 10ge
		Pause Port	0	0	RW	Configures the transmitter to run with port pause
3			[3:0]	-	-	Reserved
8	Page[7:0]		-	x	RW	Page byte 0
9	Page[15:8]		-	x	RW	Page byte 1
10	Page[23:16]		-	x	RW	Page byte 2
11	Page[31:24]		-	x	RW	Page byte 3
12	Page[39:32]		-	x	RW	Page byte 4
13	Page[47:40]		-	x	RW	Page byte 5

Table 4 Auto-Negotiation Rx Register

Offset	Register Name	Bit(s) Name	Bit	Default	Action	Description
0	Main Control	Reset	7	0	RW	Dataplane Reset. APB interface is not influenced by this signal, i.e. apb can continue to read and write registers
			6	0	RW	Reserved
		Interrupt Enable	5	0	RW	When asserted high the core will drive the interrupt line when Page.Ready is asserted
			4	-	-	Reserved.
		Lock	3	-	R	Dataplane Lock. The dataplane is locked to a valid Auto-Negotiation (Clause 73) frame. Same as an_receive_idle, except inverted.
		Bit Lock	2		R	Dataplane Bit Lock. Used for debug. It indicates that the incoming frame abides by the manchester rules
		First	1		W	Write a '1' to this bit to force the Auto-Negotiation receiver to restart its matching engine. E.g. if it has already delivered the incoming page, and the page continues to be received, writing '1' to this bit will allow another page to be received. Must set to 0 when not using this functionality.
		Page Ready	0	0	W1C	When asserted high, a page is ready in the page registers. While this signal is high, the dataplane will not make any changes to the Page Registers. Write 1 to clear.
1	ACK Control	ACK on	4	0	RW	The receiver hunts for 3 consequtive matching frames, when this bit is low the ACK is excluded from the match, when it is high it is included in the match and ACK is compare to 1'b1.
2	External Cfg/Status	Link Status	7	0	RW	When asserted the configured link is Good, i.e. PCS Status is asserted
		C49	2	0	RW	Configures the receiver to run as 10ge
		Pause Port	0	0	RW	Configures the receiver to run with port pause
3	Lane Cfg	Lane Number	[3:0]	0	RW	Identifies which lanes is used to receive Clause 73 frames
8	Page[7:0]		-	x	R	Page[0] is the first bit received
9	Page[15:8]		-	x	R	-
10	Page[23:16]		-	x	R	-
11	Page[31:24]		-	x	R	-
12	Page[39:32]		-	x	R	-
13	Page[47:40]		-	x	R	Page[47] is the last bit received

Table 5 Link Training Tx Register

Offset	Register Name	Bit(s) Name	Bit	Default	Action	Description
0	Main Control	Reset	7	0	RW	Dataplane Reset. APB interface is not influenced by this signal, i.e. apb can continue to read and write registers
		Enable	6	0	RW	When asserted high (and external bypass is low), the core dataplane drives the MDI
			5	-	-	Reserved .
		External Bypass	4	-	R	An external element prohibits the core from owning the MDI
			[3:1]	-	-	Reserved .
		Page Ready	0	0	W1SC	Write a '1' to this bit to inform the transmitter that a new page is ready for transmission in the page registers. The bit will clear when the transmit dataplane has transferred the page to its internal registers, and the apb can then start writing a new page.
4	Page[0+:8]		-	x	RW	Corresponds to Status Report Field [7:0]
5	Page[8+:8]		-	x	RW	Corresponds to Status Report Field [15:8]
6	Page[16+:8]		-	x	RW	Corresponds to Coefficient Update Field [7:0]
7	Page[24+:8]		-	x	RW	Corresponds to Coefficient Update Field [15:8]

Table 6 Link Training Rx Register

Offset	Register Name	Bit(s) Name	Bit	Default	Action	Description
0	Main Control	Reset	7	0	RW	Dataplane Reset. APB interface is not influenced by this signal, i.e. apb can continue to read and write registers
		Enable	6	0	RW	Has no function, reserved for future possibilities. If APB wants to turn off the receiver then just hold it in reset.
		Interrupt Enable	5		RW	When asserted high the core will drive the interrupt line when Page.Ready is asserted
			4	-	-	Reserved.
		Lock	3		R	Dataplane Lock. The dataplane is locked to a valid Clause 72 frame
			2	-	-	Reserved.
		First	1		W	Write a 1'b1 to force the receive to restart its matching engine. E.g. if if has already delivered the incoming page, and the page continues to be received, writing this bit will another page to be received. Always reads as zero
		Page Ready	0	0	W1C	When asserted high, a page is ready in the page registers. While this signal is high, the dataplane will not make any changes to the Page Registers. Write 1 to clear.
4	Page[0+:8]		-	-	R	Corresponds to Status Report Field [7:0]

5	Page[8+:8]		-	-	R	Corresponds to Status Report Field [15:8]
6	Page[16+:8]		-	-	R	Corresponds to Coefficient Update Field [7:0]
7	Page[24+:8]		-	-	R	Corresponds to Coefficient Update Field [15:8]

Table 7 Tx Ctrl Register

Offset	Register Name	Bit(s) Name	Bit	Default	Action	Description
0	Main Control	PMA Data	[1:0]	0	RW	PMA Tx Data Select. Used to select the PMA Tx raw data from the Tx clause blocks to transmit. This field is controlled by the Auto Negotiation firmware. 0 = PCS sublayer for 10GE (C49) 1 = PCS sublayer for 1GE (C36) - currently not supported 2 = Auto-Negotiation for back plane (C73) 3 = PMD Sublayer for Link Training (C72)
1	Parameter Read	x	3	0	R	MAC Transmitter Loopback Local Enable, reports the GUI value of CFG_MAC_TX_LPBK_LOCAL_EN.
		x	2	0	R	Reserved.
		x	1	0	-	Reserved
		x	0	0	-	Reports the GUI value of 10GBASE-R or 10GBASE-KR 0 ˉ 10GBASE-R 1 ˉ 10GBASE-KR.

Table 8 Rx Ctrl Register

Offset	Register Name	Bit(s) Name	Bit	Default	Action	Description
0	Status Read	x	1	0	-	Reserved
		pcs49 status	0	0	R	The receive status signal for 10GE. This signal indicates that the receiver is in block lock and not in hi_ber state.
1	Parameter Read	x	3	0	R	MAC Receiver Loopback Local Enable, reports the GUI value of CFG_MAC_RX_LPBK_LOCAL_EN
		x	2	0	-	Reserved
		x	1	0	-	Reserved
		x	0	0	R	Reports the GUI value of 10GBASE-R or 10GBASE-KR 0 ˉ 10GBASE-R 1 ˉ 10GBASE-KR.

Table 9 MAC Tx Config Register

Offset	Register Name	Bit(s) Name	Bit	Default	Action	Description
0	MAC Static	static_mac_tx_ifg_cnt	[13:8]	12	RW	Configure Tx IFG Count. This signal configures the IFG amount. The standard is 12, but the core supports other values. The minimum supported IFG value is 1, and the

						maximum is 48. Values less than 1 will behave as 1, and values above 48 will behave as 48. The signal is static and is used when GUI parameter CFG_MAC_TX_IFG_CNT is set to 0.
		static_mac_tx_ifg_dic_mode_en	4	1	RW	Configure Tx DIC Mode. This signal enables the IFG spacing to be performed with regards to DIC as definite by the IEEE specifications. When the signal is asserted high, DIC is enabled, when it is asserted low DIC is disabled.The signal is static and is used when GUI parameter CFG_MAC_TX_IFG_CNT is set to 0.
		static_mac_tx_preamble_en	3	0	RW	Configures the Tx core to use a customer preamble. The signal is valid when GUI parameter CFG_MAC_TX_PREAMBLE is set to 1.
		static_mac_tx_preamble_wcm1	[2:0]	SWC	RW	Configures the size of the custom preamble, measured in words. The value is `Word Count Minus 1¸, e.g. 3ȟ0 = 1 word of preamble. The signal is valid when GUI parameter CFG_MAC_TX_PREAMBLE is set to 1 and it's initial value is set to parameter SWC.
1	Pause MAC Address 1	pause_tx_mac_addr[31:0]	[31:0]	0	RW	The source MAC address inserted in pause frames. This signal is active when GUI parameter CFG_PAUSE_TX_NEW=1.
2	Pause MAC Address 2	pause_tx_mac_addr[47:32]	[15:0]	0	RW	The source MAC address inserted in pause frames. This signal is active when GUI parameter CFG_PAUSE_TX_NEW is set to 1.
3	Config	cfg_sys_mac_tx_fifo_paf	[20:17]	0	RW	Configure Tx FIFO Programmable Almost Full level. The signal configures the threshold. This signal can be changed dynamically.
		cfg_sys_mac_tx_en	16	1	RW	Configure Tx Enable. This configuration signal enables the MAC TX core to send frames onto the line. When this signal is asserted low, no data-frames will be sent. When the signal is asserted high, data flows normally. The signal is sampled on a packet boundary, i.e. no partial packets will be generated as a consequence of changing the

						assertion of this signal. The signal can be changed dynamically.
		mac_tx_max_pkt_len	[15:0]	0xC000	RW	Configure Maximum Packet Length. This is the maximum configured packet length. A valid packet length is less than or equal to this signal. The signal does not influence the transmit data-path, but it is used by the transmit stats block. When [15:14] == 2'b11 the max length check is disabled. This signal can be changed dynamically.
4	System 1	sys_mac_tx_fcs_ins	8	0	RW	Tx FCS Insert. This signal indicates if the core should insert FCS on all packets
		sys_mac_tx_fcs_err	7	0	RW	Tx FCS Error. This signal indicates if the core should insert an FCS error on the packet.. The FCS error is inserted by xoring the correct FCS with 0x5555_5555.
		sys_mac_tx_fcs_stomp	*6*	*0*	*RW*	*Tx FCS Stomp. This signal indicates if the core should insert an FCS stomp The FCS stomp is inserted by xoring the correct FCS with 0xFFFF_FFFF.*
		sys_mac_tx_ifg_cnt	[5:0]	0	RW	Tx Per Packet IFG. This signal is only used if GUI parameter CFG_MAC_TX_IFG_CNT is greater than 0.
5	System 2	mac_tx_preamble[31:0]	[31:0]	0	RW	Tx Preamble lower 32bit. This field is only used for a custom preamble when GUI parameter CFG_MAC_TX_PREAMBLE and mac_tx_preamble_en bit of MAC Tx Config Register is set to 1. Required when SWC = 1 or 2
6	System 3	mac_tx_preamble[63:32]	[31:0]	0	RW	Tx Preamble upper 32bits.

						This field is only used for a custom preamble when GUI parameter CFG_MAC_TX_PREAMBLE and mac_tx_preamble_en bit of MAC Tx Config Register is set to 1. Note: Only required when SWC = 2

Table 10 MAC Rx Config Register

Offset	Register Name	Bit(s) Name	Bit	Default	Action	Description
0	MAC Static	mac_rx_fcs_remove	3	0	RW	Configure Rx FCS Remove. This bit configurs the core to remove the FCS field. When asserted high the core strips the FCS.
		mac_rx_preamble_wcm1	[2:0]	1	RW	Configures the size of the custom preamble, measured in words. The value is `Word Count Minus 1_, e.g. 3ˇh0 = 1 word of preamble. The signal is active when GUI parameter CFG_MAC_RX_PREAMBLE is set to 1.
1	Pause MAC Address 1	pause_rx_mac_addr[31:0]	[31:0]	0	RW	The destination MAC address used for identification of pause uni-cast frames. This field is active when parameter GUI CFG_PAUSE_RX_PORT or CFG_PAUSE_RX_PFC is set to 1.
2	Pause MAC Address 2	pause_rx_mac_addr[47:32]	[15:0]	0	RW	The destination MAC address used for identification of pause uni-cast frames. This field is active when GUI parameter CFG_PAUSE_RX_PORT or CFG_PAUSE_RX_PFC is set to 1.
3	Config	sys_mac_rx_lpbk_local_en	17	0	RW	Configure Local Loopback Enable. The bit puts the Rx cores in local loopback mode. This has the effect of looping the output from the Tx MAC into the Rx MAC. The bit can be changed dynamically, but errors should be expected during the transition, especially if data is flowing when the bit is changed.
		cfg_sys_mac_rx_en	16	1	RW	Configure Rx Enable. This signal enables the reception of data from the PCS Layer. When asserted data flows normally, when de-asserted the core is effectively disabled. The bit can be changed dynamically.

		sys_mac_rx_max_pkt_len	[15:0]	0xC000	RW	Configure Rx Maximum Packet Length. A valid packet is less than or equal to this value. If a larger packet is received it will be delivered with O_SYS_MAC_RX_ERR and O_SYS_MAC_RX_ERR_W[2] flags. When [15:14] == 2ˇb11 the max length check is disabled. This bit can be changed dynamically.
4	System 1	sys_mac_rx_gfc	0	0	RW	Rx Global Flow Control. When this bit is :1ˇthe core will not read from the receive FIFO, and when the bit is :0ˇthe core reads normally from the FIFO. The response time to changes in this signal is fixed for a given core configuration, but differs between configurations. The response time is between 0 and 5 clock cycles. The signal is normally tied low

Table 11 MAC Tx Static Register

Offset	Register Name	Bit(s) Name	Bit	Default	Action	Description
12	pkt_ok	stats_pkt_ok_cnt	[31:0]	0	R	Packet error free counter
11	pkt_pad	stats_pkt_pad_cnt	[31:0]	0	R	Padded packet counter
10	pkt_vlan	stats_pkt_vlan_cnt	[31:0]	0	R	VLAN packet counter
9	pkt_control	stats_pkt_control_cnt	[31:0]	0	R	Control packet counter
8	pause	stats_pkt_pause_cnt	[31:0]	0	R	Pause packet counter
7	multicast	stats_pkt_multicast_cnt	[31:0]	0	R	Multicast packet counter
6	broadcast	stats_pkt_broadcast_cnt	[31:0]	0	R	Broadcast packet counter
5	err	stats_pkt_err_cnt_cnt	[31:0]	0	R	Errored packet counter
4	err_frm	stats_pkt_err_frm_cnt	[31:0]	0	R	Errored at framing counter
3	err_fcs	stats_pkt_err_fcs_cnt	[31:0]	0	R	Errored at FCS counter
2	err_len_short	stats_pkt_err_len_short_cnt	[31:0]	0	R	Errored at length, with short
1	err_len_check	stats_pkt_err_len_check_cnt	[31:0]	0	R	Errored at length, with check counter
0	err_len_long	stats_pkt_err_len_long_cnt	[31:0]	0	R	Errored at length, with long counter

Table 12 MAC Rx Static Register

Offset	Register Name	Bit(s) Name	Bit	Default	Action	Description
12	pkt_ok	stats_pkt_ok_cnt	[31:0]	0	R	Packet error free counter
11	pkt_pad	stats_pkt_pad_cnt	[31:0]	0	R	Padded packet counter

10	pkt_vlan	stats_pkt_vlan_cnt	[31:0]	0	R	VLAN packet counter
9	pkt_control	stats_pkt_control_cnt	[31:0]	0	R	Control packet counter
8	pause	stats_pkt_pause_cnt	[31:0]	0	R	Pause packet counter
7	multicast	stats_pkt_multicast_cnt	[31:0]	0	R	Multicast packet counter
6	broadcast	stats_pkt_broadcast_cnt	[31:0]	0	R	Broadcast packet counter
5	err	stats_pkt_err_cnt_cnt	[31:0]	0	R	Errored packet counter
4	err_frm	stats_pkt_err_frm_cnt	[31:0]	0	R	Errored at framing counter
3	err_fcs	stats_pkt_err_fcs_cnt	[31:0]	0	R	Errored at FCS counter
2	err_len_short	stats_pkt_err_len_short_cnt	[31:0]	0	R	Errored at length, with short
1	err_len_check	stats_pkt_err_len_check_cnt	[31:0]	0	R	Errored at length, with check counter
0	err_len_long	stats_pkt_err_len_long_cnt	[31:0]	0	R	Errored at length, with long counter

Nomenclature

This section provides detail on a number of specific nomenclatures.

Static Configuration Registers

The core has a number of static configuration registers. These registers are assumed to be constant while the core is running, and the core must be reset after any of these signals change values.

All these signals are defined as static_* and are in the APB control registers. I_SYS_TX_SRESET is used to reset the Tx blocks and I_SYS_RX_SRESET is used to reset the Rx blocks.

Dynamic Configuration Signals

The core has a number of dynamic configuration signals. These signals can be changed at any time.

All these signals are defined as I_CFG_* and cfg_* in the APB control registers.

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Ethernet MAC/RS Overview

The high level architecture of the Ethernet MAC/RS is depicted below;

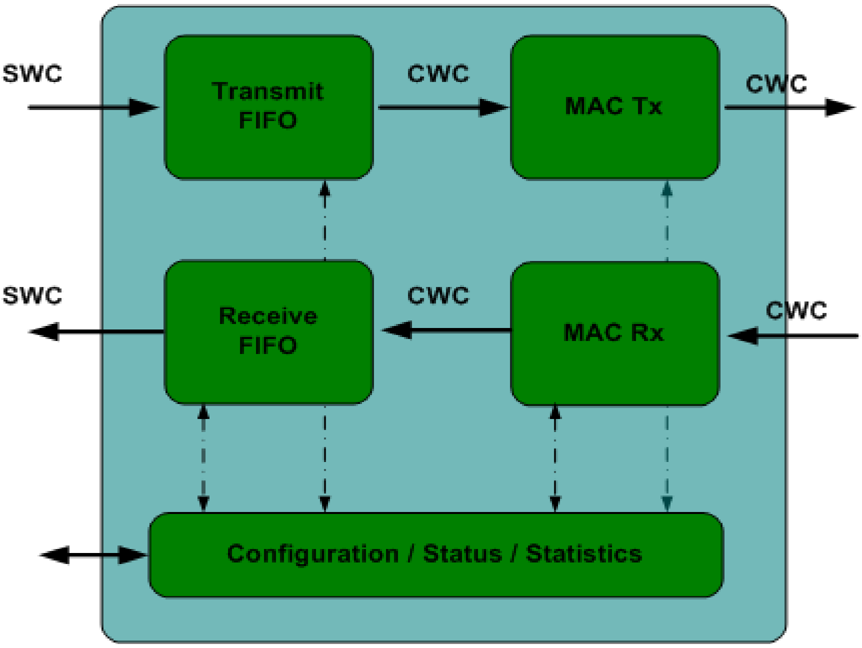

Figure 3 Ethernet TX/Rx FIFO Block Diagram

Transmit FIFO

The Transmit FIFO decouples the user domain from the transmit clock domain. The FIFO is needed by the system to allow the MAC to adhere to the IFG insertion rules. The FIFO is implemented as an asynchronous FIFO. The user side of the FIFO performs bus protocol processing of the data delivered by the user. All badly formatted data will either be dropped, or passed with an error. The error will be transmitted by the MAC as an FCS error.

The Transmit FIFO depth is configurable for depths of 32, 64, 128 or 256.

Receive FIFO

The Receive FIFO decouples the user domain from the receive clock domain. The FIFO is implemented as an asynchronous FIFO. The FIFO is controlled by the core, and the data is delivered as a data-stream to the user side, i.e. the user does not have control of the FIFO flags or read signals.

MAC Tx

The Transmit MAC performs the following;

- Reads data from the Transmit FIFO
- Adds FCS
- Adds Padding
- Adds Preamble
- Handles FIFO underrun and overflow gracefully.
- Abides by IFG
- Inserts Pause Frames
- Drives the statistics block
- Implements the Tx reconciliation layer
- Transmits data to PCS layer

MAC Rx

The Receive MAC performs the following;

- Receives data from PCS layer
- Implements the Rx reconciliation layer
- Recovers the data alignment
- Calculates and Checks FCS
- Extracts the Preamble
- Flags bad frames
- Flags pause Frames
- Drives the statistics block
- Delivers data to the receive FIFO

Statistics

The transmit and receive statistics are made available through a statistics bus and optionally available as APB addressable counters. The user can enable which counters are to be implemented in the core in the configuration GUI sections MAC Tx Counters and MAC Rx Counters

Ethernet Interface

This section expands on the different interfaces, presents timing diagrams and documents the bus conventions.

Tx Dataplane

Tx Dataplane Signal Encoding

The Tx Dataplane Bus Protocol Encoding is listed in the following table. An 8 byte system bus is used as an example.

Signal	Order
I_SYS_MAC_TX_DATA[63]	MSb
I_SYS_ MAC_TX_DATA [63:56]	MSB
I_SYS_ MAC_TX_DATA [7:0]	LSB
I_SYS_ MAC_TX_DATA [0]	LSb

The associated encoding of I_SYS_MAC_TX_BC is listed in the following table;

I_SYS_TX_BC[2:0]	Data
3 h̆0	I_SYS_ MAC_TX_DATA [63:56] valid
3 h̆1	I_SYS_ MAC_TX_DATA [63:48] valid
3 h̆2	I_SYS_ MAC_TX_DATA [63:40] valid
3 h̆3	I_SYS_ MAC_TX_DATA [63:32] valid
3 h̆4	I_SYS_ MAC_TX_DATA [63:24] valid
3 h̆5	I_SYS_ MAC_TX_DATA [63:16] valid
3 h̆6	I_SYS_ MAC_TX_DATA [63:8] valid
3 h̆7	I_SYS_ MAC_TX_DATA [63:0] valid

Tx Dataplane Interface Errors

The tx core performs complete error checks on the delivered data. Three types of errors can be introduced by the user, i.e.

- Protocol error ¯ Errors in the transmit FIFO interface usage.
- FIFO Overflow error - The FIFO becomes full during the tranmittion of a package. This will never happen if the user abides by the FIFO flags, but the core handles the event gracefully.
- FIFO Underrun error - This event happens when the user does not deliver data fast enough.

The Tx machine maintains protocol consistency during any of these events, and flags the associated error event on the associated output signal. The errors will cause the error or loss of one or more packets. The user should drive the interface so as not to introduce any of these errors.

Tx Dataplane Padding

The transmit core can be parameterized to pad or not to pad.