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Core1553BRM v4.2

Handbook

Microsemi

Table of Contents

Introduction

Microsemi Core1553BRM provides a complete MIL-STD-1553B bus controller (BC), remote terminal (RT), or bus monitor terminal (BM or MT). Core1553BRM can be configured to provide all three 1553 functions or any combination thereof. The core is supported in all recent Microsemi Flash, antifuse, and radiation-tolerant product families. A typical system implementation using Core1553BRM is shown in Figure 1.

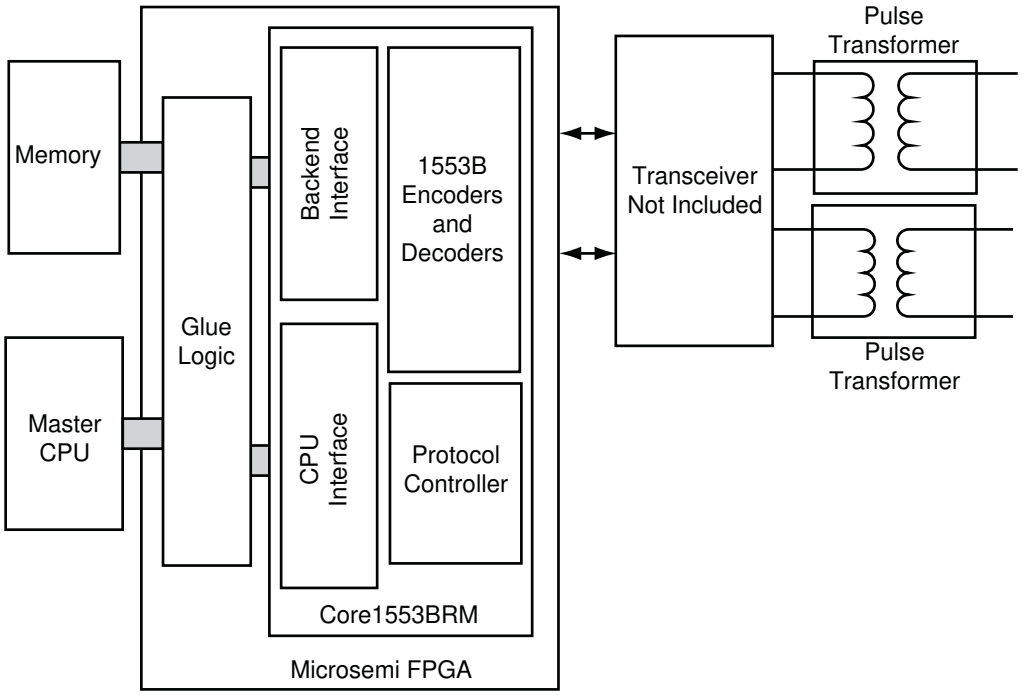


Figure 1 • **Typical Core1553BRM Application**

A typical Core1553BRM system requires connection to an external CPU, used to set up the core registers and initialize the data tables in memory. To facilitate system integration, Core1553BRM is register-compatible with the SuMMIT™ family of 1553B devices from Aeroflex Inc.

The external memory block is used to store the received and transmitted data. This memory can be internal or external to the FPGA, depending upon the family targeted. The core interfaces to the 1553 bus through an external 1553 transceiver and transformer.

Three versions of the core are available:

- An Evaluation version that allows core simulation with Microsemi Libero® System-on-Chip (SoC)/integrated design environment (IDE) or Model*Sim*®
- An Obfuscated version that provides obfuscated RTL and precompiled testbenches
- An RTL version with full access to the source code

Reference Documents

MIL-STD-1553B, Notices I and II

MIL-HDBK-1553A

Enhanced SuMMIT Family Product Handbook, October 1999, UTMC Microelectronic Systems, Inc.

Version

This handbook applies to Core1553BRM v4.2 and later.

Verification and Compliance

Core1553BRM has been fully verified against the RT Validation Test Plan (MIL-HDBK-1553A, "Verification Tests Carried Out" on page 97). This ensures that the 1553B encoders and decoders are fully compliant with the 1553B specification. Core1553BRM is implemented on the Core1553BRM development system using an SmartFusion2 M2S050FG484 device; this can be purchased from Microsemi.

Device Requirements

Core1553BRM can be implemented in multiple Microsemi FPGAs. Table 1 through Table 13 on page 13 give typical utilization figures using standard synthesis tools for the complete core. Note that utilization for Fusion and IGLOO® families is shown in Table 6 on page 9 and Table 9 on page 10. The Core column indicates the core configuration as follows:

- B: Bus Controller enabled
- R: Remote Terminal enabled
- M: Bus Monitor enabled
- 0: RT Legalization registers disabled
- 1: RT Legalization registers implemented in logic tiles
- 2: RT Legalization registers implemented using memory
- E: Actel enhanced functions enabled

Table 1 • **Device Utilization - ProASICplus Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	ProASICplus	6659	1463	8122	0	APA450	66.10%
BRM2E	ProASICplus	5854	1181	7035	2	APA450	57.30%
BRM0E	ProASICplus	5866	1182	7048	0	APA450	57.40%
BR1E	ProASICplus	5625	1268	6893	0	APA450	56.10%
BR2E	ProASICplus	4839	988	5827	2	APA450	47.40%
BR0E	ProASICplus	4812	988	5800	0	APA450	47.20%
RM1E	ProASICplus	5483	1381	6864	0	APA450	55.90%
RM2E	ProASICplus	4844	1101	5945	2	APA450	48.40%
RM0E	ProASICplus	4797	1103	5900	0	APA450	48.00%
BME	ProASICplus	4135	1018	5153	0	APA450	41.90%
BE	ProASICplus	2959	804	3763	0	APA450	30.60%

Table 1 • **Device Utilization - ProASICplus Family (continued)**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
R1	ProASICplus	4348	1168	5516	0	APA450	44.90%
R2	ProASICplus	3632	889	4521	2	APA450	36.80%
R0	ProASICplus	3598	888	4486	0	APA450	36.50%
M	ProASICplus	2347	722	3069	0	APA450	25.00%

Table 2 • **Device Utilization - ProASIC3 Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	ProASIC3	5025	1411	6436	0	A3P600	46.56%
BRM2E	ProASIC3	4498	1155	5653	1	A3P600	40.89%
BRM0E	ProASIC3	4429	1155	5584	0	A3P600	40.39%
BR1E	ProASIC3	4257	1222	5479	0	A3P600	39.63%
BR2E	ProASIC3	3753	966	4719	1	A3P600	34.14%
BR0E	ProASIC3	3660	966	4626	0	A3P600	33.46%
RM1E	ProASIC3	3932	1341	5273	0	A3P600	38.14%
RM2E	ProASIC3	3428	1085	4513	1	A3P600	32.65%
RM0E	ProASIC3	3347	1085	4432	0	A3P600	32.06%
BME	ProASIC3	3029	1000	4029	0	A3P600	29.14%
BE	ProASIC3	2211	793	3004	0	A3P600	21.73%
R1	ProASIC3	3105	1129	4234	0	A3P600	30.63%
R2	ProASIC3	2560	873	3433	1	A3P600	24.83%
R0	ProASIC3	2508	873	3381	0	A3P600	24.46%
M	ProASIC3	1719	714	2433	0	A3P600	17.60%

Table 3 • **Device Utilization - ProASIC3E Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	ProASIC3E	5025	1411	6436	0	A3PE600	46.56%
BRM2E	ProASIC3E	4498	1155	5653	1	A3PE600	40.89%
BRM0E	ProASIC3E	4429	1155	5584	0	A3PE600	40.39%
BR1E	ProASIC3E	4248	1222	5470	0	A3PE600	39.57%
BR2E	ProASIC3E	3753	966	4719	1	A3PE600	34.14%
BR0E	ProASIC3E	3660	966	4626	0	A3PE600	33.46%
RM1E	ProASIC3E	3933	1341	5274	0	A3PE600	38.15%
RM2E	ProASIC3E	3417	1085	4502	1	A3PE600	32.57%
RM0E	ProASIC3E	3350	1085	4435	0	A3PE600	32.08%

Table 3 • **Device Utilization - ProASIC3E Family (continued)**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BME	ProASIC3E	3029	1000	4029	0	A3PE600	29.14%
BE	ProASIC3E	2211	793	3004	0	A3PE600	21.73%
R1	ProASIC3E	3104	1129	4233	0	A3PE600	30.62%
R2	ProASIC3E	2560	873	3433	1	A3PE600	24.83%
R0	ProASIC3E	2488	873	3361	0	A3PE600	24.31%
M	ProASIC3E	1719	714	2433	0	A3PE600	17.60%

Table 4 • **Device Utilization - IGLOO Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	IGLOO	5025	1411	6436	0	AGL600V5	46.56%
BRM2E	IGLOO	4498	1155	5653	1	AGL600V5	40.89%
BRM0E	IGLOO	4429	1155	5584	0	AGL600V5	40.39%
BR1E	IGLOO	4248	1222	5470	0	AGL600V5	39.57%
BR2E	IGLOO	3753	966	4719	1	AGL600V5	34.14%
BR0E	IGLOO	3660	966	4626	0	AGL600V5	33.46%
RM1E	IGLOO	3938	1341	5279	0	AGL600V5	38.19%
RM2E	IGLOO	3421	1085	4506	1	AGL600V5	32.60%
RM0E	IGLOO	3347	1085	4432	0	AGL600V5	32.06%
BME	IGLOO	3029	1000	4029	0	AGL600V5	29.14%
BE	IGLOO	2211	793	3004	0	AGL600V5	21.73%
R1	IGLOO	3104	1129	4233	0	AGL600V5	30.62%
R2	IGLOO	2560	873	3433	1	AGL600V5	24.83%
R0	IGLOO	2488	873	3361	0	AGL600V5	24.31%
M	IGLOO	1719	714	2433	0	AGL600V5	17.60%

Table 5 • **Device Utilization - IGLOOE Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	IGLOOE	5025	1411	6436	0	AGLE600V5	46.56%
BRM2E	IGLOOE	4498	1155	5653	1	AGLE600V5	40.89%
BRM0E	IGLOOE	4429	1155	5584	0	AGLE600V5	40.39%
BR1E	IGLOOE	4248	1222	5470	0	AGLE600V5	39.57%
BR2E	IGLOOE	3753	966	4719	1	AGLE600V5	34.14%
BR0E	IGLOOE	3660	966	4626	0	AGLE600V5	33.46%
RM1E	IGLOOE	3933	1341	5274	0	AGLE600V5	38.15%

Table 5 • **Device Utilization - IGLOOE Family (continued)**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
RM2E	IGLOOE	3417	1085	4502	1	AGLE600V5	32.57%
RM0E	IGLOOE	3350	1085	4435	0	AGLE600V5	32.08%
BME	IGLOOE	3029	1000	4029	0	AGLE600V5	29.14%
BE	IGLOOE	2211	793	3004	0	AGLE600V5	21.73%
R1	IGLOOE	3104	1129	4233	0	AGLE600V5	30.62%
R2	IGLOOE	2560	873	3433	1	AGLE600V5	24.83%
R0	IGLOOE	2488	873	3361	0	AGLE600V5	24.31%
M	IGLOOE	1719	714	2433	0	AGLE600V5	17.60%

Table 6 • **Device Utilization - Fusion Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	Fusion	5025	1411	6436	0	AFS1500	16.76%
BRM2E	Fusion	4498	1155	5653	1	AFS1500	14.72%
BRM0E	Fusion	4429	1155	5584	0	AFS1500	14.54%
BR1E	Fusion	4248	1222	5470	0	AFS1500	14.24%
BR2E	Fusion	3753	966	4719	1	AFS1500	12.29%
BR0E	Fusion	3660	966	4626	0	AFS1500	12.05%
RM1E	Fusion	3933	1341	5274	0	AFS1500	13.73%
RM2E	Fusion	3417	1085	4502	1	AFS1500	11.72%
RM0E	Fusion	3350	1085	4435	0	AFS1500	11.55%
BME	Fusion	3029	1000	4029	0	AFS1500	10.49%
BE	Fusion	2211	793	3004	0	AFS1500	7.82%
R1	Fusion	3104	1129	4233	0	AFS1500	11.02%
R2	Fusion	2560	873	3433	1	AFS1500	8.94%
R0	Fusion	2488	873	3361	0	AFS1500	8.75%
M	Fusion	1719	714	2433	0	AFS1500	6.34%

Table 7 • **Device Utilization - SmartFusion Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	SmartFusion	3560	1118	4678	0	A2F500M3G	40.61%
BRM2E	SmartFusion	3220	845	4065	1	A2F500M3G	35.29%
BRM0E	SmartFusion	2991	841	3832	0	A2F500M3G	33.26%
BR1E	SmartFusion	2989	956	3945	0	A2F500M3G	34.24%
BR2E	SmartFusion	2478	698	3176	1	A2F500M3G	27.57%

Table 7 • **Device Utilization - SmartFusion Family (continued)**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BR0E	SmartFusion	2447	698	3145	0	A2F500M3G	27.30%
RM1E	SmartFusion	2939	1061	4000	0	A2F500M3G	34.72%
RM2E	SmartFusion	2428	790	3218	1	A2F500M3G	27.93%
RM0E	SmartFusion	2394	789	3183	0	A2F500M3G	27.63%
BME	SmartFusion	2204	669	2873	0	A2F500M3G	24.94%
BE	SmartFusion	1657	524	2181	0	A2F500M3G	18.93%
R1	SmartFusion	2331	900	3231	0	A2F500M3G	28.05%
R2	SmartFusion	1844	645	2489	1	A2F500M3G	21.61%
R0	SmartFusion	1769	644	2413	0	A2F500M3G	20.95%
M	SmartFusion	1310	534	1844	0	A2F500M3G	16.01%

Table 8 • **Device Utilization - SmartFusion2 Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	SmartFusion2	3314	1411	4725	0	M2S050T	8.38%
BRM2E	SmartFusion2	3001	1191	4192	1	M2S050T	7.44%
BRM0E	SmartFusion2	2927	1155	4082	0	M2S050T	7.25%
BR1E	SmartFusion2	2750	1222	3972	0	M2S050T	7.05%
BR2E	SmartFusion2	2460	1002	3462	1	M2S050T	6.15%
BR0E	SmartFusion2	2411	966	3377	0	M2S050T	5.99%
RM1E	SmartFusion2	2698	1341	4039	0	M2S050T	7.17%
RM2E	SmartFusion2	2363	1121	3484	1	M2S050T	6.18%
RM0E	SmartFusion2	2280	1085	3365	0	M2S050T	5.98%
BME	SmartFusion2	2002	1000	3002	0	M2S050T	5.32%
BE	SmartFusion2	1461	793	2254	0	M2S050T	4.00%
R1	SmartFusion2	2111	1129	3240	0	M2S050T	5.75%
R2	SmartFusion2	1789	909	2698	1	M2S050T	4.79%
R0	SmartFusion2	1700	873	2573	0	M2S050T	4.57%
M	SmartFusion2	1285	749	2034	0	M2S050T	3.61%

Table 9 • **Device Utilization - IGLOO2 Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	IGLOO2	3314	1411	4725	0	M2GL050T	8.38%
BRM2E	IGLOO2	3001	1191	4192	1	M2GL050T	7.44%
BRM0E	IGLOO2	2927	1155	4082	0	M2GL050T	7.25%

Table 9 • **Device Utilization - IGLOO2 Family (continued)**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BR1E	IGLOO2	2750	1222	3972	0	M2GL050T	7.05%
BR2E	IGLOO2	2460	1002	3462	1	M2GL050T	6.15%
BR0E	IGLOO2	2411	966	3377	0	M2GL050T	5.99%
RM1E	IGLOO2	2698	1341	4039	0	M2GL050T	7.17%
RM2E	IGLOO2	2363	1121	3484	1	M2GL050T	6.18%
RM0E	IGLOO2	2280	1085	3365	0	M2GL050T	5.98%
BME	IGLOO2	2002	1000	3002	0	M2GL050T	5.32%
BE	IGLOO2	1461	793	2254	0	M2GL050T	4.00%
R1	IGLOO2	2111	1129	3240	0	M2GL050T	5.75%
R2	IGLOO2	1789	909	2698	1	M2GL050T	4.79%
R0	IGLOO2	1700	873	2573	0	M2GL050T	4.57%
M	IGLOO2	1285	749	2034	0	M2GL050T	3.61%

Table 10 • **Device Utilization - Axcelerator Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	Axcelerator	2996	1444	4440	0	AX500	55.06%
BRM2E	Axcelerator	2783	1162	3945	1	AX500	48.92%
BRM0E	Axcelerator	2768	1162	3930	0	AX500	48.74%
BR1E	Axcelerator	2561	1245	3806	0	AX500	47.20%
BR2E	Axcelerator	2348	967	3315	1	AX500	41.11%
BR0E	Axcelerator	2308	967	3275	0	AX500	40.61%
RM1E	Axcelerator	2434	1371	3805	0	AX500	47.19%
RM2E	Axcelerator	2239	1087	3326	1	AX500	41.25%
RM0E	Axcelerator	2204	1085	3289	0	AX500	40.79%
BME	Axcelerator	1939	1001	2940	0	AX500	36.46%
BE	Axcelerator	1452	796	2248	0	AX500	27.88%
R1	Axcelerator	1928	1144	3072	0	AX500	38.10%
R2	Axcelerator	1710	875	2585	1	AX500	32.06%
R0	Axcelerator	1696	875	2571	0	AX500	31.88%
M	Axcelerator	1163	714	1877	0	AX500	23.28%

Table 11 • **Device Utilization – RT Axcelerator Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	RTAX-S	3004	1443	4447	0	RTAX1000S	24.51%
BRM2E	RTAX-S	2794	1161	3955	1	RTAX1000S	21.80%
BRM0E	RTAX-S	2775	1161	3936	0	RTAX1000S	21.69%
BR1E	RTAX-S	2548	1246	3794	0	RTAX1000S	20.91%
BR2E	RTAX-S	2339	966	3305	1	RTAX1000S	18.22%
BR0E	RTAX-S	2300	968	3268	0	RTAX1000S	18.01%
RM1E	RTAX-S	2428	1371	3799	0	RTAX1000S	20.94%
RM2E	RTAX-S	2255	1085	3340	1	RTAX1000S	18.41%
RM0E	RTAX-S	2204	1085	3289	0	RTAX1000S	18.13%
BME	RTAX-S	1949	1001	2950	0	RTAX1000S	16.26%
BE	RTAX-S	1453	795	2248	0	RTAX1000S	12.39%
R1	RTAX-S	1924	1144	3068	0	RTAX1000S	16.91%
R2	RTAX-S	1705	875	2580	1	RTAX1000S	14.22%
R0	RTAX-S	1688	875	2563	0	RTAX1000S	14.13%
M	RTAX-S	1167	714	1881	0	RTAX1000S	10.37%

Table 12 • **Device Utilization – SXA Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	SX-A	3345	1482	4827	0	A54SX72A	79.97%
BRM2E	SX-A	Not Supported					
BRM0E	SX-A	2935	1200	4135	0	A54SX72A	68.51%
BR1E	SX-A	2769	1270	4039	0	A54SX72A	66.92%
BR2E	SX-A	Not Supported					
BR0E	SX-A	2397	994	3391	0	A54SX72A	56.18%
RM1E	SX-A	2627	1386	4013	0	A54SX72A	66.48%
RM2E	SX-A	Not Supported					
RM0E	SX-A	2334	1102	3436	0	A54SX72A	56.93%
BME	SX-A	2003	1021	3024	0	A54SX72A	50.10%
BE	SX-A	1505	803	2308	0	A54SX72A	38.24%
R1	SX-A	2095	1171	3266	0	A54SX72A	54.11%
R2	SX-A	Not Supported					
R0	SX-A	1714	885	2599	0	A54SX72A	43.06%
M	SX-A	1242	748	1990	0	A54SX72A	32.97%

Table 13 • **Device Utilization – RT SXA Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	RTSX-S	3327	1478	4805	0	RT54SX72S	79.61%
BRM2E	RTSX-S	Not Supported					
BRM0E	RTSX-S	2966	1182	4148	0	RT54SX72S	68.72%
BR1E	RTSX-S	2768	1281	4049	0	RT54SX72S	67.08%
BR2E	RTSX-S	Not Supported					
BR0E	RTSX-S	2417	1000	3417	0	RT54SX72S	56.61%
RM1E	RTSX-S	2654	1381	4035	0	RT54SX72S	66.85%
RM2E	RTSX-S	Not Supported					
RM0E	RTSX-S	2402	1110	3512	0	RT54SX72S	58.18%
BME	RTSX-S	2019	1022	3041	0	RT54SX72S	50.38%
BE	RTSX-S	1525	802	2327	0	RT54SX72S	38.55%
R1	RTSX-S	2072	1171	3243	0	RT54SX72S	53.73%
R2	RTSX-S	Not Supported					
R0	RTSX-S	1743	888	2631	0	RT54SX72S	43.59%
M	RTSX-S	1292	760	2052	0	RT54SX72S	34.00%

Table 14 • **Device Utilization – RTG4 Family**

Core	Family	Cells or Tiles			Memory Blocks	Device	UTIL
		Combinational	Sequential	Total			
BRM1E	RTG4	3642	1412	5054	0	RT4G150	3.33%
BRM2E	RTG4	3293	1192	4485	1	RT4G150	2.95%
BRM0E	RTG4	3256	1156	4412	0	RT4G150	2.91%
BR1E	RTG4	2998	1205	4203	0	RT4G150	2.77%
BR2E	RTG4	2639	985	3624	1	RT4G150	2.39%
BR0E	RTG4	2561	949	3510	0	RT4G150	2.31%
RM1E	RTG4	2988	1342	4330	0	RT4G150	2.85%
RM2E	RTG4	2570	1122	3692	1	RT4G150	2.43%
RM0E	RTG4	2508	1086	3594	0	RT4G150	2.37%
BME	RTG4	2286	1008	3294	0	RT4G150	2.17%
BE	RTG4	1605	776	2381	0	RT4G150	1.57%
R1	RTG4	2423	1112	3535	0	RT4G150	2.33%
R2	RTG4	1947	892	2839	1	RT4G150	1.87%
R0	RTG4	1850	856	2706	0	RT4G150	1.78%
M	RTG4	1472	757	2229	0	RT4G150	1.47%

The Core1553BRM clock rate can be programmed to be 12, 16, 20, or 24 MHz. All the Microsemi families listed above easily meet the required performance.

Core1553BRM I/O requirements depend on the system requirements and external interfaces. If the core and memory blocks are implemented within the FPGA and the CPU interface has a bidirectional data bus, approximately 67 I/O pins are required. If external memory is used with a bidirectional data bus, the number of I/O pins increases to approximately 110.

External Components

There are three external components required for proper operation of Core1553BRM:

- Memory: Between 1 kbyte and 128 kbytes (16 bits wide) of internal FPGA memory or external memory used for data storage
- Transceivers: Standard 1553B transceiver
- CPU: Used to control the core

The requirements for these three blocks are discussed in "Implementation Hints" on page 90.

MIL-STD-1553B Bus Overview

The MIL-STD-1553B bus is a differential serial bus used in military and space equipment. It comprises multiple redundant bus connections and communicates at 1 Mbps.

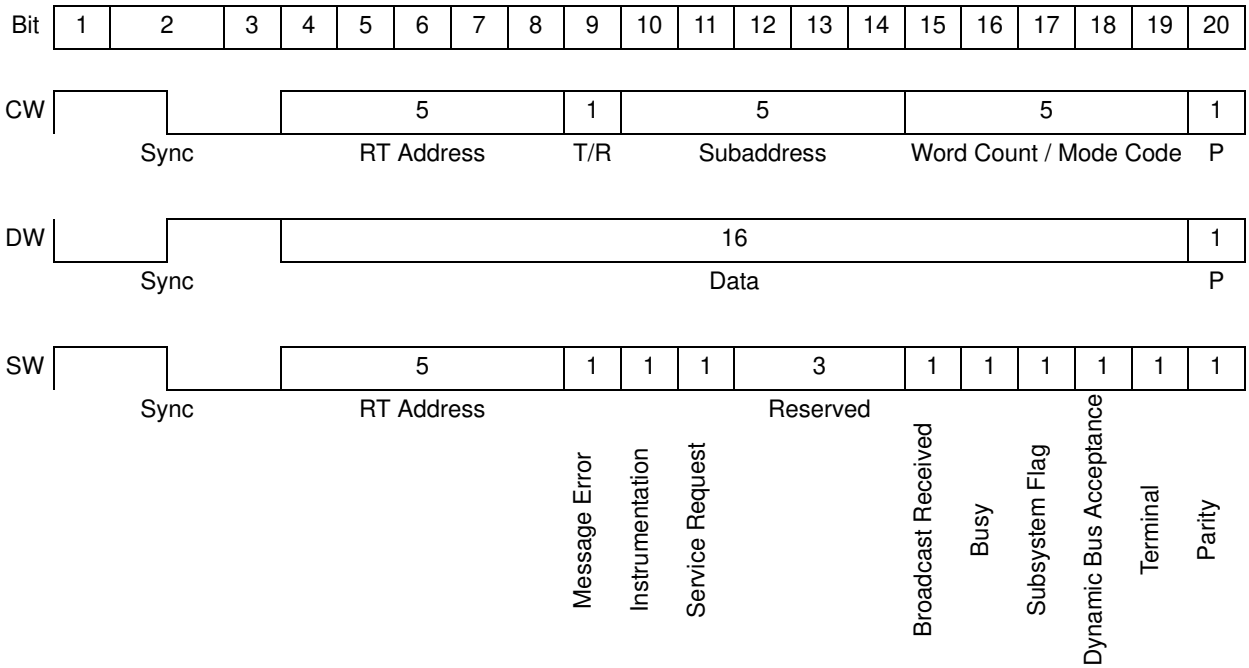
The bus has a single active BC and up to 31 RTs. The BC manages all data transfers on the bus using the command and status protocol. The BC initiates every transfer by sending a command word, and data if required. The selected RT will respond with a status word, and data if required.

The 1553B command word contains a 5-bit RT address, transmit or receive bit, 5-bit subaddress and 5-bit word count. This allows for up to 32 RTs on the bus. Normally, only 31 RTs can be connected to the bus, since RT address 31 is used to indicate a broadcast transfer. A broadcast transfer is one where all RTs accept the following data. Each RT has 30 subaddresses reserved for data transfers. The other two subaddresses (0 and 31) are reserved for mode codes used for bus control functions. Data transfers contain up to thirty-two 16-bit data words. Mode code command words are used for bus control functions such as synchronization.

Word Formats

There are only three types of words in a 1553B message: a command word (CW), a data word (DW), and a status word (SW). Each word consists of a 3-bit sync pattern, 16 bits of data, and a parity bit, making up the 20-bit word. The word formats are given in Figure 2.

Figure 2 • **1553B Word Formats**



Message Types

The 1553B bus supports 10 message transfer types, allowing basic point-to-point, broadcast, and BC-to-RT data transfers, mode code messages, and direct RT-to-RT messages. Figure 3 shows the message formats.

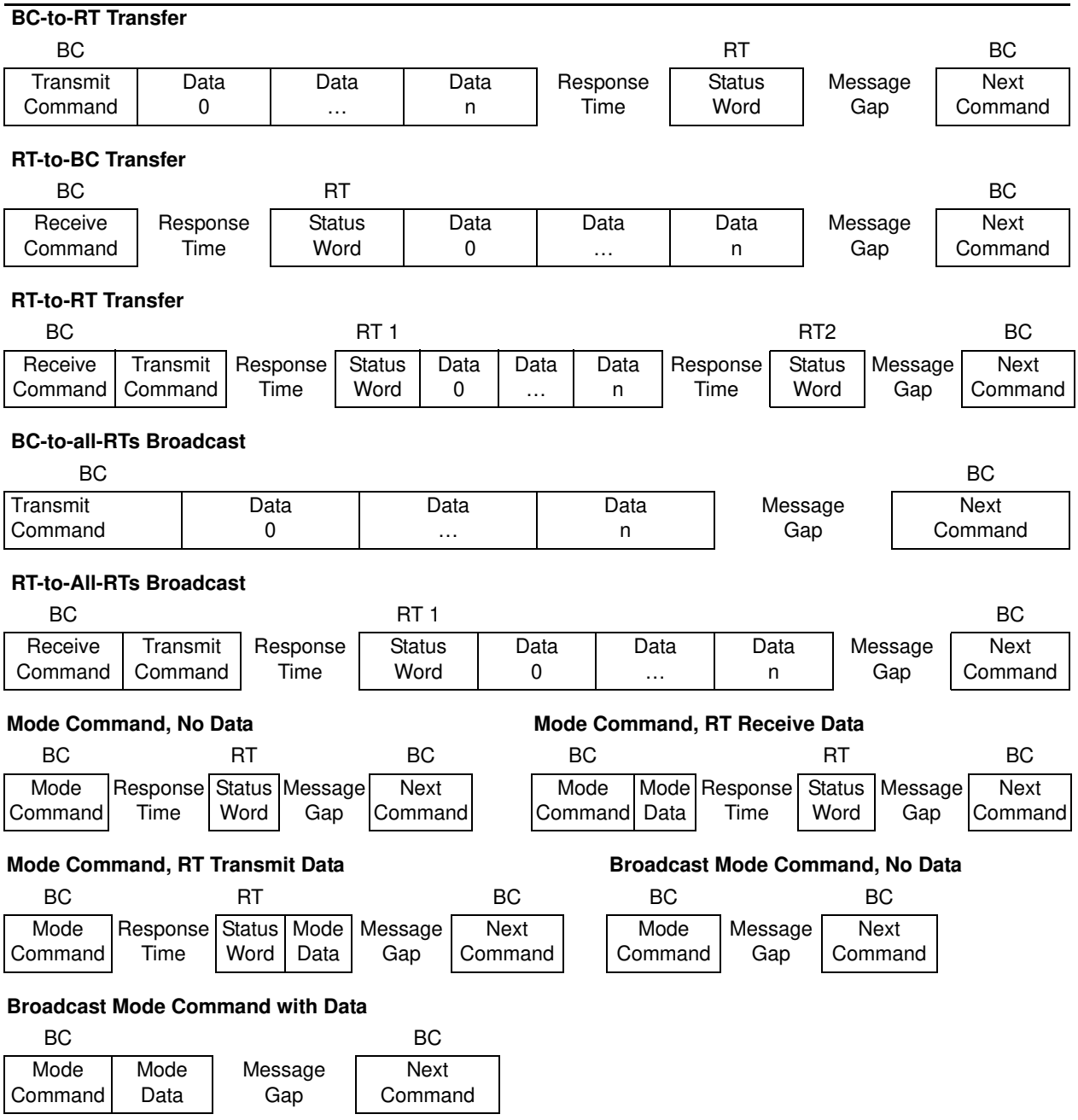


Figure 3 • **1553B Message Formats**

1 – Functional Description

The core consists of six main blocks: a 1553 encoder, 1553 decoders, a protocol controller block, a CPU interface, a command word legality interface, and a backend interface (Figure 1-1).

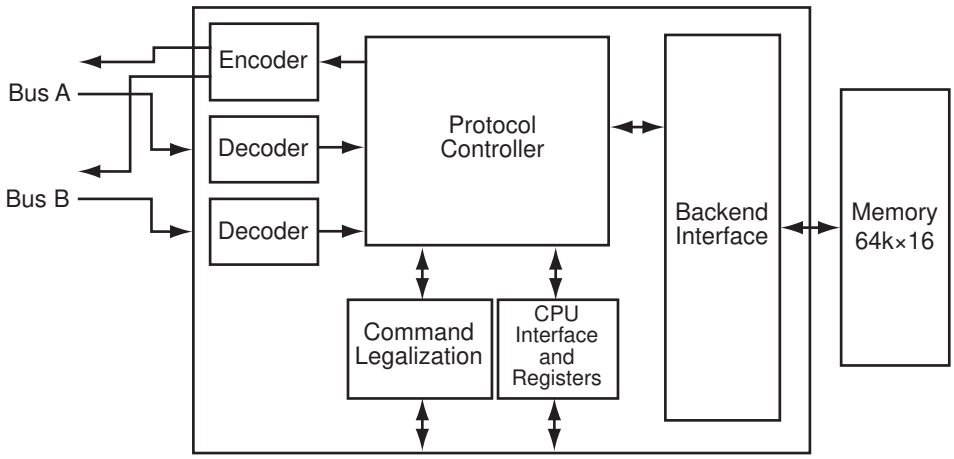


Figure 1-1 • **Core1553BRM Block Diagram (all optional blocks included)**

The core can be configured to provide all three functions—BC, RT, and MT—or any combination of the three. All core variations use all six blocks except for the command legalization interface, which is only required in RT functions that implement the RT legalization function externally.

A single 1553 encoder takes each word to be transmitted and serializes it using Manchester encoding. The encoder also includes loopback fail logic and independent logic to prevent Core1553BRM from transmitting for longer than the allowed period. The loopback logic monitors the received data and verifies that the core has correctly received every word that it transmits. The output of the encoder is gated with the bus enable signals to select which busses the core should be transmitting on.

Two decoders take the serial Manchester received data from each bus and extract the received data words. The decoder requires a 12, 16, 20, or 24 MHz clock to extract the data and clock from the serial stream.

The decoder contains a digital phase-locked loop (PLL) that generates a recovery clock used to sample the incoming serial data. The data is then deserialized and the 16-bit word decoded. The decoder detects whether a command, status, or data word has been received and checks that no Manchester encoding or parity errors have occurred in the word.

The protocol controller block handles all the message sequencing and error recovery for all three operating modes—BC, RT, and BM. This is a complex state machine that processes messages based on the message tables set up in memory, or reacts to incoming command words. The protocol controller implementation varies depending on which functions are implemented.

The CPU interface allows the system CPU to access the control registers within the core. It also allows the CPU to directly access the memory connected to the backend interface; this can simplify the system design. The core includes thirty-three 16-bit registers. Of the 33 registers, 17 are used for control functions and 16 for RT command legalization. The RT command legalization registers can be omitted from the core, reducing device utilization.

The command legality interface allows an external circuit to legalize command words that the remote terminal will respond to. The external legality checker allows a very small piece of logic to legalize command words down to word-count level, rather than using the sixteen 16-bit command legality registers within the CPU interface.

The memory interface for Core1553BRM allows a simple connection to a memory device. It can be configured to connect to either synchronous or asynchronous memory devices. This allows the core to be connected to synchronous logic or memory within the FPGA or to external memory blocks. The interface supports a standard bus request and grant protocol, and provides a WAIT input, allowing the core to interface to slow memory devices. This allows the core to share system memory rather than have its own dedicated memory block.

Registers

Core1553BRM contains thirty-three 16-bit registers (Table 1-1). One of these is used to enable enhanced Core1553BRM functions. The remaining 32 registers are used to control the core. The Control and Operation registers are used to allow a CPU to set the core operating mode; BC, RT, MT, or combined RT and MT. The function of the other registers varies depending on the operating mode.

Table 1-1 • **Registers Address Map**

Address	Name
00	Control
01	Operation and Status
02	Current Command
03	Interrupt Mask
04	Pending Interrupt
05	Interrupt Pointer
06	Built-In Test (BIT) Register
07	Time Tag
08	Descriptor Pointer
09	1553B Status Word
10	Initialization Count
11	Monitor Command Pointer
12	Monitor Data Pointer
13	Monitor Block Count
14	Monitor Filter A
15	Monitor Filter B
16–31	RT Command Legalization
32	Enhanced Features

Core Operation

Core1553BRM is designed to be software-compatible with existing 1553B solutions.

It supports the following features:

- Interrupt logs
- Programmable message timeouts
- Circular buffer operation

It does not support the following features:

- Buffer mode operation
- Built-in test functions, although the BIT register and the transmit BIT mode code are supported.
- Auto-initialization of internal registers and memory

Loopback Tests

Core1553BRM performs loopback testing on all of its transmissions; the transmit data is fed back into the receiver, and each transmitted word is compared to the original. If an error is detected, the transmitter shutdown bit is set in one of the core registers. The core also supports internal data loopback that may be used for self-testing without generating any 1553B transmissions.

Bus Transceivers

Core1553BRM needs a 1553B transceiver to drive the 1553B bus. Core1553BRM is designed to interface directly to common MIL-STD-1553 transceivers, such as Aeroflex ACT4453. When using ProASIC^{PLUS}, RTAX-S, or Axcelerator FPGAs, level translators are required to connect the 5 V outputs of the 1553B transceivers to the 3.3 V inputs of the FPGA.

In addition to the transceiver, a pulse transformer is required for interfacing to the 1553B bus. Figure 1-3 shows the connections required from Core1553BRM to the transceivers and then to the bus via the pulse transformers.

Typical System and Memory Requirements

Core1553BRM requires a master CPU to set up the registers and data tables. The CPU needs to able to access the internal core registers as well as the memory. Core1553BRM can be configured in two ways, with CPU shared memory and with its own memory (Figure 1-3).

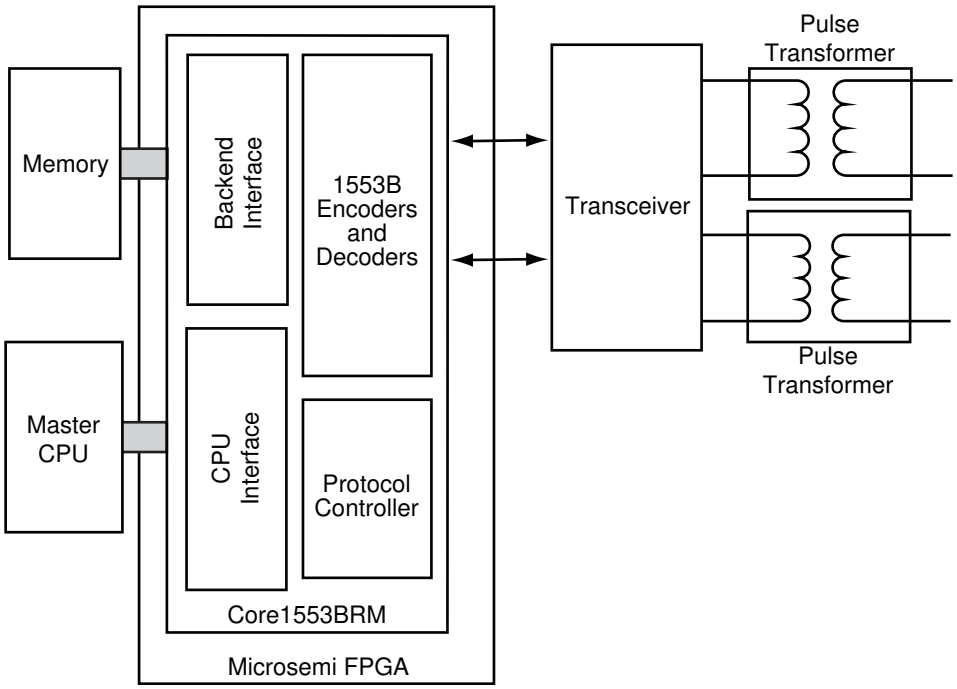


Figure 1-2 • **Core1553BRM with Its Own Memory**

When configured with its own memory, only the CPU port needs to be connected to the CPU. The CPU accesses the backend memory via Core1553BRM. This configuration also supports using internal FPGA memory connected to the core and removes the need for external bus arbitration on the CPU bus.

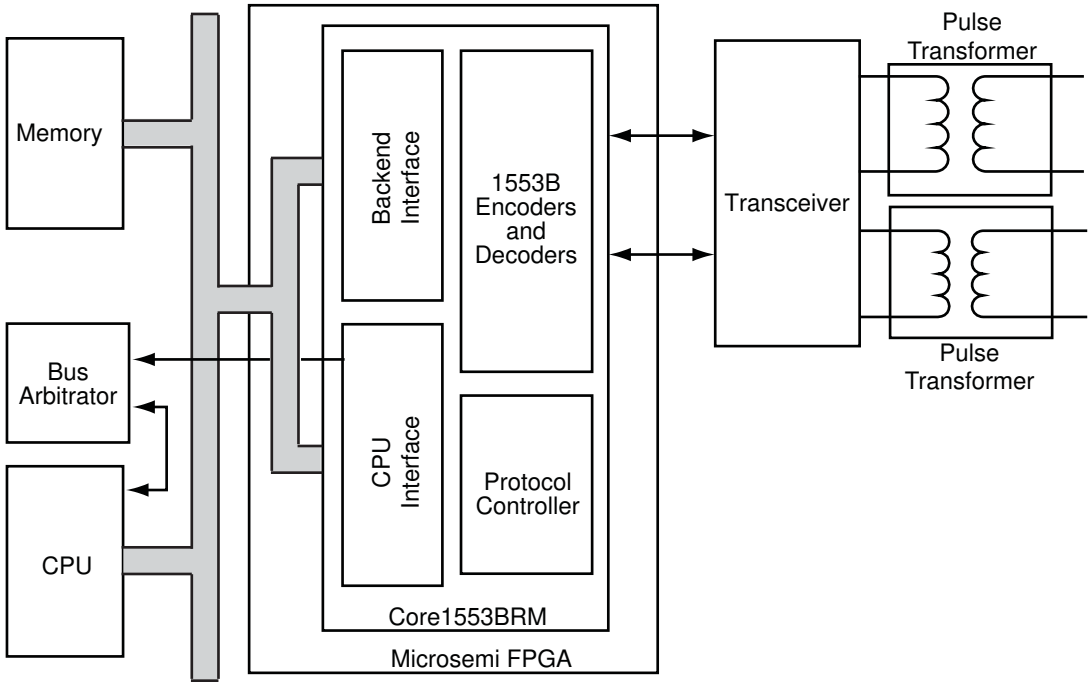


Figure 1-3 • **Core1553BRM Using Shared Memory**

Alternatively, the core can share CPU memory. In this case, both the backend memory and CPU interfaces are connected to the CPU bus. The core provides control lines that allow the memory and CPU interfaces to share the same top-level I/O pins. When in this configuration and the core needs to read or write the memory, it uses the MEMREQn, MEMGNTn, and MEMACCn signals to arbitrate for the CPU bus before completing the cycle.

Core1553BRM is compatible with legacy 1553B devices that use a single address and data bus when using a shared CPU and memory bus. The core also includes a wrapper file with a functional pinout that matches these legacy devices, allowing direct replacement.

For both shared and own memory systems, the core supports up to 128 kbytes of memory. The amount of memory required depends on the system requirements. A complete BC, RT, and MT could be created with only 1 kbyte of memory. Typical systems will have at least 4 kbytes of memory.

2 – Tool Flows

Licenses

Core1553BRM is licensed in three ways; depending on your license, tool flow functionality may be limited.

Evaluation

Precompiled simulation libraries are provided, allowing the core to be instantiated in SmartDesign and simulated within Microsemi Libero IDE/SoC, as described in the "SmartDesign" section. The design may not be synthesized, as source code is not provided.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero IDE/SoC. The RTL code for the core is obfuscated,[1] and the some of the testbench source files are not provided. They are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

Core1553BRM is available for download to the SmartDesign IP Catalog, via the Libero IDE/SoC web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, refer to the Libero IDE/SoC online help.

1. *Obfuscated means the RTL source files have had formatting and comments removed, and all instance and net names have been replaced with random character sequences.*

The core can be configured using the configuration GUI within SmartDesign, as shown in Figure 2-1. The "Parameters on Core1553BRM" section on page 24 describes the function of each of the parameters shown in Figure 2-1.

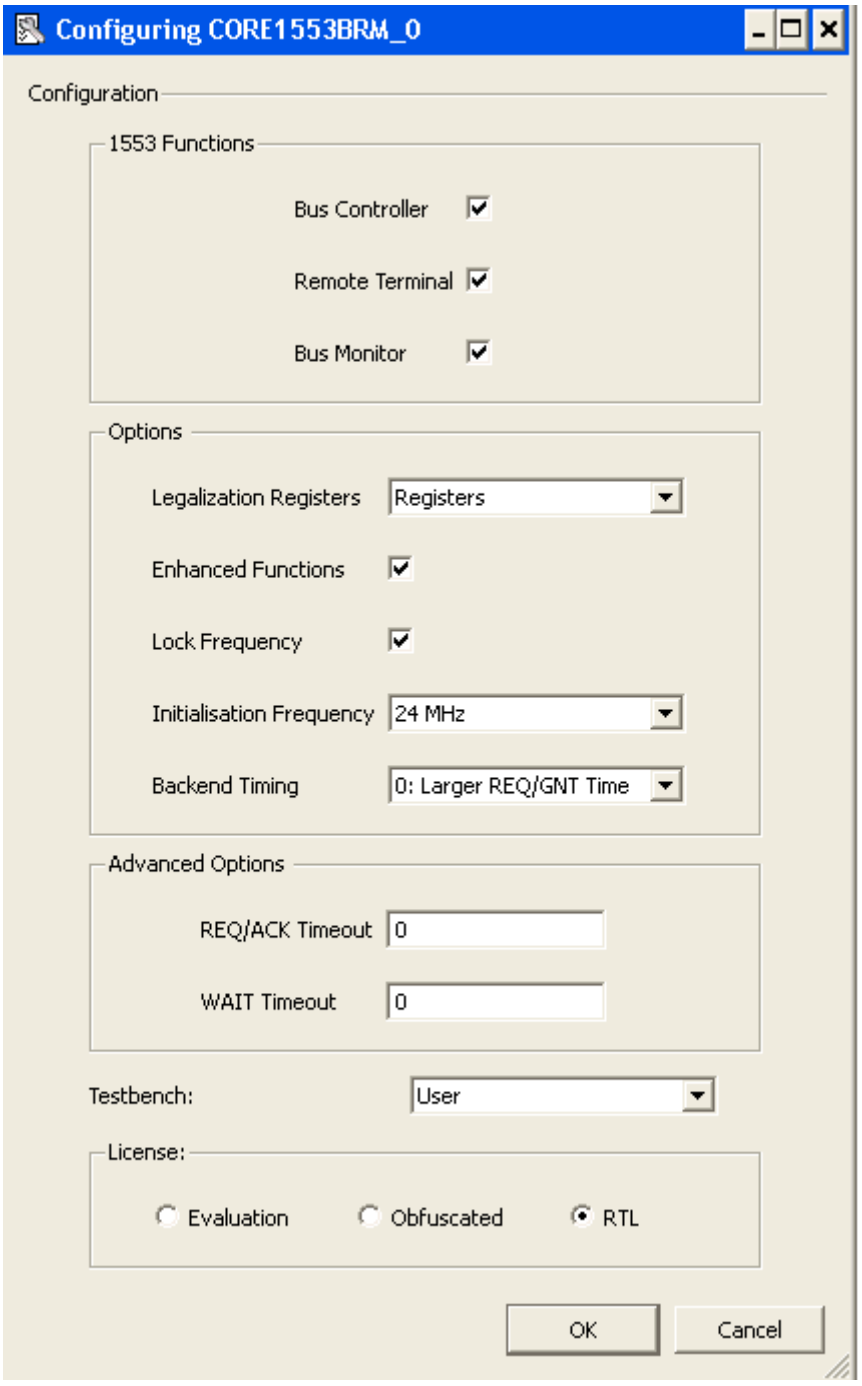


Figure 2-1 • **Core1553BRM Configuration within SmartDesign**

Once the core is configured, invoke the **Generate** function in SmartDesign. This will export all the required files to the project directory.

Simulation Flows

To run simulations, the required testbench flow must be selected within SmartDesign and **Save & Generate** must be run from the Generate pane. The required testbench is selected through the core configuration GUI in SmartDesign. The following simulation environments are supported:

- Full 1553 verification environment (VHDL only), but the user can use a VHDL verification environment to verify the Verilog core.
- Simple testbench (VHDL and Verilog)

When SmartDesign generates the Libero IDE/SoC project, it will install the appropriate testbench files. To run the testbenches, simply **set the design root to the Core1553BRM instantiation in the Libero IDE/SoC** file manager and click the **Simulation** icon in Libero IDE/SoC. This will invoke Model*Sim*® and automatically run the simulation.

ModelSim simulations contain a basic command word/data word template implemented with ModelSim cursors, to assist in reading waveforms.

Synthesis in Libero IDE/SoC

To run Synthesis on the core with parameters set in SmartDesign**, set the design root to the top of the project imported from SmartDesign**. This is a wrapper around the core that sets all the generics appropriately. Click the **Synthesis** icon in Libero IDE/SoC. The synthesis window appears, displaying the Synplicity® project. To run Synthesis, click the **Run** icon.

Place-and-Route in Libero IDE/SoC

Having set the design route appropriately and run Synthesis, click the **Layout** icon in Libero IDE/SoC to invoke Designer. Core1553BRM requires no special place-and-route settings.

3 – Interface Descriptions

Parameters on Core1553BRM

Core1553BRM has several top-level parameters (generics) that are used to select the operational modes of the core that are implemented (Table 3-1). Using these parameters allows the size of the core to be reduced when functions are not required.

Table 3-1 • **Core Parameters**

Name	Values	Description	
FAMILY	8, 9, 11, 12, 14, 15, 16, 17, 18, 19, 20, 21, 24, 25	Must be set to match the supported FPGA family: 8: SX-A 9: RTSX-S 11: Axcelerator 12: RTAX-S 14: ProASIC^{PLUS} 15: ProASIC3 16: ProASIC3E 17: Fusion 18: SmartFusion 19: SmartFusion2 20: IGLOO 21: IGLOOe 24: IGLOO2 25: RTG4	
BCENABLE	0 or 1	When 1, the BC function is implemented.	
RTENABLE	0 or 1	When 1, the RT function is implemented.	
MTENABLE	0 or 1	When 1, the MT function is implemented.	
LEGREGS	0 to 2	This controls the implementation of the RT legalization registers.	
		0	The legalization registers are not implemented. The user must use the external RT legalization interface.
		1	The legalization logic is implemented using registers within the FPGA.
		2	The legalization logic is implemented using memory within the FPGA.
ENHANCED	0 or 1	When 1, the Enhanced Features (Table 1-1 on page 18) register is implemented. When 0, the enhanced features are disabled and the sixth bit of the CPU address register is ignored.	
INITFREQ	12, 16, 20, or 24	Sets the operating frequency of the core. Legal values are 12, 16, 20, and 24 MHz. If the Enhanced Features register is enabled, the operating frequency can be modified by the CPU.	
LOCKFREQ	0 to 1	When 1, the core operating frequency is locked to the frequency set by INITFREQ. When 0, the clock frequency bits in the Enhanced Features register ("Register 32 – Enhanced Features Register" on page 72) can be used to change the clock frequency.	

Table 3-1 • **Core Parameters (continued)**

Name	Values	Description
BETIMING	0 to 2	Modifies the backend timing requirements. Refer to Table 3-11 on page 31 and Table 3-12 on page 31.
ACKVAL	0 to 255	Specifies the REQ/GNT timer value when BETIMING = 2.
WAITVAL	0 to 255	Specifies the WAIT timer value when BETIMING = 2.

I/O Signal Descriptions

1553B Bus Interface

Table 3-2 • **Bus Interface Signals**

Name	Type	Description
BUSAINEN	Out	Active high output that enables the A receiver
BUSAINP	In	Positive data input from the A receiver
BUSAINN	In	Negative data input from the A receiver
BUSBINEN	Out	Active high output that enables the B receiver
BUSBINP	In	Positive data input from the bus to the B receiver
BUSBINN	In	Negative data input from the bus to the B receiver
BUSAOUTIN	Out	Active high transmitter inhibit for the A transmitter
BUSAOUTP	Out	Positive data output to the bus A transmitter (held HIGH when no transmission)
BUSAOUTN	Out	Negative data output to the bus A transmitter (held HIGH when no transmission)
BUSBOUTIN	Out	Active high transmitter; inhibits the B transmitter
BUSBOUTP	Out	Positive data output to the bus B transmitter (held HIGH when no transmission)
BUSBOUTN	Out	Negative data output to the bus B transmitter (held HIGH when no transmission)

Core Setup Signals

Table 3-3 • **Core Setup Signals**

Name	Type	Description
LOCKn	In	When 0, prevents the internal registers overriding the RTADDRIN, RTADDRPIN, MSELIN, and ABSTDIN inputs.
RTADDRIN[4:0]	In	Sets the RT address.
RTADDRPIN	In	RT address parity input.
RTADERR	Out	Indicates that the RT address is incorrectly set; active high.
MSELIN[1:0]	In	Sets the operating mode. 00: Bus Controller 01: Remote Terminal 10: Bus Monitor 11: Bus Monitor and Remote Terminal