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Core1553BRT v4.1

Handbook

Microsemi

Table of Contents

Introduction

Core Overview

Core1553BRT provides a complete, dual-redundant MIL-STD-1553B remote terminal (RT), apart from the transceivers required to interface to the bus. A typical system implementation using Core1553BRT is shown in Figure 1 and Figure 2 on page 5.

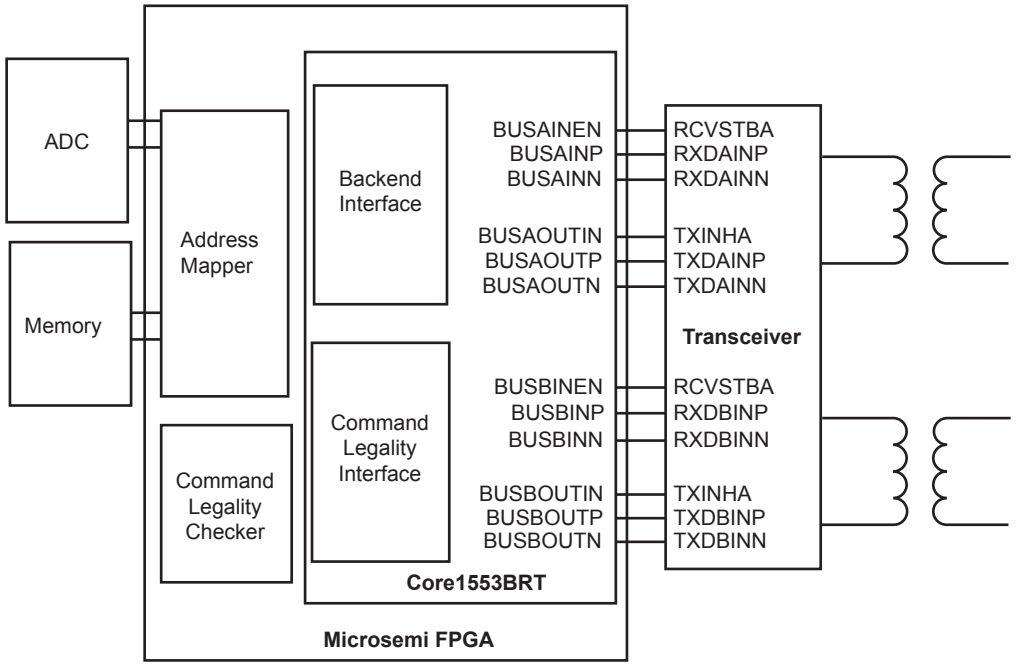


***Figure 1* • Typical Core1553BRT System**

At a high level, Core1553BRT simply provides a set of memory-mapped subaddresses that “receive data written to” or “transmit data read from.” The core can be configured to connect directly to synchronous or asynchronous memory devices. Alternatively, the core can directly connect to backend devices, removing the need for memory buffers. If memory is used, the core requires 2,048 words of memory, which can be shared with the local CPU.

The core supports all 1553B mode codes and allows the user to designate as illegal any mode code or any particular subaddress for both transmit and receive operations. The command legalization can be done within the core or in an external command legality block via the command legalization interface.

The core consists of six main blocks: 1553B encoders, 1553B decoders, the backend interface, a command decoder, RT controller blocks, and a command legalization block (Figure 2).

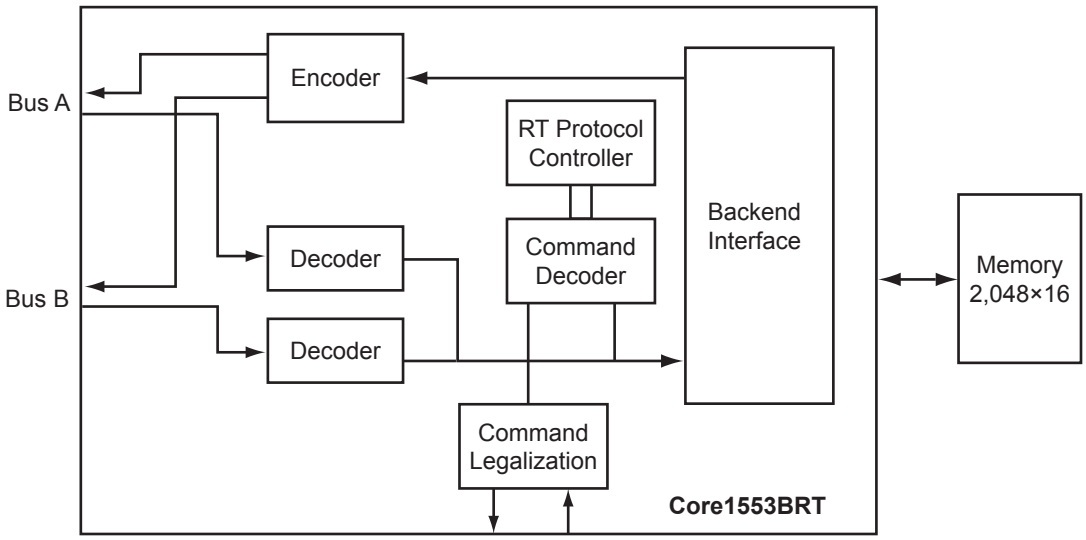


***Figure 2* • Core1553BRT RT Block Diagram**

In Core1553BRT, a single 1553B encoder is used. This takes each word to be transmitted and serializes it, after which the signal is Manchester-encoded. The encoder also includes logic to prevent the RT from transmitting for longer than the allowed period, and loopback fail logic. The loopback logic monitors the received data and verifies that the core has correctly received every word that it transmits.

The output of the encoder is gated with the bus enable signals to select which busses the RT should use to transmit.

The core includes two 1553B decoders. A decoder takes the serial Manchester data received from the bus and extracts the received data words. A decoder requires a 12, 16, 20, or 24 MHz clock to extract the data and the clock from the serial stream.

The decoder contains a digital PLL that generates a recovery clock used to sample the incoming serial data. The data is then deserialized and the 16-bit word decoded. The decoder detects whether a command or data word is received and also performs Manchester encoding and parity error checking.

The backend interface for Core1553BRT allows a simple connection to a memory device or direct connection to other devices, such as analog to digital converters. The access rates to this memory are slow, with one read or write every 20 µs. At 12 MHz operation, this is one read or write every 240 clock cycles.

The backend interface can be configured to connect to either synchronous or asynchronous memory devices. This allows the core to be connected to synchronous logic, memory within the FPGA, or external asynchronous memory.

The core implements a simple subaddress to the memory address mapping function, allowing the core to be directly connected to a memory block. The core also supports an address mapping function that allows the backend memory map to be modified to emulate legacy 1553B remote terminals, therefore minimizing system and software changes when adopting Core1553BRT. Associated with this function is the ability to create a user-specific interrupt vector.

The backend interface supports a standard bus request and grant protocol and provides a WAIT input to allow the core to interface to slow memory devices.

The command decoder and RT controller blocks decode the incoming command words, verifying their legality. Then, the protocol state machine responds to the command, transmitting or receiving data or processing a mode code.

Core1553BRT has an internal command legality block that verifies every 1553B command word. A separate interface is provided that, when enabled, allows the command legality decoder to be implemented outside Core1553BRT. This external interface is intended for use with Obfuscated versions of the core. For the RTL version of the core, this interface can be used, or the source code can be easily modified to implement this function.

The external BIST interface is used to configure the external transmit bit word or internal BIST word. The external BIST is configured when EXTERNAL_BIST parameter/generic is set and external BIST enable is set.

Verification and Compliance

Core1553BRT functionality has been verified in simulation and hardware. Full functional verification against the RT test plan, as defined in MIL-HDBK-1553A, has been carried out using a VHDL simulation environment.

To fully verify compliance, the core has been implemented on an M2S050FG484 part connected to external transceivers and memory. Test Systems Inc. has verified Core1553BRT against the remote terminal test plan in accordance with the RT validation test plan MIL-HDBK-1553A, Appendix A.

Fail-Safe State Machines

The logic design of Core1553BRT implements fail-safe state machines. All state machines include illegal state detection logic. If a state machine should ever enter an illegal state, the core will assert its FSM_ERROR output and the state machine will reset. If this occurs, Microsemi recommends that the external system reset the core and also assert the TFLAG input to inform the bus controller (BC) that a serious error has occurred within the remote terminal.

The FSM_ERROR output can be left unconnected if the system is not required to detect and report state machines entering illegal states.

Core Version

This handbook applies to Core1553BRT v4.1 and later.

Supported Families

- IGLOO®
- IGLOOe
- IGLOOPLUS
- ProASIC®3
- ProASIC3L
- ProASIC3E
- SmartFusion®
- SmartFusion2
- Fusion
- ProASICPLUS®
- Axcelerator®
- RTAX-S
- SX-A
- RTSX-S
- IGLOO®2
- RTG4™

Device Requirements

Core1553BRT can be implemented in several Microsemi FPGA devices. Table 1 gives the utilization and performance figures for the core implemented in these devices.

The core can operate with a clock of up to 24 MHz. This clock rate is easily met in all Microsemi silicon families noted in Table 1.

***Table 1* • Device Utilization and Performance**

Family	Combinatorial	Sequential	Total	Device	Utilization	Performance
ProASIC3	1066	438	1519	A3P600	11.0%	85.543
ProASIC3E	1066	438	1519	A3PE600	11.0%	82.42
IGLOO	1066	438	1519	AGL600V5	11.0%	78.223
IGLOOe	1066	438	1519	AGLE600V5	11.0%	77.304
Fusion	1066	438	1519	AFS600	11.0%	87.367
IGLOO2	756	457	1213	M2GL050T	2.2%	142.349
SmartFusion2	756	457	1213	M2S050T	2.2%	142.369
SmartFusion	1026	404	1430	A2F500M3G	12.4%	92.106
SX-A	750	451	1201	A54SX72A	19.9%	52.089
RTSX-S	742	450	1192	RT54SX72S	19.8%	46.618
Axcelerator	754	440	1194	AX500	14.8%	104.037
RTAX-S	754	440	1194	RTAX1000S	6.6%	72.611
ProASIC^{PLUS}	1404	464	1868	APA450	15.2%	68.357
RTG4	872	426	1298	RT4G150	0.85%	108.9

Utilization data was generated using standard Libero® System-on-Chip (SoC) or Integrated Design Environment (IDE) tool flows with typical core parameter settings. Utilization data will vary slightly with different parameter settings and tool usage.

1 – MIL-STD-1553B Bus Overview

The MIL-STD-1553B bus is a differential serial bus used in military and space equipment. It comprises multiple redundant bus connections and communicates at 1 MB/s.

The bus has a single active BC and up to 31 RTs. The BC manages all data transfers on the bus using the command and status protocol. The bus controller initiates every transfer by sending a command word and data if required. The selected RT will respond with a status word and data if required.

The 1553B command word contains a 5-bit RT address, transmit or receive bit, 5-bit subaddress, and 5-bit word count. This allows for 32 RTs on the bus. However, since RT address 31 is used to indicate a broadcast transfer, only 31 RTs can be connected. Each RT has 30 subaddresses reserved for data transfers. The other two subaddresses (0 and 31) are reserved for mode codes used for bus control functions. Data transfers contain up to thirty-two 16-bit data words. Mode code command words are used for bus control functions such as synchronization.

Message Types

The 1553B bus supports 10 message transfer types, allowing basic point-to-point and broadcast BC-to-RT data transfers, mode code messages, and direct RT-to-RT messages. Figure 1-1 shows the message formats.

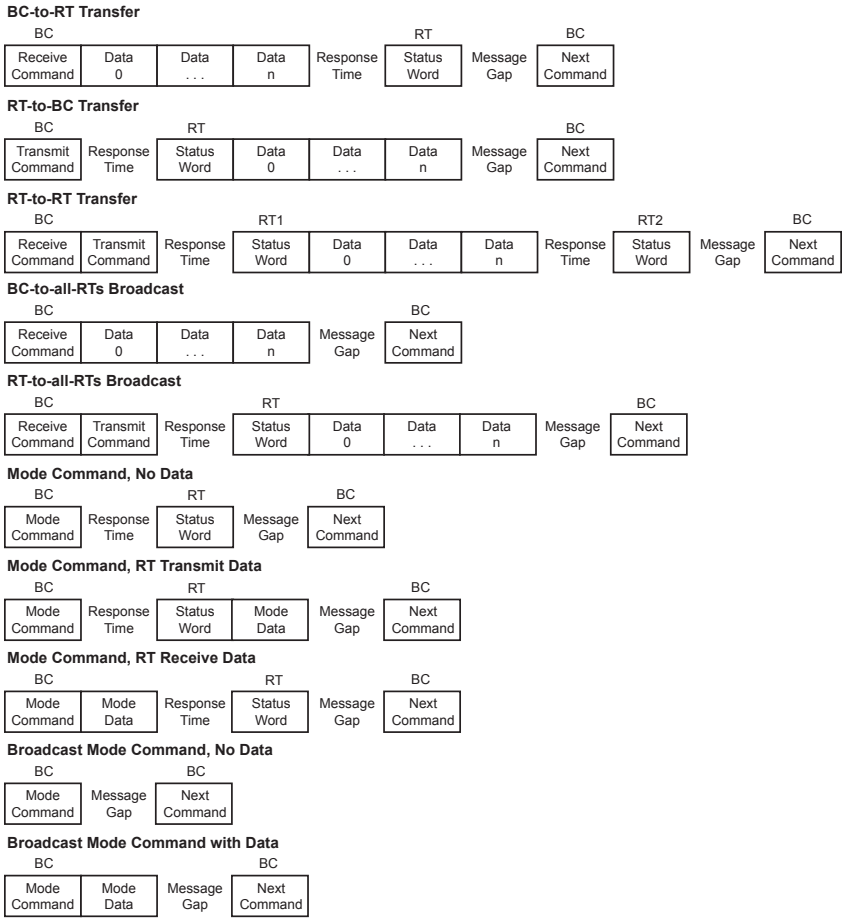


***Figure 1-1* • 1553B Message Formats**

Word Formats

There are only three types of words in a 1553B message: a command word (CW), a data word (DW), and a status word (SW). Each word consists of a 3-bit sync pattern, 16 bits of data, and a parity bit, providing the 20-bit word (Figure 1-2).

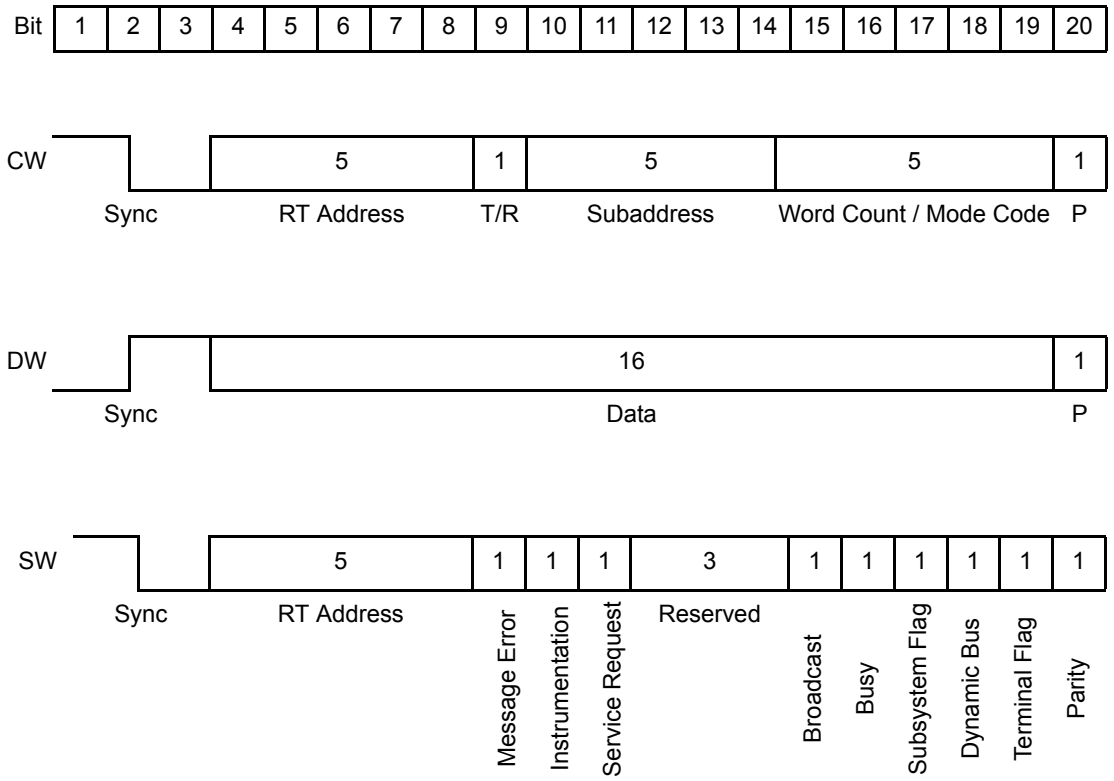


***Figure 1-2* • 1553B Word Formats**

2 – Tool Flows

SmartDesign

Core1553BRT is available for download to the SmartDesign IP Catalog, via the Libero IDE/SoC web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, please refer to the Libero IDE/SoC online help.

The core can be configured using the configuration GUI within SmartDesign, as shown in Figure 2-1.

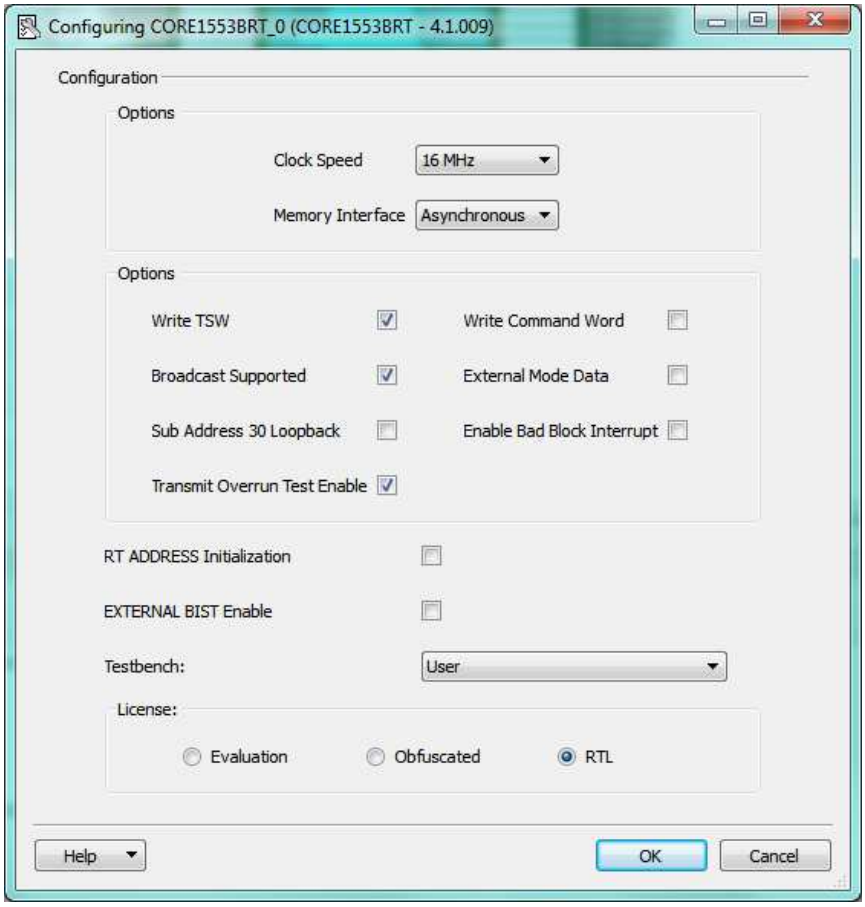


***Figure 2-1* • Core1553BRT Configuration within SmartDesign**

Simulation Flows

To run simulations, the required testbench flow must be selected within SmartDesign. The required testbench is selected through the core configuration GUI. The following simulation environments are supported:

- Full 1553 verification environment (VHDL only)
- Simple testbench (VHDL and Verilog)

When SmartDesign generates the core, it will install the appropriate testbench files. To run the testbenches, simply set the design root to the Core1553BRT instantiation in the Libero IDE/SoC file manager and click the **Simulation** icon in Libero IDE/SoC. This will invoke Model*Sim*® and automatically run the simulation.

3 – Interface Descriptions

Parameters on Core1553BRT

The parameters given in Table 3-1 are used to configure the core.

***Table 3-1* • Core1553BRT Parameters**

Parameter	Range	Description
FAMILY	2 to 24	Must be set to the required FPGA family: 8: SX-A 9: RTSX-S 11: Axcelerator 12: RTAX-S 14: ProASIC^{PLUS} 15: ProASIC3 16: ProASIC3E 17: Fusion 18: SmartFusion 19: SmartFusion2 20: IGLOO 21: IGLOOe 22: ProASIC3L 23: IGLOO PLUS 24: IGLOO2 25: RTG4
CLKSPD	12, 16, 20, or 24	Sets the clock frequency of the core to 12, 16, 20, or 24 MHz
WRTTSW	0 or 1	When 1, the core will write the transfer status word (TSW) to the memory. When 0, the core disables the writing of the transfer status word to memory. This is useful for simple RT applications that do not use memory but have a direct connection to the backend device.
WRTCMD	0 or 1	When 1, the core will write the 1553B command word to the locations used for the TSW values. If WRTTSW is also enabled, the command word is written to memory at the start of a message, and the TSW value will overwrite the command word at the end of the message, unless an external address mapping function is used.
EXTMDATA	0 or 1	When 1, the core reads and writes mode code data words from and to the external memory (except for “transmit last command” and “transmit BIT [Built-In Test] word”). The VWORD input is not used when this input is active.
BCASTEN	0 or 1	This input enables broadcast operation. When 1, broadcast operations are enabled. When 0, broadcast messages (i.e., RT address 31) are treated as normal messages. If the RTADDR input is set to 31, the RT will respond to the message.

***Table 3-1* • Core1553BRT Parameters (continued)**

Parameter	Range	Description
SA30LOOP	0 or 1	This input alters the backend memory mapping so that subaddress 30 provides automatic loopback. When 0, the RT does not loop back subaddress 30. Separate memory buffers are used for transmit and receive data buffers. When 1, the RT maps the transmit memory buffer for subaddress 30 to the receive memory buffer for subaddress 30; i.e., the upper address line is forced to 0.
ASYNCIF	0 or 1	When 1, the backend interface is in asynchronous mode. When 0, the backend interface is in synchronous mode.
INTENBBR	0 or 1	When active (1), the core generates interrupts when both good and bad 1553B messages are received. When inactive (0), the core only generates interrupts when good messages are received.
TESTTXTOUTEN	0 or 1	This enables the TESTTXTOUT input; it is for test use only. This parameter should be set to 0 if it is not required to be able to force transmission overrun for testing the internal transmit timer.
INITLASTSW	0 or 1	This input controls the last status word. When 0, the first received command is a transmit last status word. The core will respond with an undefined status word since no status word has previously been sent (same function as previous core versions.) When 1, the first received command is a transmit last status word. The core will respond with a valid RT address and all other status bits zero, even though no status word was previously sent. It requires PURSTN to be asserted at power-up. The default value of INITLASTSW is 0.
EXTERNAL_BIST	0 or 1	This parameter controls the mode code 19 support. When 0, the internal BIST value as specified in Table 5-6 on page 32 is returned in response to the Transmit BIST mode code. When 1, the input BITIN [15:0] is returned in response to the Transmit BIST mode code. The default value of EXTERNAL_BIST is 0.

I/O Signal Descriptions

Table 3-2 lists the signals for the 1553B bus interface. Table 3-3 on page 14 lists the control and status signals.

Double flip-flop metastability synchronizers are implemented on the following inputs: RTADDR[4:0], RTADDRP, BUSAINP, BUSAINN, BUSBINP, and BUSBINN.

***Table 3-2* • 1553B Bus Interface**

Port Name	Type	Description
RTADDR[4:0]	**In**	**Sets the RT address; RT address can be set to '11111' for normal operation only when BCASTEN is set to 0.**
RTADDRP	**In**	**RT address parity input. This input should be set HIGH or LOW to achieve odd parity on the RTADDR and RTADDRP inputs. If RTADDR is '00000', the RTADDRP input should be 1.**
RTADERR	Out	Indicates that the RTADDR and RTADDRP inputs have incorrect parity, or broadcast is enabled, and the RT address is set to 31. When active (HIGH), the RT is disabled and will ignore all 1553B traffic.
BUSAINEN	Out	Active high output that enables the A receiver
BUSAINP	**In**	**Positive data input from the A receiver**
BUSAINN	**In**	**Negative data input from the A receiver**
BUSBINEN	Out	Active high output that enables the B receiver
BUSBINP	**In**	**Positive data input from the bus to the B receiver**
BUSBINN	**In**	**Negative data input from the bus to the B receiver**
BUSAOUTIN	Out	Active high transmitter inhibit for the A transmitter
BUSAOUTP	Out	Positive data output to the bus A transmitter (held HIGH when no transmission)
BUSAOUTN	Out	Negative data output to the bus A transmitter (held HIGH when no transmission)
BUSBOUTIN	Out	Active high transmitter inhibits the B transmitter
BUSBOUTP	Out	Positive data output to the bus B transmitter (held HIGH when no transmission)
BUSBOUTN	Out	Negative data output to the bus B transmitter (held HIGH when no transmission)

***Table 3-3* • Control and Status Signals**

Port Name	Type	Description
CLK	In	Master clock input (12, 16, 20, or 24 MHz)
RSTn	In	Reset input asynchronous (active low)
SREQUEST	In	Directly controls the Service Request bit in the 1553B status word
RTBUSY	In	Directly controls the Busy bit in the 1553B status word
SSFLAG	In	Directly controls the Subsystem Flag bit in the 1553B status word
TFLAG	In	Controls the Terminal Flag bit in the 1553B status word. This can be masked by the "inhibit terminal flag bit" mode code.
VWORD[15:0]	In	Provides the 16-bit vector value for the "transmit vector word" mode command
BUSY	Out	Indicates that the 1553BRT is either receiving or transmitting data or handling a mode command

Note: All control inputs except RSTn are synchronous and sampled on the rising edge of the clock. All status outputs are synchronous to the rising edge of the clock.

***Table 3-3* • Control and Status Signals (continued)**

Port Name	Type	Description
CMDSYNC	Out	Pulses HIGH for a single clock cycle when the RT detects the start of a 1553B command word (or status word) on the bus. Provides an early signal that the RT may be about to receive or transmit data or mode code.
MSGSTART	Out	Pulses HIGH for a single cycle when the RT is about to start processing a 1553B message whose command has been validated for this RT.
SYNCNOW	Out	Pulses HIGH for a single clock cycle when the RT receives a “synchronize” (with or without data mode) command. The pulse occurs just after the 1553B command word (sync with no data) or data word (sync with data mode code) has been received.
BUSRESET	Out	Pulses HIGH for a single clock cycle whenever the RT receives a “reset mode” command. The core logic will also automatically reset itself on receipt of this command.
INTOUT	Out	Goes HIGH when data has been received or transmitted or a mode command processed. The reason for the interrupt is provided on INTVECT. This output will stay HIGH until INTACK goes HIGH. If INTACK is held HIGH, this output will pulse HIGH for a single clock cycle.
INTVECT[6:0]	Out	This 7-bit value contains the reason for the interrupt. It indicates which subaddress data has been received or transmitted. Bit 6:0: Bad block received1: Good block received Bit 5:0: RX data1: TX data Bits 4:0:Subaddress Further information can be found by checking the appropriate transfer status word for the appropriate subaddress.
INTACK	In	Interrupt acknowledge input. When HIGH, this resets INTOUT back to LOW. If this input is held HIGH, the INTOUT signal will pulse HIGH for one clock cycle every time an interrupt is generated.
MEMFAIL	Out	Goes HIGH if the core fails to read data from or write data to the backend interface within the required time. This can be caused by the backend not asserting MEMGNTn fast enough or asserting MEMWAITn for too long.
CLRERR	In	Used to clear MEMFAIL and other internal error conditions. Must be held HIGH for more than two clock cycles.
TESTTXTOUT	In	This input is for test use only. It should be tied LOW. When HIGH and the TESTTXTOUTEN parameter is set to 1, the RT will transmit more than 32 data words if a “transmit data” command word is received. This will cause the RT to shut down the transmitter and set the TIMEOUT bits in the BIT word.
FSM_ERROR	Out	This output will go HIGH for a single clock cycle if any of the internal state machines enter an illegal state. This output should not go HIGH in normal operation. Should it go HIGH, it is recommended that the core be reset.
PURSTN	In	Asynchronous power-up reset input (active low) that is used to initialize the last status word value. This input is valid only when the parameter INITLASTSW = 1.
BITINEN	In	Transmit bit word enable input (active high). This input is valid when parameter EXTERNAL_BIST = 1 (to support mode code 19).
BITIN[15:0]	In	Transmit bit word input. This input is valid when the parameter EXTERNAL_BIST = 1.

Note: All control inputs except RSTn are synchronous and sampled on the rising edge of the clock. All status outputs are synchronous to the rising edge of the clock.

Command Legalization Interface

The core checks the validity of all 1553B command words. In RTL and Obfuscated versions of the core, the logic may be implemented externally to the core. The command word is provided, and the logic must generate the command-valid input. The command legalization interface also provides two strobes that are used to latch the command value to enable it to be used for address mapping and interrupt vector extension functions (Table 3-4).

Table 3-4 • **Command Legalization Interface**

Port Name	Type	Description
USEEXTOK	In	When 0, the core uses its own internal command-valid logic, enabling all legal, supported mode codes and all subaddresses. When 1, the core disables its internal logic and uses the external CMDOK input for command legality.
CMDVAL[11:0]	Out	ActiveCommand 11:0: Non-broadcast 1: Broadcast 10:0: Receive 1: Transmit 9:5:Subaddress 4:0:Word count / mode code These outputs are valid throughout the complete 1553B message. They can also be used to steer data to particular backend devices. In particular, bit 11 allows non-broadcast and broadcast messages to be differentiated, as required by MIL-STD-1553B, Notice 2.
CMDSTB	Out	Single-clock-cycle pulse that indicates valid command is received on CMDVAL.
CMDOK	In	Command word is okay (active high). The external logic must set this within 3 µs from the CMDVAL output changing.
CMDOKOUT	Out	Command word is okay (output). When USEEXTOK = 0, the core puts out its “internal command word okay” validation signal.
ADDRLAT	Out	CMDVAL address latch enable output (active high). Used to latch CMDVAL when it is being used for an address mapping function. ADDRLAT should be connected to the enable of a rising-edge clock flip-flop.
INTLAT	Out	CMDVAL interrupt vector latch enable output (active high). Used to latch CMDVAL when it is being used for an extended interrupt vector function. INTLAT should be connected to the enable of a rising-edge clock flip-flop.

Backend Interface

The backend interface supports both synchronous operation (to the core clock) and asynchronous operation to backend devices (Table 3-5).

Table 3-5 • **Backend Signals**

Port Name	Type	Description
MEMREQn	Out	Memory Request (active low) output. The backend interface requires memory access completion within 10 µs of MEMREQ going LOW to avoid data loss or overrun on the 1553B interface.*
MEMGNTn	In	Memory Grant (active low) input. This input should be synchronous to CLK and needs to meet the internal register setup time. This input can be held LOW if the core has continuous access to the RAM.
MEMWRn	Out	Memory Write (active low) Synchronous mode: This output indicates that data is to be written on the rising clock edge. Asynchronous mode: This output will be LOW for a minimum of one clock period and can be extended by the MEMWAITn input. The address and data are valid one clock cycle before MEMWRn is active and held for one clock cycle after MEMWRn goes inactive.
MEMRDn	Out	Memory Read (active low) Synchronous mode: This output indicates that data will be read on the next rising clock edge. This signal is intended as the read signal for synchronous RAMs. Asynchronous mode: This output will be LOW for a minimum of one clock period and can be extended by the MEMWAITn input. The address is valid one clock cycle before MEMRDn is active and held for one clock cycle after MEMRDn goes inactive. The data is sampled as MEMRDn goes HIGH.
MEMCSn	Out	Memory Chip Select (active low). This output has the same timing as MEMADDR.
MEMWAITn	In	Memory Wait (active low) Synchronous mode: This input is not used; it should be tied HIGH. Asynchronous mode: Indicates that the backend is not ready, and the core should extend the read or write strobe period. This input should be synchronous to CLK and needs to meet the internal register setup time. It can be permanently held HIGH.
MEMOPER[1:0]	Out	Indicates the type of memory access being performed. 00: Data transfer for both data and mode code transfers 01: TSW 10: Command word 11: Not used
MEMADDR[10:0]	Out	Memory Address output (the subaddress mapping is covered in "Standard Memory Address Map" on page 18)
MEMDOUT[15:0]	Out	Memory Data output
MEMDIN[15:0]	In	Memory Data input

*Note: *The 10 µs refers to the time from MEMREQn being asserted to the core deasserting its MEMREQn signal. The core has an internal overhead of five clock cycles, and any inserted wait cycles will also reduce this time. This time increases to 19.5 µs if the WRTTSW and WRTCMD inputs are LOW.*

***Table 3-5* • Backend Signals (continued)**

Port Name	Type	Description
MEMCEN	Out	Control Signal Enable (active high). This signal is HIGH when the core is requesting the memory bus and has been granted control. It is intended to enable any tristate drivers that may be implemented on the memory control and address lines.
MEMDEN	Out	Data Bus Enable (active high). This signal is HIGH when the core is requesting the memory bus, has been granted control, and is waiting to write data. It is intended to enable any bidirectional drivers that may be implemented on the memory data bus.

*Note: *The 10 µs refers to the time from MEMREQn being asserted to the core deasserting its MEMREQn signal. The core has an internal overhead of five clock cycles, and any inserted wait cycles will also reduce this time. This time increases to 19.5 µs if the WRTTSW and WRTCMD inputs are LOW.*

Standard Memory Address Map

Core1553BRT requires an external 2,048×16 memory device. This memory is split into sixty-four 32-word data buffers. Each of the 30 subaddresses has a receive and a transmit buffer, as shown in Table 3-6.

The memory allocated to the unused receive subaddresses 0 and 31 is used to provide status information back to the rest of the system. At the end of every transfer, a TSW is written to these locations.

***Table 3-6* • Standard Memory Address Map**

Address	RAM Contents	Action
000–01F	RX transfer status words	The core only writes to these addresses (except when SA30LOOP is HIGH).
020–03F	Receive subaddress 1	
...	...	
3C0–3DF	Receive subaddress 30	
3E0–3FF	TX transfer status words	
400–41F	Not used	The core only reads from these addresses.
420–43F	TX transfer subaddress 1	
...	...	
7C0–7DF	TX transfer subaddress 30	
7E0–7FF	Not used	

4 – Interface Timing

Specifications

Memory Write Timing – Asynchronous Mode

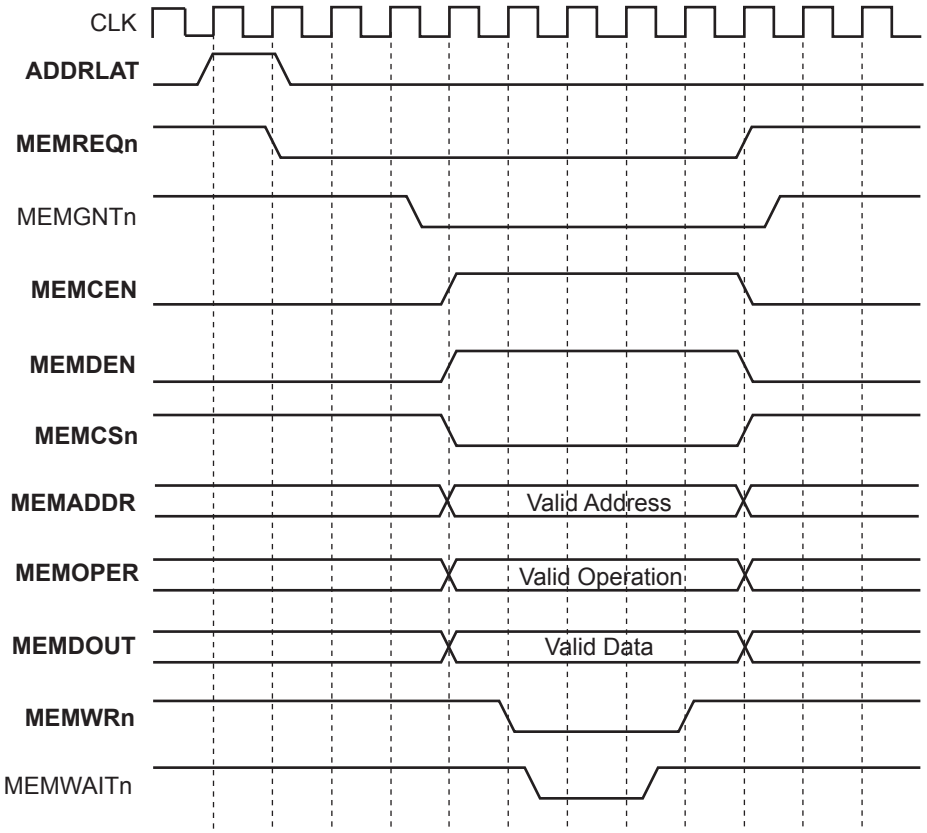


***Figure 4-1* • Memory Write Timing – Asynchronous Mode**

***Table 4-1* • Memory Write Timing**

Parameter	Description	Time
T_{pwWR}	Write pulse width (no wait states)	1 clock cycle
T_{pdGNT}	Maximum delay from MEMREQn to MEMGNTn active	12.0 µs
T_{suDATA}	Data setup time to MEMWRn LOW	1 clock cycle
T_{suADDR}	Address setup time to MEMWRn LOW	1 clock cycle
T_{hdDATA}	Data hold time from MEMWRn HIGH	1 clock cycle
T_{hdADDR}	Address hold time from MEMWRn HIGH	1 clock cycle
T_{suWAIT}	Wait setup to rising clock edge	1 clock cycle

Memory Read Timing – Asynchronous Mode

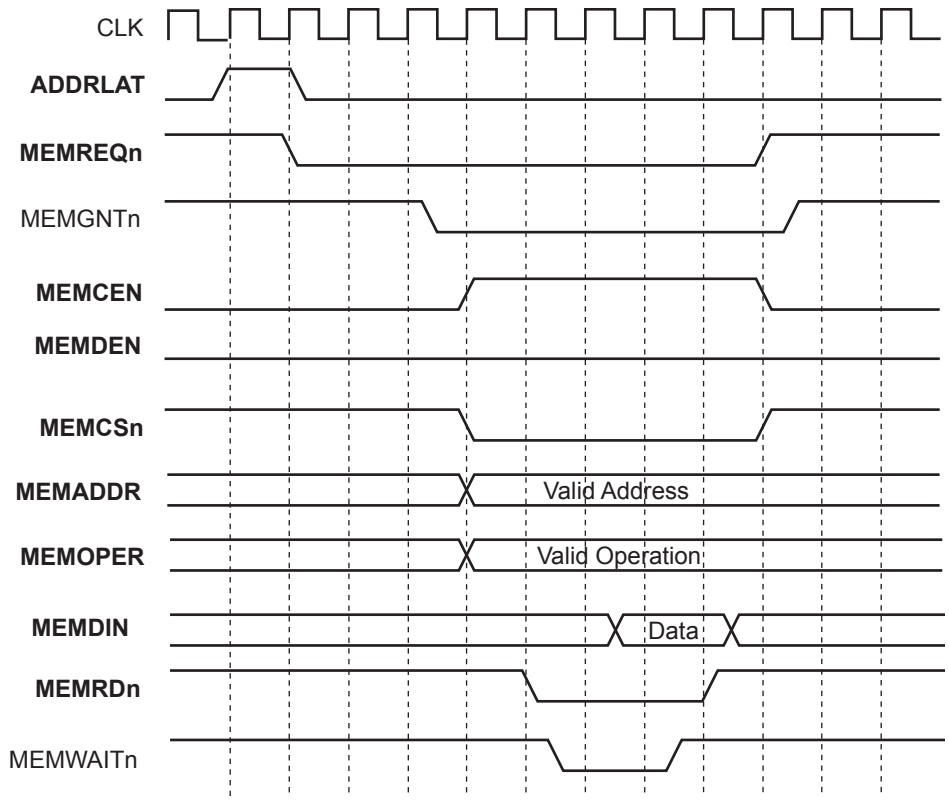


***Figure 4-2* • Memory Read Timing**

***Table 4-2* • Memory Read Timing**

Parameter	Description	Time
T_{pwRD}	Read pulse width (no wait states)	1 clock cycle
T_{pdGNT}	Maximum delay from MEMREQn to MEMGNTn active	12.0 µs
T_{suADDR}	Address setup time to MEMRDn LOW	1 clock cycle
T_{hdADDR}	Address hold time from MEMRDn HIGH	1 clock cycle
T_{suWAIT}	Wait setup to rising clock edge	15.0 ns
T_{suDATA}	Data setup time to MEMRDn HIGH	15.0 ns

Memory Write Timing – Synchronous Mode

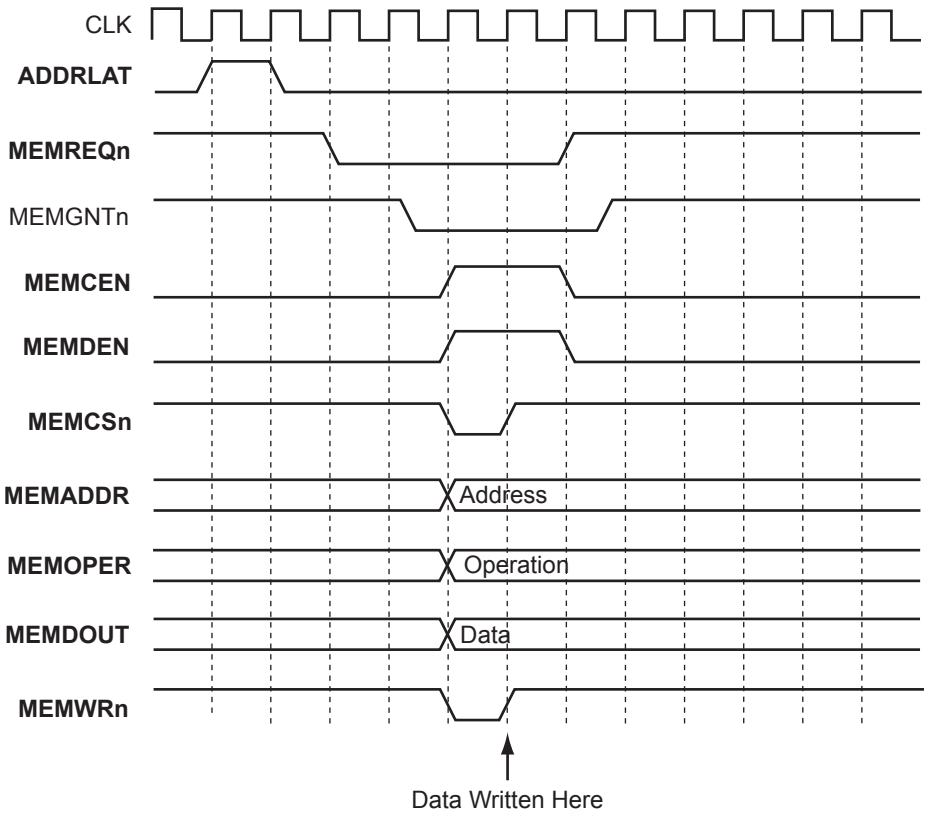


Figure 4-3 **• Memory Write Timing**

Memory Read Timing – Synchronous Mode

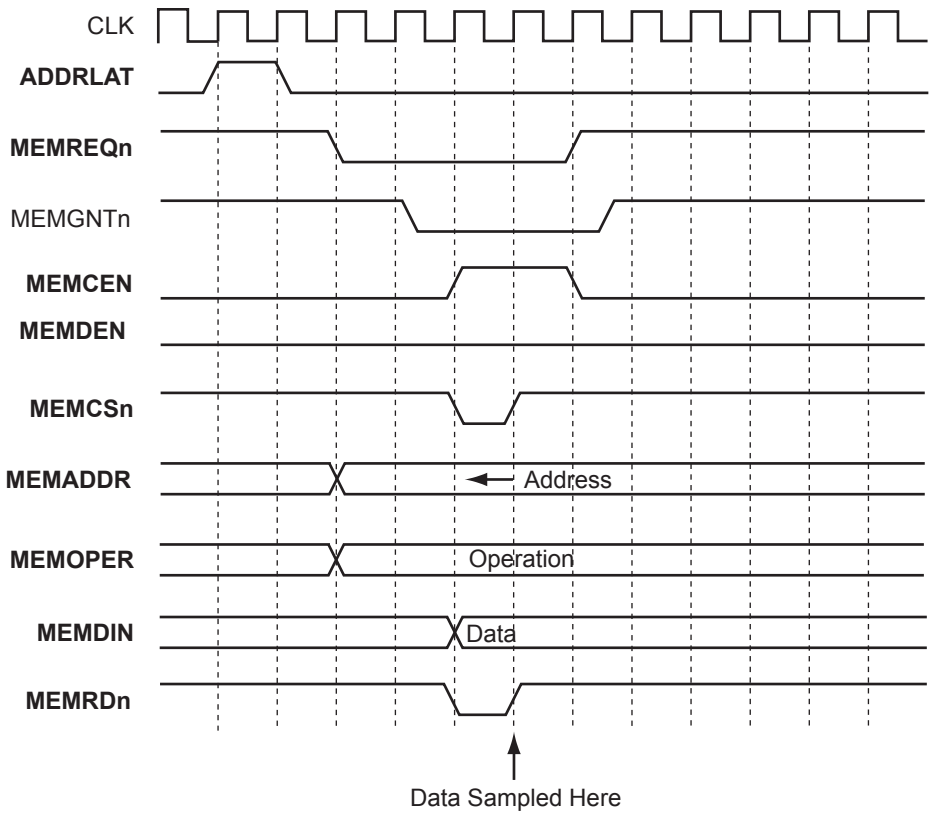


***Figure 4-4* • Memory Read Timing**

Command Word Legality Interface Timing

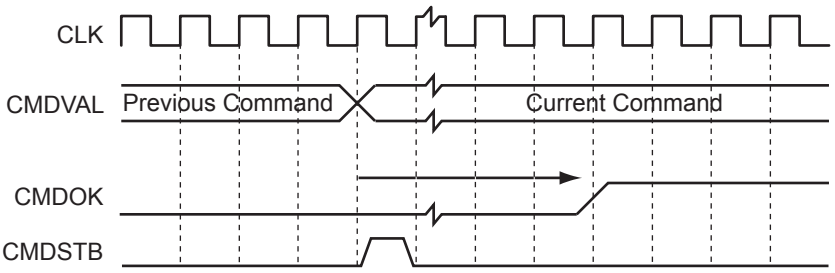
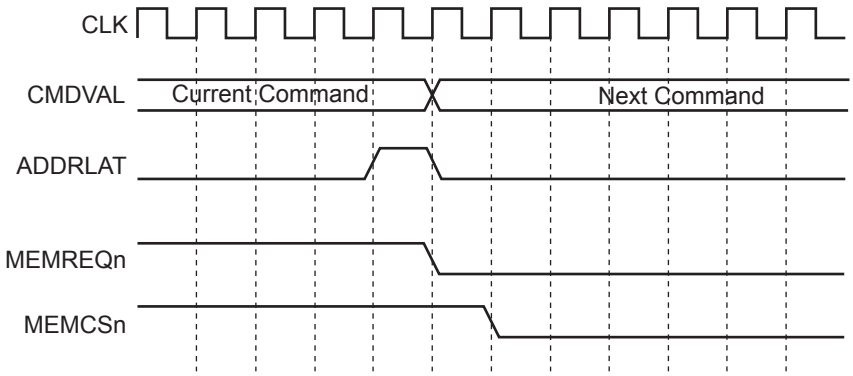


***Figure 4-5* • Command Word Legality Interface Timing**

***Table 4-3* • Command Word Legality Interface Timing**

Name	Description	Time
$T_{pdCMDOK}$	Maximum external command word legality decode delay	3 µs

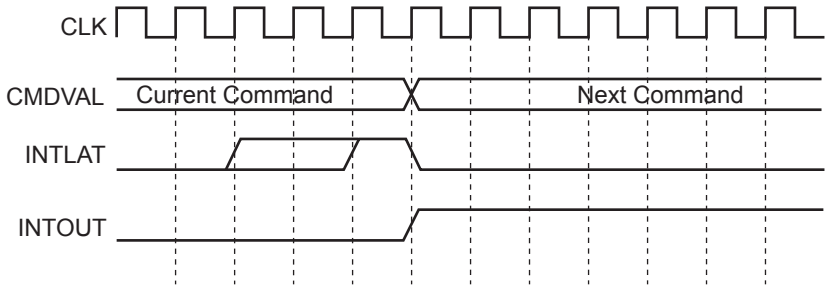
Address Mapper Timing



Note: This figure shows the worst-case timing when a second 1553B command arrives as the core starts a backend transfer and MEMGNTn is held LOW.

***Figure 4-6* • Address Mapper Timing**

Interrupt Vector Extender Timing



Note: This figure shows the worst-case timing when a second 1553B command arrives as the core asserts an interrupt request. Also, INTLAT may be active for several clock cycles prior to INTOUT.

***Figure 4-7* • Interrupt Vector Extender Timing**

RT Response Times

RT response time is from the midpoint of the parity bit in the command word to the midpoint of the status word sync (Table 4-4).

***Table 4-4* • RT Response Times**

Spec	Description	At 12 MHz	At 16 MHz	At 20 MHz	At 24 MHz
T_{rtresp}	RT response time	4.75 to 7.0 µs	4.75 to 7.0 µs	4.75 to 7.0 µs	4.75 to 7.0 µs
T_{rtrtto}	RT-to-RT timeout	57 µs	57 µs	57 µs	57 µs
T_{xxto}	Transmitter timeout	704 µs	668 µs	691 µs	693 µs

The RT-to-RT timeout is from the first command word parity bit to the expected sync of the first data word.

Transceiver Loopback Delays

Core1553BRT verifies that all transmitted data words are correctly transmitted. As data is transmitted by the transceiver on the 1553B bus, the data on the bus is monitored by the transceiver and decoded by Core1553BRT. The core requires that the loopback delay, i.e., the time from BUSAOUTP to BUSAINP, be less than the values given in the Table 4-5.

***Table 4-5* • Transceiver Loopback Requirements**

Clock Speed	Maximum Loopback Delay
12 MHz	2.3 µs
16 MHz	2.3 µs
20 MHz	2.3 µs
24 MHz	2.3 µs

The loopback delay is a function of the internal FPGA delay, PCB routing delays, and internal transceiver delay as well as transmission effects from the 1553B bus. Additional register stages can be inserted on either the 1553B data input or output within the FPGA, providing the loopback delays in Table 4-5 are not violated. This is recommended if additional gating logic is inserted inside the FPGA between the core and transceiver to minimize skew between the differential inputs and outputs.

Clock Requirements

To meet the 1553B transmission bit rate requirements, the Core1553BRT clock input must be 12 MHz, 16 MHz, 20 MHz, or 24 MHz 0.1% (+/- 1000 Hz) long term and 0.01% (+/- 100 Hz) short term.

5 – Operation

Standard Memory Address Map

Core1553BRT requires an external 2,048×16 memory device. This memory is split into sixty-four 32-word data buffers. Each of the 30 subaddresses has a receive and a transmit buffer, as shown in Table 5-1.

The memory allocated to the unused receive subaddresses 0 and 31 is used to provide status information back to the rest of the system. At the end of every transfer, a transfer status word is written to these locations.

***Table 5-1* • Standard Memory Address Map**

Address	RAM Contents	Action
000–01F	RX transfer status words	The core only writes to these addresses (except when SA30LOOP is HIGH).
020–03F	Receive subaddress 1	
...	...	
3C0–3DF	Receive subaddress 30	
3E0–3FF	TX transfer status words	
400–41F	Not used	The core only reads from these addresses.
420–43F	TX transfer subaddress 1	
...	...	
7C0–7DF	TX transfer subaddress 30	
7E0–7FF	Not used	

If the SA30LOOP input is set HIGH, the RT maps transmit subaddress 30 to receive subaddress 30; i.e., the upper address bit is forced to 0. This provides a loopback subaddress, as per MIL-STD-1553B, Notice 2. The TSW is still written to address 03FE. It should be noted that this is not strictly compliant with the specification, since the transmit buffer will contain invalid data if the received command fails, e.g., with a parity error. The transmit buffer should only be updated if the receive command had no errors. To implement this function in full compliance, the SA30LOOP input should be tied LOW, and the RT backend should copy the receive memory buffer to the transmit memory buffer only after the RT signals that the message was received with no errors.