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CP2108

SINGLE-CHIP USB-TO-QUAD-UART BRIDGE

Single-Chip USB-to-QUAD UART Data Transfer

- Four independent UART interfaces
- Integrated USB transceiver; no external resistor required
- Integrated clock; no external crystal required
- Integrated programmable EEPROM for storing customizable product information
- On-chip power-on reset circuit
- On-chip voltage regulator: 3.3 V output

USB Peripheral Function Controller

- USB Specification 2.0 compliant; full-speed (12 Mbps)
- USB suspend states supported via SUSPEND pins

Virtual COM Port Drivers

- Works with existing COM port PC applications
- Royalty-free distribution license
- Windows 8/7/Vista/XP/Server 2003
- Mac OS X
- Linux

Supply Voltage

- Self-powered: 3.0 to 3.6 V
- USB bus powered: 4.0 to 5.5 V
- V_{IO} voltage: 3.0 to VDD
- V_{IOHD} voltage: 2.7 to 6 V

UART Interface Features

Each UART interface supports the following:

- Supports hardware flow control (RTS/CTS)
- Supports all modem control signals
- Data formats supported:
  - Data bits: 5, 6, 7, and 8
  - Stop bits: 1, 1.5, and 2
  - Parity: odd, even, set, mark and none
- Baud rates: 300 bps to 2 Mbps
- UART 3 (pins 1–6) supports interfacing to devices up to 6 V

GPIO Interface Features

- Total of 16 GPIO pins with configurable options
- Suspend pin support
- Usable as inputs, open-drain or push-pull outputs
- 4 configurable clock outputs for external devices
- RS-485 bus transceiver control
- Toggle LED upon transmission
- Toggle LED upon reception

Package Options

- RoHS-UART 3 compliant 64-pin QFN (9x9 mm)

Temperature Range

- –40 to +85 °C

Ordering Part Number

- CP2108-B02-GM

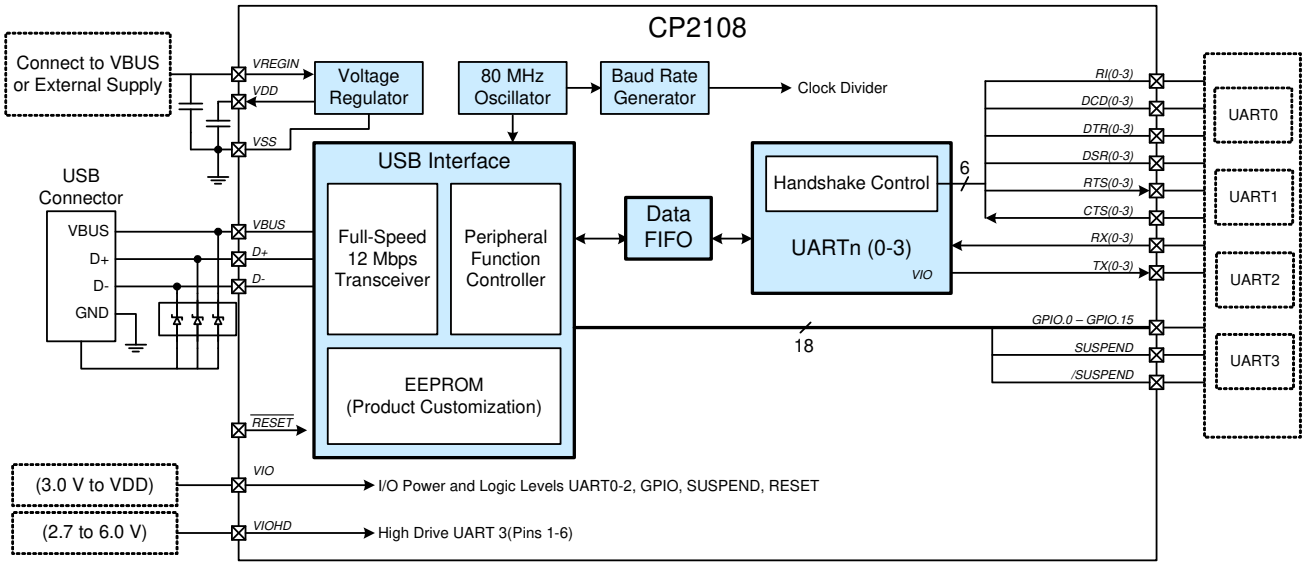

Figure 1. Example System Diagram

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1. System Overview

The CP2108 is a highly integrated USB-to-Quad-UART Bridge Controller providing a simple solution for updating RS-232/RS-485 designs to USB using a minimum of components and PCB space. The CP2108 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM, and four asynchronous serial data buses (UART) with full modem control signals in a compact 9 x 9 mm QFN-64 package (sometimes called “MLF” or “MLP”).

The on-chip EEPROM may be used to customize the USB Vendor ID (VID), Product ID (PID), Product Description String, Power Descriptor, Device Release Number, Interface Strings, Device Serial Number, Modem, and GPIO configuration as desired for OEM applications. The EEPROM is programmed on-board via the USB, allowing the programming step to be easily integrated into the product manufacturing and testing process.

Royalty-free Virtual COM Port (VCP) device drivers provided by Silicon Labs allow a CP2108-based product to appear as four COM ports in PC applications. The CP2108 UART interfaces implement all RS-232/RS-485 signals including control and handshaking, so existing system firmware does not need to be modified. The device also features a total of sixteen GPIO signals that can be user-defined for status and control information. See www.silabs.com/appnotes for the latest application notes and product support information for the CP2108.

An evaluation kit for the CP2108 is available. It includes a CP2108-based USB-to-UART/RS-232 evaluation board, a complete set of VCP device drivers, USB and RS-232 cables, and full documentation. Contact a Silicon Labs sales representative or go to www.silabs.com/products/interface/Pages/CP2108EK.aspx to order the CP2108 Evaluation Kit.

2. Ordering Part Number Information

Table 1. Ordering Part Numbers

Ordering Part Number	Notes
CP2108-B02-GM	Recommended for new designs
CP2108-B01-GM	Not recommended for new designs

See "12. Device Specific Behavior" on page 28 for more information about the differences between the orderable part numbers. The revision of the CP2108 can be determined by looking at the package marking or by querying the device using the application described in application note “AN721: CP21xx Device Customization Guide.”

The second row of the package marking will read as “B01-GM” or “B02-GM”. The link to application note AN721 is available in “11. Relevant Application Notes” .

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 2, unless stated otherwise.

Table 2. Recommended Operating Conditions[1]

V_{DD}= 3.0 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage VDD	V_{DD}		3.0	—	3.6	V
Operating Supply Voltage VREGIN[2]	V_{REGIN}		4.0	—	5.5	V
Operating Supply Voltage VIO	V_{IO}		3.0	—	V_{DD}	V
Operating Supply Voltage VIOHD	V_{IOHD}		2.7		6.0	V
Supply Current—Normal[3]	I_{DD}	Normal Operation	—	56	—	mA
Supply Current—Suspended[3]	I_{DD}	Bus Powered	—	460	—	µA
		Self Powered		330	—	µA
Supply Current—USB Pull-up[4]	I_{PU}		—	200	228	µA
Operating Ambient Temperature	T_A		–40	—	85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Notes:

1. All voltages are with respect to V_{SS}.
2. This applies only when using the regulator. When not using the regulator, VREGIN and V_{DD} are tied together externally and it is allowable for VREGIN to be equal to V_{DD}.
3. If the device is connected to the USB bus, the USB pull-up current should be added to the supply current for total supply current.
4. The USB pull-up supply current values are calculated values based on USB specifications.

Table 3. UART, GPIO, and Suspend I/O

V_{DD}= 3.0 to 3.6 V, V_{IO}=1.8 V to V_{DD}, V_{IOHD} = 2.7 V to 6.0 V, –40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (All pins except High Drive UART 3 pins 1–6)	V_{OH}		V_{IO} – 0.7	—	—	V
Output High Voltage (High Drive UART 3 pins 1–6)			V_{IOHD} – 0.7	—	—	V
Output Low Voltage (All pins except High Drive pins 1–6)	V_{OL}	Low Drive I_{OL} = 3 mA	—	—	0.6	V
Output Low Voltage (High Drive pins 1–6)		High Drive I_{OL} = 12.5 mA			0.6	V
Input High Voltage	V_{IH}	3.0 ≤ V_{IO} ≤ 3.6	V_{IO} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Weak Pull-up Current (V_{IN} = 0 V)	I_{PU}	V_{IO} = 3.6 V	–30	–20	–10	µA
Weak Pull-up Current UART 3 (pins 1–6)	I_{PU}	V_{IOHD} = 2.7 V	–15	–10	–5	µA
		V_{IOHD} = 6.0 V	–30	–20	–10	µA

Table 4. GPIO Output Specifications

–40 to +85°C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RS-485 Active Time After Stop Bit	t_{ACTIVE}		—	1	—	bit time*
TX Toggle Rate	f_{TXTOG}		—	15	—	Hz
RX Toggle Rate	f_{RXTOG}		—	15	—	Hz
Clock Output Rate	f_{CLOCK}		78k	—	20M	Hz
***Note:** Bit-time is calculated as 1 / baud rate.						

Table 5. Reset

–40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{DD}	—	1.4	—	V
		Falling Voltage on V_{DD}	0.8	1	1.3	V
V_{DD} Ramp Time	t_{RMP}	Time to V_{DD} ≥ 3.0 V	10	—	3000	µs
$\overline{\text{RESET}}$ Input High Voltage	$V_{IHRESET}$	3.0 ≤ VIO ≤ 3.6	V_{IO} – 0.6	—	—	V
$\overline{\text{RESET}}$ Input Low Voltage	$V_{ILRESET}$		—	—	0.6	V
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns

Table 6. Voltage Regulator

–40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage (at V_{DD} pin)	V_{DDOUT}		3.15	3.3	3.4	V
Output Current (at V_{DD} pin)*	I_{DDOUT}		—	—	150	mA
Output Load Regulation	V_{DDLR}		—	0.1	1	mV/mA
Output Capacitance	C_{VDD}		1	—	10	µF
***Note:** This is the total current the voltage regulator is capable of providing. Any current consumed by the CP2108 reduces the current available to external devices powered from V_{DD}.						

Table 7. USB Transceiver

–40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Valid Supply Range (for USB Compliance)	V_{DD}		3.0	—	3.6	V
VBUS Pull-Down Leakage Current	I_{VBUSL}	V_{BUS} = 5 V, V_{IO} = 3.3 V	—	10	—	µA
VBUS Detection Input Threshold	V_{VBUSTH}	3.0 ≤ VIO ≤ 3.6	V_{IO} – 0.6	—	—	V
Transmitter						
Output High Voltage	V_{OH}		2.8	—	—	V
Output Low Voltage	V_{OL}		—	—	0.8	V
Output Crossover Point	V_{CRS}		1.3	—	2.0	V
Output Impedance	Z_{DRV}	Driving High Driving Low	— —	38 38	— —	Ω
Pull-up Resistance	R_{PU}	Full Speed (D+ Pull-up) Low Speed (D– Pull-up)	1.425	1.5	1.575	kΩ
Output Rise Time	t_R	Low Speed Full Speed	75 4	— —	300 20	ns
Output Fall Time	t_F	Low Speed Full Speed	75 4	— —	300 20	ns
Receiver						
Differential Input Sensitivity	V_{DI}	| (D+) – (D–) |	0.2	—	—	V
Differential Input Common Mode Range	V_{CM}		0.8	—	2.5	V
Input Leakage Current	I_L	Pull-ups Disabled	—	<1.0	—	µA
Note: Refer to the USB Specification for timing diagrams and symbol definitions						

Table 8. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}		—	25	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

3.2. Absolute Maximum Ratings

Stresses above those listed under Table 9 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on VDD	V_{DD}		V_{SS}–0.3	4.2	V
Voltage on VREGIN	V_{REGIN}		V_{SS}–0.3	6.0	V
Voltage on VBUS	V_{BUS}	$V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
Voltage on VIO	V_{IO}		V_{SS}–0.3	4.2	V
Voltage on VIOHD	V_{IOHD}		V_{SS}–0.3	6.5	V
Voltage on $\overline{\text{RESET}}$	V_{IN}	$V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
Voltage on GPIO or UART pins	V_{IN}	GPIO/UART pins except 1–6	V_{SS}–0.3	V_{IO}+0.3	V
		UART pins 1–6	V_{SSHD}– 0.3	V_{IOHD}+0.3	V
Voltage on D+ or D–	V_{IN}	$V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
Total Current Sunk into Supply Pins	I_{SUPP}	V_{DD}, V_{REGIN}, V_{IO},V_{IOHD}	—	400	mA
Total Current Sourced out of Ground Pins	I_{VSS}		400	—	mA
Current Sourced or Sunk by Any I/O Pin	I_{PIO}	UART,GPIO,Suspend I/O, $\overline{\text{RESET}}$ except for UART 3 pins1–6	–100	100	mA
		UART 3 pins 1–6	–300	300	mA
Current Injected on Any I/O Pin	I_{INJ}	UART,GPIO,Suspend I/O, $\overline{\text{RESET}}$ except for UART 3 pins1–6	–100	100	mA
		UART 3 pins 1–6	–300	300	mA
Total Injected Current on I/O Pins	ΣI_{INJ}	Sum of all I/O and $\overline{\text{RESET}}$	–400	400	mA
Power Dissipation at T_A = 85 °C	P_D		—	800	mW

Note: V_{SS} and V_{SSHD} provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.

3.3. Throughput and Flow Control

The throughput values in Table 10 are typical values based on bench testing and can serve as a guideline for expected performance. Other factors such as PC system performance and USB bus loading will have an effect on throughput. Each column in the table shows the typical throughput using 1, 2, 3 or all 4 UART interfaces for the set baud rate.

1. It is not necessary to use hardware flow control if all CP2108 interfaces are configured for 230,400 bps or lower.
2. For baud rates above 230,400 bps, hardware flow control should be used to guarantee reception of all bytes across the UART. Also, sending data across multiple interfaces simultaneously will cause a reduction in the effective throughput for each interface.
3. UART 3 has lower throughput rates than UARTS 0-2. If the application is configured such that different interfaces will operate at different baud rates, the interface at the lowest baud rate should be put on UART 3. UART 3 throughput is 5% to 20% slower than the other interfaces.
4. The performance of UART 3 starts to become significantly slower than the other UART interfaces at baud rates greater than 230,400 bps.

Table 10. Throughput Guidelines Comparing UARTS in Operation at Different Set Baud Rates

Set Baud Rate	230,400 (bps)	460,800 (bps)	921,600 (bps)	2M (bps)
1 UART in operation: Throughput	196,900 (bps)	387,200 (bps)	694,200 (bps)	760,000 (bps)
2 UARTS in operation: Throughput	200,400 (bps)	381,600 (bps)	463,700 (bps)	537,400 (bps)
3 UARTS in operation: Throughput	200,300 (bps)	259,800 (bps)	314,800 (bps)	388,000 (bps)
4 UARTS in operation: Throughput	180,300 (bps)	208,900 (bps)	234,000 (bps)	288,200 (bps)

4. Pin Definitions and Packaging Information

4.1. Pin Definitions

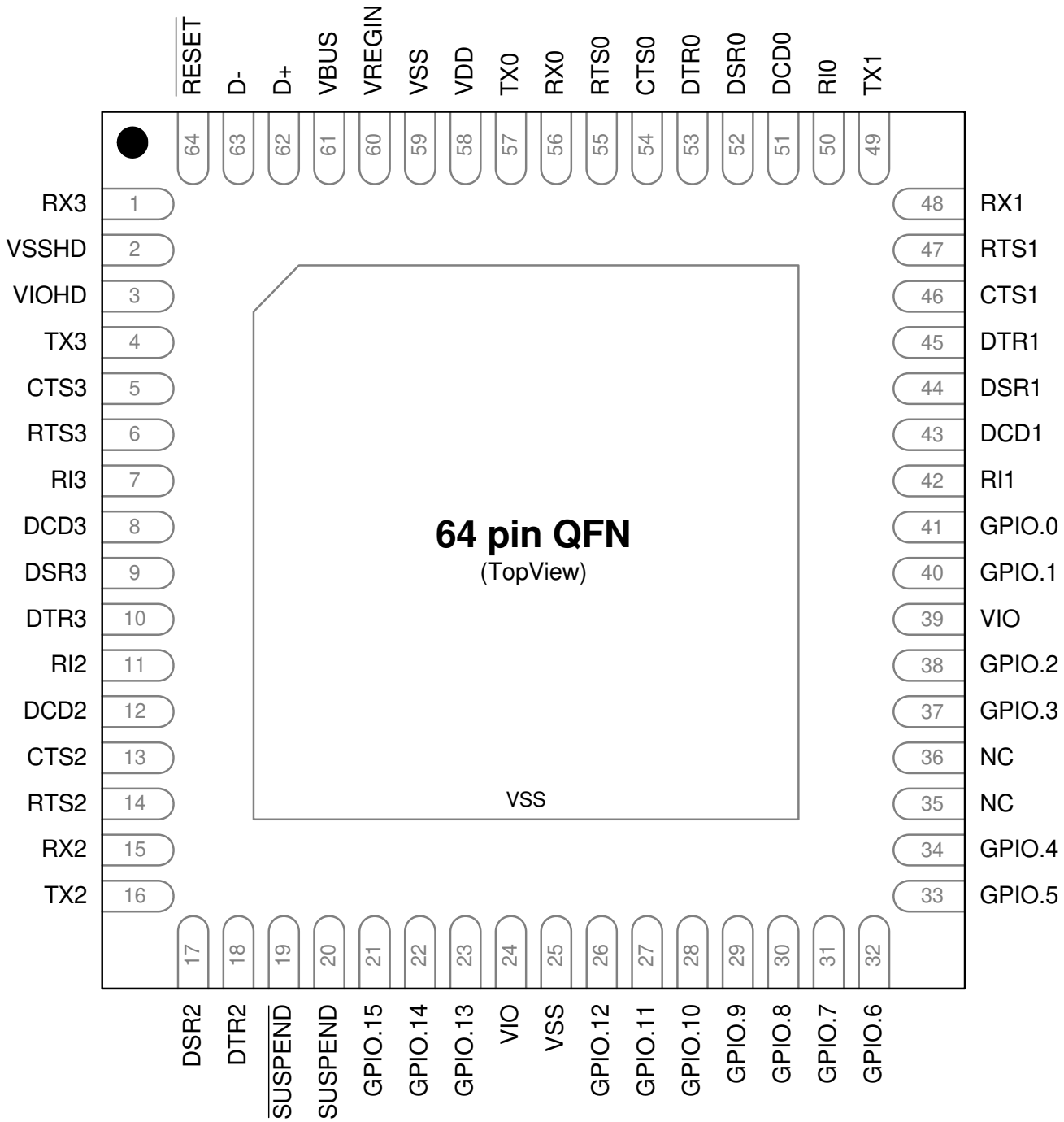


Figure 2. QFN-64 Pinout

Table 11. Pin Definitions and Alternate Functions

Pin Name	Type	Pin	Primary Function	Alternate Function
VSS	Ground	25 59	Device Ground	
VSSHD	Ground	2	High Drive Device Ground UART 3 pins 1–6. Connect to Device Ground.	
VDD	Power (Core)	58	Power Supply Voltage Input Voltage Regulator Output	
VIO	Power (I/O) Non High Drive	24 39	Non High Drive I/O Supply Voltage Input	
VIOHD	Power (I/O) High Drive	3	High Drive I/O Supply Voltage Input	
VREGIN	Power (Regulator)	60	Voltage Regulator Input. This pin is the input to the on-chip voltage regulator.	
$\overline{\text{RESET}}$	Active-low Reset	64	Device Reset. Open-drain output of internal POR or VDD monitor. An external source can initiate a system reset by driving this pin low for the time specified in Table 5.	
D–	USB Data-	63	USB D–	
D+	USB Data+	62	USB D+	
VBUS	USB Bus Sense	61	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network.	
TX0	Digital Output	57	UART 0 Transmit (TX)	
RX0	Digital Input	56	UART 0 Receive (RX)	
RTS0	Digital Output	55	UART 0 Ready to Send (RTS) Indicates to the modem that the UART is ready to receive data.	
CTS0	Digital Input	54	UART 0 Clear to Send (CTS) Indicates the modem is ready to send data to the UART	
DTR0	Digital Output	53	UART 0 Data Terminal Ready (DTR) Informs the modem that the UART is ready to establish a communications link.	

Table 11. Pin Definitions and Alternate Functions (Continued)

Pin Name	Type	Pin	Primary Function	Alternate Function
DSR0	Digital Input	52	UART 0 Data Set Ready (DSR) Indicates that the modem is ready to establish the communications link with the UART	
DCD0	Digital Input	51	UART 0 Data Carrier Detect (DCD) Indicates that the data carrier has been detected by the modem	
RI0	Digital Input	50	UART 0 Ring Indicator (RI) Indicates that a telephone ringing signal has been detected by the modem	
TX1	Digital Output	49	UART 1 Transmit (TX)	
RX1	Digital Input	48	UART 1 Receive (RX)	
RTS1	Digital Output	47	UART 1 Ready to Send (RTS)	
CTS1	Digital Input	46	UART 1 Clear to Send (CTS)	
DTR1	Digital Output	45	UART 1 Data Terminal Ready (DTR)	
DSR1	Digital Input	44	UART 1 Data Set Ready (DSR)	
DCD1	Digital Input	43	UART 1 Data Carrier Detect (DCD)	
RI1	Digital Input	42	UART 1 Ring Indicator (RI)	
GPIO.0	Digital I/O	41	General Purpose I/O 0	UART 0 TX Toggle0
GPIO.1	Digital I/O	40	General Purpose I/O 1	UART 0 RX Toggle
GPIO.2	Digital I/O	38	General Purpose I/O 2	UART 0 RS-485
GPIO.3	Digital I/O	37	General Purpose I/O 3	Clock Output 0
GPIO.4	Digital I/O	34	General Purpose I/O 4	UART 1 TX Toggle
GPIO.5	Digital I/O	33	General Purpose I/O 5	UART 1 RX Toggle
GPIO.6	Digital I/O	32	General Purpose I/O 6	UART 1 RS-485
GPIO.7	Digital I/O	31	General Purpose I/O 7	Clock Output 1
GPIO.8	Digital I/O	30	General Purpose I/O 8	UART 2 TX Toggle
GPIO.9	Digital I/O	29	General Purpose I/O 9	UART 2 RX Toggle
GPIO.10	Digital I/O	28	General Purpose I/O 10	UART 2 RS-485
GPIO.11	Digital I/O	27	General Purpose I/O 11	Clock Output 2

Table 11. Pin Definitions and Alternate Functions (Continued)

Pin Name	Type	Pin	Primary Function	Alternate Function
GPIO.12	Digital I/O	26	General Purpose I/O 12	UART 3 TX Toggle
GPIO.13	Digital I/O	23	General Purpose I/O 13	UART 3 RX Toggle
GPIO.14	Digital I/O	22	General Purpose I/O 14	UART 3 RS-485
GPIO.15	Digital I/O	21	General Purpose I/O 15	Clock Output 3
SUSPEND	Digital Output	20	Suspend Indicator - Active High	
$\overline{\text{SUSPEND}}$	Digital Output	19	Suspend Indicator - Active Low	
DTR2	Digital Output	18	UART 2 Data Terminal Ready (DTR)	
DSR2	Digital Input	17	UART 2 Data Set Ready (DSR)	
TX2	Digital Output	16	UART 2 Transmit (TX)	
RX2	Digital Input	15	UART 2 Receive (RX)	
RTS2	Digital Output	14	UART 2 Ready to Send (RTS)	
CTS2	Digital Input	13	UART 2 Clear to Send (CTS)	
DCD2	Digital Input	12	UART 2 Data Carrier Detect (DCD)	
RI2	Digital Input	11	UART 2 Ring Indicator (RI)	
DTR3	Digital Output	10	UART 3 Data Terminal Ready (DTR)	
DSR3	Digital Input	9	UART 3 Data Set Ready (DSR)	
DCD3	Digital Input	8	UART 3 Data Carrier Detect (DCD)	
RI3	Digital Input	7	UART 3 Ring Indicator (RI)	
RTS3	Digital Output	6	UART 3 Ready to Send (RTS) High Drive	
CTS3	Digital Input	5	UART 3 Clear to Send (CTS) High Drive	
TX3	Digital Output	4	UART 3 Transmit (TX) High Drive	
RX3	Digital Input	1	UART 3 Receive (RX) High Drive	
NC	No Connect	35 36		

4.2. QFN-64 Package Specifications

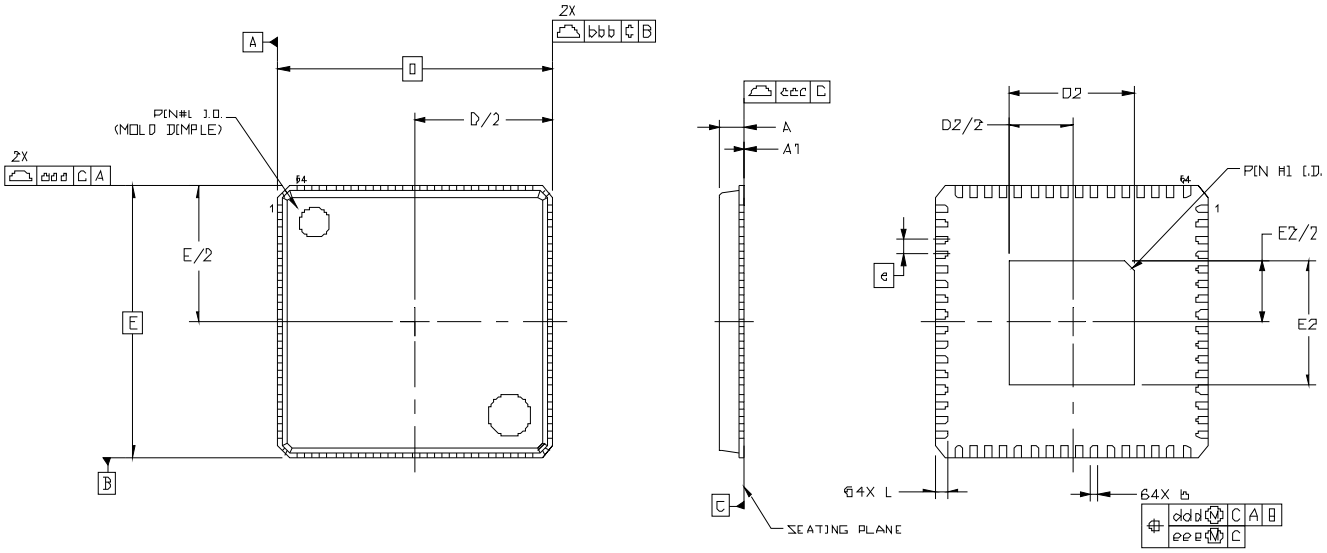


Figure 3. QFN-64 Package Drawing

Table 12. QFN-64 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		9.00 BSC	
E2	3.95	4.10	4.25
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

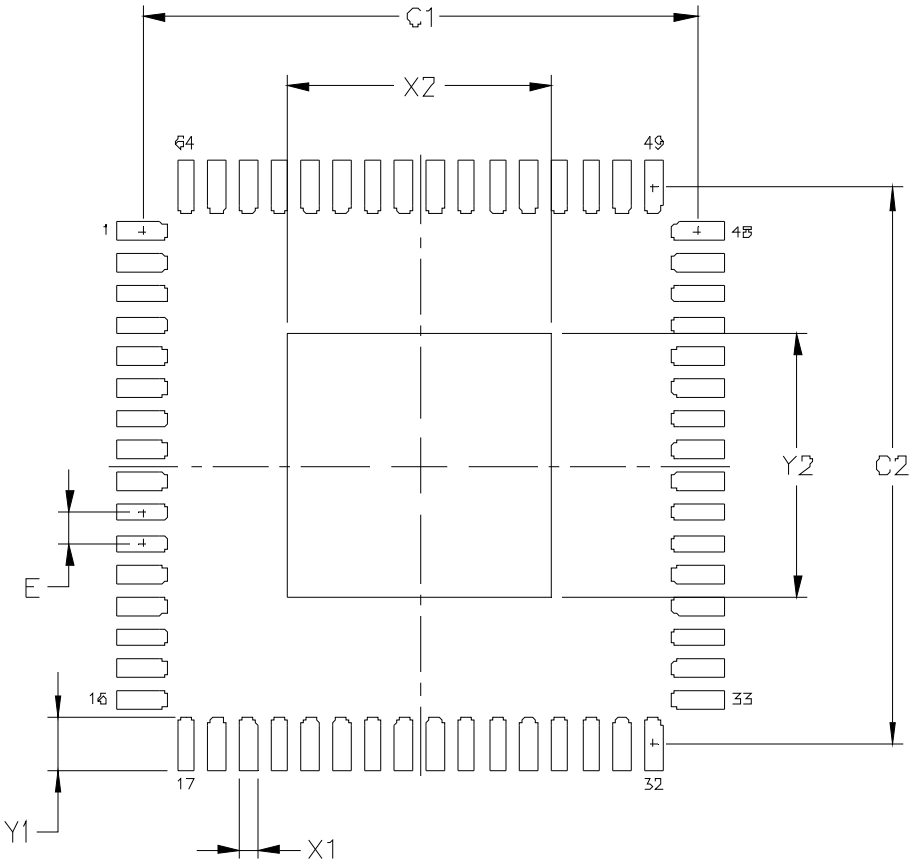


Figure 4. QFN-64 Landing Diagram

Table 13. QFN-64 Landing Diagram Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	4.25
Y2	4.25

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

4.2.1. QFN-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

4.1.1. QFN-64 Stencil Design

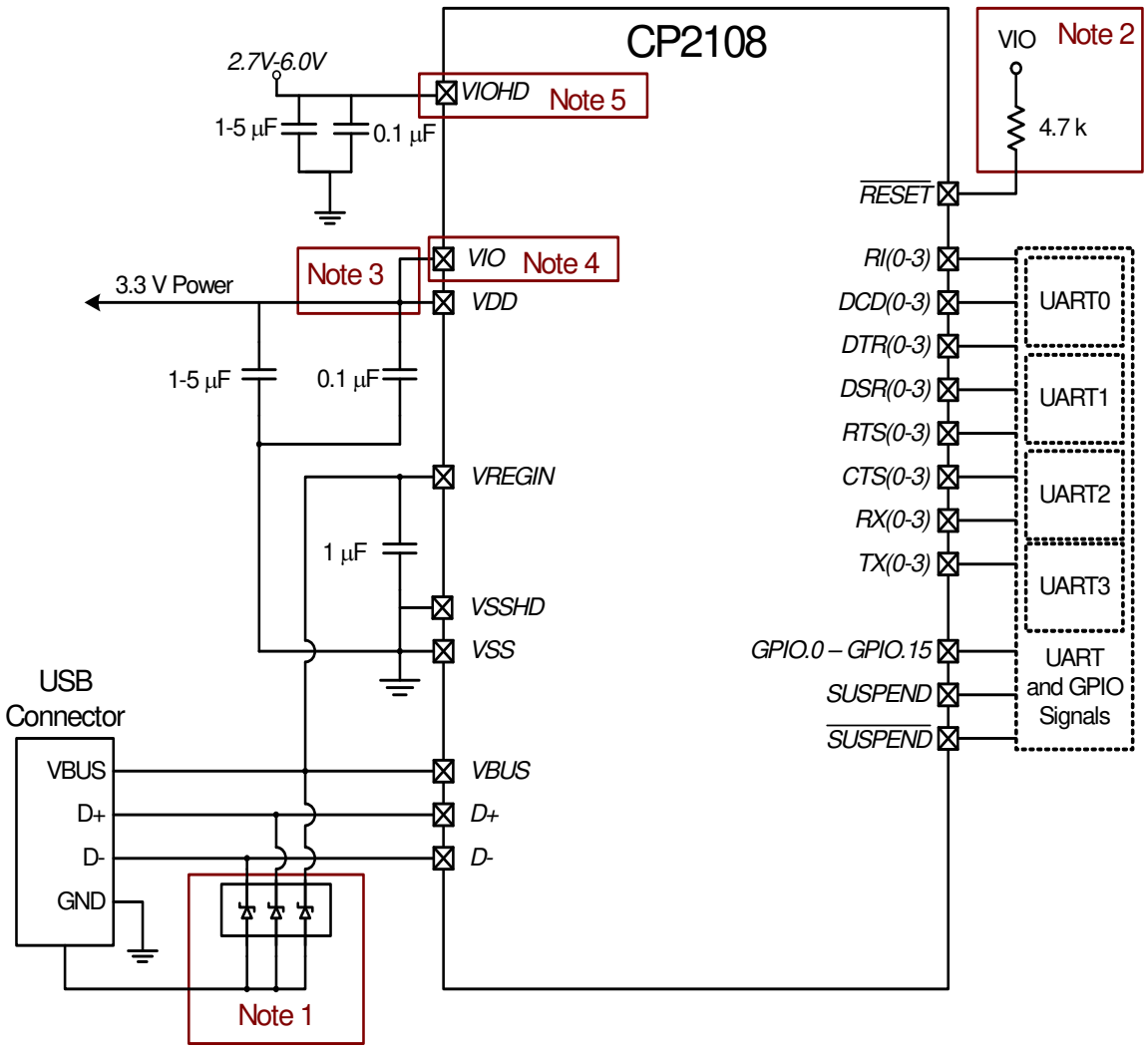
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.0 mm square openings on a 1.5 mm pitch should be used for the center ground pad.

4.1.2. QFN-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. Typical Connection Diagrams

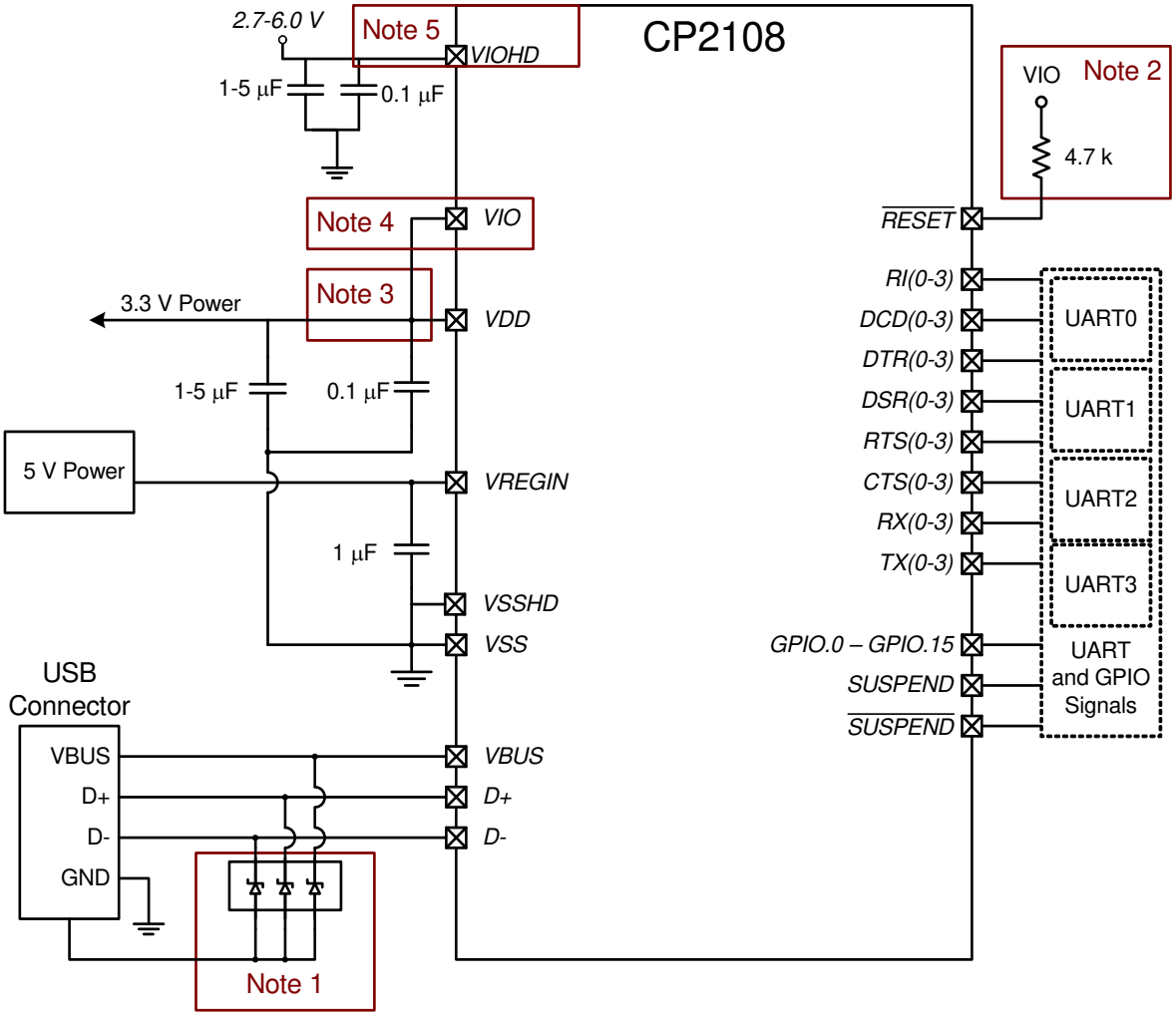
The CP2108 includes an on-chip 5 to 3.3 V voltage regulator, which allows the CP2108 to be configured as either a USB bus-powered device or a USB self-powered device. Figure 5 shows a typical connection diagram of the device in a bus-powered application using the regulator. When used, the voltage regulator output appears on the VDD pin and can be used to power external devices. See Table 6 for the voltage regulator electrical characteristics.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply in the range of 3.0-3.6 V.
Note 4: There are 2 VIO pins. All should be connected together. Each pin requires a separate 1 µF and a 0.1 µF capacitor. VIO can also be connected to VIOHD if VIOHD is in the range of 3.0-3.6 V.
Note 5 : VIOHD can be connected directly to VDD or to a supply in the range of 3.0-6 V.

Figure 5. Typical Bus-Powered Connection Diagram

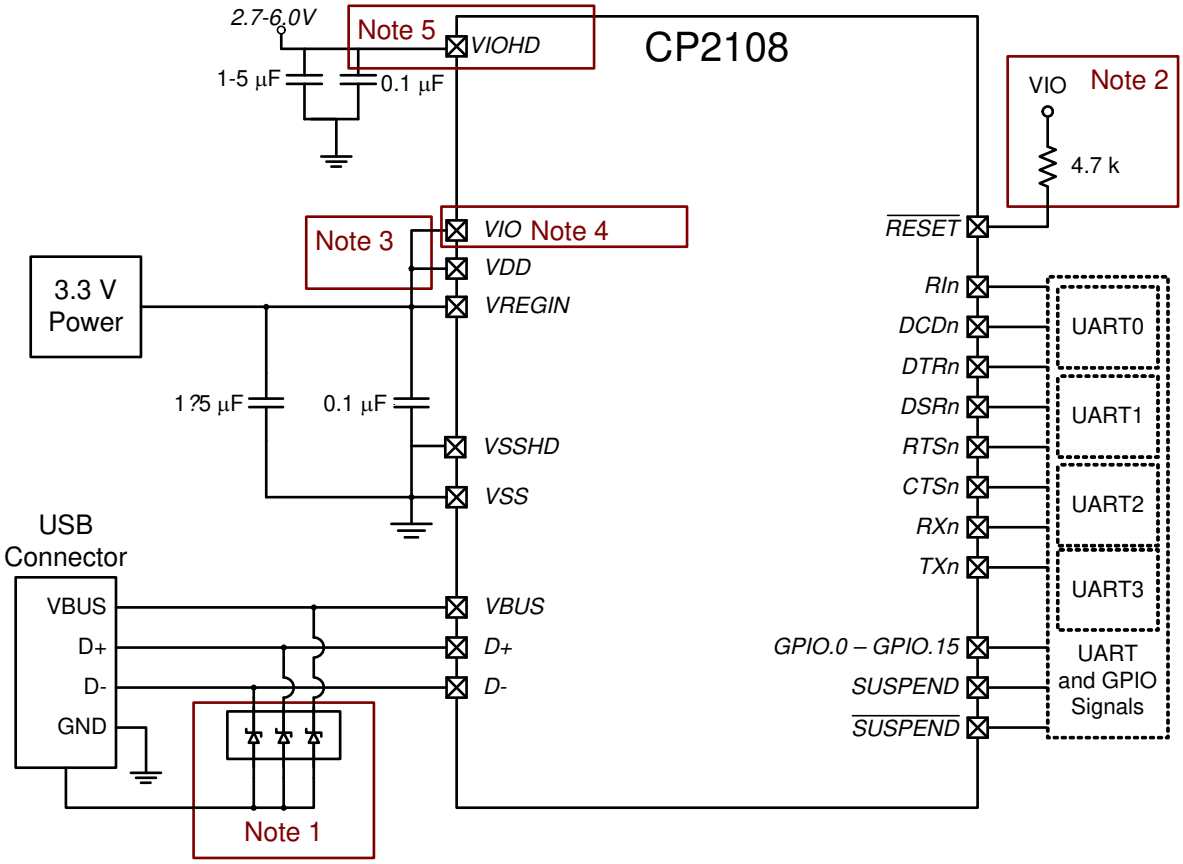
There are two configurations for self-powered applications: regulator used and regulator bypassed. To provide VDD in a self-powered application using the regulator, use the same connections from Figure 5, but connect VREGIN to an on-board 5 V supply and disconnect it from the VBUS pin. The typical self-powered connections with the regulator used is shown in Figure 6.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply in the range of 3.0-3.6 V.
Note 4: There are 2 VIO pins. All should be connected together. Each pin requires a separate 1 µF and a 0.1 µF capacitor. VIO can also be connected to VIOHD if VIOHD is in the range of 3.0-3.6 V.
Note 5 : VIOHD can be connected directly to VDD or to a supply in the range of 3.0-6 V.

Figure 6. Typical Self-Powered (Regulator Used) Connection Diagram

Alternatively, if 3.0 to 3.6 V power is supplied to the VDD pin, the CP2108 can function as a USB self-powered device with the voltage regulator bypassed. For this configuration, the VREGIN input should be tied to VDD to bypass the voltage regulator. Figure 7 shows a typical connection diagram showing the device in a self-powered application with the regulator bypassed.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply in the range of 3.0-3.6 V.
Note 4 : There are 2 VIO pins. All should be connected together. Each pin requires a separate 1 µF and a 0.1 µF capacitor. VIO can also be connected to VIOHD if VIOHD is in the range of 3.0-3.6 V.
Note 5 : VIOHD can be connected directly to VDD or to a supply in the range of 3.0-6 V.

Figure 7. Typical Self-Powered Connection Diagram (Regulator Bypass)

6. USB Function Controller and Transceiver

The Universal Serial Bus (USB) function controller in the CP2108 is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pull-up resistors. The USB function controller manages all data transfers between the USB and the UARTs as well as command requests generated by the USB host controller and commands for controlling the function of the UARTs and GPIO pins.

Device pins for UART 0–2 are powered by VIO, while UART 3 pins 1–6 are powered through VIOHD and are high drive pins. These high drive pins have higher input voltage requirements than other pins which are noted in all the electrical tables.

The USB Suspend and Resume signals are supported for power management of both the CP2108 device as well as external circuitry. The CP2108 will enter Suspend mode when Suspend signaling is detected on the bus. Upon entering Suspend mode, the CP2108 asserts the SUSPEND and SUSPEND signals. SUSPEND and SUSPEND signals are also asserted after a CP2108 reset until device configuration during USB enumeration is complete.

The CP2108 exits the Suspend mode when any of the following occur: resume signaling is detected or generated, a USB Reset signal is detected, or a device reset occurs. On exit of Suspend mode, the SUSPEND and SUSPEND signals are de-asserted. SUSPEND and SUSPEND are weakly pulled to VIO in a high impedance state during a CP2108 reset. If this behavior is undesirable, a strong pulldown (10 kΩ) can be used to ensure SUSPEND remains low during reset.

The logic level and output mode (push-pull or open-drain) of various pins during USB Suspend is configurable in the EEPROM. See Section 9 for more information.

The USB max power and power attributes descriptor must match the device power usage and configuration. See application note “AN721: CP210x/CP211x Device Customization Guide” on www.silabs.com/appnotes for information on how to customize USB descriptors for the CP2108.

7. Asynchronous Serial Data Bus (UART) Interfaces

The CP2108 contains four UART interfaces, each consisting of the TX (transmit) and RX (receive) data signals and RTS and CTS flow control signals. The UARTs also support modem flow control (DSR, DTR, DCD, RI).

The UARTs are programmable to support a variety of data formats and baud rates. The Virtual COM Port (VCP) drivers are used to set the data format and baud rate during COM port configuration on the PC. The data formats and baud rates available to each UART interface are listed in Table 14.

Table 14. Data Formats and Baud Rates (All UART Interfaces)

Data Bits*	5, 6, 7, 8 (normal mode or fixed mode)
Stop Bits	1, 1.5, 2
Parity Type	Odd, Even, Set, Mark, None
Baud Rate	300 bps to 2.0 Mbps*

***Note:** Review Table 10 for expected throughput based on selected UART Interface(s) and Baud Rate.

7.1. Baud Rate Generation

The baud rate generator for the interface is very flexible, allowing any baud rate in the range from 300 bps to 2.0 Mbps. If the baud rate cannot be directly generated from the 80 MHz oscillator, the device will choose the closest possible option. The actual baud rate is dictated by Equation 1 and Equation 2.

$$\text{Clock Divider} = \frac{80\ \text{MHz}}{2 \times \text{Requested Baud Rate}} - 1$$

Equation 1. Clock Divider Calculation

$$\text{Actual Baud Rate} = \frac{80\ \text{MHz}}{2 \times \text{Clock Divider}}$$

Equation 2. Baud Rate Calculation

Most baud rates can be generated with an error of less than 1.0%. A general rule of thumb for the majority of UART applications is to limit the baud rate error on both the transmitter and the receiver to no more than ±2%. The clock divider value obtained in Equation 1 is rounded to the nearest integer, which may produce an error source. Another error source will be the 80 MHz oscillator, which is accurate to ±0.25%. Knowing the actual and requested baud rates, the total baud rate error can be found using Equation 3.

$$\text{Baud Rate Error (\%)} = 100 \times \left(1 - \frac{\text{Actual Baud Rate}}{\text{Requested Baud Rate}}\right) \pm 0.25\%$$

Equation 3. Baud Rate Error Calculation

The UART interfaces support the transmission and reception of a line break. The CP2108 detects a line break when the RX line is held low for longer than one byte time at the configured baud rate. The length of a transmitted line break is application-specific: the application sends a SET_BREAK command to set the TX line low, and the line stays low until the application sends a CLEAR_BREAK command.

8. GPIO and UART Pins

The CP2108 supports sixteen user-configurable GPIO pins for status and control information. Each of these GPIO pins are usable as inputs, open-drain outputs, or push-pull outputs. By default, all of the GPIO pins are configured as a GPIO input. A logic high, open-drain output pulls the pin to the VIO rail through an internal, pull-up resistor. A logic high, push-pull output directly connects the pin to the VIO voltage. Open-drain outputs and push-pull outputs are identical when driving a logic low.

The speed to read and write the GPIO pins from an application is subject to the timing of the USB bus. GPIO pins configured as inputs or outputs are not recommended for real-time signaling.

In addition to the primary GPIO function, each GPIO pin has an alternate function listed in Table 15.

More information regarding the configuration and usage of the GPIO pins can be found in application note “AN721: CP210x/CP211x Customization Guide” available on the Silicon Labs website: www.silabs.com/appnotes.

Table 15. GPIO Mode Alternate Functions

GPIO Pin	Alternate Functions
GPIO.0	UART 0 TX Toggle
GPIO.1	UART 0 RX Toggle
GPIO.2	UART 0 RS-485
GPIO.3	Clock Output 0
GPIO.4	UART 1 TX Toggle
GPIO.5	UART 1 RX Toggle
GPIO.6	UART 1 RS-485
GPIO.7	Clock Output 1

GPIO Pin	Alternate Functions
GPIO.8	UART 2 TX Toggle
GPIO.9	UART 2 RX Toggle
GPIO.10	UART 2 RS-485
GPIO.11	Clock Output 2
GPIO.12	UART 3 TX Toggle
GPIO.13	UART 3 RX Toggle
GPIO.14	UART 3 RS-485
GPIO.15	Clock Output 3

8.1. GPIO Alternate Clock Outputs

There are four alternate clock outputs. The clock output frequency is shown in Equation 4. Each clock has a 1-byte divider value. GPIO pins 3,7,11, and 15 can output a configurable CMOS clock output. The clock output appears at the pin at the same time the device completes enumeration and exits USB Suspend mode. The clock output is removed from the pin when the device enters USB Suspend mode.

The clocks are derived by dividing the CP2108 core clock, allowing external components to be clocked synchronously with the CP2108.

$$\text{Clock Frequency Output} = \frac{40\ \text{MHz}}{2 \times \text{ClockDivider}}$$

Equation 4. Clock Frequency Output

Note: A clock divider value of 0x00 will be treated as 256.

8.2. GPIO: Transmit and Receive Toggle

GPIO.0, GPIO.1, GPIO.4, GPIO.5, GPIO.8, GPIO.9, GPIO.12, and GPIO.13 pins are configurable as Transmit Toggle and Receive Toggle pins for the four UART interfaces. These pins are logic high when a device is not transmitting or receiving data, and they toggle at a fixed rate as specified in Table 4 when data transfer is in progress. Typically, these pins are connected to two LEDs to indicate data transfer.

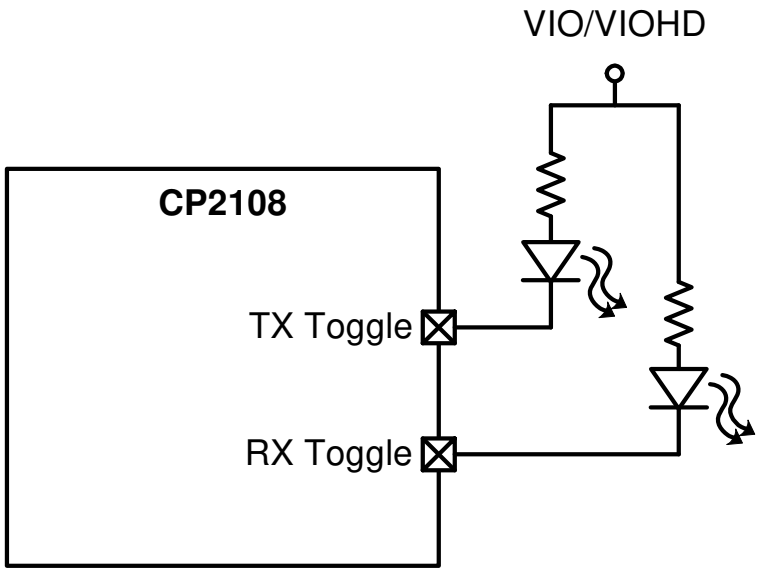


Figure 8. Transmit and Receive Toggle Typical Connection Diagram

8.3. RS-485 Transceiver Bus Control

GPIO.2, GPIO.6, GPIO.10, and GPIO.14 are alternatively configurable as RS-485 bus transceiver control pins. When configured for RS-485 mode, the pin is asserted during UART data transmission and line break transmission. The RS-485 mode is active-high by default, but the pins can also be configured for active-low mode.

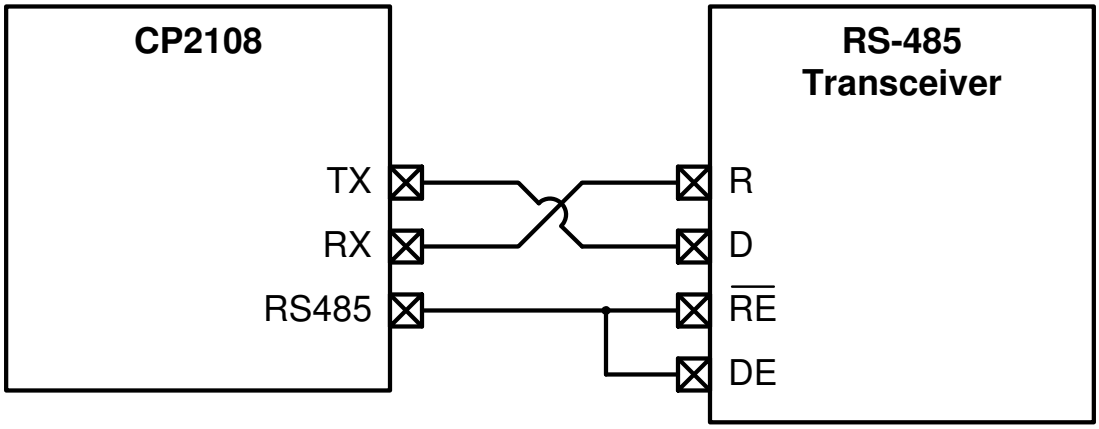


Figure 9. RS-485 Transceiver Typical Connection Diagram

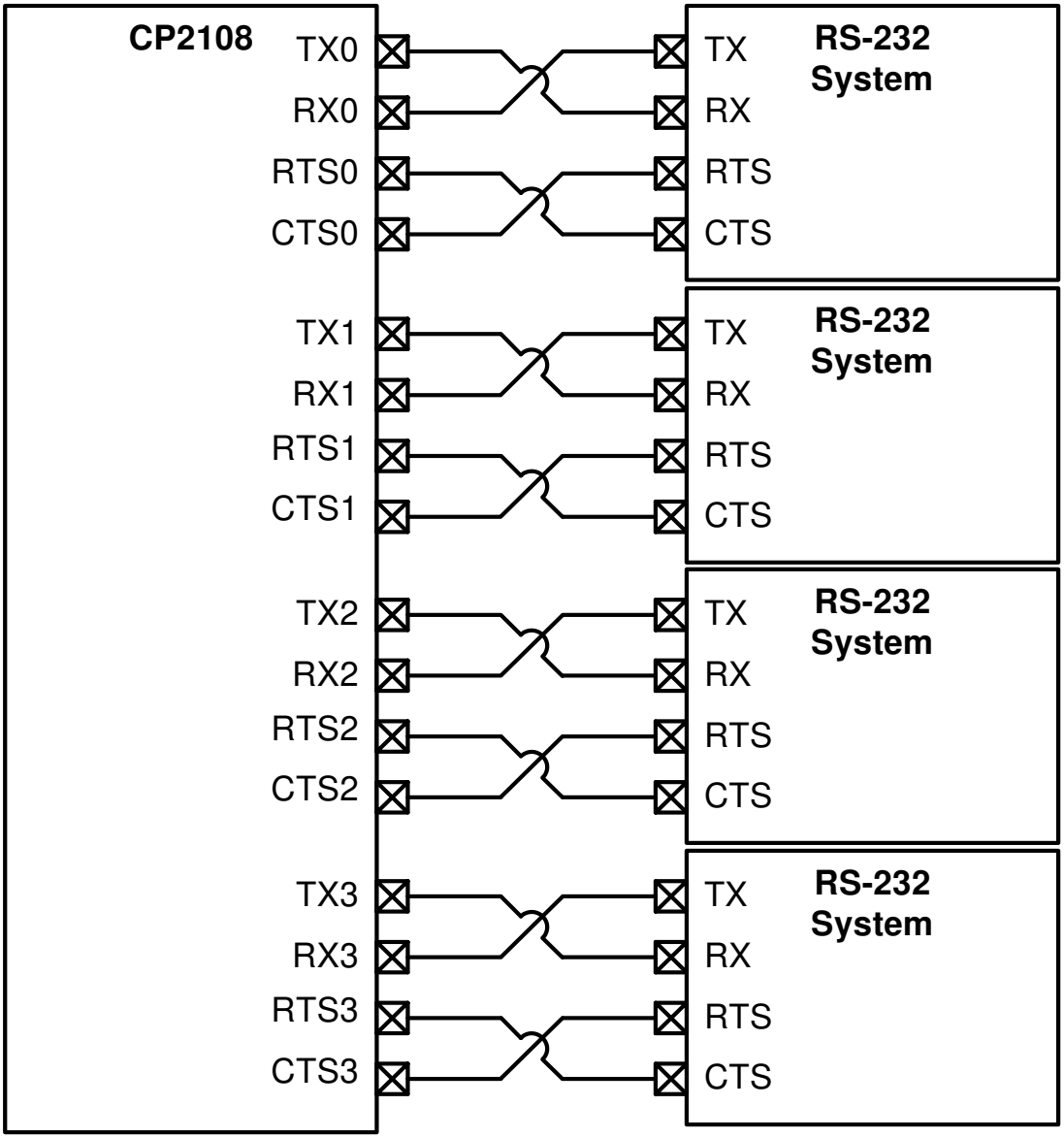


Figure 10. Hardware Flow Control Typical Connection Diagram

8.4. Hardware Flow Control (RTS and CTS)

To utilize the functionality of the RTS and CTS pins of the CP2108, each interface must be configured to use hardware flow control.

RTS, or Ready To Send, is an active-low output from the CP2108 and indicates to the external UART device that the CP2108's UART RX FIFO has not reached the watermark level of 1536 bytes and is ready to accept more data. When the amount of data in the RX FIFO reaches the watermark, the CP2108 pulls RTS high to indicate to the external UART device to stop sending data.

CTS, or Clear To Send, is an active-low input to the CP2108 and is used by the external UART device to indicate to the CP2108 when the external UART device's RX FIFO is getting full. The CP2108 will not send more than two bytes of data once CTS is pulled high.

The CP2108 stores the received data in internal buffers. It is possible for the CP2108 to receive data on the RX line before a handle to it is opened. In this case the user may wish to send the data to the USB pipe or may wish to flush it. Similarly, the user may close the handle while data is still in the internal transmit buffer. It may be desirable to continue sending all of the data out the TX pin after the handle has been closed. The flush buffer configuration options allow the user to define whether each buffer is flushed when a handle to the device is opened or closed. By default all the buffers will be flushed when a handle is opened and will not be flushed when a handle is closed. These options are configurable using AN721SW: CP210x/CP211x Customization Guide as shown in Figure 11.

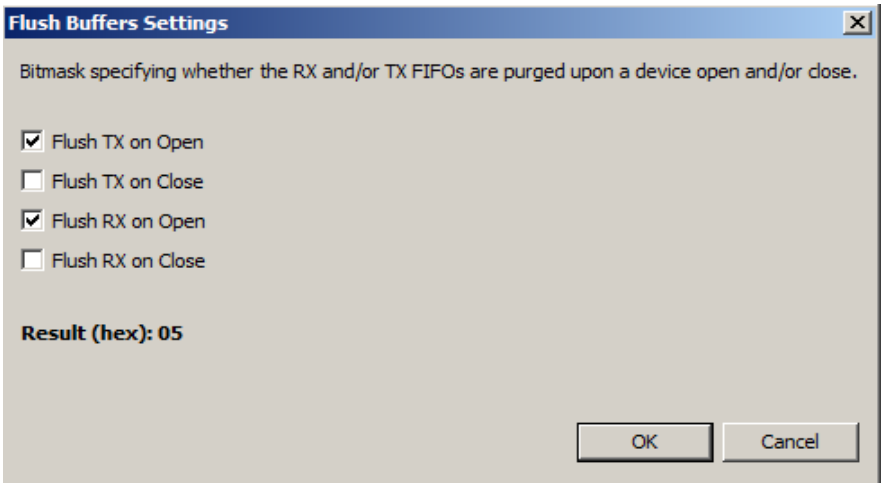


Figure 11. Flush Buffers Options in AN721SW Device Customization

8.5. High Drive Pins UART 3 Pins 1–6

The UART 3 pins 1–6 are high drive pins that have different input voltage conditions than the other UART and GPIO pins. If an input voltage for VDD, VIO, and VIOHD is used that is overlapping for the three ranges, then these pins can all be tied together. One of the benefits of this variation is that UART 3 can accept an input of up to 6 V and therefore can be connected directly to a 5 V device without additional circuitry.