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# USBXpress™ USB Audio to I2S Digital Audio Bridge Family

## CP2114 Data Sheet

The CP2114 devices, part of the USBXpress family, are designed to enable rapid development of USB-based audio applications.

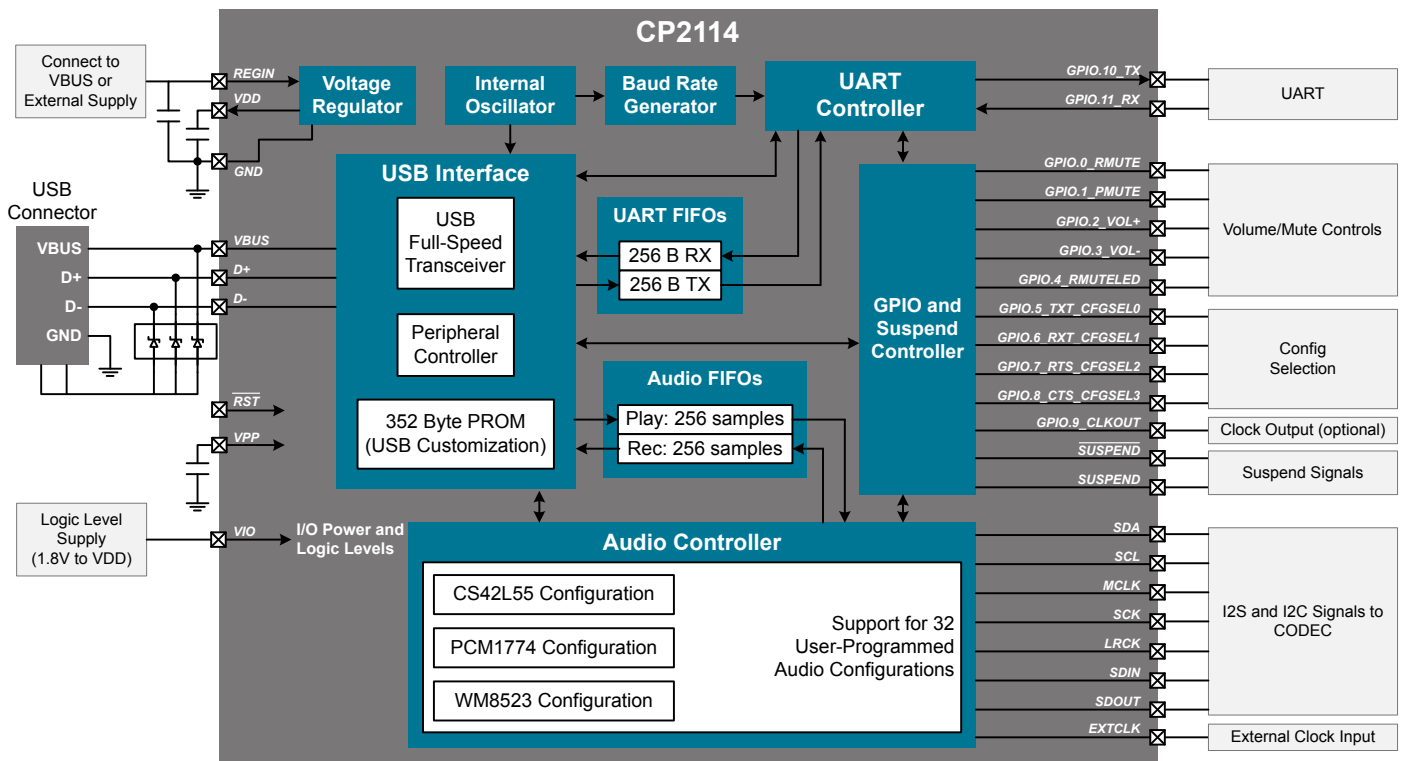
The CP2114 simplifies the process of transferring audio data from USB to I2S without any code development, speeding time to market for USB audio accessories such as USB speakers, USB headphones and USB music boxes, as well as VoIP systems. The CP2114 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, I2S (audio) interface, I2C (control) interface and UART interface in a compact 5 x 5 mm QFN-32 package ideal for space-constrained portable audio applications.

CP2114 is ideal for a wide range of USB Audio applications, including the following:

- USB speakers
- USB headphones/headsets
- MP3 accessories
- Point of sale terminals
- Navigation systems
- Music boxes

### KEY FEATURES

- Single chip USB Audio to I2S Digital Audio Bridge
- Supports USB HID Consumer Controls for Volume and Mute Synchronization
- Integrated USB transceiver; no external resistors required
- Integrated clock; no external crystal required
- On-chip voltage regulator: 3.45 V output
- Self-powered or Bus-powered
- No firmware development required



## 1. Feature List and Ordering Information

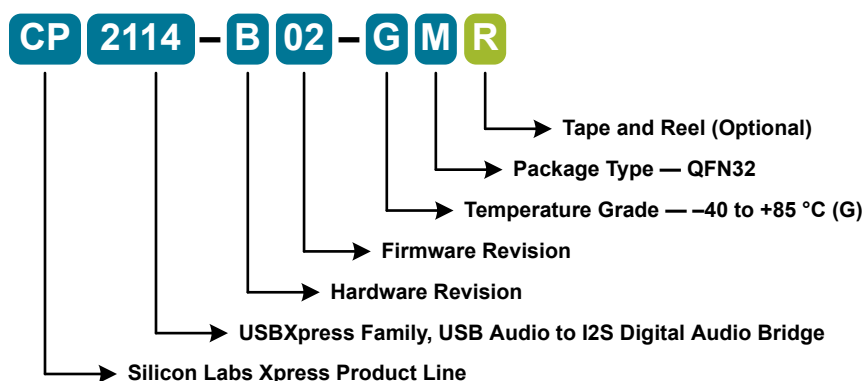


Figure 1.1. CP2114 Part Numbering

The CP2114 devices have the following features:

- **Single-Chip USB Audio to I<sup>2</sup>S Digital Audio Bridge**
  - USB HID to I<sup>2</sup>C to communicate with codecs
  - Supports I<sup>2</sup>C communication with other slave devices in the system (B02 only)
  - Supports I<sup>2</sup>S and left-justified audio interface formats
  - Supports USB HID Consumer Controls for Volume and Mute Controls
  - Integrated USB transceiver
  - Integrated clock; no external crystal required
  - Integrated One-Time Programmable ROM for product customization
  - On-chip voltage regulator
- **Supports a Wide Range of codecs**
  - Preloaded configurations for three popular codec DAC devices
  - Internal programmable memory supports additional codec configurations
- **USB Audio Class v1.0 support**
  - Natively supported (no custom driver required) on Windows/Mac/Linux/iOS
  - Supports 16-bit Play/Record at 48 kHz sample rate
  - Also supports 24-bit Play or Record (CP2114-B02 only)
  - Supports Asynchronous or Synchronous Modes
- **USB Peripheral Function Controller**
  - USB Specification 2.0 compliant; full-speed (12 Mbps)
  - USB Suspend states supported via SUSPEND pins
- **USB HID to UART Auxiliary Communication Interface**
  - APIs for quick application development
  - HID devices natively supported by Windows/Mac/Linux
- **12 Configurable GPIO Pins with Alternate Functions**
  - Usable as inputs, open-drain or push-pull outputs
  - UART signals, audio playback controls, codec select pins
  - Configurable clock output
  - Toggle LEDs upon UART transmission or reception
- **Supply Voltage**
  - Self-powered: 3.0 to 3.6 V
  - USB bus powered: 4.0 to 5.25 V
  - I/O voltage: 1.8 V to V<sub>DD</sub>
- **Package**
  - RoHS-compliant 32-pin QFN (5 x 5 mm)
- **Ordering Part Number**
  - CP2114-B02-GM
  - CP2114-B01-GM (not recommended for new designs)
- **Temperature Range: -40 to +85 °C**

**Note:**

1. For brevity, the term 'codec' is used to refer to the external audio device, which may be a codec, DAC, or ADC. The terms 'DAC' and 'ADC' are used when the context is applicable to only those devices.
2. The CP2114 may not operate correctly when connected to a USB hub. The most common problem in this configuration is audio packet loss.

## 2. Electrical Specifications

### 2.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [2.1.1 Recommended Operating Conditions](#), unless stated otherwise.

#### 2.1.1 Recommended Operating Conditions

**Table 2.1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage ( $V_{DD}$ )	$V_{DD}$		3.0	—	3.6	V
Digital Port I/O Supply Voltage ( $V_{IO}$ )	$V_{IO}$		1.8	—	$V_{DD}$	V
Digital Supply Current (USB Active Mode) <sup>1</sup>	$I_{DD}$	Bus Powered Mode Self Powered Mode with Regulator enabled Self Powered Mode with Regulator disabled	—	18	28	mA
Digital Supply Current (USB Suspend Mode) <sup>1</sup>	$I_{DD}$	Bus Powered Mode Self Powered Mode with Regulator enabled	—	750	940	$\mu$ A
		Self Powered Mode with Regulator disabled	—	0.99	1.2	mA
Supply Current - USB Pull-up <sup>2</sup>	$I_{PU}$		—	200	228	$\mu$ A
Operating Ambient Temperature	$T_A$		-40	—	85	$^{\circ}$ C

**Note:**

1. If the device is connected to the USB bus, the USB Pull-up Current should be added to the supply current for total supply current.
2. The USB Pull-up supply current values are calculated values based on USB specifications.

## 2.1.2 I2S, I2C, UART and Suspend I/O

**Table 2.2. I2S, I2C, UART and GPIO DC Electrical Characteristics**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -10 μA	V <sub>IO</sub> - 0.1	—	—	V
		I <sub>OH</sub> = -3 mA	V <sub>IO</sub> - 0.2	—	—	V
		I <sub>OH</sub> = -10 mA	—	V <sub>IO</sub> - 0.4	—	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 10 μA	—	—	0.1	V
		I <sub>OL</sub> = 8.5 mA	—	—	0.4	V
		I <sub>OL</sub> = 25 mA	—	0.6	—	V
Input High Voltage	V <sub>IH</sub>		V <sub>IO</sub> × 0.7	—	—	V
Input Low Voltage	V <sub>IL</sub>		—	—	0.6	V
Input Leakage Current	I <sub>LK</sub>	Weak Pull-Up Off	—	—	1	μA
		Weak Pull-Up On, V <sub>IO</sub> = 0 V	—	25	50	μA
Maximum Input Voltage	V <sub>IN_MAX</sub>	Open drain, logic high (1)	—	—	5.8	V

## 2.1.3 Reset

**Table 2.3. Reset Electrical Characteristics**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
/RST Input High Voltage	V <sub>IH</sub>		V <sub>IO</sub> × 0.75	—	—	V
/RST Input Low Voltage	V <sub>IL</sub>		—	—	0.6	V
Minimum /RST Low Time to Generate Reset	t <sub>RSTL</sub>		15	—	—	μs
V <sub>DD</sub> Ramp Time for Power On	t <sub>RMP</sub>		—	—	1	ms

## 2.1.4 Voltage Regulator

**Table 2.4. Voltage Regulator Electrical Specifications**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range	V <sub>REGIN</sub>		3.0	—	5.25	V
Output Voltage	V <sub>REGOUT</sub>	Output Current = 1 to 100 mA <sup>1</sup>	3.3	3.45	3.6	V
VBUS Detection Input Threshold	V <sub>VBUS</sub>		2.5	—	—	V
Bias Current	I <sub>REGOUT</sub>		—	—	120	μA

**Note:**

1. The maximum regulator supply current is 100 mA. This includes the supply current of the CP2114.

## 2.1.5 GPIO Output

**Table 2.5. GPIO Output Specifications**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
GPIO.9 Clock Output Tolerance	$f_{CLK}$		$f_{OUT} \times 0.985$	$f_{OUT}$	$f_{OUT} \times 1.015$	Hz
GPIO.9 Clock Output Programmable Frequency Range	$f_{RANGE}$	SYSCLK = 48 MHz	0.093750	—	24.0	MHz
		SYSCLK = 49.152 MHz	0.096000	—	24.576	MHz
TX Toggle Rate	$f_{TX}$		—	20	—	Hz
RX Toggle Rate	$f_{RX}$		—	20	—	Hz

## 2.1.6 One Time Programmable Memory

$V_{DD} = 3.3$  to  $3.6$  V,  $-40$  to  $+85$  °C unless otherwise specified.

**Table 2.6. One Time Programmable Memory Specifications**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Digital Port I/O Supply Voltage ( $V_{IO}$ ) during programming	$V_{PROG}$		3.3	—	$V_{DD}$	V
Voltage on $V_{PP}$ with respect to GND during a programming operation	$V_{PP}$	$V_{IO} \geq 3.3$ V	5.75	—	$V_{IO} + 3.6$	V
Capacitor on $V_{PP}$ for programming	$C_{PROG}$		—	4.7	—	$\mu$ F

## 2.1.7 System Clock

$V_{DD} = 3.3$  to  $3.6$  V,  $-40$  to  $+85$  °C unless otherwise specified.

**Table 2.7. System Clock Specifications**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Oscillator	$f_{OSC}$	SF/SystemClockFrequency = 0	—	48	—	MHz
		SF/SystemClockFrequency = 1	—	49.152	—	MHz
External CMOS clock input frequency	$f_{EXTOSC}$	SF/SystemClockFrequency = 0	47.880	48	48.120	MHz
		SF/SystemClockFrequency = 1	49.029	49.152	49.275	MHz

**Note:**

- Depending on the requirements of the external codec, the system clock frequency will be either 48.0 or 49.152 MHz. See [3.2.3 CP2114 Clock Configuration](#) for more information.
- The USB specification requires a clock accuracy of  $\pm 0.25\%$ .

## 2.1.8 I<sup>2</sup>S Digital Audio Interface

V<sub>DD</sub> = 3.3 to 3.6 V, -40 to +85 °C unless otherwise specified.

**Table 2.8. I<sup>2</sup>S Digital Audio Interface Specifications**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution (analog output)	N <sub>bits_out</sub>	PlaybackIs24Bit = 1 AudioInterfaceFormat = 1 (LJ)	—	24	—	bits
		PlaybackIs24Bit = 1 AudioInterfaceFormat = 0 (I2S)	—	23	—	bits
		PlaybackIs24Bit = 0	—	16	—	bits
Resolution (analog input)	N <sub>bits_in</sub>	RecordIs24Bit = 1 AudioInterfaceFormat = 1 (LJ)	—	24	—	bits
		RecordIs24Bit = 1 AudioInterfaceFormat = 0 (I2S)	—	23	—	bits
		RecordIs24Bit = 0 AudioInterfaceFormat = 1 (LJ)	—	16	—	bits
		RecordIs24Bit = 0 AudioInterfaceFormat = 0 (I2S)	—	15	—	bits
MCLK frequency	f <sub>MCLK</sub>	SYSCLK = 48 MHz	—	12	—	MHz
		SYSCLK = 49.152 MHz	—	12.288	—	MHz
LRCK frequency	f <sub>LRCK</sub>		—	48	—	MHz
SCK frequency	f <sub>SCK</sub>	SYSCLK = 48 MHz	—	3.429	—	MHz
		SYSCLK = 49.152 MHz	—	3.511	—	MHz
MCLK/LRCK jitter		SCS = 0 (external Si500S clock)	—	20	—	ps RMS <sup>1</sup>
		SCS = 1 (internal oscillator)	—	140	—	ps RMS <sup>1</sup>
<b>Note:</b>						
1. Measurement bandwidth: 100 Hz – 40 kHz.						

## 2.1.9 I<sup>2</sup>C

V<sub>DD</sub> = 3.3 to 3.6 V, -40 to +85 °C unless otherwise specified.

**Table 2.9. I<sup>2</sup>C Specifications**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL frequency	f <sub>SCL</sub>	I2C_CK = 0	—	400	—	kHz
		I2C_CK = 1	—	100	—	kHz

### 2.1.10 Analog Output/Input Characteristics (CS42L55 Daughtercard)

Data in the table below represents performance at 25 °C, bus-powered, USB synchronization mode: asynchronous, digital audio interface mode: I2S, DAC/ADC gains set to 0 dB, test signal for analog output: uncompressed WAV file, full-scale sine wave at 997 Hz, measurement bandwidth 20 Hz to 20 kHz Additional parameters that apply to this table are as follows:

- VA = VCP = VLDO = 2.5 V
- Internal oscillator mode

**Table 2.10. Analog Output/Input Characteristics (CS42L55 daughtercard)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Output (Line Output)						
THD + Noise		0 dB input	—	-80	—	dB
		-20 dB input	—	-91	—	dB
		-60 dB input	—	-91	—	dB
Dynamic Range		A-weighted	—	92	—	dB
Noise Level		Output muted	—	-112	—	dB
Frequency response		20 Hz – 20 kHz	—	+0.03, -0.07	—	dB
Analog Input						
THD + Noise		-1 dB input	—	-85	—	dB
		-20 dB input	—	-87	—	dB
		-60 dB input	—	-87	—	dB
Dynamic Range		A-weighted	—	90	—	dB
Noise Level		Analog input locally muted	—	0 <sup>1</sup>	—	sample values
<b>Note:</b>						
1. When analog input is locally muted, the CP2114 transmits sample values of 0 to the host.						



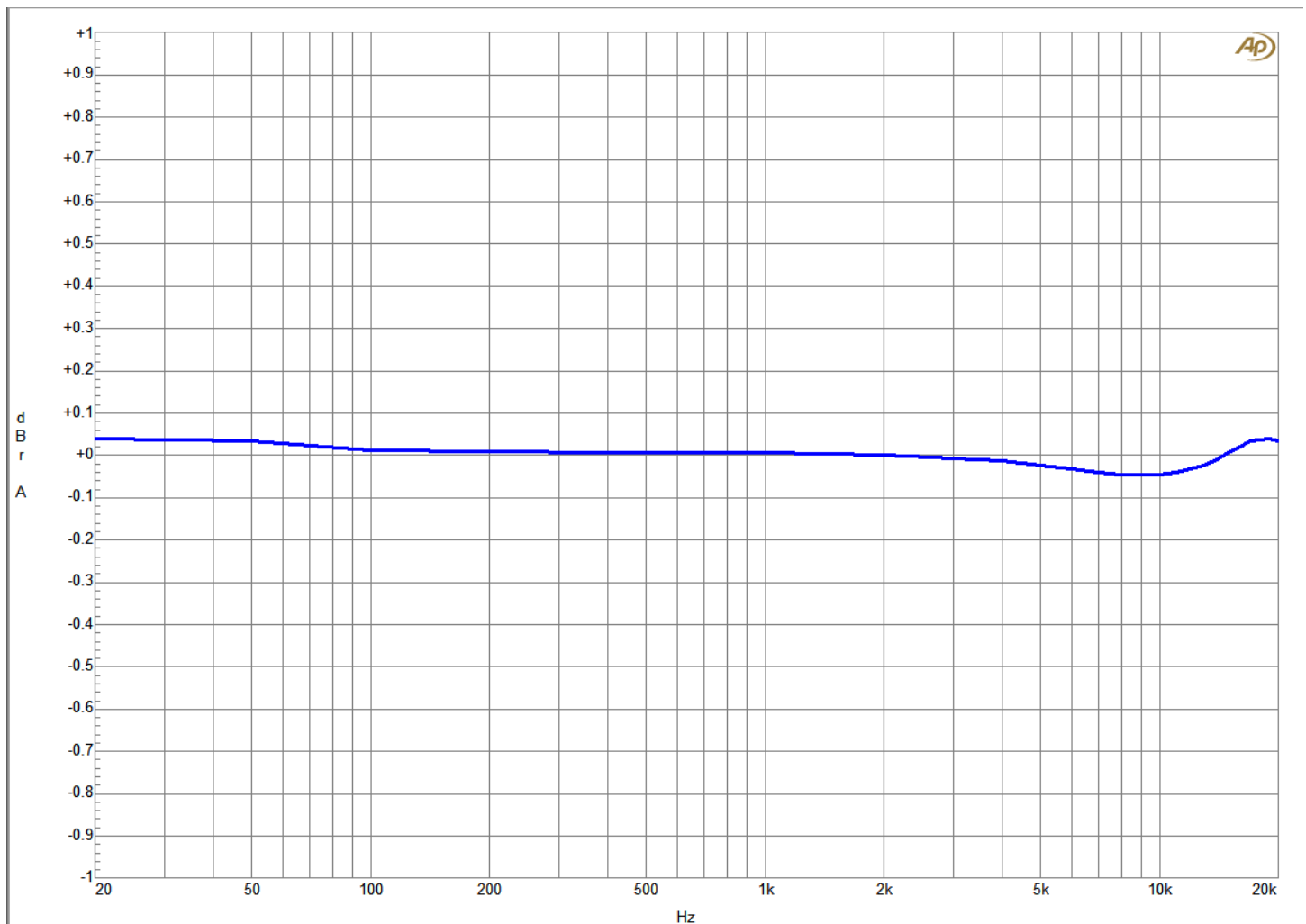
### 2.1.11 Analog Output/Input Characteristics (WM8523 Daughtercard)

Data in the table below represents performance at 25 °C, bus-powered, USB synchronization mode: asynchronous, digital audio interface mode: I2S, DAC/ADC gains set to 0 dB, test signal for analog output: uncompressed WAV file, full-scale sine wave at 997 Hz, measurement bandwidth 20 Hz to 20 kHz Additional parameters that apply to this table are as follows:

- LINEVDD = AVDD = 3.3 V
- Internal oscillator mode
- External headphone amplifier disconnected, no lowpass filter on LINEVOUTL/LINEVOUTR

**Table 2.11. Analog Output/Input Characteristics (WM8523 daughtercard)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
THD + Noise		0 dB FS input	—	-83	—	dB
		-20 dB FS input	—	-91	—	dB
		-60 dB FS input	—	-91	—	dB
Dynamic Range		A-weighted	—	94	—	dB
Noise Level		Output muted	—	-99	—	dB
Frequency response		20 Hz – 20 kHz	—	+0.04, -0.05	—	dB



**Figure 2.1. WM8523 Frequency Response (0 dB FS)**

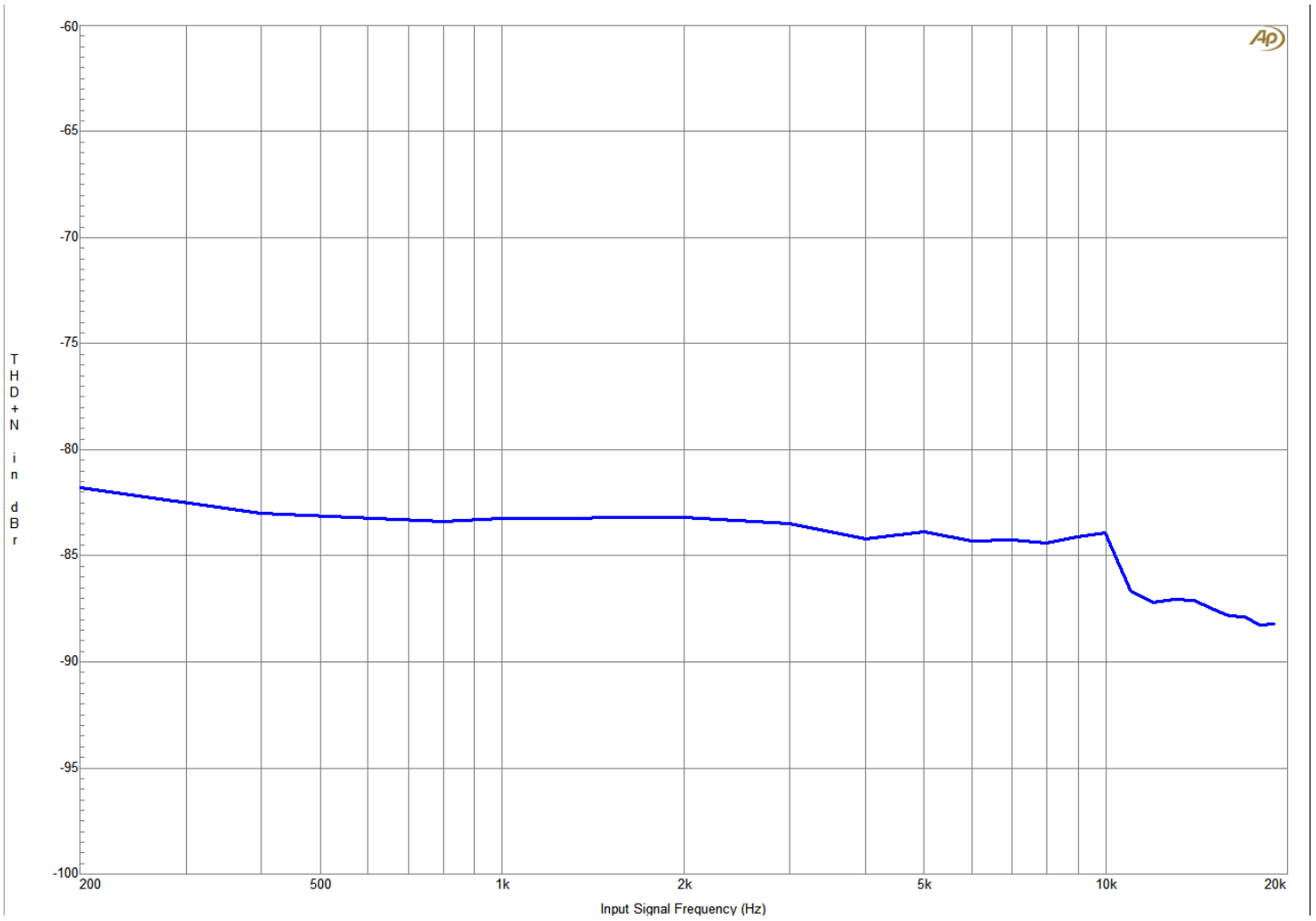


Figure 2.2. WM8523 THD+N vs. Frequency (0 dB FS)

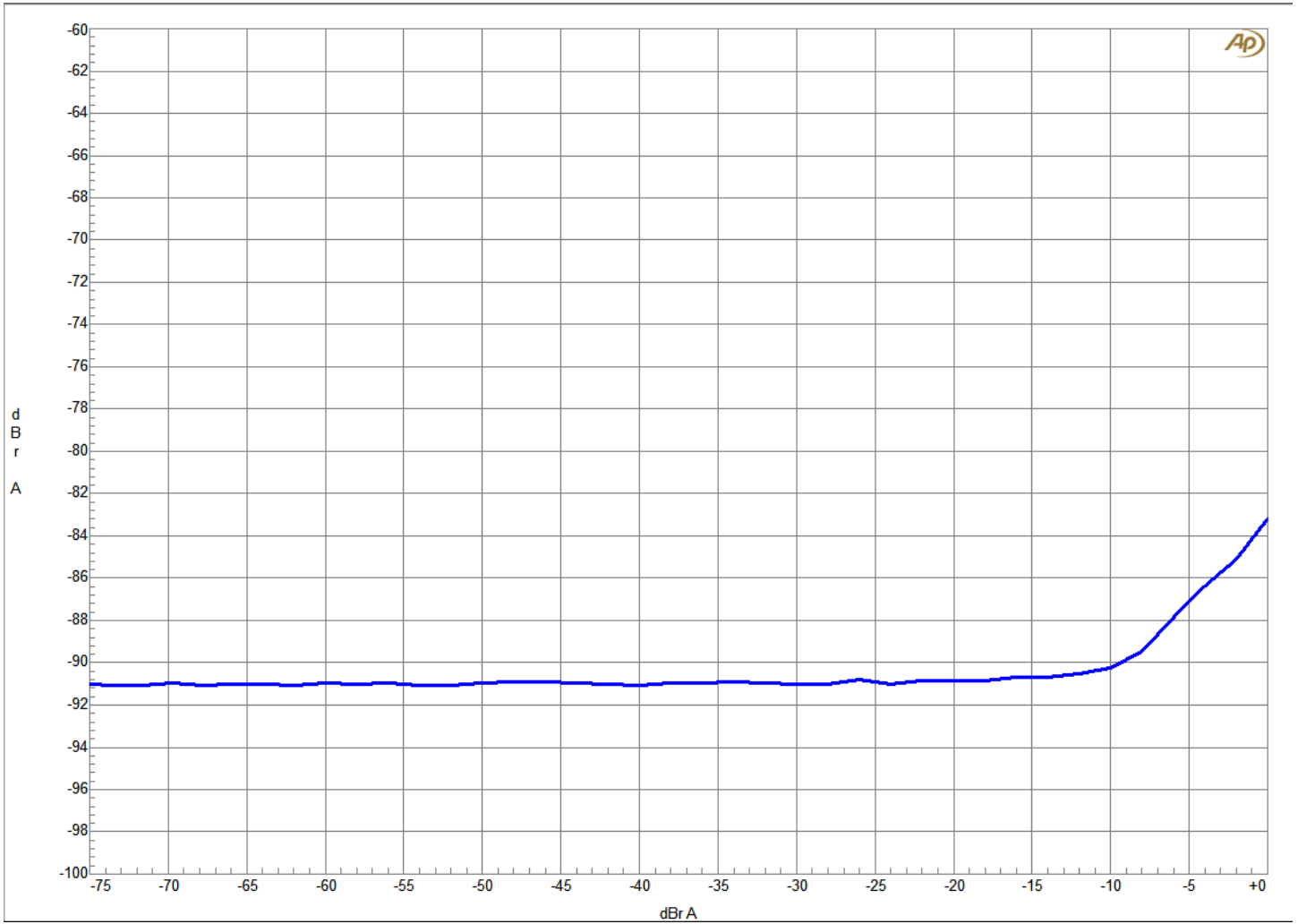


Figure 2.3. WM8523 THD+N vs. Amplitude (997 Hz)

### 2.1.12 Analog Output/Input Characteristics (PCM1774 Daughtercard)

Data in the table below represents performance at 25 °C, bus-powered, USB synchronization mode: asynchronous, digital audio interface mode: I2S, DAC/ADC gains set to 0 dB, test signal for analog output: uncompressed WAV file, full-scale sine wave at 997 Hz, measurement bandwidth 20 Hz to 20 kHz Additional parameters that apply to this table are as follows:

- VIO = VDD = VCC = VPA = 3.3 V
- AOUT\_L and AOUT\_R outputs have 4.7 Ω series resistors
- Internal oscillator mode

**Table 2.12. Analog Output/Input Characteristics (PCM1774 daughtercard)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
THD + Noise		0 dB FS input	—	-82	—	dB
		-20 dB FS input	—	-89	—	dB
		-60 dB FS input	—	-89	—	dB
Dynamic Range		A-weighted	—	89	—	dB
Noise Level		Output muted	—	-103	—	dB
Frequency response		20 Hz – 20 kHz	—	+0.04, -0.11	—	dB

## 2.2 Thermal Conditions

**Table 2.13. Thermal Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	$\theta_{JA}$	Air velocity = 0 m/s	—	25	—	°C/W

**Note:**

1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

### 2.3 Absolute Maximum Ratings

Stresses above those listed in [2.3 Absolute Maximum Ratings](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 2.14. Absolute Maximum Ratings**

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	$T_{BIAS}$		-55	125	°C
Storage Temperature	$T_{STG}$		-65	150	°C
Voltage on /RST, GPIO, I <sup>2</sup> S, I <sup>2</sup> C, or UART Pins with respect to GND	$V_{IN}$	$V_{IO} \geq 2.2\text{ V}$	-0.3	5.8	V
		$V_{IO} < 2.2\text{ V}$	-0.3	$V_{IO}+3.6$	V
Voltage on VBUS with respect to GND	$V_{BUS}$	$V_{DD} \geq 3.0\text{ V}$	-0.3	5.8	V
		$V_{DD}$ not powered	-0.3	$V_{IO}+3.6$	V
Voltage on $V_{DD}$ with respect to GND	$V_{DD}$		-0.3	4.2	V
Voltage on $V_{IO}$ with respect to GND	$V_{IO}$		-0.3	4.2	V
Maximum Total Current through $V_{DD}$ , $V_{IO}$ , and GND	$I_{VDD}$		—	500	mA
Maximum Output Current Sunk by /RST or any I/O pin	$I_{IO}$		—	100	mA

**Note:**

1. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 3. Functional Description

### 3.1 System Overview

All major operating systems (e.g. Windows, Linux, Mac, iOS, Android) contain drivers that support the standard Universal Serial Bus Device Class Definition for Audio Devices Release 1.0. This specification is often abbreviated as 'USB Audio Class 1' or 'UAC1'. Codecs typically have only an I<sup>2</sup>S (Inter-IC Sound) digital interface, and thus cannot connect directly to a host system. In addition, when a codec is powered on, it typically must be configured by the host via an I<sup>2</sup>C (inter-integrated-circuit) digital interface, with a non-standard protocol. Finally, in order to support push button volume and mute controls, the target USB device must support the standard USB-HID Consumer Control interface. Thus, adding USB digital audio to an embedded system or as dongle or appliance typically involves complex USB protocol programming as well as I<sup>2</sup>S and I<sup>2</sup>C programming capability, prototyping, integration and testing. The CP2114 USB Audio Bridge is specifically designed to overcome all these issues and commoditize USB Audio and codec configuration for turn-key product development.

The CP2114 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, one-time programmable read-only memory (ROM), I<sup>2</sup>S (audio) interface, I<sup>2</sup>C (control) interface, and UART interface in a compact 5 x 5 mm QFN-32 package (sometimes called "MLF" or "MLP"). The one-time programmable ROM on the device may be used to customize both product information (including USB fields such as Vendor ID, Product ID, Strings, etc...) and external codec configuration strings. The CP2114 provides the following features:

- Enumerates to the host as a standard USB Audio Class 1 device and HID Consumer Control supporting:
  - USB Digital Audio Out (Audio Playback Device)
  - USB Digital Audio In (Microphone/Recording Device)
  - HID Consumer Control handling standard volume and mute functionality
- Pre-configured support for 3 commercial codecs
  - Handles all I<sup>2</sup>C configuration of the codec automatically at boot
  - Handles all volume and mute traffic converting from USB to I<sup>2</sup>C messages to the codec
- Tested for USB plug & play and audio quality on all major operating systems

**Note:** Using the CP2114 with a host that does not provide a standard USB type-A receptacle (e.g. iOS device) may require the use of an appropriate hardware adapter.

- UART interface using standard USB HID device class which is natively supported by most operating systems
  - No custom driver required
  - Dynamic libraries provided for Windows/Mac/Linux
  - Supports hardware flow control (CTS, RTS)
  - Baud rate support from 375 to 1 Mbps, support for 5-8 data bits, 5 parity options, 3 stop bit options
- 12 GPIO signals support alternate functions
  - Volume control, UART transmit and receive, UART hardware flow control, UART transmit/receive toggle, configurable clock output, and codec selection
  - Support for I/O interface voltages down to 1.8 V is provided via a VIO pin.

Various CP2114 Evaluation Kits are available. Contact a Silicon Labs sales representatives or go to [www.silabs.com](http://www.silabs.com) to order a CP2114 Evaluation Kit.

### 3.2 Audio Interface

The I<sup>2</sup>S interface provides the digital audio stream and related clock signals to the codec.

### 3.2.1 Audio Interface Modes — I<sup>2</sup>S and Left-Justified

The CP2114 supports I<sup>2</sup>S and Left-Justified digital audio formats. Note that the difference in the two modes is that for the I<sup>2</sup>S format, the MSB of the data streams (SDOUT and SDIN) are delayed by one clock (SCK) cycle after the channel clock (LRCK) transitions as compared to the Left Justified format. The digital audio format can be configured in the CP2114 one-time programmable ROM.

The MCLK (Master Clock) and LRCK (Left/Right Clock) outputs are derived from SYSCLK and have a fixed phase relationship. Although the SCK (Serial Clock) signal is also derived from SYSCLK, the phase relationship of SCK to MCLK and LRCK is not fixed.

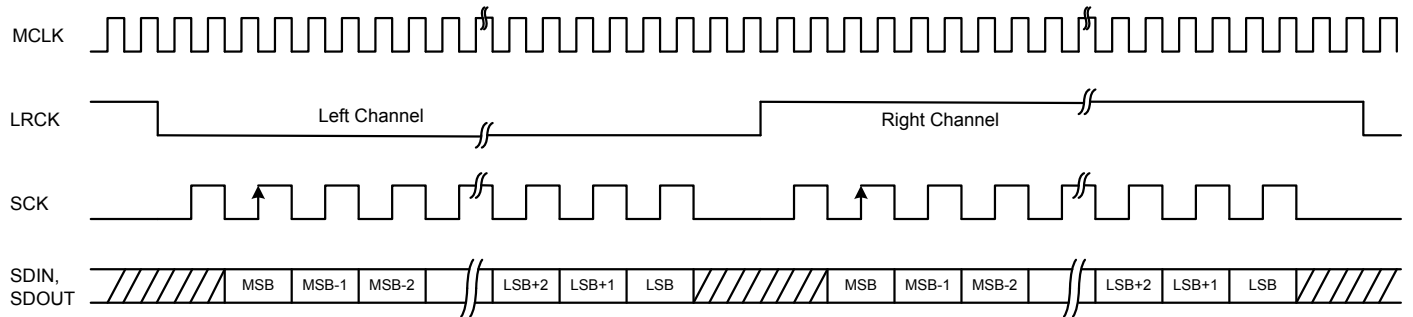


Figure 3.1. I<sup>2</sup>S Format

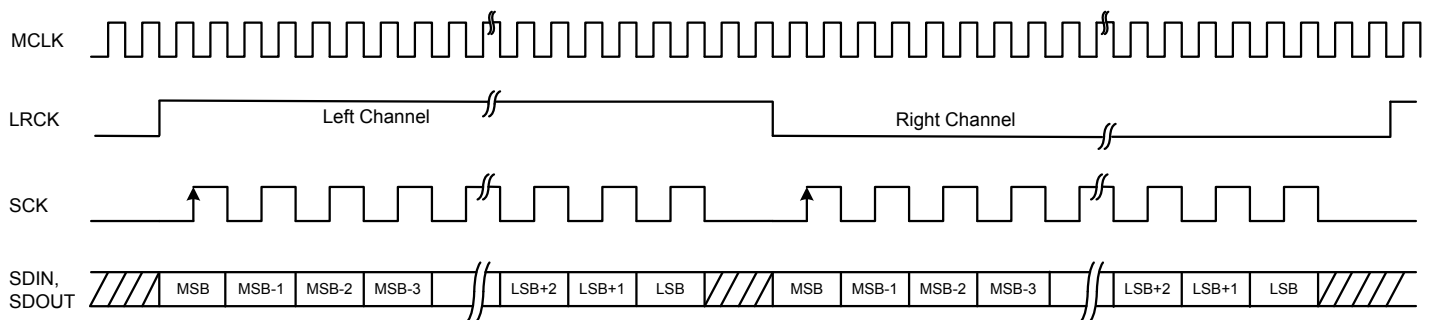


Figure 3.2. Left-Justified Format

**MCLK**

Master Clock. This is a high frequency clock to the connected audio used for the Digital to Analog conversion process within the connected audio device. This clock will be a multiple of the LRCK going to the connected audio device. Typically  $MCLK = 250 \cdot LRCK$  or  $MCLK = 256 \cdot LRCK$ .

**LRCK**

Left-Right Clock (WS in I<sup>2</sup>S specification). This is used to synchronize the connected audio device audio data word timing with the CP2114 audio data word timing (i.e., edges are used to synchronize the beginning of the left and right audio samples).

**SCK**

Serial Bit Clock. This provides a timing signal used by the connected audio device to latch the audio output data bits on SDOUT and assert the audio input data bits on SDIN.

**SDOUT**

Serial audio data output, typically connected to an external DAC.

**SDIN**

Serial audio data input, typically connected to an external ADC.

**Note:** MCLK, LRCK, SCK and SDOUT are driven by the CP2114. SDIN is driven by the connected audio device.

The CP2114 supports only 48 kHz, 16 bit digital audio. This is typically not an issue for source USB audio as the device capabilities are reported to the host and any sample rate conversion (for say 44.1 kHz audio) is done automatically by the host. However, some audio devices may require 24-bit digital audio data on the I<sup>2</sup>S data stream. In this case, the CP2114 will send the useful 16-bit audio to the connected audio device on SDOUT in the most significant 16 bits and pad the remaining 8 bits of data with 0s. Likewise the CP2114 will read the MSB 16 bits of data on DIN and throw out the LSB 8 bits from SDIN. The CP2114 can be configured in 16 bit or 24 bit mode via a configuration option in the CP2114 one-time programmable ROM.

### 3.2.2 USB and Digital Audio Clock Requirements

The CP2114 supports a number of clock configurations allowing support for a variety of audio devices and associated clocking options to optimize cost and quality. The two clocks of consideration are:

- USB Clock — Full speed USB requires devices have a 12 MHz clock with tolerance of  $\pm 0.25\%$ . This means the USB device (CP2114) must maintain its USB clock in the range of  $11.97 \text{ MHz} < \text{USB Clock} < 12.03 \text{ MHz}$ . This range is supported by the CP2114 which also has built-in USB clock recovery. However, it does have implications on the audio device.
- Digital Audio Clock (MCLK) — Audio devices typically require that MCLK must be a multiple of LRCK, and this multiple is typically required to be 250 or 256. Given an audio sample rate of  $LRCK = 48 \text{ kHz}$ , the resulting MCLK requirement is shown in the equations below.

$$MCLK = 250 \times 48 \text{ kHz} = 12.000 \text{ MHz}$$

$$MCLK = 256 \times 48 \text{ kHz} = 12.288 \text{ MHz}$$

An audio device accepting a multiple of 250 is thus compatible with USB clock requirements, whereas an audio device requiring a 256 multiple is fundamentally incompatible with USB clock requirements. In this case, an external 48.000 MHz or 49.152 MHz clock is required. The CP2114 clocking configurations are discussed in [3.2.3 CP2114 Clock Configuration](#).



### 3.2.3 CP2114 Clock Configuration

The CP2114 always reports its capabilities to the USB host at a sample rate of 48 kHz and sample size of 16 bits. For source audio files differing from this format the USB host will automatically perform sample rate conversion. The CP2114 has the following configuration options:

**Table 3.1. Clock Configuration Options**

Configuration Parameter	Options
Stream Type	Asynchronous Synchronous
USB Clock Source	Internal External
System Clock Source	Internal External
System Clock Frequency	48 MHz 49.152 MHz
MCLK/LRCK Ratio	250 256

The table below shows all possible clock configuration settings for the CP2114. The CP2114 divides the USB source clock by 4 so a clock of 48 MHz provides the 12 MHz clock needed for USB. The CP2114 divides the system clock by 4 to derive MCLK. So a 48 MHz system clock will generate MCLK = 12 MHz.

When operating in Synchronous Mode, the CP2114 continually adjusts its internal oscillator to match the host sample rate. Operating in Synchronous Mode with an external SYSCLK is not recommended because the inevitable host/device clock mismatch causes periodic sample buffer overrun or underrun, which results in audio glitches.

In Asynchronous Mode the CP2114 clock is held at a constant frequency and the inevitable host/device clock mismatch is accommodated through the use of explicit or implicit feedback as dictated in the relevant USB specifications. Operating in Asynchronous Mode can provide significantly better THD+N performance, especially when the THD+N analyzer has a very narrow notch filter. (Per the AES17 standard, a standard notch filter used for THD+N testing must have an electrical Q of at least 1 and not more than 5.) The best THD+N performance is obtained in Asynchronous Mode using an external low-jitter clock.

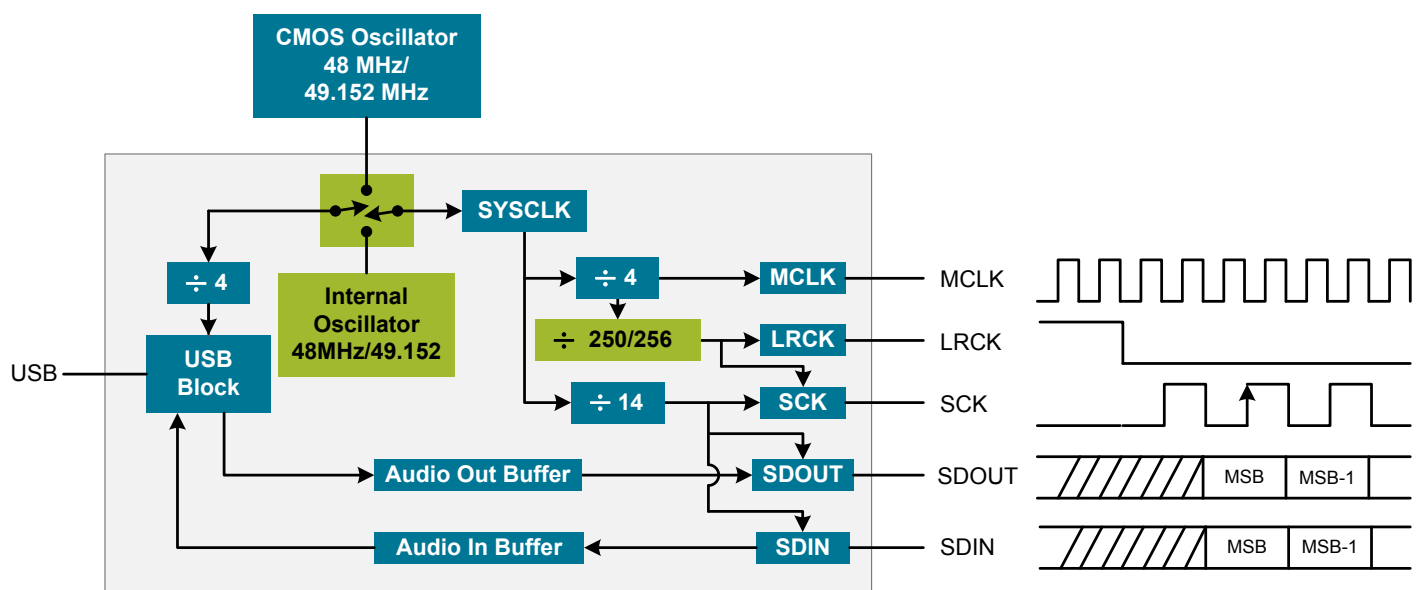
**Table 3.2. Valid Clock Configuration Modes**

Mode	USB Clock (USBCLK) Source	System Clock (SYSCLK) Source	Int Freq (MHz)	MCLK/LRCK Ratio	Ext Osc Freq (MHz)	Notes
1	Int	Int	48	250	NA	<ul style="list-style-type: none"> <li>Lowest cost - no external clock required</li> <li>Audio device must support 12.0 MHz MCLK</li> <li>Sync mode: IntOsc adjusted to accommodate clock mismatch</li> </ul>
2	Int	Ext	48	256	49.152	<ul style="list-style-type: none"> <li>Async mode: best audio quality</li> <li>Sync mode: not recommended when using external SYSCLK</li> </ul>
3	Ext	Int	48 49.152	250 256	48	<ul style="list-style-type: none"> <li>IntOsc frequency dictated by audio device MCLK/LRCK ratio</li> <li>Sync mode: IntOsc adjusted to accommodate clock mismatch</li> </ul>
4	Ext	Ext		250	48	<ul style="list-style-type: none"> <li>Audio device must support 12.0 MHz MCLK</li> <li>Async mode: best audio quality</li> <li>Sync mode: not recommended when using external SYSCLK</li> </ul>

The following figure shows the clocking scheme, with the configurable options shown in light green/black text boxes.

- The USB clock frequency must always be 48 MHz whether using the internal or an external oscillator.
- MCLK is SYSCLK/4 and so will be 12 MHz or 12.288 MHz (as determined by the audio device clock requirement).
- LRCK is MCLK divided by 250 or 256 in order to get the correct 48 kHz sample rate conversion.
  - For MCLK = 12.288 MHz, the LRCK divisor must be 256.
  - For MCLK = 12.000 MHz, the LRCK divisor must be 250.

**Note:** An external oscillator is required if the codec oversampling rate is 256.



**Figure 3.3. Clock Configuration Block Diagram**

### 3.3 USB Function Controller and Transceiver

The Universal Serial Bus (USB) function controller in the CP2114 is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pullup resistors. The USB function controller manages all control, audio, and UART transfers between the USB and the CP2114. The USB Suspend and Resume modes are supported for power management of both the CP2114 device as well as external circuitry. The CP2114 will enter Suspend mode when Suspend signaling is detected on the bus. On entering Suspend mode, the Suspend signals are asserted. The Suspend signals are also asserted after a CP2114 reset until device configuration during USB enumeration is complete. The SUSPEND pin is logic high when the device is in the Suspend state, and logic low when the device is in the normal mode. The /SUSPEND pin has the opposite logic value of the SUSPEND pin.

The CP2114 exits Suspend mode when any of the following occur: Resume signaling is detected or generated, a USB Reset signal is detected, or a device reset occurs. SUSPEND and /SUSPEND are weakly pulled to VIO in a high impedance state during a CP2114 reset. If this behavior is undesirable, a strong pull-down (10 k $\Omega$ ) can be used to ensure /SUSPEND remains low during reset.

The logic level and output mode (push-pull or open-drain) of various pins during USB Suspend is configurable in the PROM. See [3.6 One-Time Programmable ROM](#) for more information.

#### 3.3.1 Real-Time Programming

The USB HID interface of the CP2114 can be used to:

- Read and write one-time-programmable parameters (e.g. device and audio configurations)
- Read and write dynamically-programmable parameters (e.g. GPIO state)
- Read and write codec registers via I<sup>2</sup>C
- Read and write other I<sup>2</sup>C slave devices (B02 only)

For more information, see the following documents:

- *AN433: CP2110/CP2114 HID to UART API Specification*
- *AN434: CP2110/4 Interface Specification*

### 3.4 Asynchronous Serial Data Bus (UART) Interfaces

The UART interface consists of the TX (transmit) and RX (receive) data signals as well as RTS (ready to send) and CTS (clear to send) flow control signals. The UART is programmable to support a variety of data formats and baud rates. The data formats and baud rates available are listed in the table below.

**Table 3.3. Data Formats and Baud Rates**

Parameter	Value
Data Bits	5, 6, 7, and 8
Stop Bits	1, 1.5 <sup>1</sup> , and 2
Parity Type	None, Even, Odd, Mark, Space
Baud Rate	375 bps to 1 Mbps <sup>2</sup>
<b>Note:</b> 1. 1.5 stop bits only available when using 5 data bits. 2. Baud rates above 500,000 baud are not supported with 5 or 6 data bits.	

On the USB bus, audio data transfers take priority over HID transfers used for UART transmit/receive data. Similarly, the CP2114 prioritizes audio-related tasks above UART-related tasks, which receive processing time only on an as-available basis. For this reason, the available UART transmit/receive throughput will be (sometimes significantly) less than the maximum possible throughput for the given baud rate and character size.

The CP2114 maximum usable baud rate and average UART data transfer throughput are highly dependent on the following conditions:

- Audio play and/or record streaming (Active/Inactive)
- Communication mode (Simplex/Duplex)
- Flow control mechanism (Hardware/None)

When using hardware flow control the maximum baud rate of 1 Mbps may be used as long as the remote terminal behaves properly when the CP2114 deasserts its RTS output (i.e. the remote terminal should not transmit additional characters after its CTS input becomes deasserted). If this is not the case, the maximum usable baud rate may be less than 1 Mbps.

With no flow control, the maximum usable baud rates depend on audio activity and whether the UART communication is simplex or duplex:

**Table 3.4. Maximum Baud Rates with Hardware Flow Control Disabled**

Audio Activity	Maximum Baud Rate (bps)
No Audio	230400
Play Only	64000
Record Only	57600
Play and Record	28800 (simplex)
	9600 (duplex)

The baud rate generator for the UART interface is very flexible, allowing the user to request any baud rate in the range from 375 bps to 1 Mbps. The actual baud rate is dictated by the equations below.

$$\text{Ideal Clock Divider} = \frac{48 \text{ MHz}}{2 \times \text{Requested Baud Rate}}$$

$$\text{Integer Clock Divider} = \text{Floor}(\text{Ideal Clock Divider})$$

$$\text{Actual Baud Rate} = \frac{48 \text{ MHz}}{2 \times \text{Integer Clock Divider}}$$

In both equations,  $\text{Floor}(\text{Clock Divider})$  represents the integer part of the Clock Divider computed above.

Most baud rates can be generated with an error of less than 1.0%. A general rule of thumb for the majority of UART applications is to limit the baud rate error on both the transmitter and the receiver to no more than  $\pm 2\%$ . The clock divider value obtained in the first equation above is rounded to the nearest integer, which may produce an error source. Another error source will be the 48 MHz oscillator, which is accurate to  $\pm 0.25\%$ . Knowing the actual and requested baud rates, the total baud rate error can be found using the following equation.

$$\text{Baud Rate Error (\%)} = 100 \times \left( 1 - \frac{48 \text{ MHz}}{2 \times \text{Integer Clock Divider}} \right) \pm 0.25\%$$

When the system clock is 49.152 MHz, the specified baud rate should be the desired baud rate divided by 1.024 to compensate for the 2.4% difference in clock speeds. For example, to achieve a baud rate of 115200 bps on a system with the system clock set to 49.152 MHz, the specified baud rate should be  $115200 / 1.024 = 112500$ .

The UART also supports the transmission of a line break. The length of time for a line break is programmable from 1 to 125 ms, or it can be set to transmit indefinitely until a stop command is sent from the application.

### 3.5 GPIO Pins

The CP2114 supports twelve user-configurable GPIO pins. Each of these GPIO pins are usable as inputs, open-drain outputs, or push-pull outputs. All of the pins have alternate functions which are listed in the table below. To use the pin as a GPIO, the pin must first be configured for that mode. More information regarding the configuration and usage of these pins is available in *AN721: CP210x/CP21xx Device Customization Guide* available on the Silicon Labs website. The configuration of the pins is one-time programmable for each device. See [3.6 One-Time Programmable ROM](#) for more information about programming the GPIO pin functionality.

**Table 3.5. GPIO Alternate Functions**

Pin	Default Function	Alternate Function 1 (GPIO Function)	Alternate Function 2
GPIO.0_RMUTE	Record Mute	GPIO.0	—
GPIO.1_PMUTE	Playback Mute	GPIO.1	—
GPIO.2_VOL-	Volume Down	GPIO.2	—
GPIO.3_VOL+	Volume Up	GPIO.3	—
GPIO.4_RMUTELED	Record Mute LED	GPIO.4	—
GPIO.5_TXT_CFGSEL0	Config Selector 0	GPIO.5	TX Toggle
GPIO.6_RXT_CFGSEL1	Config Selector 1	GPIO.6	RX Toggle
GPIO.7_RTS_CFGSEL2	Config Selector 2	GPIO.7	UART RTS
GPIO.8_CTS_CFGSEL3	Config Selector 3	GPIO.8	UART CTS
GPIO.9_CLKOUT	Clock Output	GPIO.9	—
GPIO.10_TX	UART TX	GPIO.10	—
GPIO.11_RX	UART RX	GPIO.11	—

The difference between an open-drain output and a push-pull output is when the GPIO output is driven to logic high. A logic high, open-drain output pulls the pin to the VIO rail through an internal, pull-up resistor. A logic high, push-pull output directly connects the pin to the VIO voltage. Open-drain outputs are typically used when interfacing to logic at a higher voltage than the VIO pin. These pins can be safely pulled to the higher, external voltage through an external pull-up resistor. The maximum external pull-up voltage is 5 V.

The speed of reading and writing the GPIO pins is subject to the timing of the USB bus. GPIO pins configured as inputs or outputs are not recommended for real-time signaling.

### 3.5.1 GPIO.0-4—Audio Playback and Record

The CP2114 includes several audio playback and record signals, such as volume increase, volume decrease, playback mute, and record mute. When connected over USB, the CP2114 can control the host volume settings with these pins via the standard USB HID Consumer Control Interface. On the CP2114 evaluation board, these pins are all connected to buttons. Single-pressing the volume increase (GPIO.3\_VOL+) and volume decrease (GPIO.2\_VOL-) buttons will increase or decrease the volume; holding the button will continue increasing or decreasing the volume. If playback is muted, changing the volume with either of these buttons will unmute playback. In addition, there are two mute functions implemented as well. Single-pressing the record mute (GPIO.0\_RMUTE) and the playback mute (GPIO.1\_PMUTE) buttons will toggle between mute and unmute states. When record is muted, the signal GPIO.4\_RMUTELED will be driven low (and illuminate an LED on the evaluation board).

### 3.5.2 GPIO.5-8—Config Selection

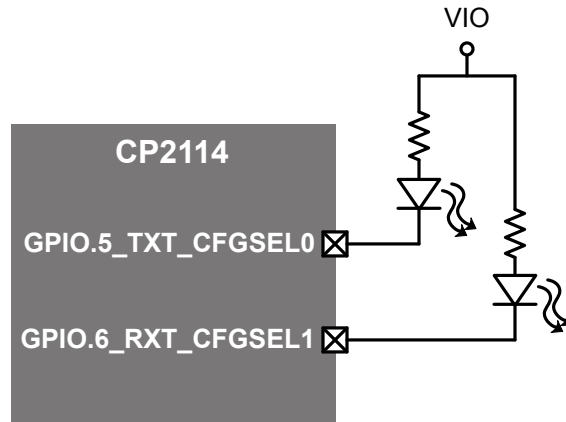
The state of GPIO.5 through GPIO.8 specify which configuration will be loaded after reset. By default, GPIO.5, GPIO.6, GPIO.7, and GPIO.8 are all configured for the Config Select function (Alternate Function 1). If the four GPIO.5 through GPIO.8 pins are all configured as Config Select inputs (their default configuration), the state of these pins specifies which configuration will be loaded after reset (see Table 22). The boot configuration specified by the one-time programmable ROM will be used if the state of these Config Select pins is 1110b (Index 14), or if any of the four GPIO.5-8 pins have been configured to something other than Config Select. The Default Configuration option (1111b, i.e., Index 15) should be used when bringing up a new codec. Using this configuration, configuration text files can be written to RAM and tested until the configuration string is finalized. At that point, the configuration string can be programmed into the one-time programmable ROM. Config selection pin mapping is shown in the table below.

**Table 3.6. Config Selection Pin Mapping**

Index	GPIO.8 CFGSEL3	GPIO.7 CFGSEL2	GPIO.6 CFGSEL1	GPIO.5 CFGSEL0	Boot Configuration
0	0	0	0	0	Config[0]: CS42L55
1	0	0	0	1	Config[1]: WM8523
2	0	0	1	0	Config[2]: PCM1774
3	0	0	1	1	User-programmed configurations
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	Default Configuration

### 3.5.3 GPIO.5-6—UART Transmit and Receive Toggle

GPIO.5 and GPIO.6 are configurable as UART Transmit Toggle and Receive Toggle pins. These pins are logic high when a device is not transmitting or receiving data, and they toggle at a fixed rate as specified in [2.1.5 GPIO Output](#) when UART data transfer is in progress. Typically, these pins are connected to two LEDs to indicate data transfer.



**Figure 3.4. Transmit and Receive Toggle Typical Connection Diagram**

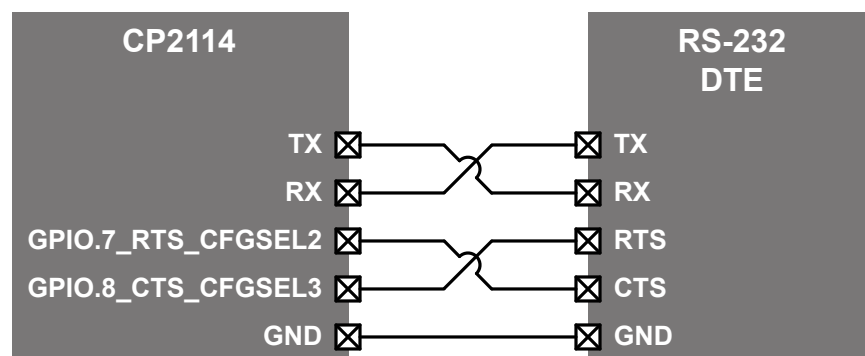
**Note:** Reconfiguring either of these pins as TXT or RXT disables the Config Select function.

### 3.5.4 GPIO.7-8—Hardware Flow Control (RTS and CTS)

To utilize the functionality of the RTS and CTS pins of the CP2114, the device must be configured to use hardware flow control.

RTS, or Ready To Send, is an active-low output from the CP2114 and indicates to the external UART device that the CP2114's UART RX FIFO has not reached the watermark level and is ready to accept more data. When the CP2114 is processing audio, the watermark level is 2 bytes. When the CP2114 is not processing audio, the watermark is 226 bytes. When the amount of data in the RX FIFO reaches the watermark, the CP2114 pulls RTS high to indicate to the external UART device to stop sending data.

CTS, or Clear To Send, is an active-low input to the CP2114 and is used by the external UART device to indicate to the CP2114 when the external UART device's RX FIFO is getting full. The CP2114 will not send more than two bytes of data once CTS is pulled high.



**Figure 3.5. Hardware Flow Control Typical Connection Diagram**

**Note:** Reconfiguring either of these pins as RTS or CTS disables the Config Select function.

### 3.5.5 GPIO.9—Clock Output

GPIO.9 is configurable to output a configurable CMOS clock output. The clock output appears at the pin at the same time the device completes enumeration and exits USB Suspend mode. The clock output is removed from the pin when the device enters USB Suspend mode. The output frequency is determined by the formula:

$$\text{GPIO.9 Clock Frequency} = \frac{\text{SYSCLK}}{2 \times \text{Clock Divider}}$$

**Note:** A Clock Divider value of 0 behaves as if it were 256. All other Clock Divider values are interpreted literally.

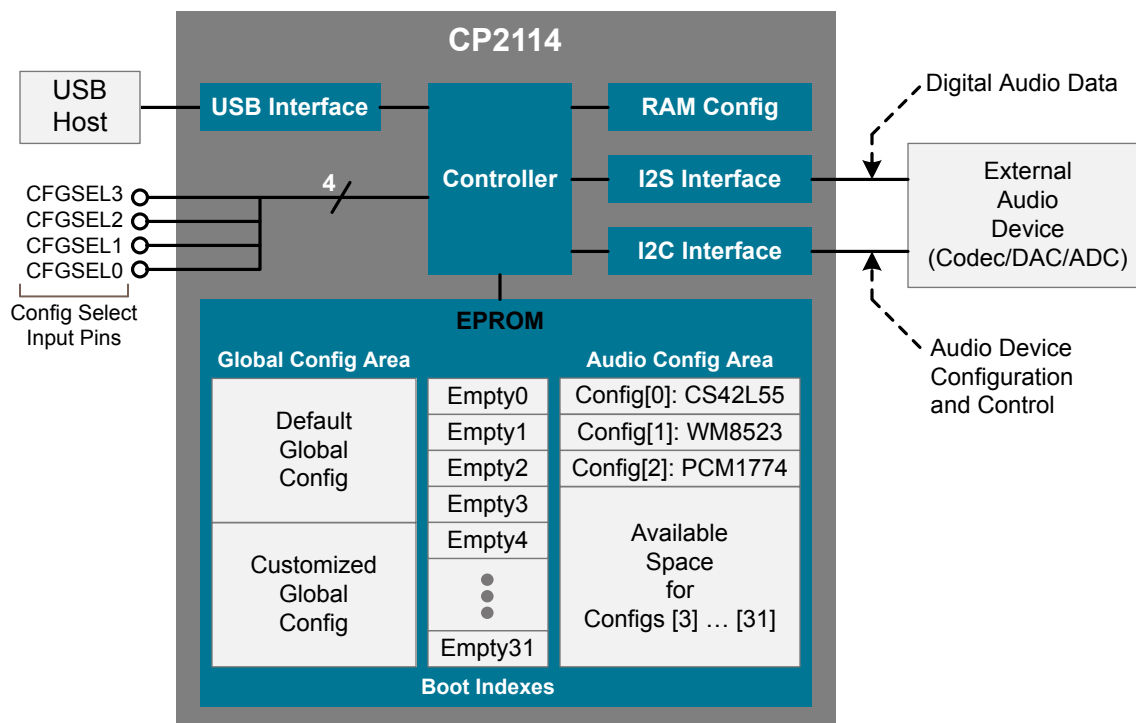
### 3.6 One-Time Programmable ROM

The CP2114 has an internal one-time programmable ROM used to store device and audio configuration information. There are two configuration areas in the one-time programmable ROM:

1. Global configuration area. This area stores the USB string descriptors and GPIO pin configuration. The CP2114 ships with default global configuration settings that allow the CP2114 to be used as-is for customer production. There is also a Customer Global Configuration area that provides customization of the device if desired.
2. Audio configuration area. This area stores up to 32 different audio configurations. The configurations determine the behavior of the CP2114 audio functions as well as contain configuration data for the external codec.

The one-time programmable ROM is shown in Figure 14. Note that the CP2114 standard device ships with three preprogrammed for three different audio configurations, with the desired configuration being selected via the Config Select pins (CFGSEL0, CFGSEL1, CFGSEL2, CFGSEL3). Additional configurations can be added by the user, and configuration of that codec is controlled by a one-time programmable ROM setting or by the Config Select pins. If the programmable ROM has not been programmed, the device uses the default configuration data shown in [Table 3.12 Default USB Configuration Data on page 41](#) and [Table 3.13 Default GPIO Data on page 41](#).

The configuration data ROM can be programmed by Silicon Labs prior to shipment with the desired configuration information. It can also be programmed in-system over the USB interface. If the configuration ROM is to be programmed in-system, a 4.7 μF capacitor must be present between the VPP pin and ground. No other circuitry should be connected to VPP during a programming operation, and VIO must remain at 3.3 V or higher to successfully write to the configuration ROM.



**Figure 3.6. One-Time Programmable ROM Configuration Block Diagram**



### 3.6.1 One-Time Programmable ROM Configuration Programming

The CP2114 contains onboard one-time programmable ROM to store up to 32 different audio configurations. Three of the 32 slots are preprogrammed configurations, which leaves 29 slots available for user customization. The configurations can be selected as boot configurations and will automatically configure the CP2114 and the I2C connected codec when the CP2114 is powered on. Alternatively, any of the first 14 custom configurations can be used as the boot configuration by setting the state of the Config Select pins. The boot configuration is then selected by pin-strapping the CFGSEL (config select) pins. Silicon Labs provides software tools to program configurations in CP2114 one-time programmable ROM. The CP2114 can also be programmed in-situ on a production line, or can be provided to the customer as a pre-programmed device with a custom part number.

### 3.6.2 Audio Configuration Area

The Audio configuration area is used to configure the boot index as well as the audio configuration strings. The boot index determines which of the programmed audio configurations will be loaded after reset.

The global configurations are automatically loaded when the CP2114 powers up. The audio boot configuration depends on the Config Select pin settings according to flow chart shown in the figure below. The audio configuration can be set by a one-time programmable ROM boot index or by reading the boot index from the Config Select pins. Setting the Config Select pins to 0x0F will load the default configuration. The one-time programmable ROM can be programmed in-system or Silicon Labs can provide custom preprogrammed parts with multiple customer-specified configurations.

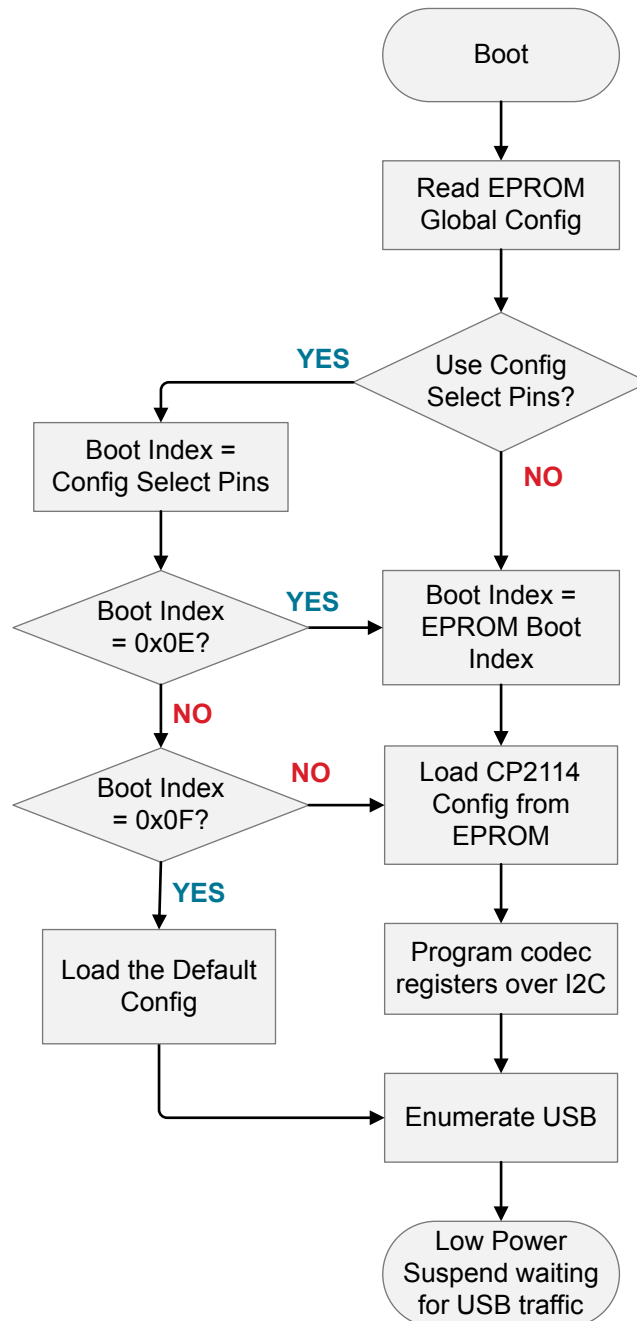


Figure 3.7. Boot Configuration Flowchart

There are two components to the audio configuration of the CP2114:

1. A fixed-size block that contains configuration elements that determine the CP2114 behavior.
2. A variable-sized block composed of codec register settings and special in-band commands and associated parameters.