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CP2200/1

SINGLE-CHIP ETHERNET CONTROLLER

Ethernet Controller
- Integrated IEEE 802.3 MAC and 10 BASE-T PHY
- Fully compatible with 100/1000 BASE-T networks
- Full/Half duplex with auto-negotiation
- Automatic polarity detection and correction
- Automatic retransmission on collision
- Automatic padding and CRC generation
- Supports broadcast and multi-cast MAC addressing

Parallel Host Interface (30 Mbps Transfer Rate)
- 8-bit multiplexed or non-multiplexed mode
- Only 11 I/O pins required in multiplexed mode
- Intel® or Motorola® Bus Format
- Interrupt on received packets and Wake-on-LAN

8 kB Flash Memory
- 8192 bytes ISP non-volatile memory
- Factory pre-programmed unique 48-bit MAC Address
- No external EEPROM required

Other Features
- LED output drivers (Link/Activity)
- Dedicated 2 kB RAM transmit buffer and 4 kB RAM receive FIFO buffer
- Power-on Reset
- 5 V Tolerant I/O

Software Support
- Royalty-free TCP/IP stack with device drivers
- TCP/IP Stack Configuration Wizard
- Hardware diagnostic software and example code

Example Applications
- Remote sensing and monitoring
- Inventory management
- VoIP phone adapters
- Point-of-sale devices
- Network clocks
- Embedded Web Server
- Remote Ethernet-to-UART bridge

Supply Voltage
- 3.1 to 3.6 V

Package
- Pb-free 48-pin TQFP (9x9 mm footprint)
- Pb-free 28-pin QFN (5x5 mm footprint)

Ordering Part Number
- CP2200-GQ (48-pin)
- CP2201-GM (28-pin)

Temperature Range: –40 to +85 °C

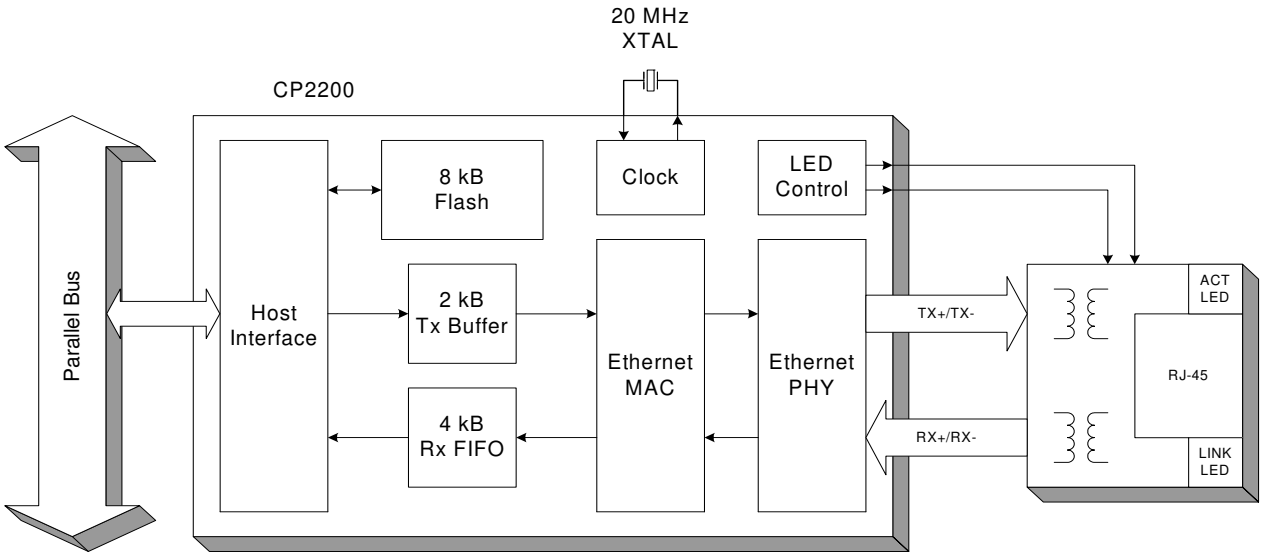

Figure 1. Example System Diagram

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Section **Page**

1. System Overview

The CP2200/1 is a single-chip Ethernet controller containing an integrated IEEE 802.3 Ethernet Media Access Controller (MAC), 10BASE-T Physical Layer (PHY), and 8 kB Non-Volatile Flash Memory available in a compact 5 x 5 mm QFN-28 package (sometimes called “MLF” or “MLP”) and a 48-pin TQFP package. The CP2200/1 can add Ethernet connectivity to any microcontroller or host processor with 11 or more Port I/O pins. The 8-bit parallel interface bus supports both Intel and Motorola bus formats in multiplexed and non-multiplexed mode. The data transfer rate in non-multiplexed mode can exceed 30 Mbps.

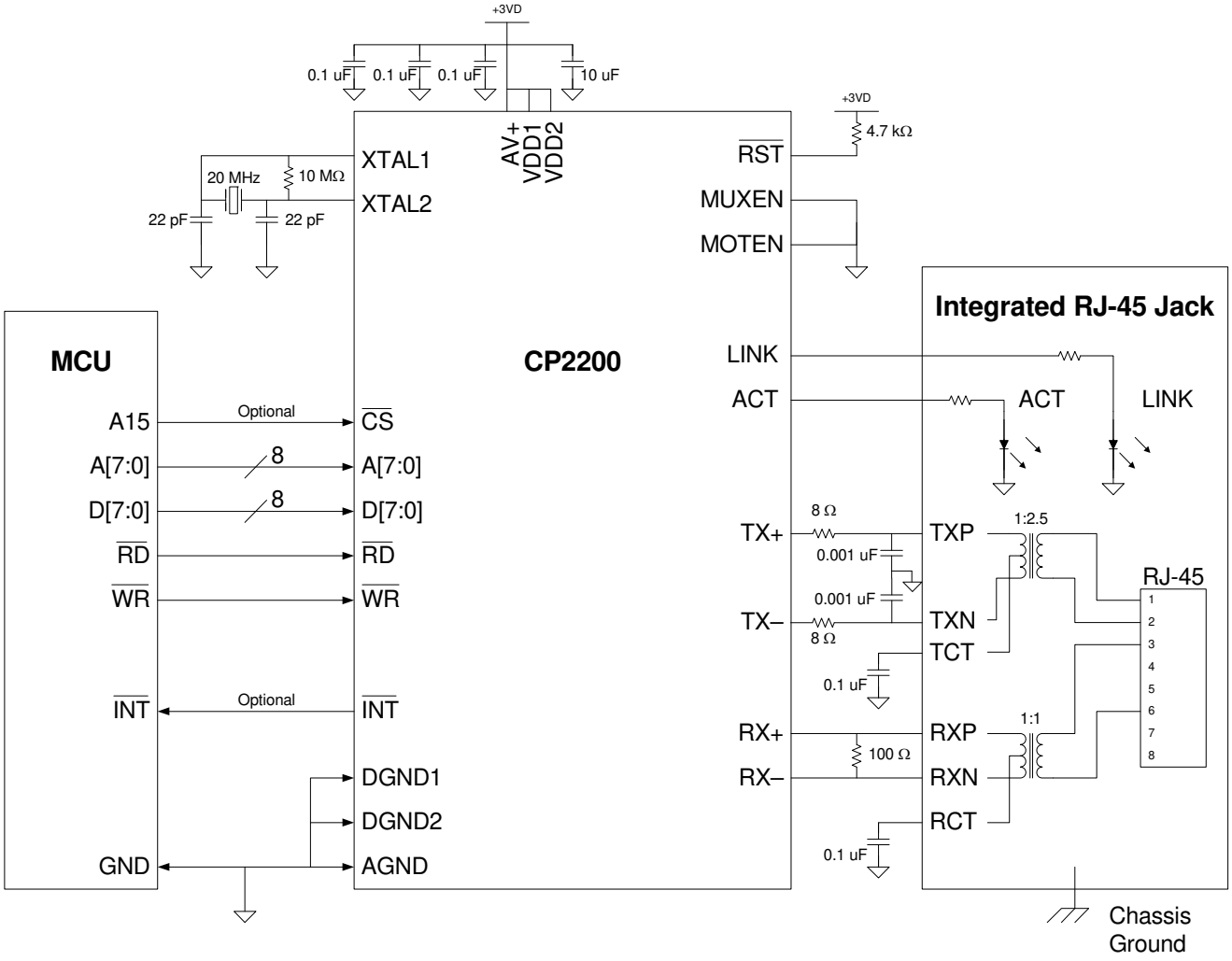
The on-chip Flash memory may be used to store user constants, web server content, or as general purpose non-volatile memory. The Flash is factory preprogrammed with a unique 48-bit MAC address stored in the last six memory locations. Having a unique MAC address stored in the CP2200/1 often removes the serialization step from the product manufacturing process of most embedded systems.

The CP2200/1 has four power modes with varying levels of functionality that allow the host processor to manage the overall system power consumption. The optional interrupt pin also allows the host to enter a “sleep” mode and awaken when a packet is received or when the CP2200/1 is plugged into a network. Auto-negotiation allows the device to automatically detect the most efficient duplex mode (half/full duplex) supported by the network.

The Ethernet Development Kit (Ethernet-DK) bundles a C8051F120 MCU Target Board, CP2200 Ethernet Development Board (AB4), the Silicon Laboratories IDE, all necessary debug hardware, and a TCP/IP Configuration Wizard. The Ethernet Development Kit includes all hardware, software, and examples necessary to design an embedded system using the CP2200. The CP2200 Ethernet Development Board is also compatible with the C8051F020TB and C8051F340TB. Individual target boards may be purchased online by visiting www.silabs.com.

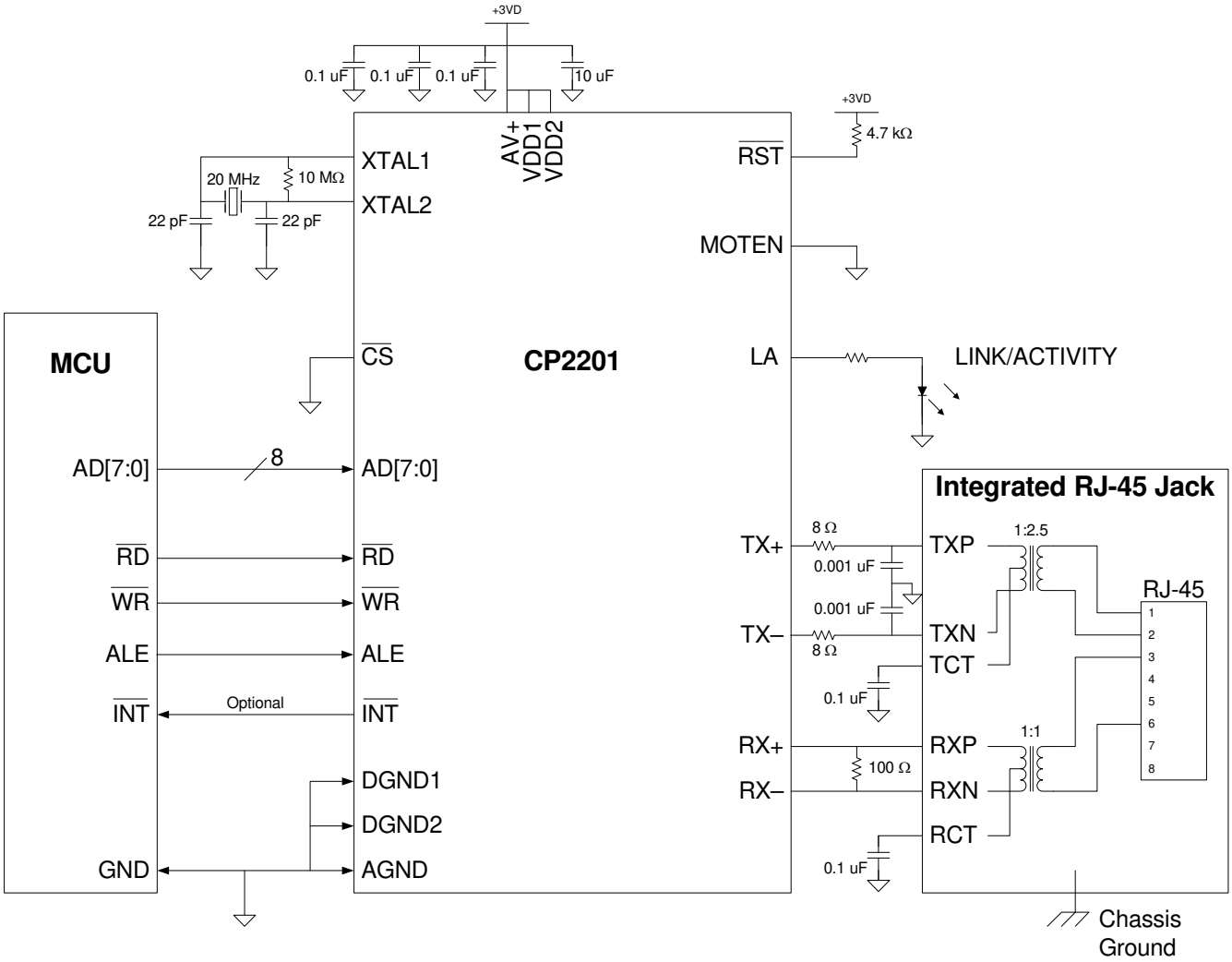
2. Typical Connection Diagram

Figure 2 and Figure 3 show typical connection diagrams for the 48-pin CP2200 and 28-pin CP2201.



Note: The CP220x should be placed within 1 inch of the transformer for optimal performance.

Figure 2. Typical Connection Diagram (Non-Multiplexed)



Note: The CP220x should be placed within 1 inch of the transformer for optimal performance.

Figure 3. Typical Connection Diagram (Multiplexed)

3. Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any I/O Pin or $\overline{\text{RST}}$ with respect to GND		–0.3	—	5.8	V
Voltage on V_{DD} with respect to GND		–0.3	—	4.2	V
Maximum Total current through V_{DD} and GND		—	—	500	mA
Maximum output current sunk by $\overline{\text{RST}}$ or any I/O pin		—	—	100	mA

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at or exceeding the conditions in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4. Electrical Characteristics

Table 2. Global DC Electrical Characteristics

V_{DD} = 3.1 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		3.1	3.3	3.6	V
Supply Current in Normal Mode (Transmitting)	V_{DD} = 3.3 V	—	75	155	mA
Supply Current in Normal Mode (No Network Traffic)	V_{DD} = 3.3 V	—	60	—	mA
Supply Current with Transmitter and Receiver Disabled (Memory Mode)	V_{DD} = 3.3 V	—	47	—	mA
Supply Current in Reset	V_{DD} = 3.3 V	—	15	—	mA
Supply Current in Shutdown Mode	V_{DD} = 3.3 V	—	6.5	—	mA
Specified Operating Temperature Range		–40	—	+85	°C

Table 3. Digital I/O DC Electrical Characteristics

V_{DD} = 3.1 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	UNITS
Output High Voltage (V_{OH})	I_{OH} = –3 mA I_{OH} = –10 µA I_{OH} = –10 mA	V_{DD} – 0.7 V_{DD} – 0.1 —	— — V_{DD} – 0.8	— — —	V
Output Low Voltage (V_{OL})	I_{OL} = 8.5 mA I_{OL} = 10 µA I_{OL} = 25 mA	— — —	— — 1.0	0.6 0.1 —	V
Input High Voltage (V_{IH})		2.0	—	—	V
Input Low Voltage (V_{IL})		—	—	0.8	V
Input Leakage Current		—	25	50	µA

5. Pinout and Package Definitions

Table 4. CP2200/1 Pin Definitions

Name	Pin Numbers		Type	Description
	48-pin	28-pin		
AV+	5	3	Power In	3.1–3.6 V Analog Power Supply Voltage Input.
AGND	4	2		Analog Ground
V_{DD1}	13	8	Power In	3.1–3.6 V Digital Power Supply Voltage Input.
DGND1	14	9		Digital Ground
V_{DD2}	30	19	Power In	3.1–3.6 V Digital Power Supply Voltage Input.
DGND2	31	20		Digital Ground
$\overline{RST}$	15	10	D I/O	Device Reset. Open-drain output of internal POR and V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs.
LINK	3*	—	D Out	Link LED. Push-pull output driven high when valid 10BASE-T link pulses are detected (Link Good) and driven low when valid 10BASE-T link pulses are not detected (Link Fail).
ACT	2*	—	D Out	Activity LED. Push-pull output driven high for 50 ms when any packet is transmitted or received and driven low all other times.
LA	—	1*	D Out	Link or Activity LED. Push-pull output driven high when valid link pulses are detected (Link Good) and driven low otherwise (Link Fail). The output is toggled for each packet transmitted or received, then returns to its original state after 50 ms.
XTAL1	46	28	A In	Crystal Input. This pin is the return for the external oscillator driver. This pin can be overdriven by an external CMOS clock.
XTAL2	45*	27*	A Out	Crystal Output. This pin is the excitation driver for a quartz crystal.
TX+	9	6	A Out	10BASE-T Transmit, Differential Output (Positive).
TX–	10	7	A Out	10BASE-T Transmit, Differential Output (Negative).
RX+	7	5	A In	10BASE-T Receive, Differential Input (Positive).
RX–	6	4	A In	10BASE-T Receive, Differential Input (Negative).
MOTEN	43	26	D In	Motorola Bus Format Enable. This pin should be tied directly to V_{DD} for Motorola bus format or directly to GND for Intel bus format.
MUXEN	44	—	D In	Multiplexed Bus Enable. This pin should be tied directly to V_{DD} for multiplexed bus mode or directly to GND for non-multiplexed bus mode.
$\overline{INT}$	42	25	D Out	Interrupt Service Request. This pin provides notification to the host.

***Note:** Pins can be left unconnected when not used.

Table 4. CP2200/1 Pin Definitions (Continued)

Name	Pin Numbers		Type	Description
	48-pin	28-pin		
$\overline{CS}$	41	24	D In	Device Chip Select.
$\overline{RD}$/(DS)	39	22	D In	Read Strobe (Intel Mode) or Data Strobe (Motorola Mode)
$\overline{WR}$/(R/$\overline{W}$)	40	23	D In	Write Strobe (Intel Mode) or Read/Write Strobe (Motorola Mode)
D0/AD0	16	11	D I/O	Bit 0, Non-Multiplexed Data Bus or Multiplexed Address/Data Bus
D1/AD1	17	12	D I/O	Bit 1, Non-Multiplexed Data Bus or Multiplexed Address/Data Bus
D2/AD2	18	13	D I/O	Bit 2, Non-Multiplexed Data Bus or Multiplexed Address/Data Bus
D3/AD3	19	14	D I/O	Bit 3, Non-Multiplexed Data Bus or Multiplexed Address/Data Bus
D4/AD4	20	15	D I/O	Bit 4, Non-Multiplexed Data Bus or Multiplexed Address/Data Bus
D5/AD5	21	16	D I/O	Bit 5, Non-Multiplexed Data Bus or Multiplexed Address/Data Bus
D6/AD6	22	17	D I/O	Bit 6, Non-Multiplexed Data Bus or Multiplexed Address/Data Bus
D7/AD7	23	18	D I/O	Bit 7, Non-Multiplexed Data Bus or Multiplexed Address/Data Bus
A0	27*	—	D In	Bit 0, Non-Multiplexed Address Bus
A1	28*	—	D In	Bit 1, Non-Multiplexed Address Bus
A2	29*	—	D In	Bit 2, Non-Multiplexed Address Bus
A3/ALE/(AS)	32	—	D In	Bit 3, Non-Multiplexed Address Bus ALE Strobe (Multiplexed Intel Mode) Address Strobe (Multiplexed Motorola Mode)
ALE/(AS)	—	21	D In	ALE Strobe (Intel Mode) Address Strobe (Motorola Mode)
A4	33*	—	D In	Bit 4, Parallel Interface Non-Multiplexed Address Bus
A5	34*	—	D In	Bit 5, Parallel Interface Non-Multiplexed Address Bus
A6	37*	—	D In	Bit 6, Parallel Interface Non-Multiplexed Address Bus
A7	38*	—	D In	Bit 7, Parallel Interface Non-Multiplexed Address Bus
NC	1, 8, 11,12 24–26 35,36 47, 48	—		These pins should be left unconnected or tied to V_{DD}.
***Note:** Pins can be left unconnected when not used.				

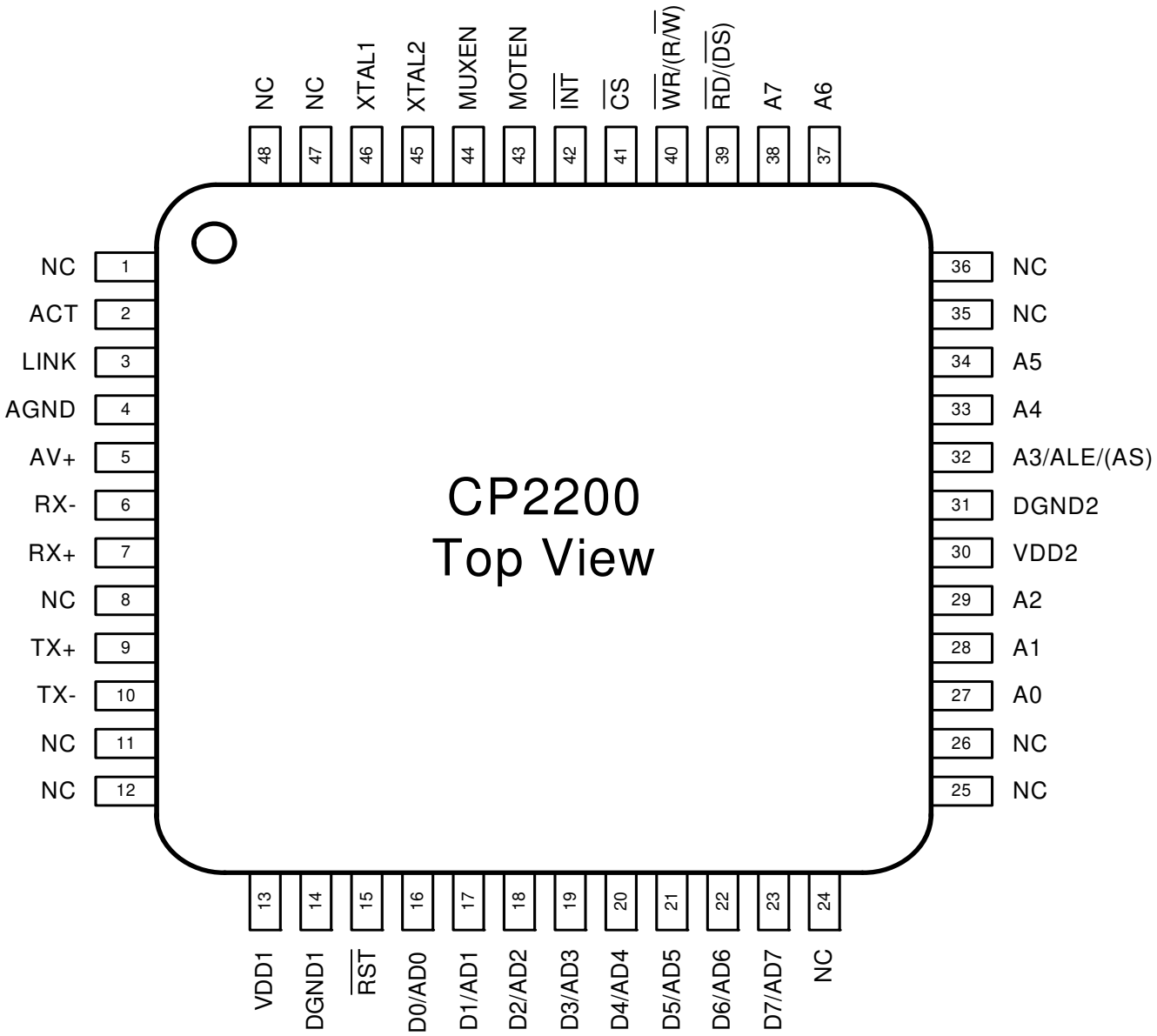


Figure 4. 48-pin TQFP Pinout Diagram

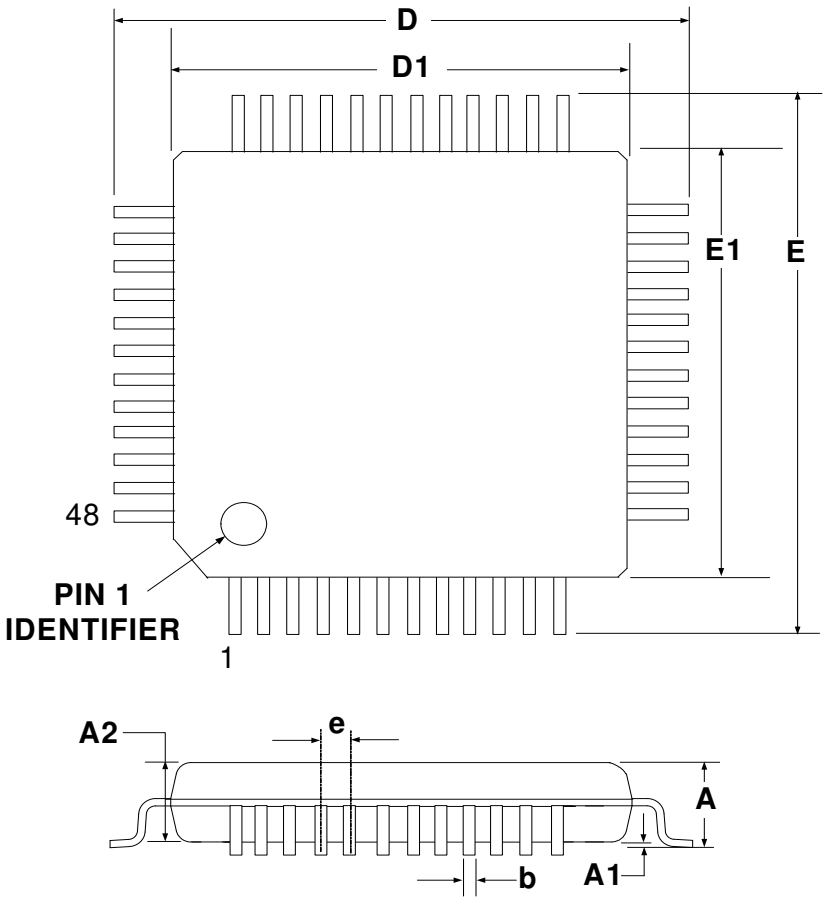


Table 5. TQFP-48 Package Dimensions

	MM		
	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D	—	9.00	—
D1	—	7.00	—
E	—	9.00	—
e	—	0.50	—
E1	—	7.00	—

Figure 5. 48-pin TQFP Package Dimensions

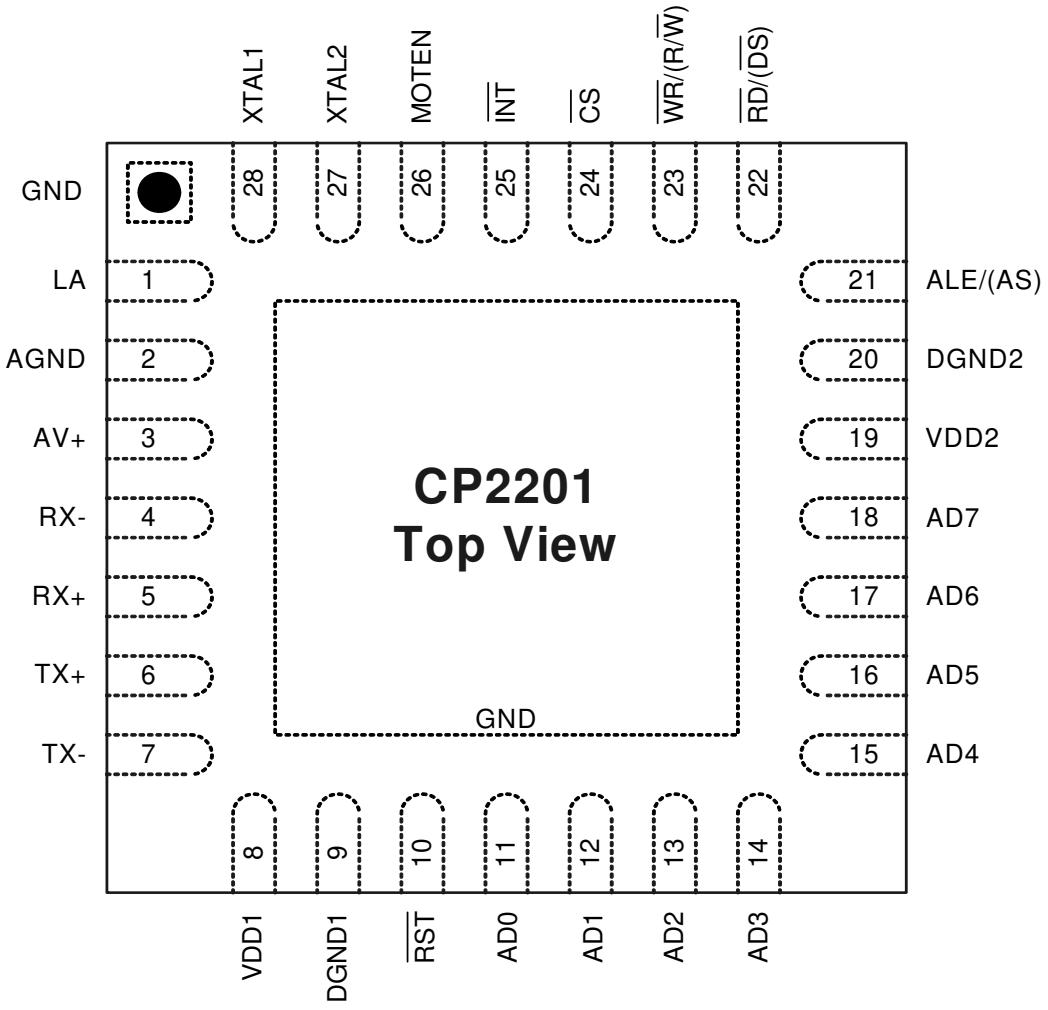


Figure 6. QFN-28 Pinout Diagram (Top View)

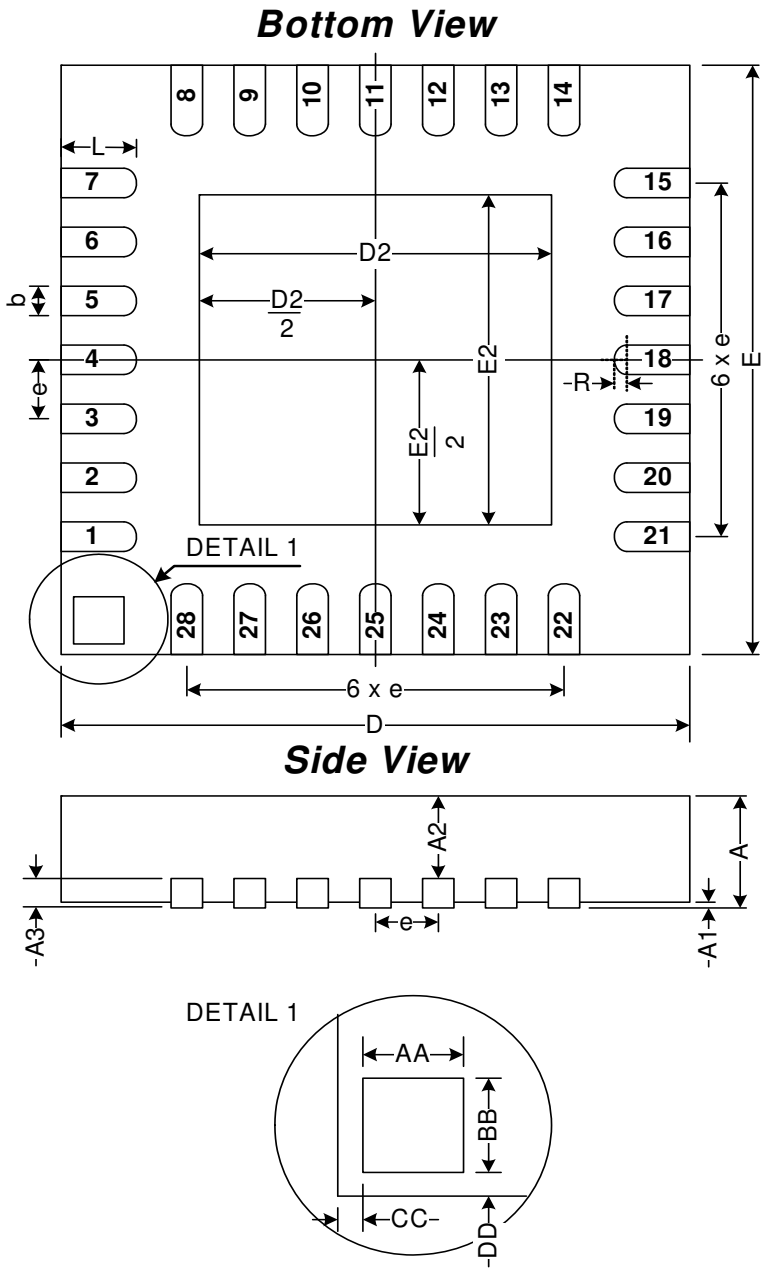


Table 6. QFN-28 Package Dimensions

	MM		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3	—	0.25	—
b	0.18	0.23	0.30
D	—	5.00	—
D2	2.90	3.15	3.35
E	—	5.00	—
E2	2.90	3.15	3.35
e	—	0.5	—
L	0.45	0.55	0.65
N	—	28	—
ND	—	7	—
NE	—	7	—
R	0.09	—	—
AA	—	0.435	—
BB	—	0.435	—
CC	—	0.18	—
DD	—	0.18	—

Figure 7. QFN-28 Package Drawing

Top View

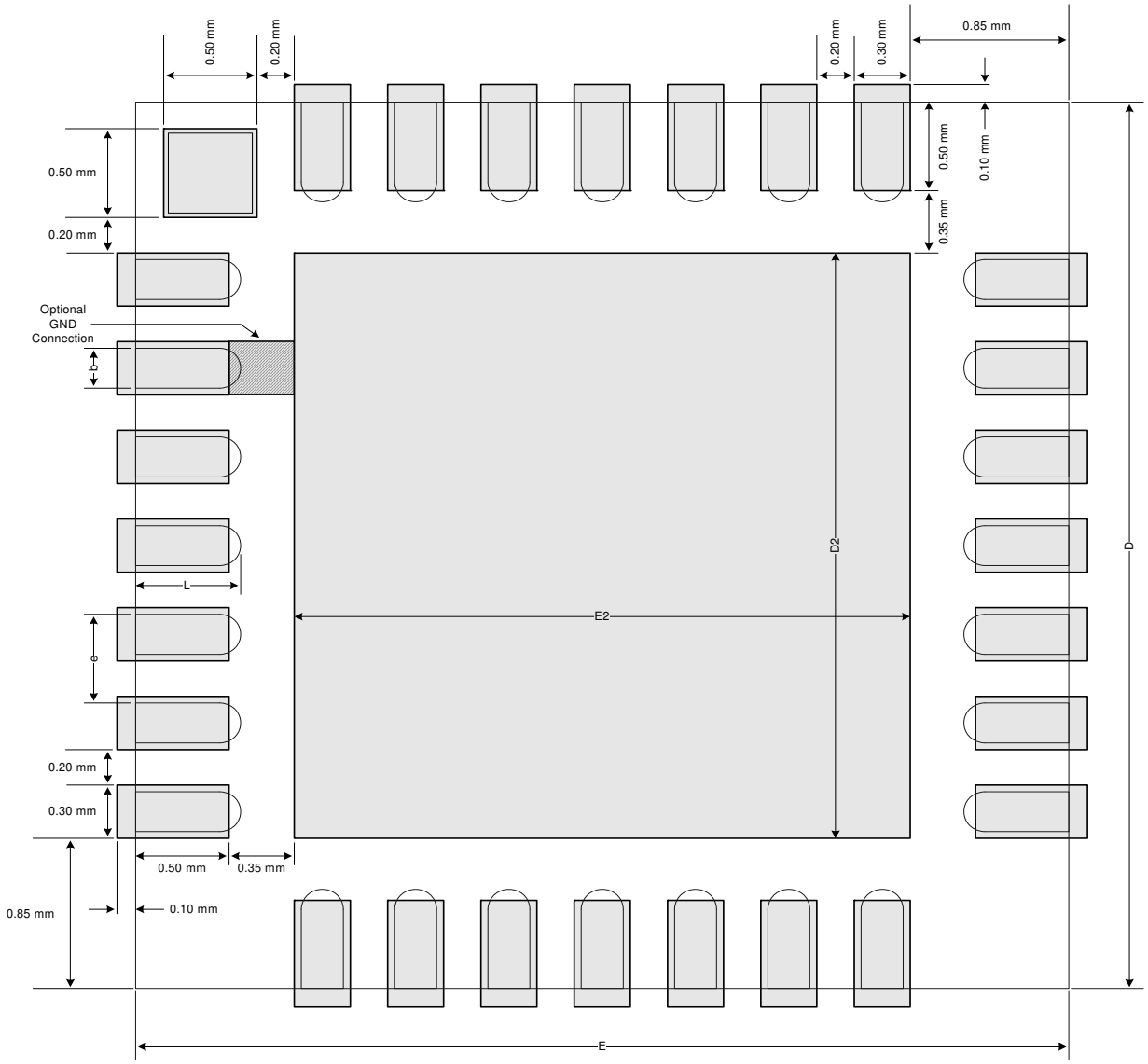


Figure 8. Typical QFN-28 Landing Diagram

Top View

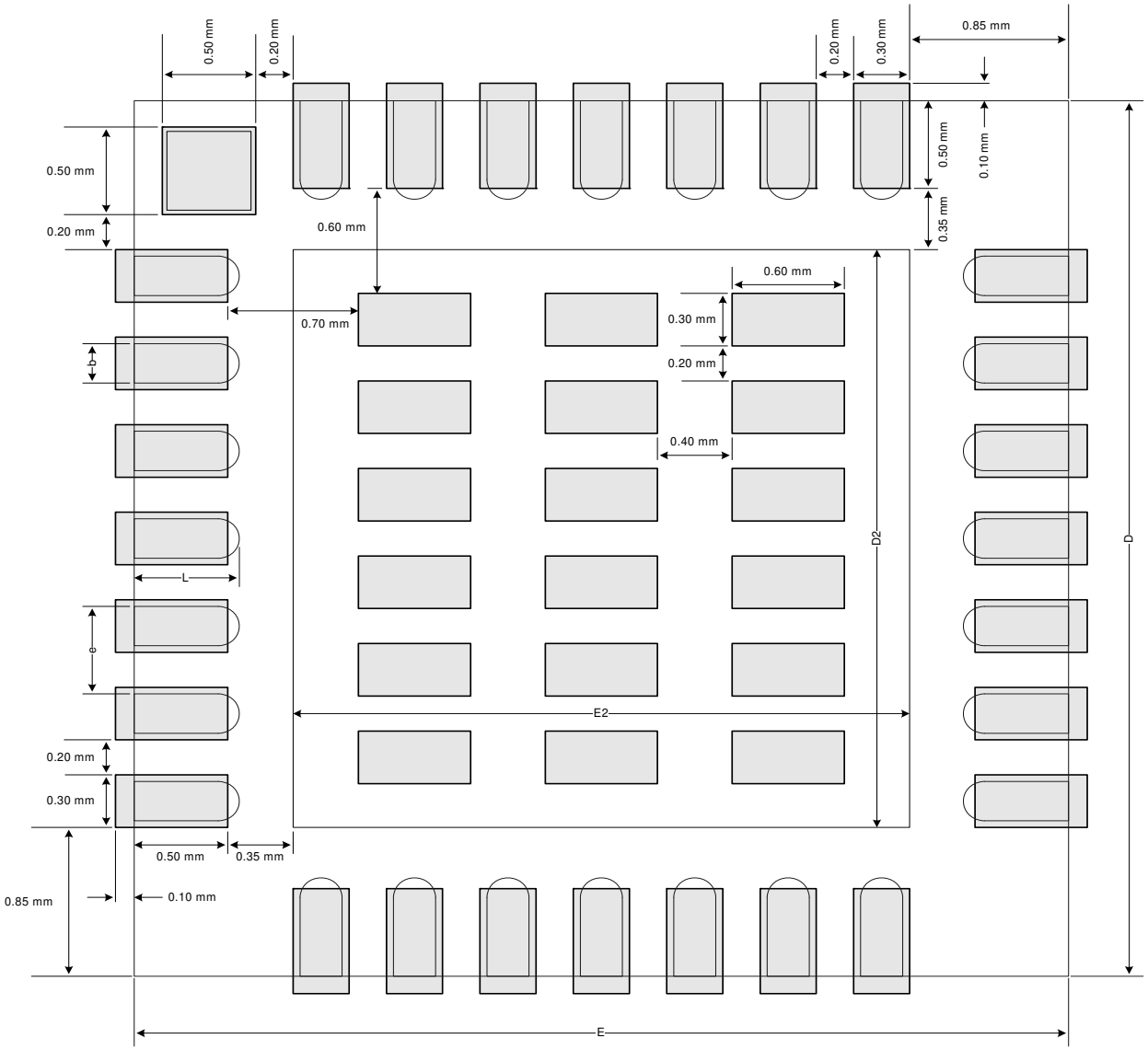


Figure 9. Typical QFN-28 Solder Paste Diagram

6. Functional Description

6.1. Overview

In most systems, the CP2200/1 is used for transmitting and receiving Ethernet packets, non-volatile data storage, and controlling Link and Activity LEDs. The device is controlled using direct and indirect internal registers accessible through the parallel host interface. All digital pins on the device are 5 V tolerant.

6.2. Reset Initialization

After every CP2200/1 reset, the following initialization procedure is recommended to ensure proper device operation:

Step 1: Wait for the reset pin to rise. This step takes the longest during a power-on reset.

Step 2: Wait for Oscillator Initialization to complete. The host processor will receive notification through the interrupt request signal once the oscillator has stabilized.

Step 3: Wait for Self Initialization to complete. The INT0 interrupt status register on page 31 should be checked to determine when Self Initialization completes.

Step 4: Disable interrupts (using INT0EN and INT1EN on page 33 and page 36) for events that will not be monitored or handled by the host processor. By default, all interrupts are enabled after every reset.

Step 5: Initialize the physical layer. See “15.7. Initializing the Physical Layer” on page 90 for a detailed physical layer initialization procedure.

Step 6: Enable the desired Activity, Link, or Activity/Link LEDs using the IOPWR register on page 45.

Step 7: Initialize the media access controller (MAC). See “14.1. Initializing the MAC” on page 78 for a detailed MAC initialization procedure.

Step 8: Configure the receive filter. See “12.4. Initializing the Receive Buffer, Filter and Hash Table” on page 59 for a detailed initialization procedure.

Step 9: The CP2200/1 is ready to transmit and receive packets.

6.3. Interrupt Request Signal

The CP2200/1 has an interrupt request signal ($\overline{\text{INT}}$) that can be used to notify the host processor of pending interrupts. The $\overline{\text{INT}}$ signal is asserted upon detection of any enabled interrupt event. Host processors that cannot dedicate a port pin to the $\overline{\text{INT}}$ signal can periodically poll the interrupt status registers to see if any interrupt generating events have occurred. If the /INT signal is not used, pending interrupts such a Receive FIFO Full must still be serviced.

The 14 interrupt sources are listed below. Interrupts are enabled on reset and can be disabled by software. Pending interrupts can be cleared (allowing the $\overline{\text{INT}}$ signal to de-assert) by reading the self-clearing interrupt registers. See “8. Interrupt Sources” on page 30 for a complete description of the CP2200/1 interrupts.

- End of Packet Reached
- Receive FIFO Empty
- Receive FIFO Full
- Oscillator Initialization Complete
- Self Initialization Complete
- Flash Write/Erase Complete
- Packet Transmitted
- Packet Received
- “Wake-on-LAN” Wakeup Event
- Link Status Changed
- Jabber Detected
- Auto-Negotiation Failed
- Remote Fault Notification
- Auto-Negotiation Complete

6.4. Clocking Options

The CP2200/1 can be clocked from an external parallel-mode crystal oscillator or CMOS clock. Figure 10 and Figure 11 show typical connections for both clock source types. If a crystal oscillator is chosen to clock the device, the crystal is started once the device is released from reset and remains on until the device reenters the reset state or loses power.

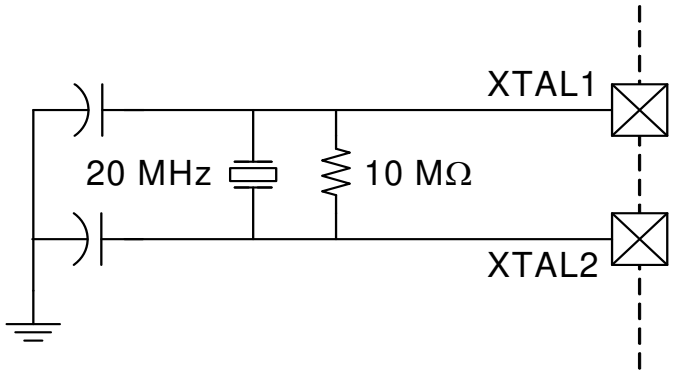


Figure 10. Crystal Oscillator Example

Important note on external crystals: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device. The traces should be as short as possible and shielded with a ground plane from any other traces that could introduce noise or interference.

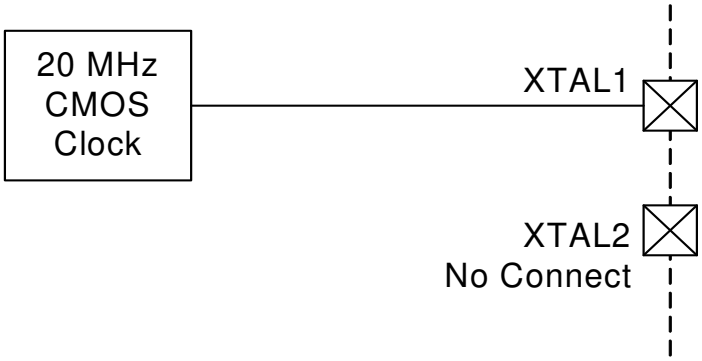


Figure 11. External CMOS Clock Example

Table 7 lists the clocking requirements of the CP2200/1 when using a crystal oscillator or CMOS clock. Table 8 shows the electrical characteristics of the XTAL1 pin. These characteristics are useful when selecting an external CMOS clock.

Table 7. Clocking Requirements

V_{DD} = 3.1 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	UNITS
Frequency		—	20	—	MHz
Frequency Error		—	—	±50	ppm
Duty Cycle		45	50	55	%

Table 8. Input Clock Pin (XTAL1) DC Electrical Characteristics

V_{DD} = 3.1 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	UNITS
XTAL1 Input Low Voltage		—	—	0.7	V
XTAL1 Input High Voltage		2.0	—	—	V

6.5. LED Control

The CP2200/1 can be used to control link status and activity LEDs. The CP2200 (48-pin TQFP) has two push-pull LED drivers that can source up to 10 mA each. The CP2201 (28-pin QFN) has a single push-pull LED driver that turns the LED on or off based on the link status and blinks the LED when activity is detected on a good link. Table 9 shows the function of the LED signals available on the CP2200/1.

Table 9. LED Control Signals

Signal	Device	Description
LINK	CP2200	Asserted when valid link pulses are detected.
ACT	CP2200	Asserted for 50 ms for each packet transmitted or received.
LA	CP2201	Asserted when valid link pulses are detected and toggled for 50 ms for each packet transmitted or received.

Figure 12 shows a typical LED connection for the CP2200. The CP2201 uses an identical connection for the LA (link/activity) pin. The LED drivers are enabled and disabled using the IOPWR register on page 45.

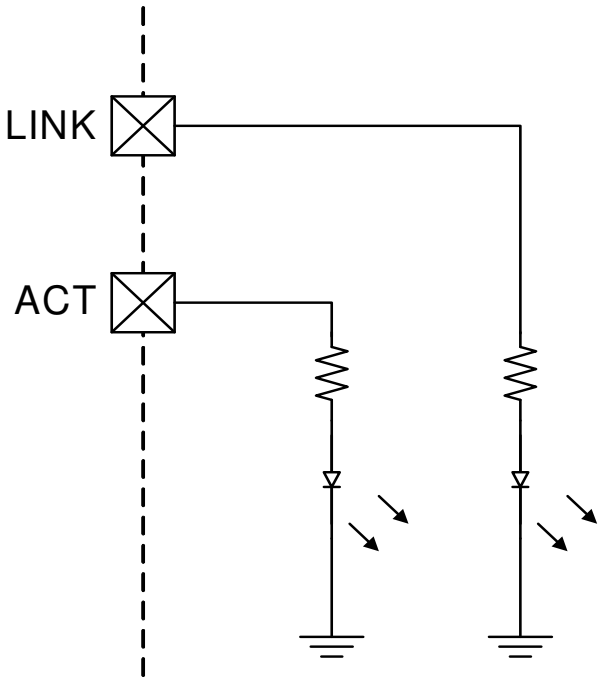


Figure 12. LED Control Example (CP2200)

6.6. Sending and Receiving Packets

After reset initialization is complete, the CP2200/1 is ready to send and receive packets. Packets are sent by loading data into the transmit buffer using the AutoWrite register and writing '1' to TXGO. See "11.2. Transmitting a Packet" on page 48 for detailed information on how to transmit a packet using the transmit interface. A Packet Transmitted interrupt will be generated once transmission is complete.

Packet reception occurs automatically when reception is enabled in the MAC and the receive buffer is not full. Once a packet is received, the host processor is notified by generating a Packet Received interrupt. The host may read the packet using the AutoRead interface. See "12.2. Reading a Packet Using the Autoread Interface" on page 58 and "12.4. Initializing the Receive Buffer, Filter and Hash Table" on page 59 for additional information on using and initializing the receive interface.

7. Internal Memory and Registers

The CP2200/1 is controlled through direct and indirect registers accessible through the parallel host interface. The host interface provides an 8-bit address space, of which there are 114 valid direct register locations (see Table 11 on page 25). All remaining addresses in the memory space are reserved and should not be read or written. The direct registers provide access to the RAM buffers, Flash memory, indirect MAC configuration registers, and other status and control registers for various device functions.

Figure 13 shows the RAM and Flash memory organization. The transmit and receive RAM buffers share the same address space and are both accessed using the RAMADDRH:RAMADDRL pointer. Each of the buffers has a dedicated data register. The Flash memory has a separate address space and a dedicated address pointer and data register. See “13. Flash Memory” on page 73 for detailed information on how to read and write to Flash.

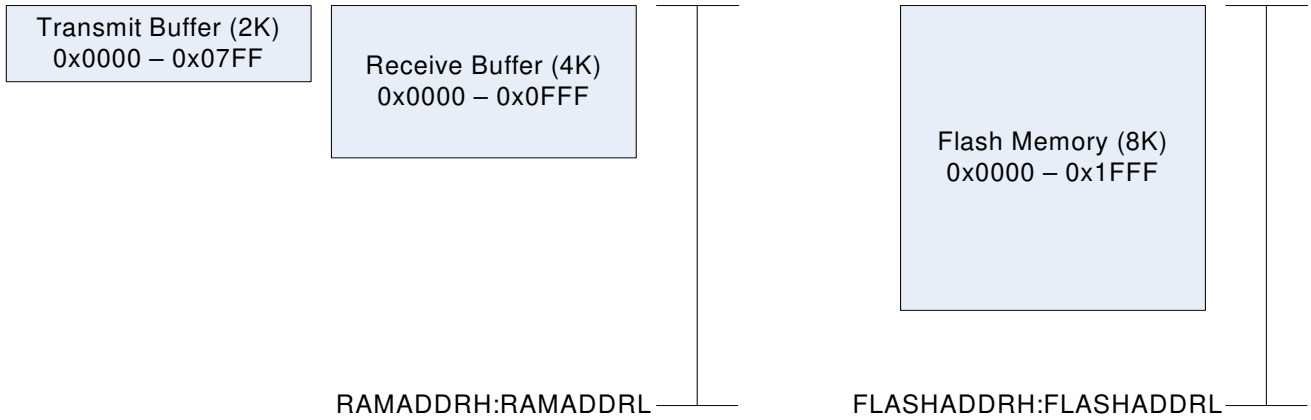


Figure 13. RAM Buffers and Flash Memory Organization

7.1. Random Access to RAM Transmit and Receive Buffers

The most common and most efficient methods for accessing the transmit and receive buffers are the AutoWrite and AutoRead interfaces. These interfaces allow entire packets to be written or read at a time. In very few cases, the transmit and receive buffers may need to be accessed randomly. An example of this is a system in which a specific byte in the packet is checked to determine whether to read the packet or discard it. The following procedure can be used to read or write data to either RAM buffer:

Step 1: Write the address of the target byte to RAMADDRH:RAMADDRL.

Step 2: **Transmit Buffer:**
Read or write 8-bit data to RAMTXDATA to read or write from the target byte in the transmit buffer.

Receive Buffer:
Read or write 8-bit data to RAMRXDATA to read or write from the target byte in the receive buffer.

Note: Reads and writes of the RAM buffers using the random access method are independent of the AutoRead and AutoWrite interfaces. Each of the interfaces has a dedicated set of address and data registers. See “11.2. Transmitting a Packet” on page 48 and “12.2. Reading a Packet Using the Autoread Interface” on page 58 for additional information about the AutoRead and AutoWrite interfaces.

Register 1. RAMADDRH: RAM Address Pointer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address:
								0x08

Bits7–0: RAMADDRH: RAM Address Register High Byte
Holds the most significant eight bits of the target RAM address.

Register 2. RAMADDRL: RAM Address Pointer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address:
								0x09

Bits7–0: RAMADDRL: RAM Address Register Low Byte
Holds the least significant eight bits of the target RAM address.

Register 3. RAMTXDATA: RAM Transmit Buffer Data Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address:
								0x04

Bits7–0: RAMTXDATA: Transmit Buffer Data Register
Read: Returns data in the transmit buffer at location RAMADDRH:RAMADDRL.
Write: Writes data to the transmit buffer at location RAMADDRH:RAMADDRL.

Register 4. RAMRXDATA: RAM Receive Buffer Data Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address:
								0x02

Bits7–0: RAMRXDATA: Receive Buffer Data Register
Read: Returns data in the receive buffer at location RAMADDRH:RAMADDRL.
Write: Writes data to the receive buffer at location RAMADDRH:RAMADDRL.

7.2. Internal Registers

The CP2200/1 has 114 direct internal registers and 9 indirect registers. The registers are grouped into ten categories based on function. Table 10 lists the register groups and provides links to the detailed register descriptions for each group. Table 11 lists all direct registers available on the device.

Table 10. CP2200/1 Register Groups

RAM Access Registers	Section 7.1 on page 23
Interrupt Status and Control Registers	Section 8 on page 30
Reset Source Registers	Section 9 on page 37
Power Mode Registers	Section 10 on page 43
Transmit Status and Control Registers	Section 11.5 on page 49
Receive Interface Status and Control Registers	Section 12.5 on page 60
Receive Buffer Status and Control Registers	Section 12.7 on page 67
FLASH Access Registers	Section 13.3 on page 75
MAC Access Registers	Section 14.2 on page 78
MAC Indirect Registers	Section 14.3 on page 80
PHY Status and Control Registers	Section 15 on page 88

Table 11. Direct Registers

Register	Address	Description	Page No.
CPADDRH	0x21	Current RX Packet Address High Byte	page 65
CPADDRL	0x22	Current RX Packet Address Low Byte	page 65
CPINFOH	0x1D	Current RX Packet Information High Byte	page 63
CPINFOL	0x1E	Current RX Packet Information Low Byte	page 64
CPLENH	0x1F	Current RX Packet Length High Byte	page 64
CPLENL	0x20	Current RX Packet Length Low Byte	page 64
CPTLB	0x1A	Current RX Packet TLB Number	page 67
FLASHADDRH	0x69	Flash Address Pointer High Byte	page 76
FLASHADDRL	0x68	Flash Address Pointer Low Byte	page 76
FLASHAUTORD	0x05	Flash AutoRead w/ increment	page 77
FLASHDATA	0x06	Flash Read/Write Data Register	page 77
FLASHERASE	0x6A	Flash Erase	page 77
FLASHKEY	0x67	Flash Lock and Key	page 76
FLASHSTA	0x7B	Flash Status	page 75