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CP2400/1/2/3

128/64 Segment LCD Driver

LCD Driver
- Controls up to 128 segments (48-pin packages) or 64 segments (32-pin package)
- Supports static, 2-mux, 3-mux, and 4-mux displays
- On-chip bias generation with internal charge pump
- Low power blink capability

GPIO Expander
- Expands GPIO count by up to 36 pins (48-pin packages) or 20 pins (32-pin package)
- GPIO pins may be configured to push-pull or open-drain outputs with two drive levels. GPIO may also be used as digital inputs (CP2400/1/2/3 pullups included)
- Port Match Capability can wake up host controller using interrupt pin
- 5 V Tolerant I/O

Real Time Clock, SmaRTClock
- Precision time keeping with 32.768 kHz watch crystal; self-oscillate mode requires no external crystal; accepts external 32 kHz CMOS clock
- 36-hour programmable counter with wake up alarm
- Can wake up the host controller using interrupt pin
- Low power (<1.5 µA)

256 Bytes RAM
- General purpose RAM expands the memory available to host controller.

16-bit Timers
- Two general purpose 16-bit timers

Clock Sources
- 20 MHz Internal oscillator
- Can be clocked from an external CMOS clock

Digital Bus Interface
- 4-wire SPI Interface operates up to 2.5 Mbps with synchronous external clock or up to 1 Mbps with internal clock (CP2400/2 only).
- 2-wire SMBus/I^{2}C Interface operates up to 400 kHz with internal clock (CP2401/3 only).
- Dedicated $\overline{\text{RST}}$ and $\overline{\text{INT}}$ pins.
- Optional $\overline{\text{CLK}}$ pin can be used as a CMOS clock input.
- Optional $\overline{\text{PWR}}$ pin (SMBus/I^{2}C devices only) places the device in a low power mode. SPI devices use the NSS pin to place the device in a low power mode.

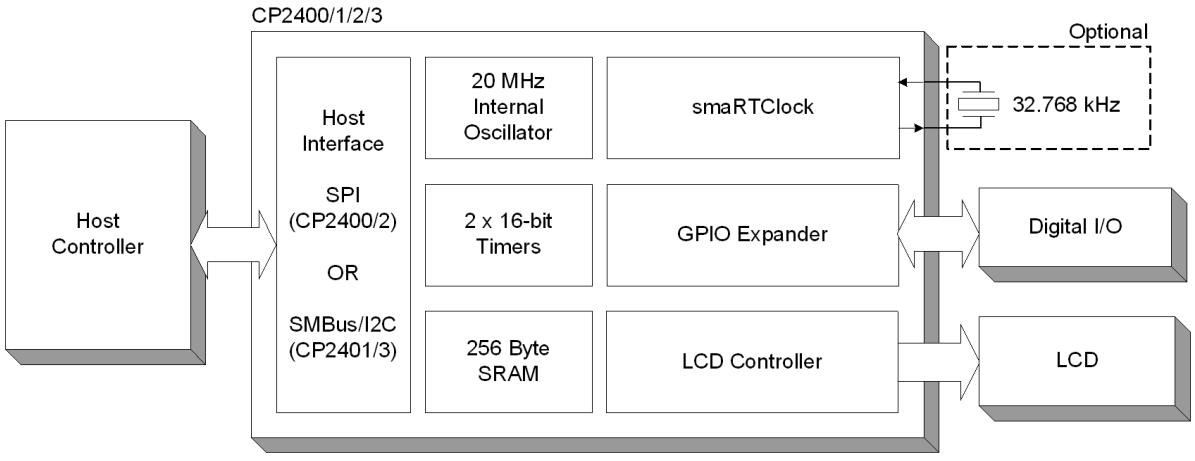
Low Power
- 1.8–3.6 V operation with integrated LDO
- Ultra Low Power Mode w/ LCD (<3 µA typical)
- Shutdown current (0.05 µA typical)

Example Applications
- Handheld Equipment
- Utility Meters
- Thermostat Display
- Home Security Systems

Packages
- Pb-free 48-pin QFP (9x9 mm footprint) [-Q]
- Pb-free 48-pin QFN (7x7 mm footprint) [-M]
- Pb-free 32-pin QFN (5x5 mm footprint)

Ordering Part Numbers
- CP2400-G[M|Q] (SPI Interface)
- CP2401-G[M|Q] (SMBus/I^{2}C Interface)
- CP2402-GM (SPI Interface)
- CP2403-GM (SMBus/I^{2}C Interface)

Temperature Range: –40 to +85 °C



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1. System Overview

CP2400/1/2/3 devices are fixed function LCD drivers that can also be used for expanding GPIO, timekeeping, and increasing available system RAM by up to 256 bytes. The device is controlled using direct and indirect internal registers accessible through the 4-wire SPI or 2-wire SMBus interface. All digital pins on the device are 5 V tolerant.

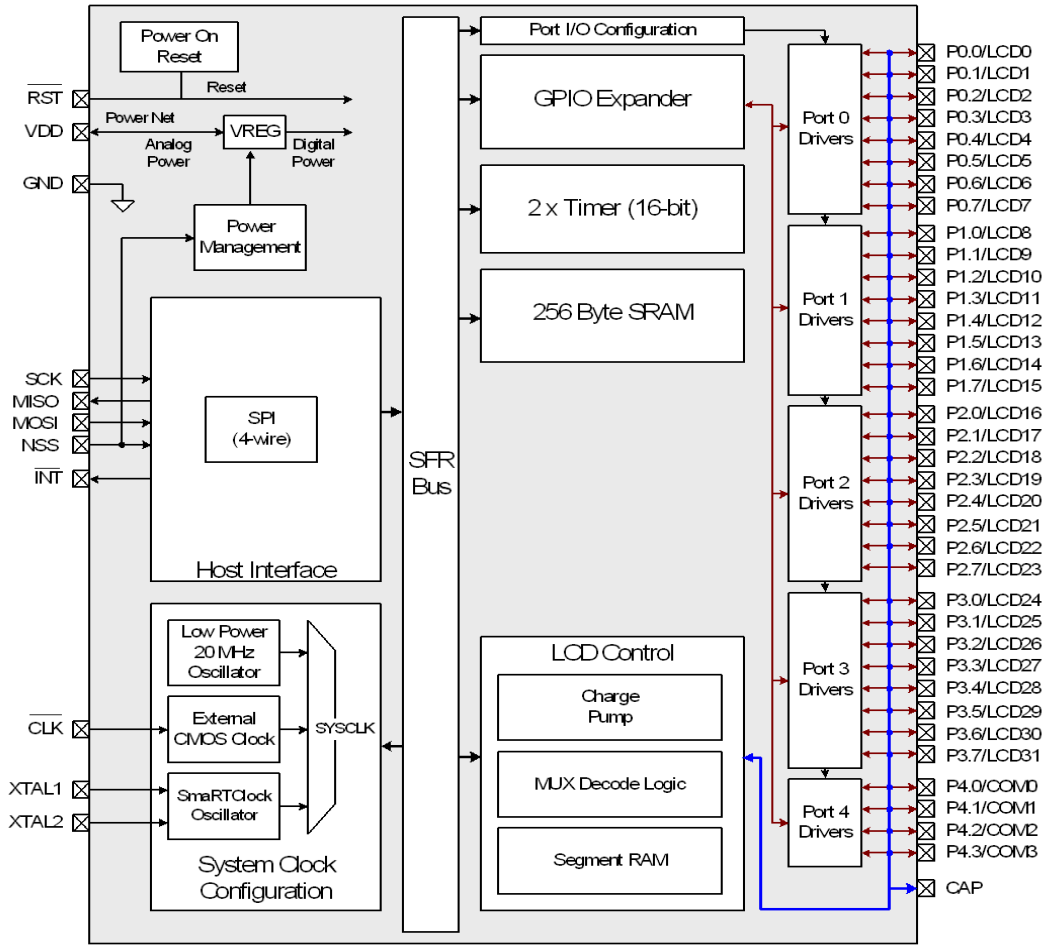


Figure 1.1. CP2400 Block Diagram

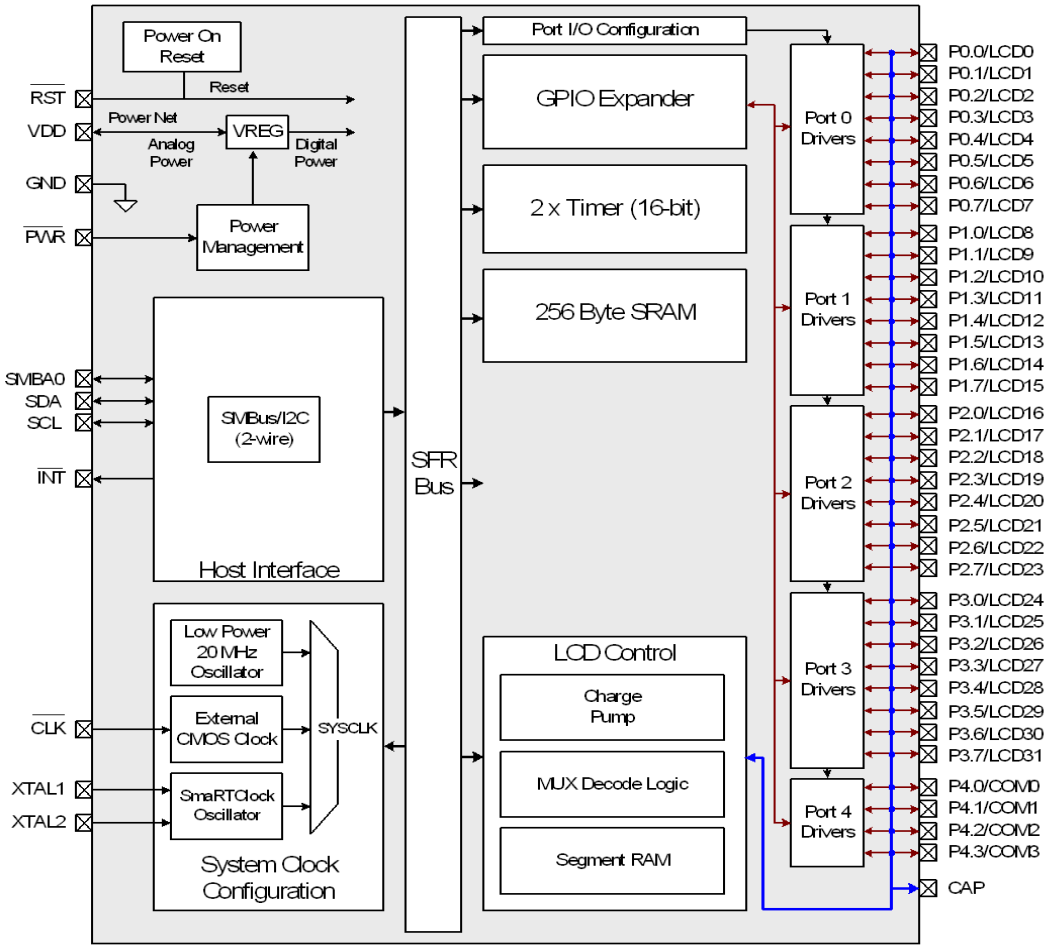


Figure 1.2. CP2401 Block Diagram

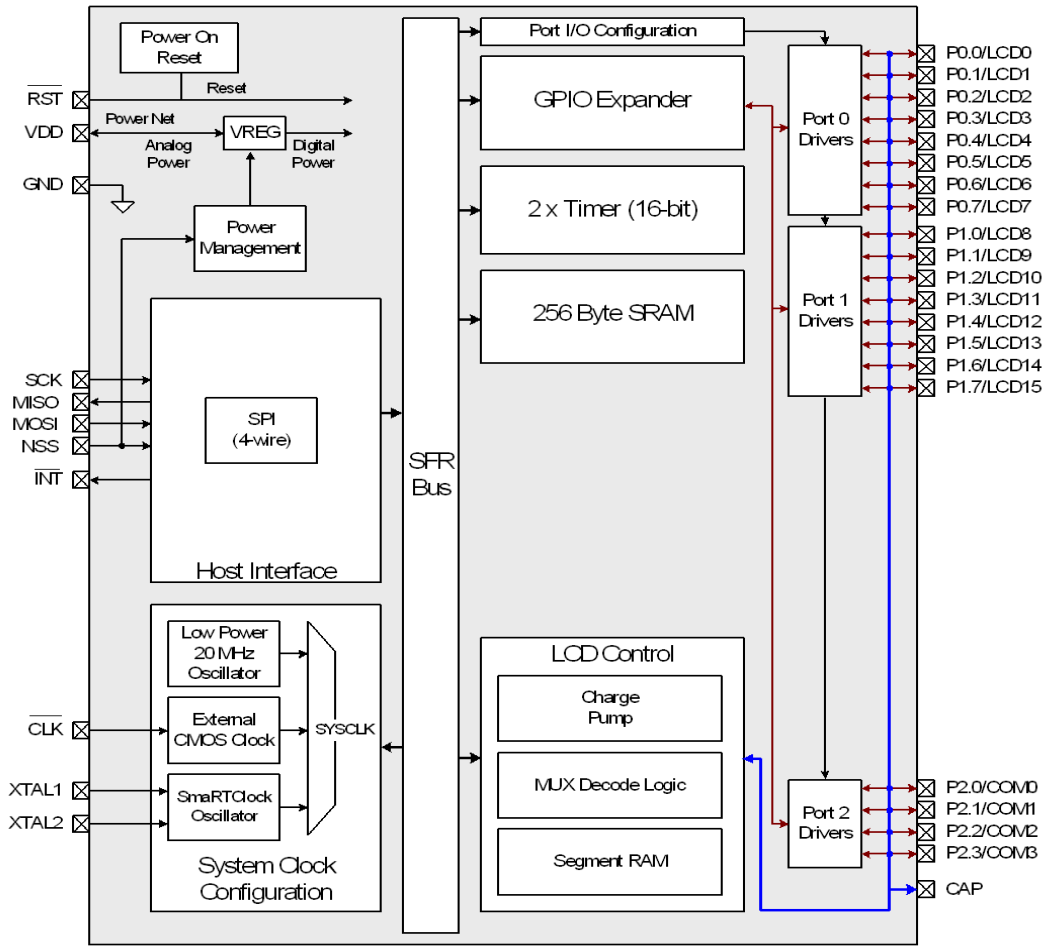


Figure 1.3. CP2402 Block Diagram

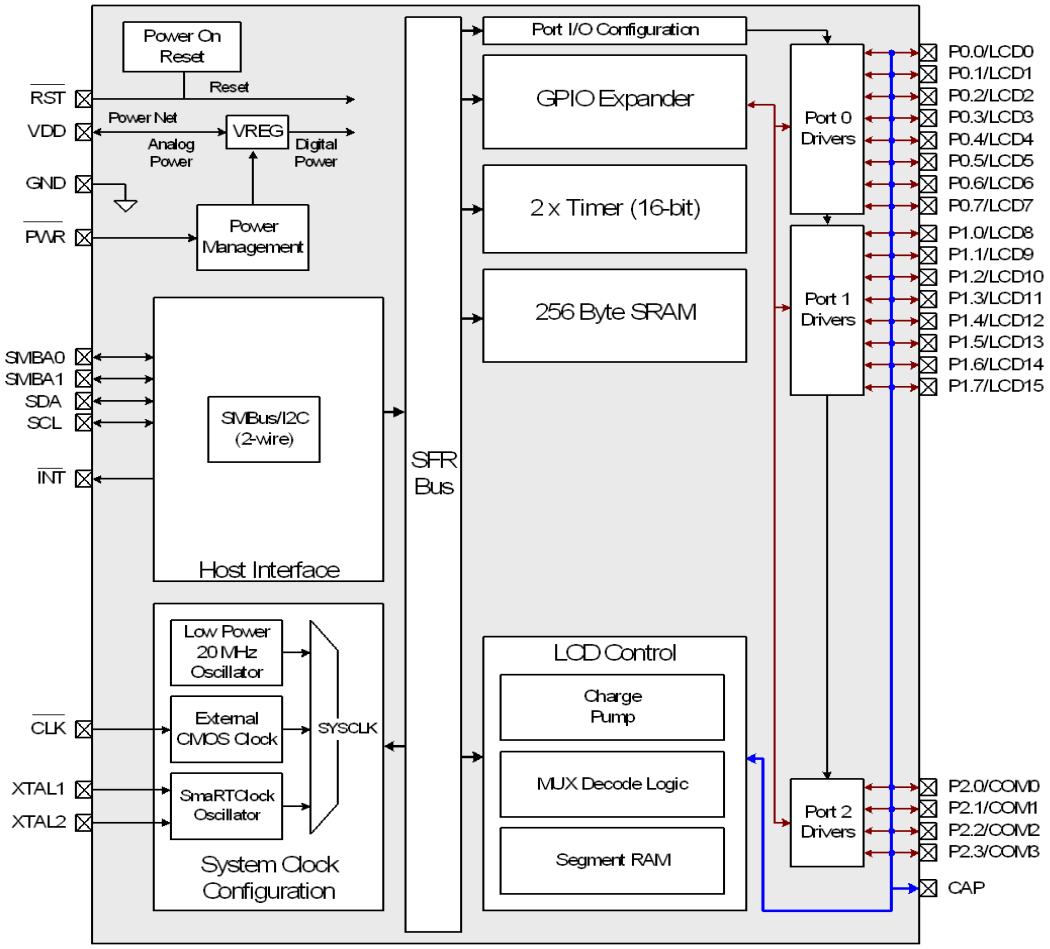


Figure 1.4. CP2403 Block Diagram

1.1. Typical Connection Diagram

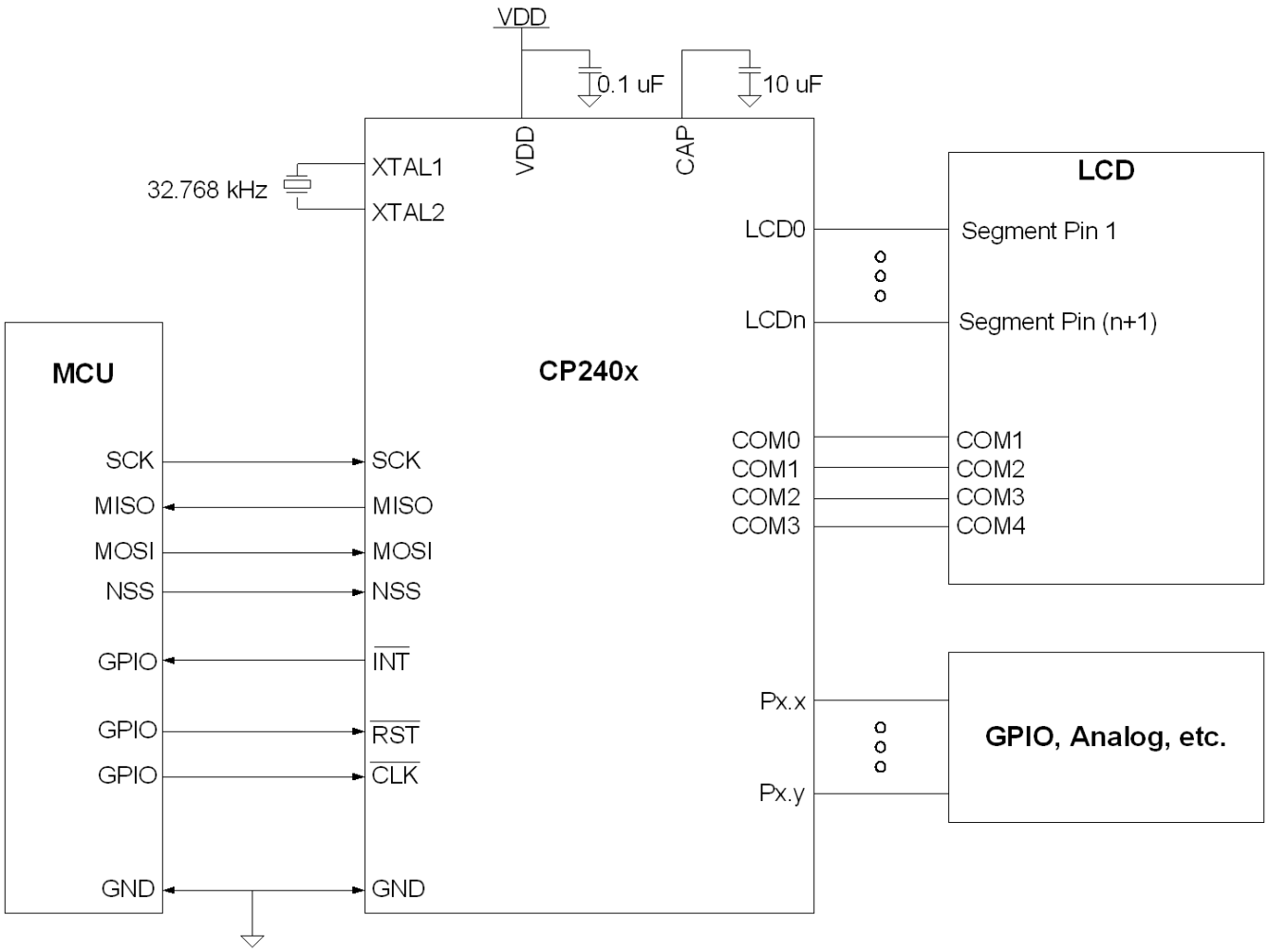


Figure 1.5. Typical Connection Diagram (SPI Interface)

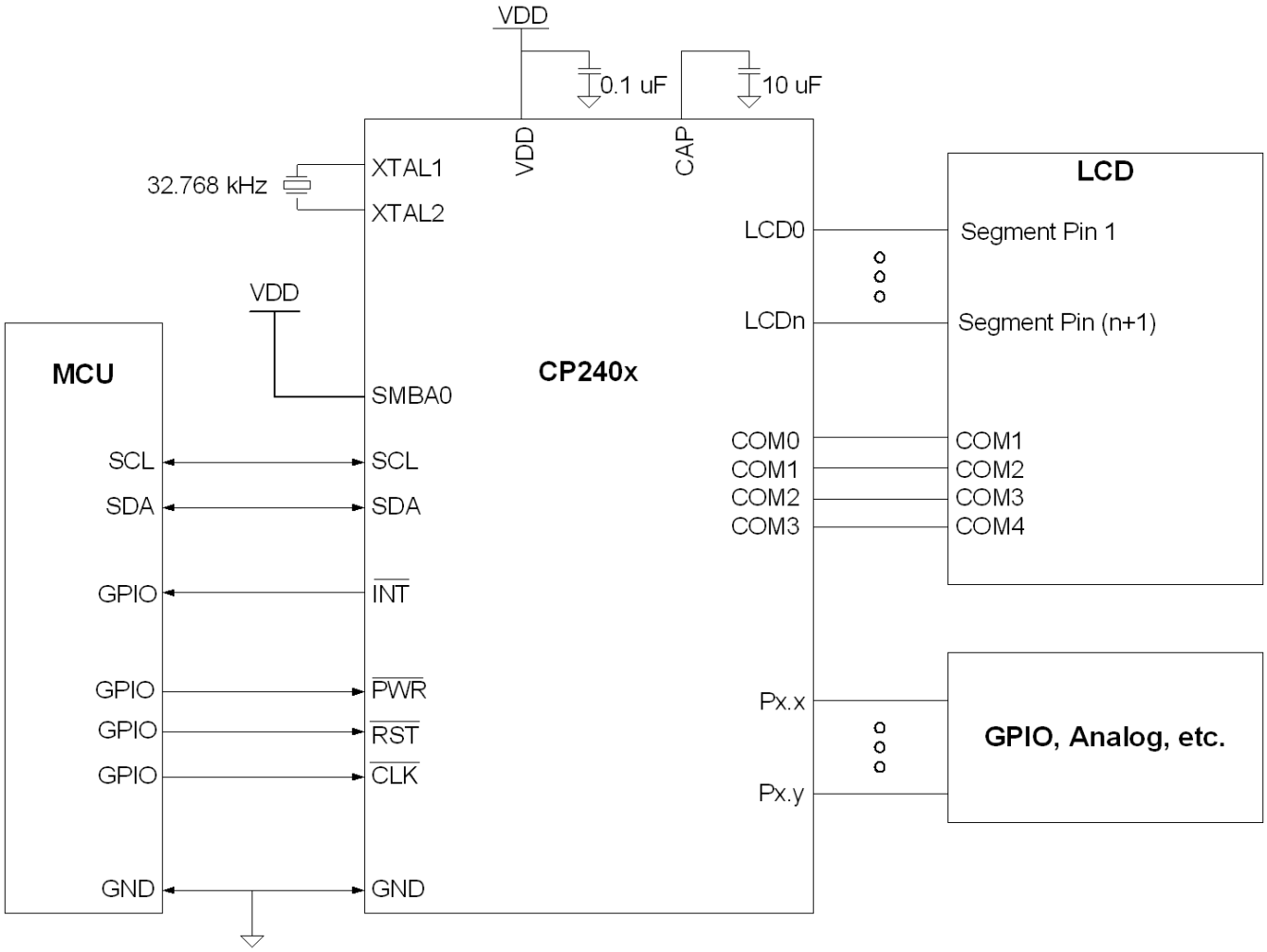


Figure 1.6. Typical Connection Diagram (SMBus/I^{2}C Interface)

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any I/O Pin or $\overline{RST}$ with respect to GND	V_{DD} > 2.2 V V_{DD} < 2.2 V	–0.3	—	5.8 V_{DD} + 3.6	V
Voltage on V_{DD} with respect to GND		–0.3	—	4.2	V
Maximum Total current through V_{DD} and GND		—	—	500	mA
Maximum output current sunk by $\overline{RST}$ or any I/O pin		—	—	100	mA

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at or exceeding the conditions in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. Electrical Characteristics

Table 3.1. Global Electrical Characteristics

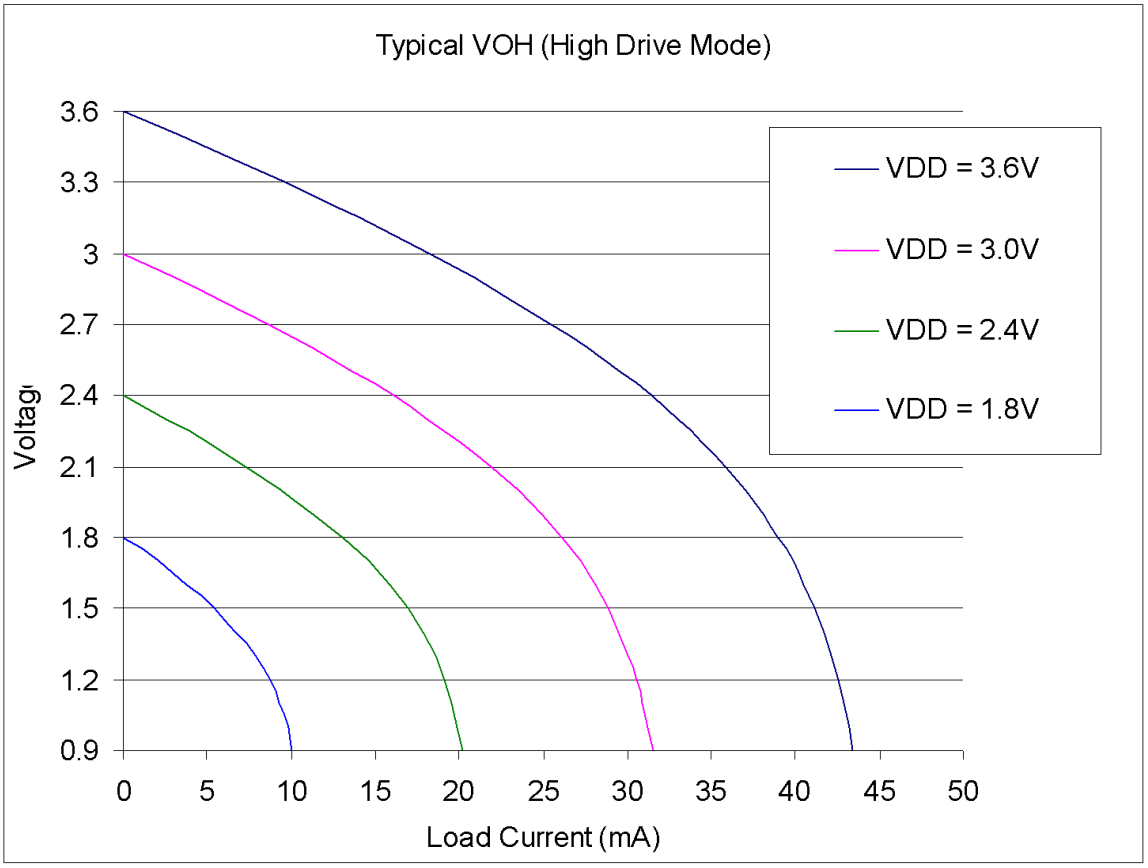
V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		1.8	3.3	3.6	V
SYSCLK		0	—	25	MHz
T_{SYSH} (SYSCLK High Time)		18	—	—	ns
T_{SYSL} (SYSCLK Low Time)		18	—	—	ns
Specified Operating Temperature Range		–40	—	+85	°C
Normal Mode Supply Current (V_{DD} = 3.0 V, 25 °C unless otherwise specified)					
20 MHz Internal Oscillator divided by 1, SYSCLK = 20 MHz, SPI data rate = 1 Mbps*	V_{DD} = 3.6 V V_{DD} = 3.0 V V_{DD} = 1.8 V	— — —	740 700 630	790 — —	µA
Accessing RAM at 1 Mbps		—	740	—	µA
SYSCLK = 10 MHz, SPI data rate* = 500 kbps		—	380	—	µA
SYSCLK = 5 MHz, SPI data rate* = 250 kbps		—	230	—	µA
SYSCLK = 2.5 MHz, SPI data rate* = 125 kbps		—	150	—	µA
RAM Preservation Mode Supply Current (V_{DD} = 3.0 V, 25 °C unless otherwise specified)					
32.768 kHz SmaRTClock Selected as the System Clock, Internal Oscillator Disabled		—	20	—	µA
Ultra Low Power LCD Mode Supply Current (V_{DD} = 3.0 V, 25 °C unless otherwise specified)					
LCD Enabled with Charge Pump Enabled, 60 Hz Refresh Rate, No Load SmaRTClock with 32.768 kHz crystal	4-Mux mode 3-Mux mode 2-Mux mode static mode	— — — —	2.3 2.3 2.2 2.1	— — — —	µA
LCD Enabled with Charge Pump Enabled, 60 Hz Refresh Rate, No Load SmaRTClock in Self-Oscillate Mode (AGC Enabled, LOADCAP = 0x0F)	4-Mux mode 3-Mux mode 2-Mux mode static mode	— — — —	1.7 1.7 1.7 1.5	— — — —	µA
Ultra Low Power SmaRTClock Mode Supply Current (V_{DD} = 3.0 V, 25 °C unless otherwise specified)					
External Crystal (RTC Timer Enabled)	Fosc = 32.768 kHz	—	2.5	—	µA
CMOS Clock Input on XTAL1 and XTAL2 Pins (RTC Timer Enabled)	Fosc = 32.768 kHz	—	2.3	—	µA
Self-Oscillate Mode (AGC enabled, LOADCAP = 0x0F) (RTC Timer Enabled)	Fosc = 14 kHz	—	2.0	—	µA
Shutdown Mode (V_{DD} = 3.0 V, 25 °C unless otherwise specified)					
Shutdown (no clocks active, regulator disabled)	V_{DD} = 3.6 V V_{DD} = 3.0 V V_{DD} = 1.8 V	— — —	0.030 0.020 0.015	— — —	µA
***Note:** Indicates maximum allowed SPI data rate in this mode. Power measurement taken with no SPI traffic.					

Table 3.2. Port I/O DC Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	High Drive Strength, PnDRV.n = 1				
	I_{OH} = –3 mA, Port I/O push-pull	V_{DD} – 0.7	—	—	
	I_{OH} = –10 µA, Port I/O push-pull	V_{DD} – 0.1	—	—	
	I_{OH} = –10 mA, Port I/O push-pull	—	See Chart	—	
	Low Drive Strength, PnDRV.n = 0				V
	I_{OH} = –1 mA, Port I/O push-pull	V_{DD} – 0.7	—	—	
	I_{OH} = –10 µA, Port I/O push-pull	V_{DD} – 0.1	—	—	
	I_{OH} = –3 mA, Port I/O push-pull	—	See Chart	—	
Output Low Voltage	High Drive Strength, PnDRV.n = 1				
	I_{OL} = 8.5 mA	—	—	0.6	
	I_{OL} = 10 µA	—	—	0.1	
	I_{OL} = 15 mA	—	See Chart	—	
	Low Drive Strength, PnDRV.n = 0				V
	I_{OL} = 1.4 mA	—	—	0.6	
	I_{OL} = 10 µA	—	—	0.1	
	I_{OL} = 4 mA	—	See Chart	—	
Input High Voltage	V_{DD} = 2.0 to 3.6 V	V_{DD} – 0.6	—	—	V
	V_{DD} = 1.8 to 2.0 V	0.7 x V_{DD}	—	—	V
Input Low Voltage	V_{DD} = 2.0 to 3.6 V	—	—	0.6	V
	V_{DD} = 1.8 to 2.0 V	—	—	0.3 x V_{DD}	V
Input Leakage Current	Weak Pullup On, V_{IN} = 0 V, V_{DD} = 1.8 V	—	4	—	µA
	Weak Pullup On, Vin = 0 V, V_{DD} = 3.6 V	—	20	30	



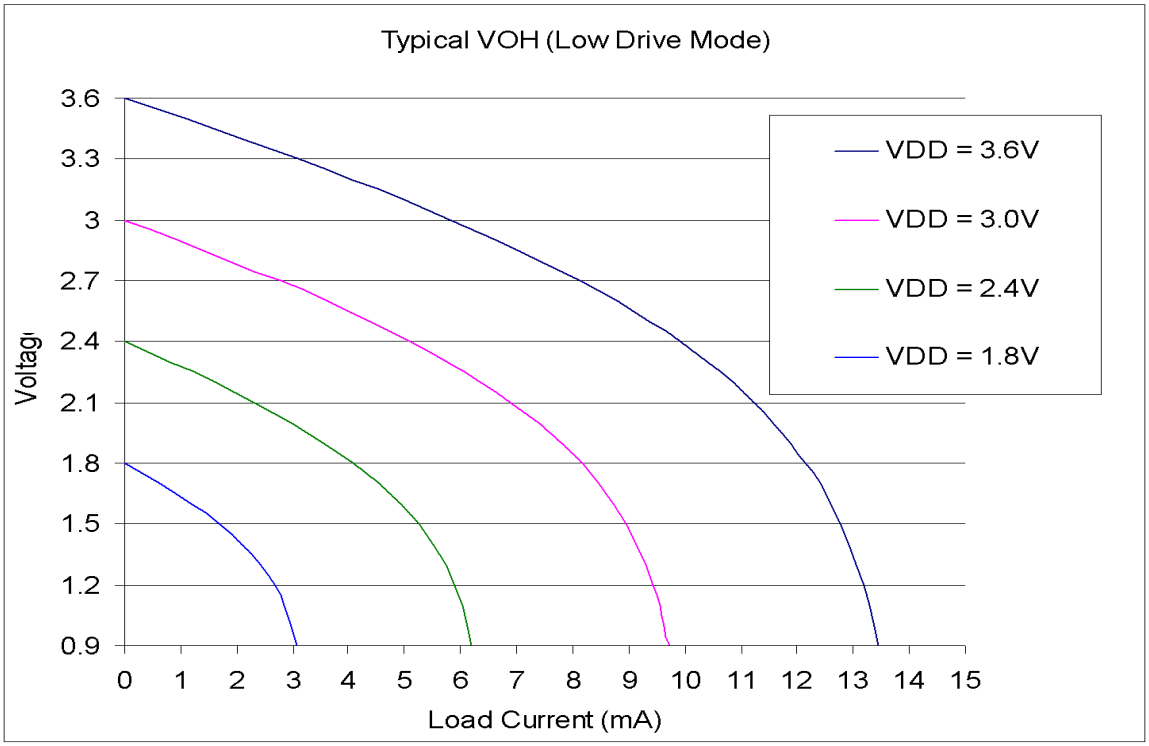
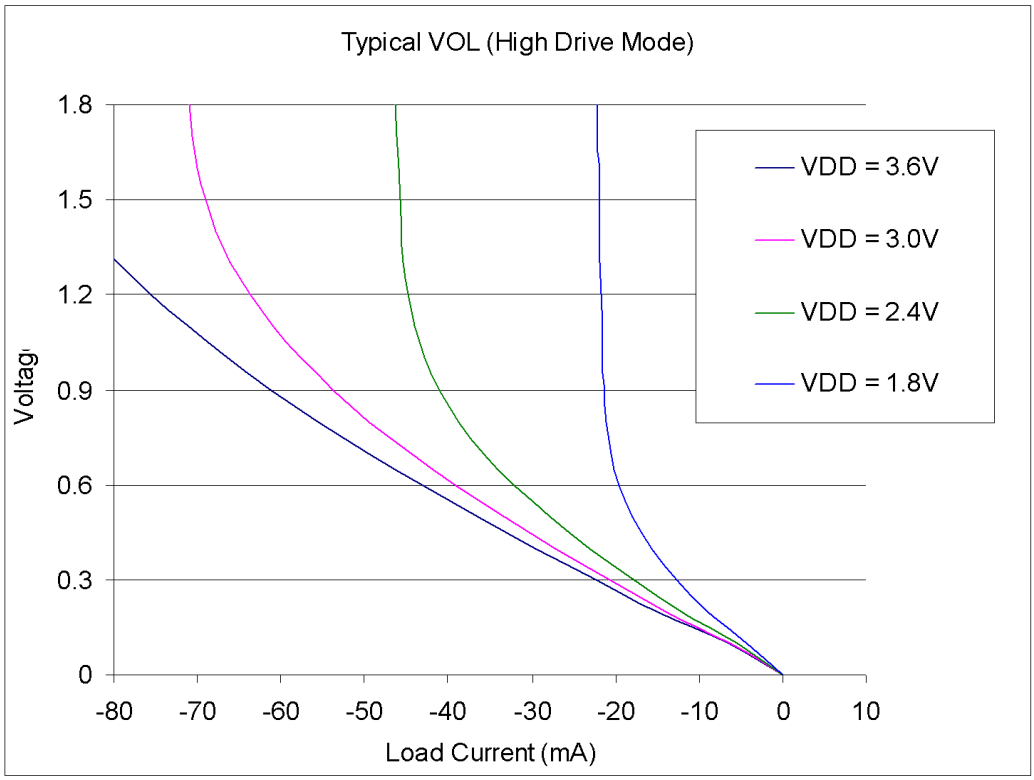


Figure 3.1. Typical VOH



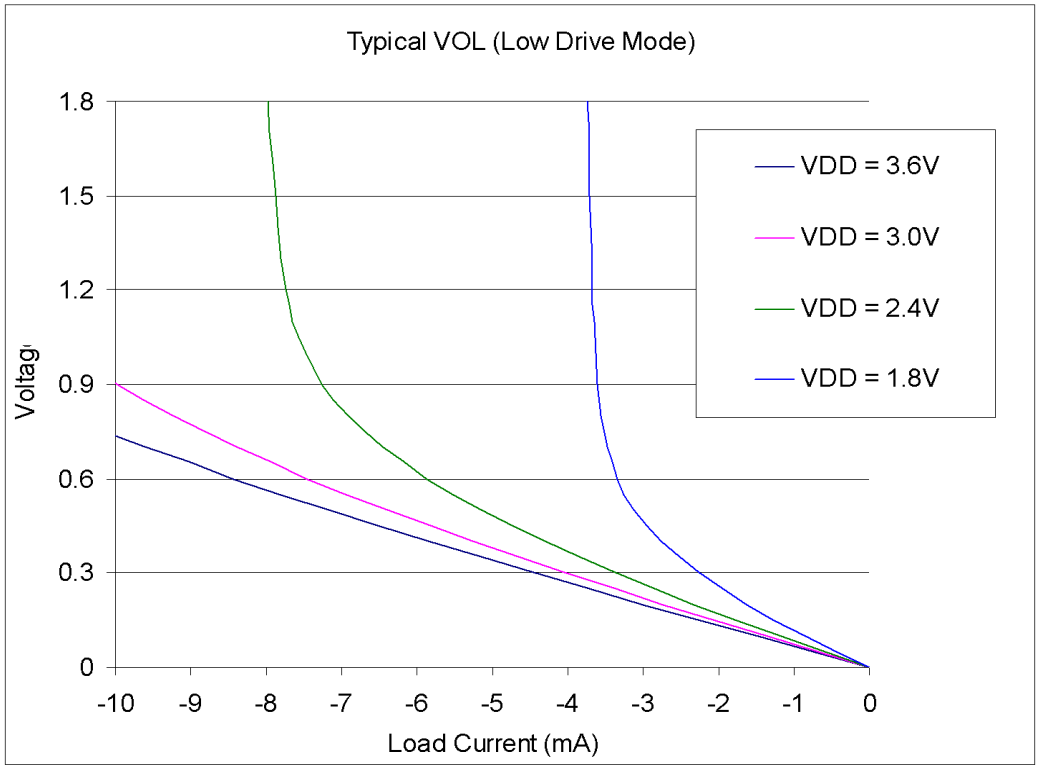


Figure 3.2. Typical VOL

Table 3.3. Reset Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	UNITS
$\overline{RST}$ Input High Voltage		0.7 x V_{DD}	—	—	V
$\overline{RST}$ Input Low Voltage		—	—	0.3 x V_{DD}	V
$\overline{RST}$ Input Pullup Current	$\overline{RST}$ = 0 V, V_{DD} = 1.8 V $\overline{RST}$ = 0 V, V_{DD} = 3.6 V	— —	4 20	— 30	µA
V_{DD} Ramp Time for Power On[1]	V_{DD} Ramp from 0–1.8 V	—	—	1	ms
Power on Reset Delay ($T_{PORDelay}$) from Start of Ramp until the Reset Complete Interrupt	V_{DD} = 1.8 V V_{DD} = 3.0 V V_{DD} = 3.6 V	— — —	1200 660 575	— 900 —	µs
Required $\overline{RST}$ Low Time to guarantee a System Reset (T_{RST})	See Note 2	15	—	—	µs
Startup Delay from Reset De-asserted until the Reset Complete Interrupt ($T_{STARTUP}$)	Pin Reset	—	90	100	µs

Notes:
1. There is no restriction on VDD ramp time if the $\overline{RST}$ pin is toggled at the end of the ramp.
2. If the $\overline{RST}$ pin is held low for a shorter time period, a device reset may occur.

Table 3.4. Power Management Electrical Specifications

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
RAM Preservation Mode Wake-Up Time	From the falling edge of $\overline{CLK}$ until host interface ready		10		ns
ULP Mode Wake-Up Time (from the falling edge of NSS/PWR to the reset complete interrupt)	Port Match or SmaRTClock Wakeup NSS/PWR Pin Wakeup	3 7	— —	4 8	RTC Cycles

Table 3.5. Internal Oscillator Electrical Characteristics

V_{DD} = 1.8 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	–40 to +85 °C, V_{DD} = 1.8–3.6 V	15	20	25	MHz
Oscillator Supply Current (from V_{DD})	25 °C	—	50	—	µA

Table 3.6. LCD Electrical Characteristics

V_{DD} = 1.8 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Charge Pump Output Voltage Error		—	±30	—	mV

4. Pinout and Package Definitions

Table 1. CP2400/1/2/3 Pin Definitions

Name	Pin Numbers				Type	Description
	48-pin		32-pin			
	SPI	I^2C	SPI	I^2C		
XTAL1	1	1	1	1	A In	Crystal Input. This pin is the return for the external oscillator driver. This pin can be overdriven by an external CMOS clock.
XTAL2	2	2	2	2	A Out	Crystal Output. This pin is the excitation driver for a quartz crystal.
V_{DD}	3	3	3	3	Power In	1.8–3.6 V Power Supply Voltage Input.
GND	4	4	4	4		Ground
CAP	48	48	32	32	Power Out	LCD Power Supply Voltage Output. This pin requires a 10 µF decoupling capacitor.
$\overline{CLK}$	47	47	31	31	D In	CMOS clock input. This pin should not be left floating.
$\overline{RST}$	46	46	30	30	D In	Device Reset. An external source can initiate a system reset by driving this pin low for at least 15 µs. This pin has an internal weak pullup.
$\overline{INT}$	45	45	29	29	D Out	Interrupt Service Request. This pin provides notification to the host. This pin is a push-pull output.
NSS	44	—	28	—	D In	Slave select signal for SPI interface. This pin should not be left floating.
MOSI	43	—	27	—	D In	Master Out/Slave In data signal for SPI interface. This pin should not be left floating.
MISO	42	—	26	—	D Out	Master In/Slave Out data signal for SPI interface
SCK	41	—	25	—	D In	Clock signal for SPI interface. This pin should not be left floating.
$\overline{PWR}$	—	44	—	28	D In	Allows SMBus device to enter the Ultra Low Power mode. This pin should not be left floating.
SCL	—	43	—	27	D I/O	Clock signal for SMBus interface. This pin should not be left floating.
SDA	—	42	—	26	D I/O	Data signal for SMBus interface. This pin should not be left floating.
SMBA0	—	41	—	25	D In	Bit 0, SMBus Slave Address. This pin should not be left floating.
P0.0 LCD0	40	40	24	24	D I/O A Out	Bit 0, Port 0
P0.1 LCD1	39	39	23	23	D I/O A Out	Bit 1, Port 0

Table 1. CP2400/1/2/3 Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	48-pin		32-pin			
	SPI	I^2C	SPI	I^2C		
P0.2 LCD2	38	38	22	22	D I/O A Out	Bit 2, Port 0
P0.3 LCD3	37	37	21	21	D I/O A Out	Bit 3, Port 0
P0.4 LCD4	36	36	20	20	D I/O A Out	Bit 4, Port 0
P0.5 LCD5	35	35	19	19	D I/O A Out	Bit 5, Port 0
P0.6 LCD6	34	34	18	18	D I/O A Out	Bit 6, Port 0
P0.7 LCD7	33	33	17	17	D I/O A Out	Bit 7, Port 0
P1.0 LCD8	32	32	16	16	D I/O A Out	Bit 0, Port 1
P1.1 LCD9	31	31	15	15	D I/O A Out	Bit 1, Port 1
P1.2 LCD10	30	30	14	14	D I/O A Out	Bit 2, Port 1
P1.3 LCD11	29	29	13	13	D I/O A Out	Bit 3, Port 1
P1.4 LCD12	28	28	12	12	D I/O A Out	Bit 4, Port 1
P1.5 LCD13	27	27	11	11	D I/O A Out	Bit 5, Port 1
P1.6 LCD14	26	26	10	10	D I/O A Out	Bit 6, Port 1
P1.7 LCD15	25	25	9	9	D I/O A Out	Bit 7, Port 1
P2.0 LCD16	24	24	—	—	D I/O A Out	Bit 0, Port 2
P2.1 LCD17	23	23	—	—	D I/O A Out	Bit 1, Port 2

Table 1. CP2400/1/2/3 Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	48-pin		32-pin			
	SPI	I^2C	SPI	I^2C		
P2.2 LCD18	22	22	—	—	D I/O A Out	Bit 2, Port 2
P2.3 LCD19	21	21	—	—	D I/O A Out	Bit 3, Port 2
P2.0 COM0	—	—	8	8	D I/O A Out	Bit 0, Port 2
P2.1 COM1	—	—	7	7	D I/O A Out	Bit 1, Port 2
P2.2 COM2	—	—	6	6	D I/O A Out	Bit 2, Port 2
P2.3 COM3	—	—	5	5	D I/O A Out	Bit 3, Port 2
P2.4 LCD20	20	20	—	—	D I/O A Out	Bit 4, Port 2
P2.5 LCD21	19	19	—	—	D I/O A Out	Bit 5, Port 2
P2.6 LCD22	18	18	—	—	D I/O A Out	Bit 6, Port 2
P2.7 LCD23	17	17	—	—	D I/O A Out	Bit 7, Port 2
P3.0 LCD24	16	16	—	—	D I/O A Out	Bit 0, Port 3
P3.1 LCD25	15	15	—	—	D I/O A Out	Bit 1, Port 3
P3.2 LCD26	14	14	—	—	D I/O A Out	Bit 2, Port 3
P3.3 LCD27	13	13	—	—	D I/O A Out	Bit 3, Port 3
P3.4 LCD28	12	12	—	—	D I/O A Out	Bit 4, Port 3
P3.5 LCD29	11	11	—	—	D I/O A Out	Bit 5, Port 3

Table 1. CP2400/1/2/3 Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	48-pin		32-pin			
	SPI	I^2C	SPI	I^2C		
P3.6 LCD30	10	10	—	—	D I/O A Out	Bit 6, Port 3
P3.7 LCD31	9	9	—	—	D I/O A Out	Bit 7, Port 3
P4.0 COM0	8	8	—	—	D I/O A Out	Bit 0, Port 4
P4.1 COM1	7	7	—	—	D I/O A Out	Bit 1, Port 4
P4.2 COM2	6	6	—	—	D I/O A Out	Bit 2, Port 4
P4.3 COM3	5	5	—	—	D I/O A Out	Bit 3, Port 4

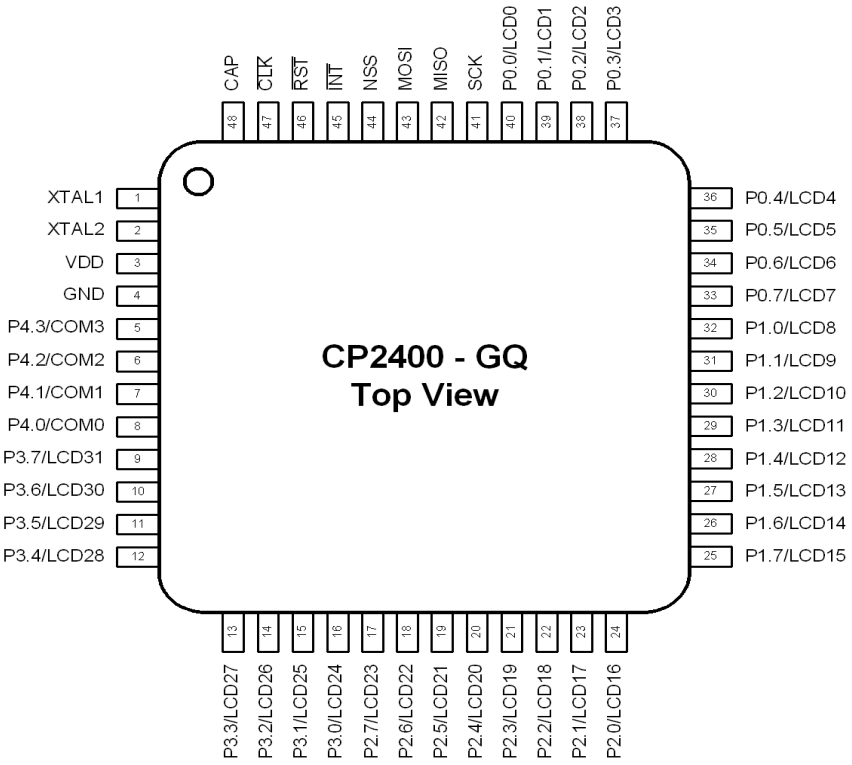


Figure 4.1. CP2400-GQ Pinout (SPI Interface)

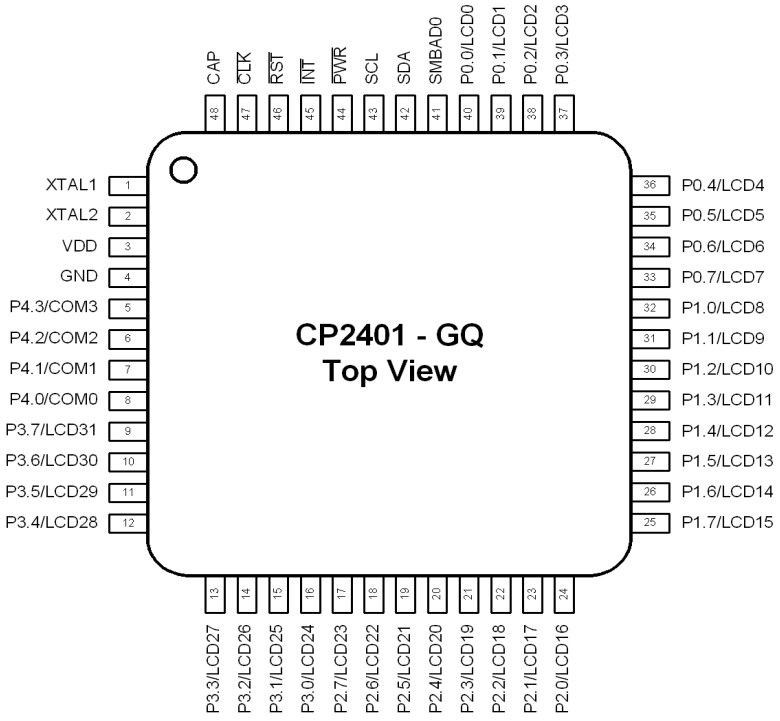


Figure 4.2. CP2401-GQ Pinout (SMBus/I^2C Interface)

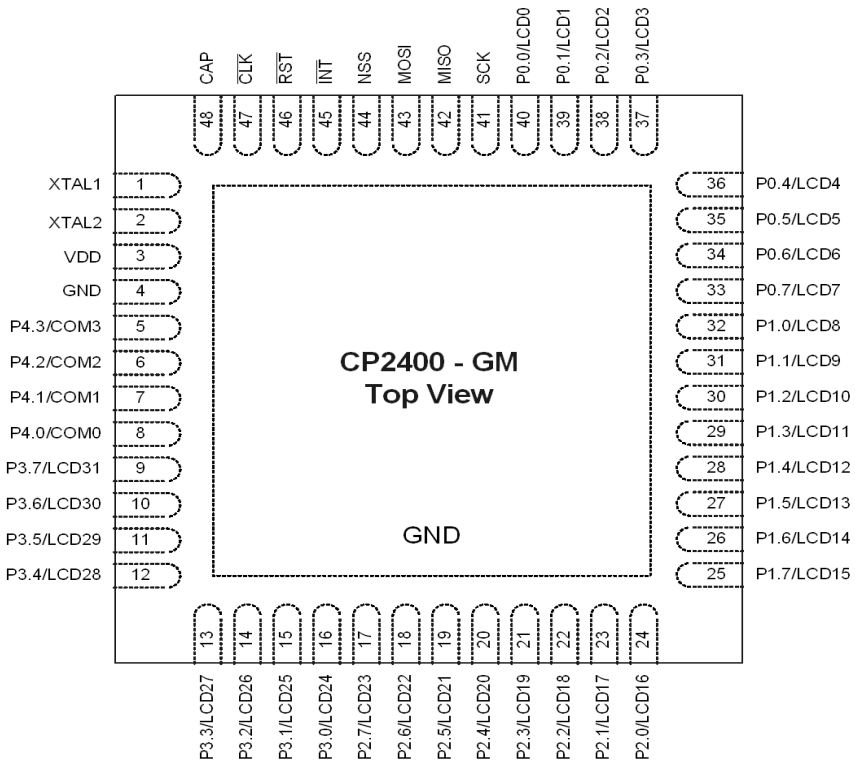


Figure 4.3. CP2400-GM Pinout (SPI Interface)

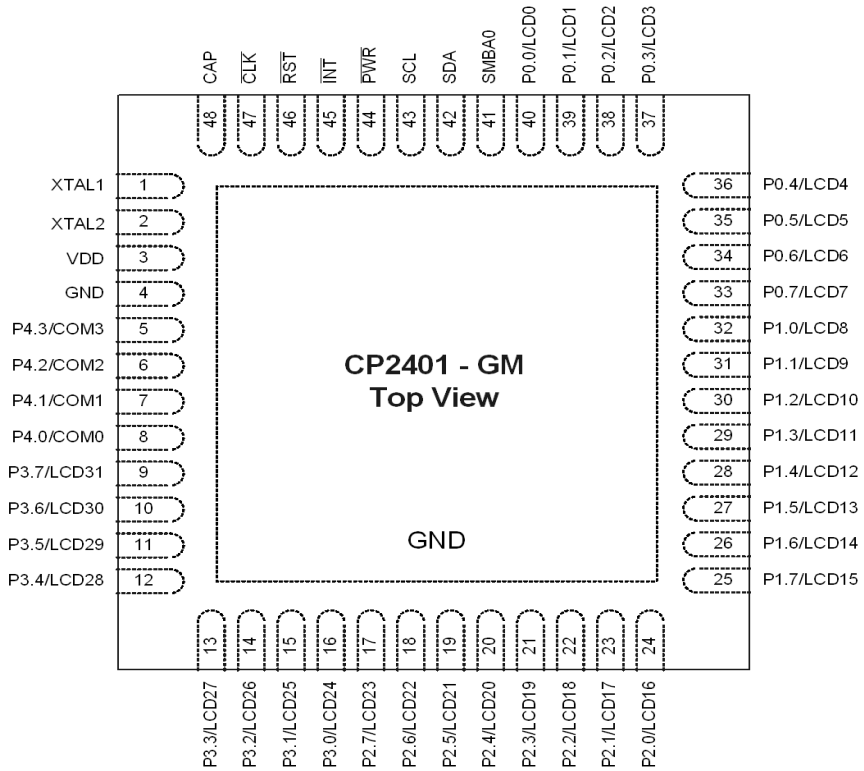


Figure 4.4. CP2401-GM Pinout (SMBus/I^{2}C Interface)

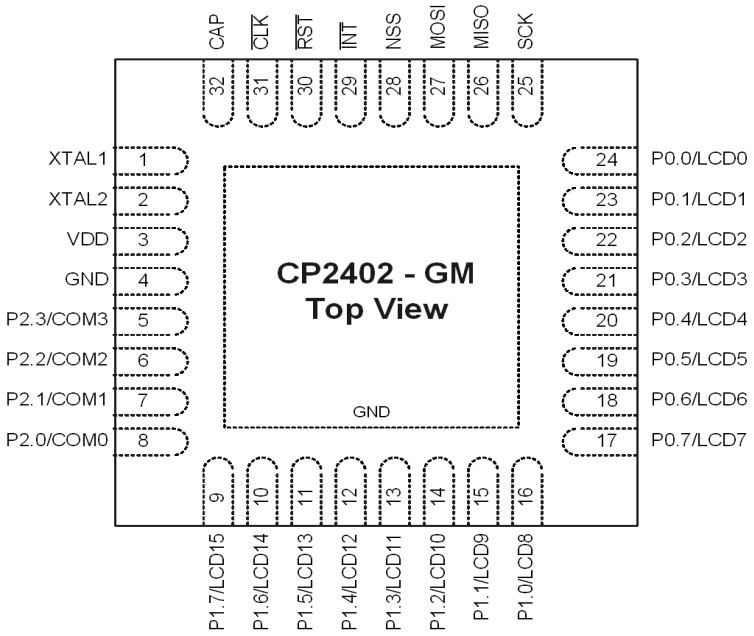


Figure 4.5. CP2402-GM Pinout (SPI Interface)

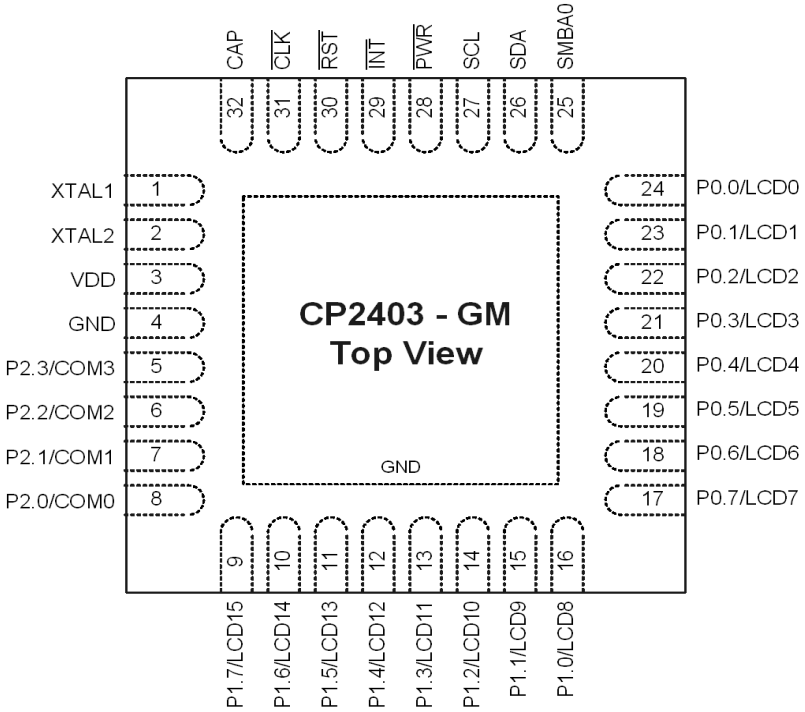
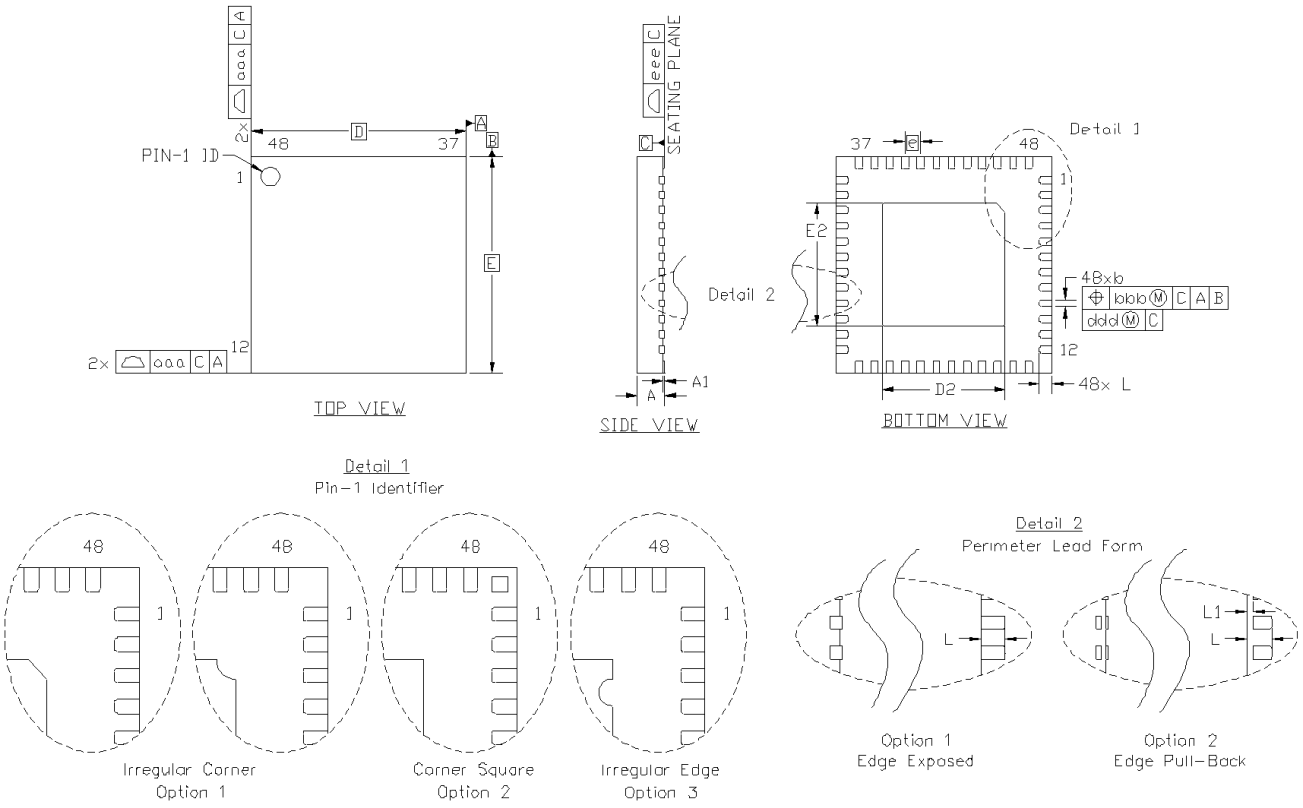


Figure 4.6. CP2403-GM Pinout (SMBus Interface)



Dimension	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	- -	0.05
b	0.18	0.23	0.30
D		7.00 BSC.	
D2	3.90	4.00	4.10
e		0.50 BSC.	
E		7.00 BSC.	
E2	3.90	4.00	4.10
L	0.30	0.40	0.50
L1	0.00	- -	0.10
aaa	--	--	0.10
bbb	--	--	0.10
ddd	--	--	0.05
eee	--	--	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VKKD-4 except for features D2 and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Figure 4.7. QFN-48 Package Drawing

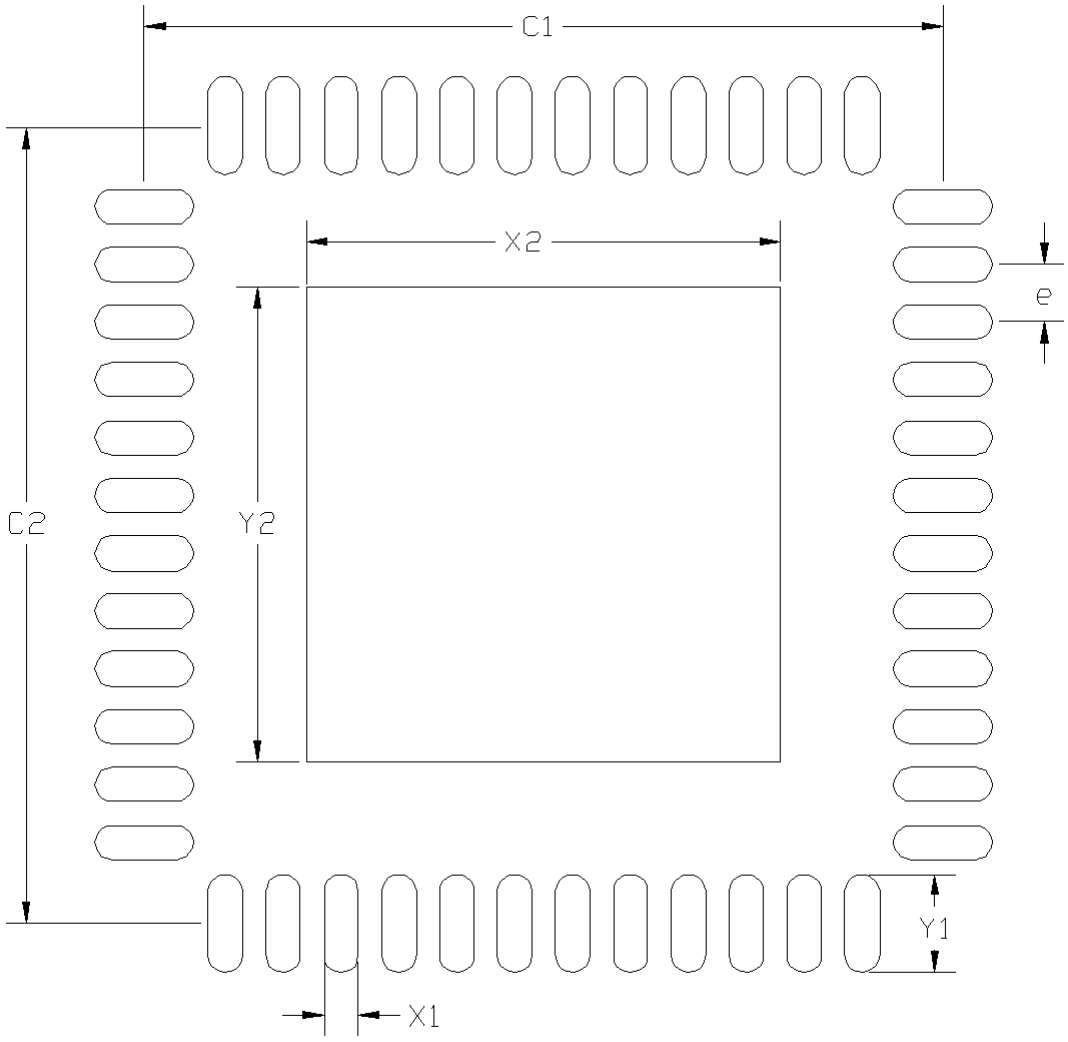


Figure 4.8. QFN-48 Landing Diagram