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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

intersil™

Datasheet August 19, 2015 FN2957.4

CMOS 16-Bit Microprocessor

The Intersil 80C86 high performance 16-bit CMOS CPU is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). Two modes of operation, minimum for small systems and maximum for larger applications such as multiprocessing, allow user configuration to achieve the highest performance level. Full TTL compatibility (with the exception of CLOCK) and industry standard operation allow use of existing NMOS 8086 hardware and software designs.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
CP80C86-2Z (Note)	CP80C86-2Z	0 to +70	40 Ld PDIP* (Pb-free)	E40.6
MD80C86-2/883	MD80C86-2/883	-55 to +125	40 Ld CERDIP	F40.6
MD80C86-2/B	MD80C86-2/B	-55 to +125	40 Ld CERDIP	F40.6
8405202QA	8405202QA	-55 to +125	40 Ld CERDIP (SMD)	F40.6

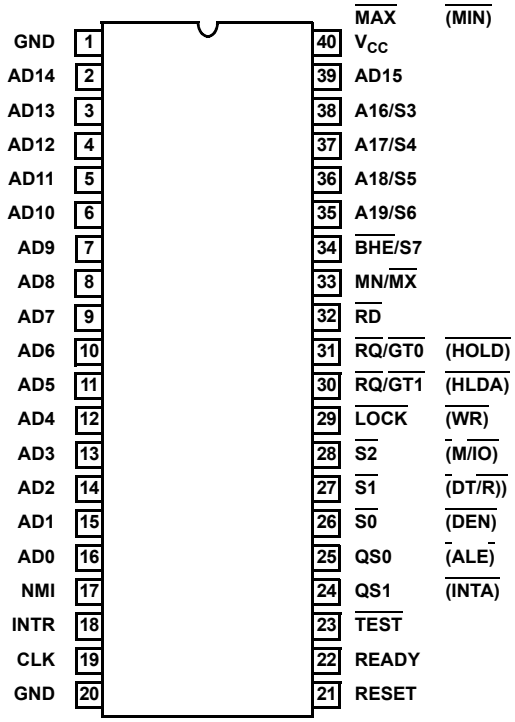
*Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications. NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

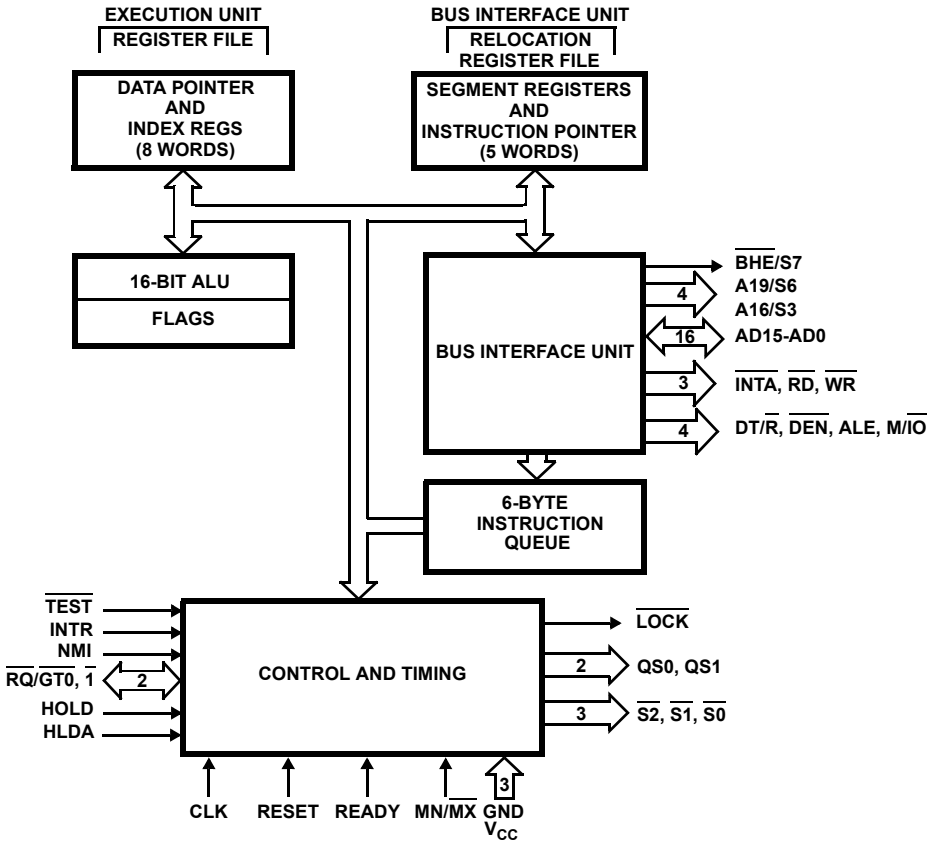
- **Compatible with NMOS 8086**
- **Completely Static CMOS Design**
  - **DC . . . . . .8MHz (80C86-2)**
- **Low Power Operation**
  - **ICCSB . . . . . 500mA Max**
  - **ICCOP . . . . . 10mA/MHz Typ**
- **1MByte of Direct Memory Addressing Capability**
- **24 Operand Addressing Modes**
- **Bit, Byte, Word and Block Move Operations**
- **8-Bit and 16-Bit Signed/Unsigned Arithmetic**
  - **Binary, or Decimal**
  - **Multiply and Divide**
- **Wide Operating Temperature Range**
  - **C80C86 . . . . . 0°C to +70°C**
  - **M80C86 . . . . . -55°C to +125°C**
- **Pb-Free Available (RoHS Compliant)**

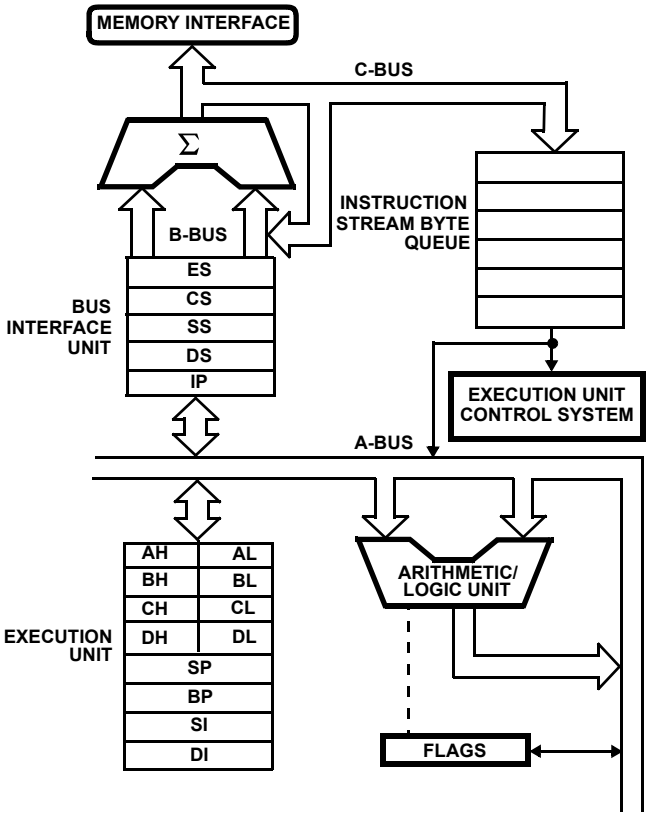
Pinout

80C86
(40 LD PDIP, CERDIP)
TOP VIEW



Functional Diagram





Pin Descriptions

The following pin function descriptions are for 80C86 systems in either minimum or maximum mode. The “Local Bus” in these description is the direct multiplexed bus interface connection to the 80C86 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
AD15-AD0	2-16, 39	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (t1) and data (t2, t3, tW, t4) bus. A0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D7-D0. It is LOW during Ti when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A0 to condition chip select functions (See $\overline{BHE}$). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus “hold acknowledge” or “grant sequence”.
A19/S6 A18/S5 A17/S4 A16/S3	35-38	O	ADDRESS/STATUS: During t1, these are the 4 most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during t2, t3, tW, t4. S6 is always LOW. The status of the interrupt enable FLAG bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown. This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus “hold acknowledge” or “grant sequence”.
$\overline{BHE}$/S7	34	O	BUS HIGH ENABLE/STATUS: During t1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D15-D8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during t1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during t2, t3 and t4. The signal is active LOW, and is held at high impedance to the last valid logic level during interrupt acknowledge and local bus “hold acknowledge” or “grant sequence”, it is LOW during t1 for the first interrupt acknowledge cycle.
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the M/$\overline{IO}$ or $\overline{S2}$ pin. This signal is used to read devices which reside on the 80C86 local bus. $\overline{RD}$ is active LOW during t2, t3 and tW of any read cycle, and is guaranteed to remain HIGH in t2 until the 80C86 local bus has floated. This line is held at a high impedance logic one state during “hold acknowledge” or “grand sequence”.
READY	22	I	READY: The acknowledgment from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C84A Clock Generator to form READY. This signal is active HIGH. The 80C86 READY input is not synchronized. Correct operation is not guaranteed if the Setup and Hold Times are not met.
INTR	18	I	INTERRUPT REQUEST: A level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.

S4	S3	CHARACTERISTICS
0	0	Alternate Data
0	1	Stack
1	0	Code or None
1	1	Data

BHE	A0	CHARACTERISTICS
0	0	Whole Word
0	1	Upper Byte From/to Odd Address
1	0	Lower Byte From/to Even address
1	1	None

Pin Descriptions (Continued)

The following pin function descriptions are for 80C86 systems in either minimum or maximum mode. The “Local Bus” in these description is the direct multiplexed bus interface connection to the 80C86 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{TEST}$	23	I	TEST: input is examined by the “Wait” instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an “Idle” state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: An edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: Causes the processor to immediately terminate its present activity. The signal must transition LOW to HIGH and remain active HIGH for at least 4 clock cycles. It restarts execution, as described in the “Instruction Set Summary” on page 31 when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: Provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VCC	40		VCC: +5V power supply pin. A 0.1µF capacitor between pins 20 and 40 is recommended for decoupling.
GND	1, 20		GND: Ground. Note: Both must be connected. A 0.1µF capacitor between pins 1 and 20 is recommended for decoupling.
MN/$\overline{MX}$	33	I	MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

Minimum Mode System

The following pin function descriptions are for the 80C86 in minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described in the following.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
M/$\overline{IO}$	28	O	STATUS LINE: Logically equivalent to $\overline{S2}$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the t4 preceding a bus cycle and remains valid until the final t4 of the cycle (M = HIGH, I/O = LOW). M/$\overline{IO}$ is held to a high impedance logic one during local bus “hold acknowledge”.
$\overline{WR}$	29	O	WRITE: Indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for t2, t3 and tW of any write cycle. It is active LOW, and is held to high impedance logic one during local bus “hold acknowledge”.
$\overline{INTA}$	24	O	INTERRUPT ACKNOWLEDGE: Used as a read strobe for interrupt acknowledge cycles. It is active LOW during t2, t3 and tW of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: Provided by the processor to latch the address into the 82C82/82C83 address latch. It is a HIGH pulse active during clock LOW of t1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: Needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in maximum mode, and its timing is the same as for M/$\overline{IO}$ (T = HIGH, R = LOW). DT/$\overline{R}$ is held to a high impedance logic one during local bus “hold acknowledge”.
$\overline{DEN}$	26	O	DATA ENABLE: Provided as an output enable for a bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of t2 until the middle of t4, while for a write cycle it is active from the beginning of t2 until the middle of t4. $\overline{DEN}$ is held to a high impedance logic one during local bus “hold acknowledge”.

Minimum Mode System (Continued)

The following pin function descriptions are for the 80C86 in minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described in the following.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
HOLD HLDA	31, 30	I O	HOLD: indicates that another master is requesting a local bus “hold”. To be an acknowledged, HOLD must be active HIGH. The processor receiving the “hold” will issue a “hold acknowledge” (HLDA) in the middle of a t4 or TI clock cycle. Simultaneously with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

Maximum Mode System

The following pin function descriptions are for the 80C86 system in maximum mode (i.e., MN/$\overline{MX}$ - GND). Only the pin functions which are unique to maximum mode are described in the following.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	26 27 28	O O O	STATUS: is active during t4, t1 and t2 and is returned to the passive state (1, 1, 1) during t3 or during tW when READY is HIGH. This status is used by the 82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$ or $\overline{S0}$ during t4 is used to indicate the beginning of a bus cycle, and the return to the passive state in t3 or tW is used to indicate the end of a bus cycle. These signals are held at a high impedance logic one state during “grant sequence”.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

Maximum Mode System (Continued)

The following pin function descriptions are for the 80C86 system in maximum mode (i.e., MN/$\overline{MX}$ - GND). Only the pin functions which are unique to maximum mode are described in the following.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{RQ}/\overline{GT0}$ $\overline{RQ}/\overline{GT1}$	31, 30	I/O	REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GTO}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ}/\overline{GT}$ Sequence Timing) 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 80C86 (pulse 1). 2. During a t4 or TI clock cycle, a pulse 1 CLK wide from the 80C86 to the requesting master (pulse 2) indicates that the 80C86 has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse 1 CLK wide from the requesting master indicates to the 80C86 (pulse 3) that the "hold" request is about to end and that the 80C86 can reclaim the local bus at the next CLK. The CPU then enters t4 (or TI if no bus cycles pending). Each Master-Master exchange of the local bus is a sequence of 3 pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low. If the request is made while the CPU is performing a memory cycle, it will release the local bus during t4 of the cycle when all the following conditions are met: 1. Request occurs on or before t2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next cycle. 2. A memory cycle will start within three clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	29	O	LOCK: output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a high impedance logic one state during "grant sequence". In MAX mode, $\overline{LOCK}$ is automatically generated during t2 of the first INTA cycle and removed during t2 of the second INTA cycle.
QS1, QSO	24, 25	O	QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS1 and QS0 provide status to allow external tracking of the internal 80C86 instruction queue. Note that QS1, QS0 never become high impedance. QSI / QSO / — 0 / 0 / No Operation 0 / 1 / First byte of op code from queue 1 / 0 / Empty the queue 1 / 1 / Subsequent byte from queue

Functional Description

Static Operation

All 80C86 circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C86 can operate from DC to the specified upper frequency limit. The processor clock may be stopped in either state (HIGH/LOW) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C86 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C86 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the 80C86 power requirement is the standby current, (500µA maximum).

Internal Architecture

The internal functions of the 80C86 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the “Functional Diagram” on page 3.

These units can interact directly, but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces “dead-time” on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20-bit address to memory, which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra and stack segments of up to 64k bytes each, with each segment falling on 16-byte boundaries (see Figure 1).

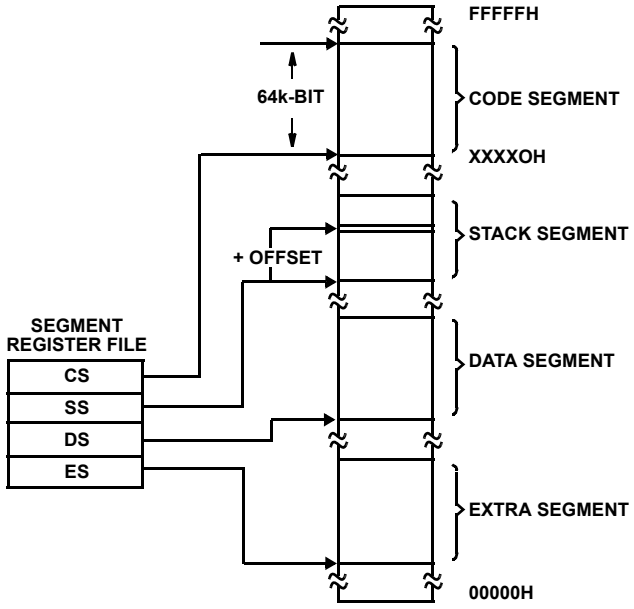


FIGURE 1. 80C86 MEMORY ORGANIZATION

TABLE 1.

TYPE OF MEMORY REFERENCE	DEFAULT SEGMENT BASE	ALTERNATE SEGMENT BASE	OFFSET
Instruction Fetch	CS	None	IP
Stack Operation	SS	None	SP
Variable (except following)	DS	CS, ES, SS	Effective Address
String Source	DS	CS, ES, SS	SI
String Destination	ES	None	DI
BP Used As Base Register	SS	CS, DS, ES	Effective Address

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the specific rules of Table 1. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into re-locatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster and more structured (see Table 1).

Word (16-bit) operands can be located on even or odd address boundaries and are thus, not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses; one, if the word operand is on an even byte boundary and two, if it is on an odd byte boundary. Except for the performance penalty**,** this double access is transparent to the software. The performance penalty does not occur for instruction fetches; only word operands.

Physically, the memory is organized as a high bank (D15-D8) and a low bank (D7-D0) of 512k bytes addressed in parallel by the processor's address lines.

Byte data with even addresses is transferred on the D7-D0 bus lines, while odd addressed byte data (A0 HIGH) is transferred on the D15-D8 bus lines. The processor provides two enable signals, BHE and A_0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor at the byte level as necessary.

In referencing word data, the BIU requires one or two memory cycles depending on whether the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (see Figure 2). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed through its own pair of 16-bit pointers (segment address pointer and offset address pointer). The first pointer, used as the offset address, is loaded into the IP and the second pointer, which designates the base address is loaded into the CS. At this point, program control is transferred to the interrupt routine. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

Minimum and Maximum Operation Modes

The requirements for supporting minimum and maximum 80C86 systems are sufficiently different that they cannot be met efficiently using 40 uniquely defined pins. Consequently, the 80C86 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the 80C86 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to V_{CC}, the 80C86 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode 80C86 can be used with either a multiplexed or demultiplexed bus. This architecture provides the 80C86 processing power in a highly integrated form.

The demultiplexed mode requires two 82C82 latches (for 64k addressability) or three 82C82 latches (for a full megabyte of addressing). An 82C86 or 82C87 transceiver can also be used if data bus buffering is required (see Figure 6A.) The 80C86 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 82C88 bus controller (see Figure 6B). The 82C88 decodes status lines $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$, and provides the system with all bus control signals.

Moving the bus control to the 82C88 provides better source and sink current capability to the control lines, and frees the 80C86 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 80C86 in maximum mode. These features allow coprocessors in local bus and remote bus configurations.

Bus Operation

The 80C86 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40 lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of 82C82 address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least 4 CLK cycles. These are referred to as t1, t2, t3 and t4 (see Figure 3). The address is emitted from the processor during t1 and data transfer occurs on the bus during t3 and t4. t2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (tW) are inserted between t3 and t4. Each inserted wait state is the same duration as a CLK cycle. Periods can occur between 80C86 driven bus cycles. These are referred to as idle" states (T_I) or inactive CLK cycles. The processor uses these cycles for internal housekeeping and processing.

During t1 of any bus cycle, the ALE (Address Latch Enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing

edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to Table 2.

TABLE 2.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (No Bus Cycle)

Status bits S3 through S7 are time multiplexed with high order address bits and the $\overline{BHE}$ signal, and are therefore valid during t2 through t4. S3 and S4 indicate which segment register (see “Instruction Set Summary” on page 31) was used for this bus cycle in forming the address, according to Table 3.

S5 is a reflection of the PSW interrupt enable bit. S3 is always zero and S7 is a spare status bit.

TABLE 3.

S4	S3	CHARACTERISTICS
0	0	Alternate Data (Extra Segment)
0	1	Stack
1	0	Code or None
1	1	Data

I/O Addressing

In the 80C86, I/O operations can address up to a maximum of 64k I/O byte registers or 32k I/O word registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D7-D0 bus lines and odd addressed bytes on D15-D8. Care must be taken to ensure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

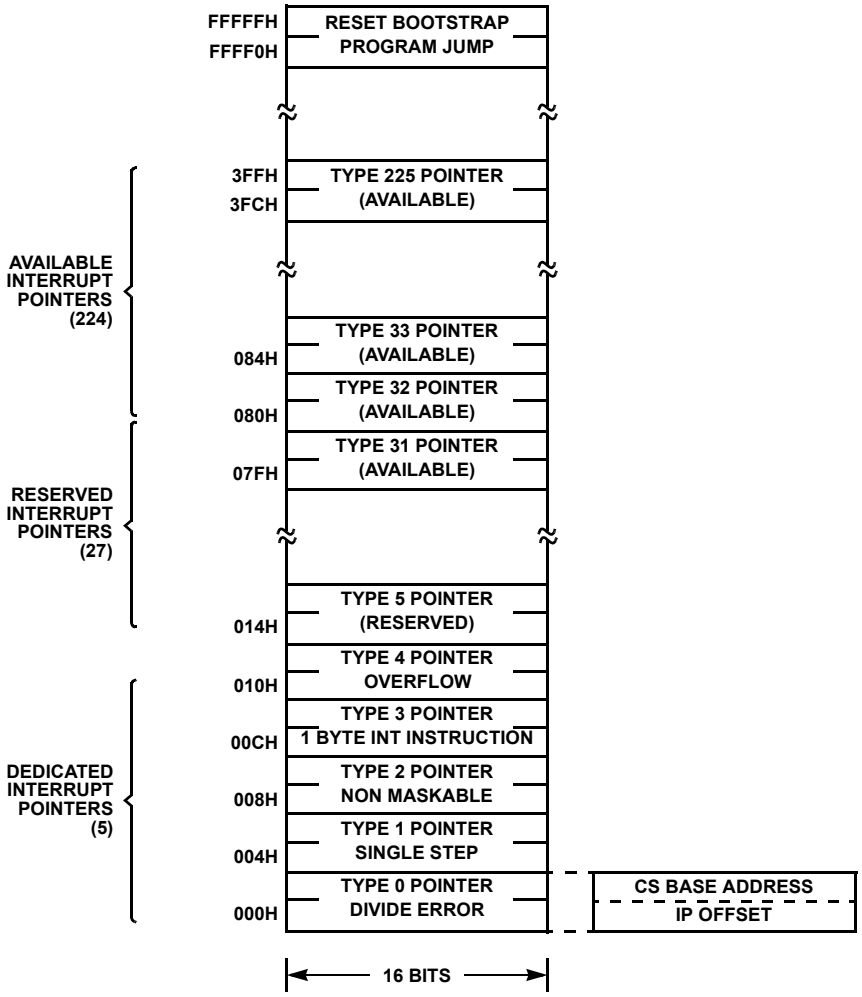


FIGURE 2. RESERVED MEMORY LOCATIONS

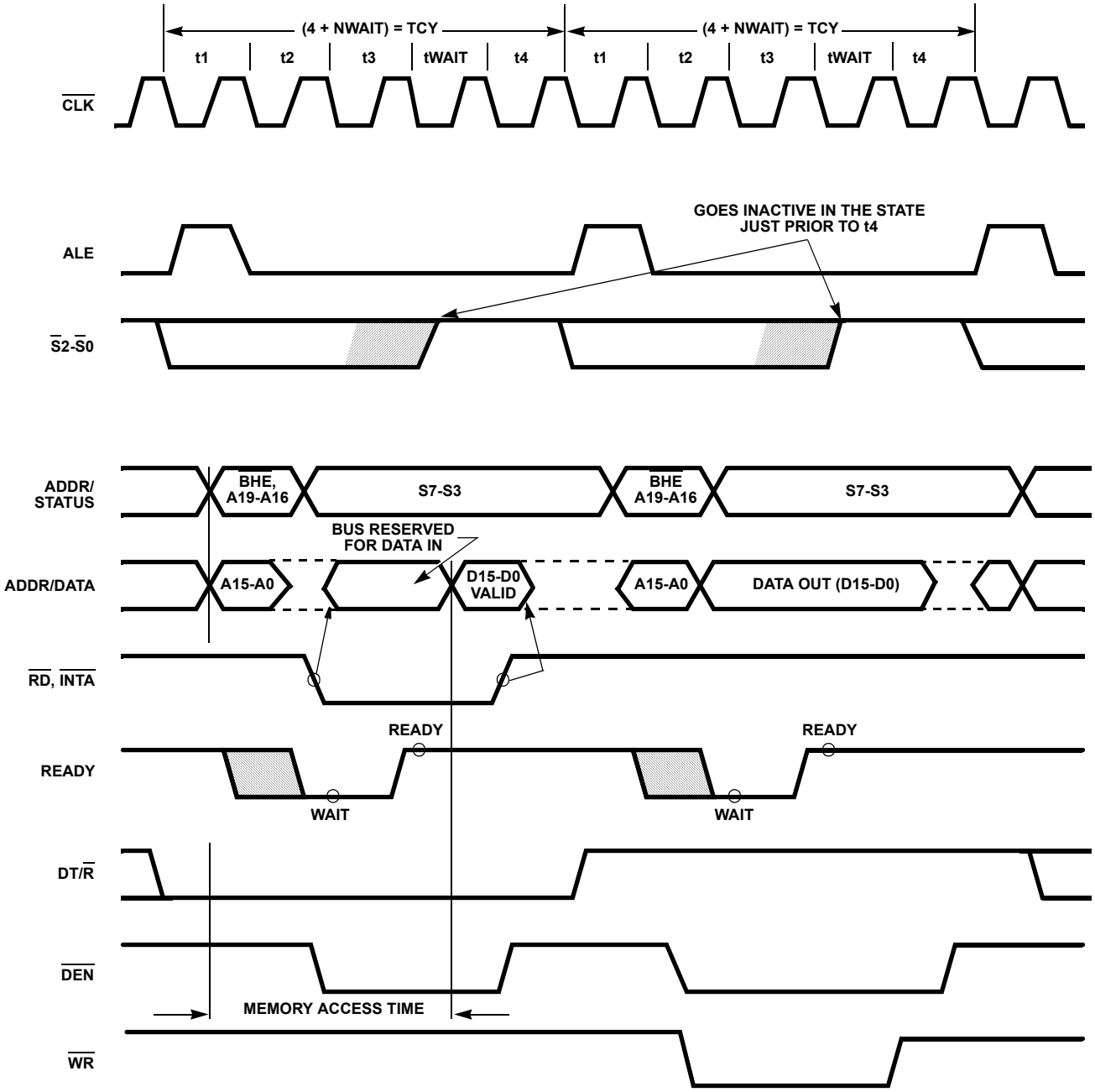


FIGURE 3. BASIC SYSTEM TIMING

External Interface

Processor RESET and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C86 RESET is required to be HIGH for greater than 4 CLK cycles. The 80C86 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 CLK cycles. After this interval, the 80C86 operates normally beginning with the instruction in absolute location FFFF0H (see Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH-to-LOW transition of RESET must occur no sooner than 50µs (or 4 CLK cycles, whichever is greater) after power-up, to allow complete initialization of the 80C86.

NMI will not be recognized prior to the second CLK cycle following the end of RESET. If NMI is asserted sooner than nine clock cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate need for pull-up/down resistors, “bus-hold” circuitry has been used on the 80C86 pins 2-16, 26-32 and 34-39 (see Figures 4A and 4B). These circuits will maintain the last valid logic state if no driving source is present (i.e., an unconnected pin or a driving source which goes to a high impedance state). To overdrive the “bus hold” circuits, an external driver must be capable of supplying approximately 400µA minimum sink or source current at valid input voltage levels. Since this “bus hold” circuitry is active and not a “resistive” type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

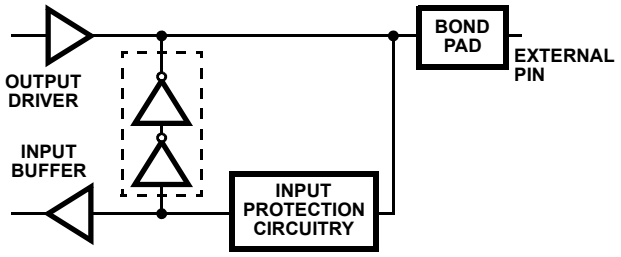


FIGURE 4A. BUS HOLD CIRCUITRY PINS 2-16, 34-39

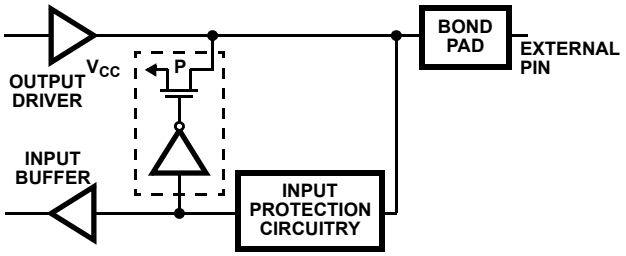


FIGURE 4B. BUS HOLD CIRCUITRY PINS 26-32

FIGURE 4. INTERNAL BUS HOLD DEVICES

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the “Instruction Set Summary” on page 31. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH, which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt “type”. An interrupting device supplies an 8-bit type number during the interrupt acknowledge sequence, which is used to “vector” through the appropriate element to the new interrupt service program location. All flags and both the Code Segment and Instruction Pointer register are saved as part of the $\overline{\text{INTA}}$ sequence. These are restored upon execution of an Interrupt Return (IRET) instruction.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any positive transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during or after the servicing of NMI. Another positive edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 80C86 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable flag (IF) status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. INTR may be removed anytime after the falling edge of the first $\overline{\text{INTA}}$ signal. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored, the enable bit will be zero unless specifically set by an instruction.

During the response sequence (see Figure 5) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 80C86 emits the $\overline{\text{LOCK}}$ signal (Max mode only) from t2 of the first bus cycle until t2 of the second. A local bus “hold” request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is supplied to the 80C86 by the 82C59A Interrupt Controller, which identifies the source (type) of the interrupt. This byte is multiplied by 4 and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

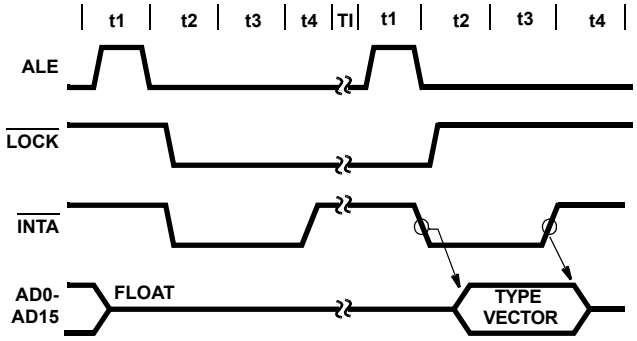


FIGURE 5. INTERRUPT ACKNOWLEDGE SEQUENCE

Halt

When a software “HALT” instruction is executed, the processor indicates that it is entering the “HALT” state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ and the 82C88 bus controller issues one ALE. The 80C86 will not leave the “HALT” state when a local bus “hold” is entered while in “HALT”. In this case, the processor reissues the HALT indicator at the end of the local bus hold. An NMI or interrupt request (when interrupts enabled) or RESET will force the 80C86 out of the “HALT” state.

Read/Modify/Write (Semaphore)

Operations Via $\overline{Lock}$

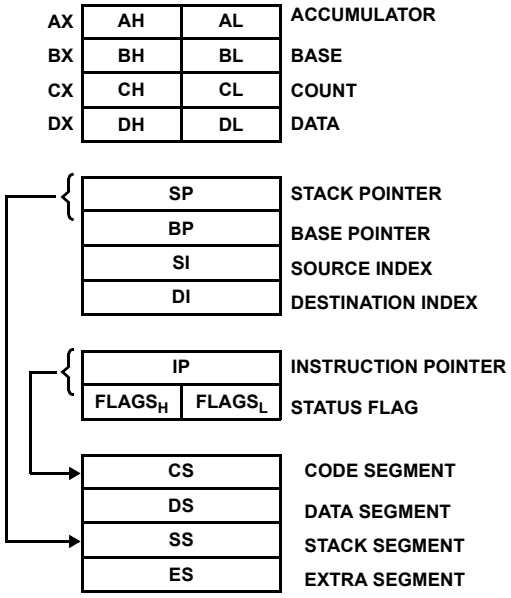
The LOCK status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This gives the processor the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish “test and set lock” operations. The LOCK signal is activated (forced LOW) in the clock cycle following decoding of the software “LOCK” prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the “LOCK” prefix instruction. While LOCK is active a request on a RQ/GT pin will be recorded and then honored at the end of the LOCK.

External Synchronization Via TEST

As an alternative to interrupts, the 80C86 provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{TEST}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 80C86 three-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the 80C86 will recognize interrupts and process them when it regains control of the bus. The WAIT instruction is then refetched, and re-executed.

TABLE 4. 80C86 REGISTER



Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 6A and 6B, respectively. In minimum mode, the MN/$\overline{MX}$ pin is strapped to VCC and the processor emits bus control signals (e.g. $\overline{RD}$, $\overline{WR}$, etc.) directly. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller uses to generate MULTIBUS compatible bus control signals. Figure 3 shows the signal timing relationships.

System Timing - Minimum System

The read cycle begins in t1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0-AD15) at this time, into the 82C82/82C83 latch. The $\overline{BHE}$ and A0 signals address the low, high or both bytes. From t1 to t4 the M/$\overline{IO}$ signal indicates a memory or I/O operation. At t2, the address is removed from the address/data bus and the bus is held at the last valid logic state by internal bus hold devices. The read control signal is also asserted at t2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again three-state its bus drivers. If a transceiver (82C86/82C87) is

required to buffer the 80C86 local bus, signals DT/R and $\overline{DEN}$ are provided by the 80C86.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/$\overline{IO}$ signal is again asserted to indicate a memory or I/O write operation. In t2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of t4. During t2, t3 and tW, the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of t2 as opposed to the read which is delayed somewhat into t2 to provide time for output drivers to become inactive.

The $\overline{BHE}$ and A0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to Table 5.

TABLE 5.

$\overline{BHE}$	A0	CHARACTERISTICS
0	0	Whole word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D7-D0 bus lines and odd address bytes on D15-D8.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is held at the last valid logic state by internal bus hold devices (see Figure 4). In the second of two successive $\overline{INTA}$ cycles a byte of information is read from the data bus (D7-D0) as supplied by the interrupt system logic (i.e., 82C59A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by 4 and used as a pointer into an interrupt vector lookup table, as described earlier.

Bus Timing - Medium Size Systems

For medium complexity systems the MN/$\overline{MX}$ pin is connected to GND and the 82C88 Bus Controller is added to the system as well as an 82C82/82C83 latch for latching the system address, and an 82C86/82C87 transceiver to allow for bus loading greater than the 80C86 is capable of handling. Signals ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The 80C86 status outputs ($\overline{S2}$, $\overline{S1}$ and $\overline{S0}$) provide type-of-cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The 82C86/82C87 transceiver receives the usual T and $\overline{OE}$ inputs from the 82C88 DT/$\overline{R}$ and DEN signals.

The pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can be derived from an 82C59A located on either the local bus or the system bus. If the master 82C59A Priority Interrupt Controller is positioned on the local bus, the 82C86/82C87 transceiver must be disabled when reading from the master 82C59A during the interrupt acknowledge sequence and software “poll”.

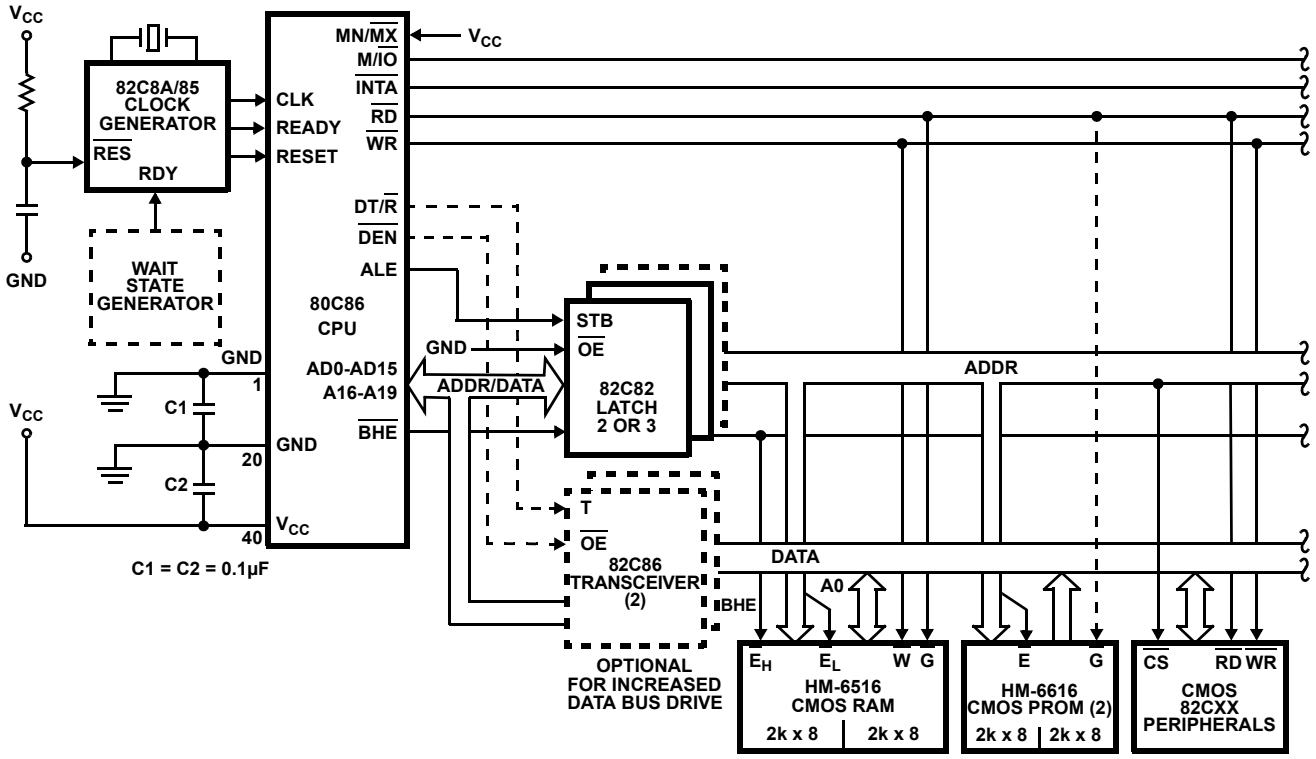


FIGURE 6A. MINIMUM MODE 80C86 TYPICAL CONFIGURATION

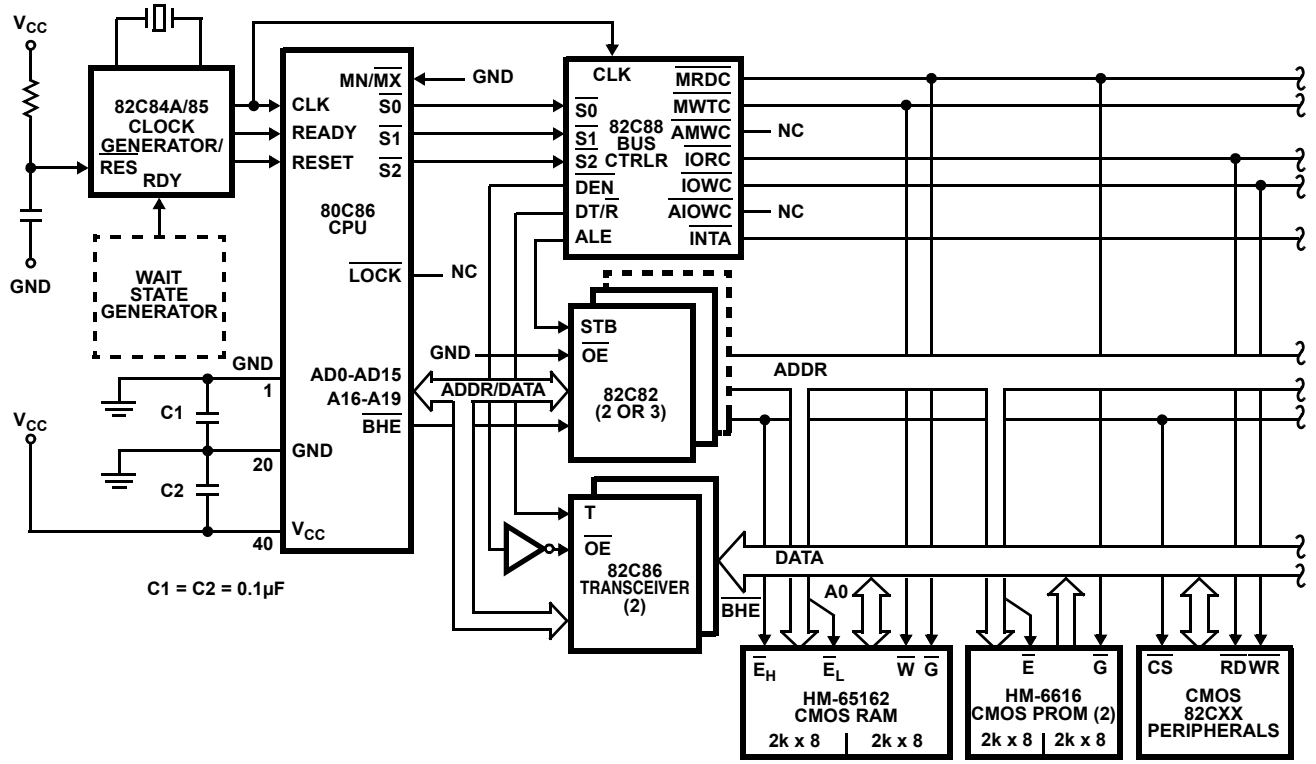


FIGURE 6B. MAXIMUM MODE 80C86 TYPICAL CONFIGURATION

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
Gate Count. . . . . 9750 Gates
ESD Classification . . . . . Class 1

Operating Conditions

Operating Supply Voltage . . . . . +4.5V to +5.5V
M80C86-2 ONLY . . . . . +4.75V to +5.25V
Temperature Range
C80C86-2 . . . . . 0°C to +70°C
M80C86-2. . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
PDIP Package* (Note 1)	50	N/A
CERDIP Package (Notes 1, 2)	30	6

Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature
Ceramic Packages . . . . . +175°C
Plastic Packages . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

DC Electrical Specifications

V_{CC} = 5.0V, ±10%; T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V, ±10%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V, ±5%; T_A = -55°C to +125°C (M80C86-2). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNITS
V_{IH}	Logical One	C80C86 (Note 6)	2.0		V
	Input Voltage	M80C86 (Note 6)	2.2		V
V_{IL}	Logical Zero Input Voltage			0.8	V
V_{IHC}	CLK Logical One Input Voltage		V_{CC} - 0.8		V
V_{ILC}	CLK Logical Zero Input Voltage			0.8	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA	3.0		V
		I_{OH} = -100µA	V_{CC} - 0.4		V
V_{OL}	Output Low Voltage	I_{OL} = +2.5mA		0.4	V
I_I	Input Leakage Current	V_{IN} = GND or V_{CC} DIP Pins 17-19, 21-23, 33	-1.0	1.0	µA
I_{BHH}	Input Current-Bus Hold High	V_{IN} = - 3.0V (Note 3)	-40	-400	µA
I_{BHL}	Input Current-Bus Hold Low	V_{IN} = - 0.8V (Note 4)	40	400	µA
I_O	Output Leakage Current	V_{OUT} = GND (Note 6)	-	-10.0	µA
I_{CCSB}	Standby Power Supply Current	V_{CC} = - 5.5V (Note 5)	-	500	µA
I_{CCOP}	Operating Power Supply Current	FREQ = Max, V_{IN} = V_{CC} or GND, Outputs Open (Note 7)	-	10	mA/MHz

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	25	pF	FREQ = 1MHz. All measurements are referenced to device GND
C_{OUT}	Output Capacitance	25	pF	FREQ = 1MHz. All measurements are referenced to device GND
$C_{I/O}$	I/O Capacitance	25	pF	FREQ = 1MHz. All measurements are referenced to device GND

NOTES:

3. IBHH should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0V on the following pins 2-16, 26-32, 34-39.
4. IBHL should be measured after lowering V_{IN} to GND and then raising to 0.8V on the following pins: 2-16, 34-39.
5. ICCSB tested during clock high time after halt instruction executed. V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs unloaded.
6. IO should be measured by putting the pin in a high impedance state and then driving V_{OUT} to GND on the following pins: 26-29 and 32.
7. MN/$\overline{MX}$ is a strap option and should be held to V_{CC} or GND.

AC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V ±100%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C86-2). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SYMBOL		PARAMETER	TEST CONDITIONS	80C86		80C86-2		UNITS
				MIN	MAX	MIN	MAX	
MINIMUM COMPLEXITY SYSTEM								
Timing Requirements								
(1)	TCLCL	Cycle Period		200		125		ns
(2)	TCLCH	CLK Low Time		118		68		ns
(3)	TCHCL	CLK High Time		69		44		ns
(4)	TCH1CH2	CLK Rise Time	From 1.0V to 3.5V		10		10	ns
(5)	TCL2C1	CLK Fall Time	From 3.5V to 1.0V		10		10	ns
(6)	TDVCL	Data In Setup Time		30		20		ns
(7)	TCLDX1	Data In Hold Time		10		10		ns
(8)	TR1VCL	RDY Setup Time into 82C84A (Notes 8, 9)		35		35		ns
(9)	TCLR1X	RDY Hold Time into 82C84A (Notes 8, 9)		0		0		ns
(10)	TRYHCH	READY Setup Time into 80C86		118		68		ns
(11)	TCHRYX	READY Hold Time into 80C86		30		20		ns
(12)	TRYLCL	READY Inactive to CLK (Note 10)		-8		-8		ns
(13)	THVCH	HOLD Setup Time		35		20		ns
(14)	TINVCH	INTR, NMI, $\overline{TEST}$ Setup Time (Note 9)		30		15		ns
(15)	TILIH	Input Rise Time (Except CLK)	From 0.8V to 2.0V		15		15	ns
(16)	TIHIL	Input Fall Time (Except CLK)	From 2.0V to 0.8V		15		15	ns
Timing Responses								
(17)	TCLAV	Address Valid Delay	C_L = 100pF	10	110	10	60	ns
(18)	TCLAX	Address Hold Time	C_L = 100pF	10		10		ns
(19)	TCLAZ	Address Float Delay	C_L = 100pF	TCLAX	80	TCLAX	50	ns
(20)	TCHSZ	Status Float Delay	C_L = 100pF		80		50	ns
(21)	TCHSV	Status Active Delay	C_L = 100pF	10	110	10	60	ns
(22)	TLHLL	ALE Width	C_L = 100pF	TCLCH - 20		TCLCH - 10		ns

AC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V ±100%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C86-2). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

SYMBOL		PARAMETER	TEST CONDITIONS	80C86		80C86-2		UNITS
				MIN	MAX	MIN	MAX	
(23)	TCLLH	ALE Active Delay	C_L = 100pF		80		50	ns
(24)	TCHLL	ALE Inactive Delay	C_L = 100pF		85		55	ns
(25)	TLLAX	Address Hold Time to ALE Inactive	C_L = 100pF	TCHCL - 10		TCHCL - 10		ns
(26)	TCLDV	Data Valid Delay	C_L = 100pF	10	110	10	60	ns
(27)	TCLDX2	Data Hold Time	C_L = 100pF	10		10		ns
(28)	TWHDX	Data Hold Time After $\overline{WR}$	C_L = 100pF	TCLCL - 30		TCLCL - 30		ns
(29)	TCVCTV	Control Active Delay 1	C_L = 100pF	10	110	10	70	ns
(30)	TCHCTV	Control Active Delay 2	C_L = 100pF	10	110	10	60	ns
(31)	TCVCTX	Control Inactive Delay	C_L = 100pF	10	110	10	70	ns
(32)	TAZRL	Address Float to READ Active	C_L = 100pF	0		0		ns
(33)	TCLRL	$\overline{RD}$ Active Delay	C_L = 100pF	10	165	10	100	ns
(34)	TCLRH	$\overline{RD}$ Inactive Delay	C_L = 100pF	10	150	10	80	ns
(35)	TRHAV	$\overline{RD}$ Inactive to Next Address Active	C_L = 100pF	TCLCL - 45		TCLCL - 40		ns
(36)	TCLHAV	HLDA Valid Delay	C_L = 100pF	10	160	10	100	ns
(37)	TRLRH	$\overline{RD}$ Width	C_L = 100pF	2TCLCL - 75		2TCLCL - 50		ns
(38)	TWLWH	$\overline{WR}$ Width	C_L = 100pF	2TCLCL - 60		2TCLCL - 40		ns
(39)	TAVAL	Address Valid to ALE Low	C_L = 100pF	TCLCH - 60		TCLCH - 40		ns
(40)	TOLOH	Output Rise Time	From 0.8V to 2.0V		20		15	ns
(41)	TOHOL	Output Fall Time	From 2.0V to 0.8V		20		15	ns

NOTES:

8. Signal at 82C84A shown for reference only.
9. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
10. Applies only to t2 state (8ns into t3).

Waveforms

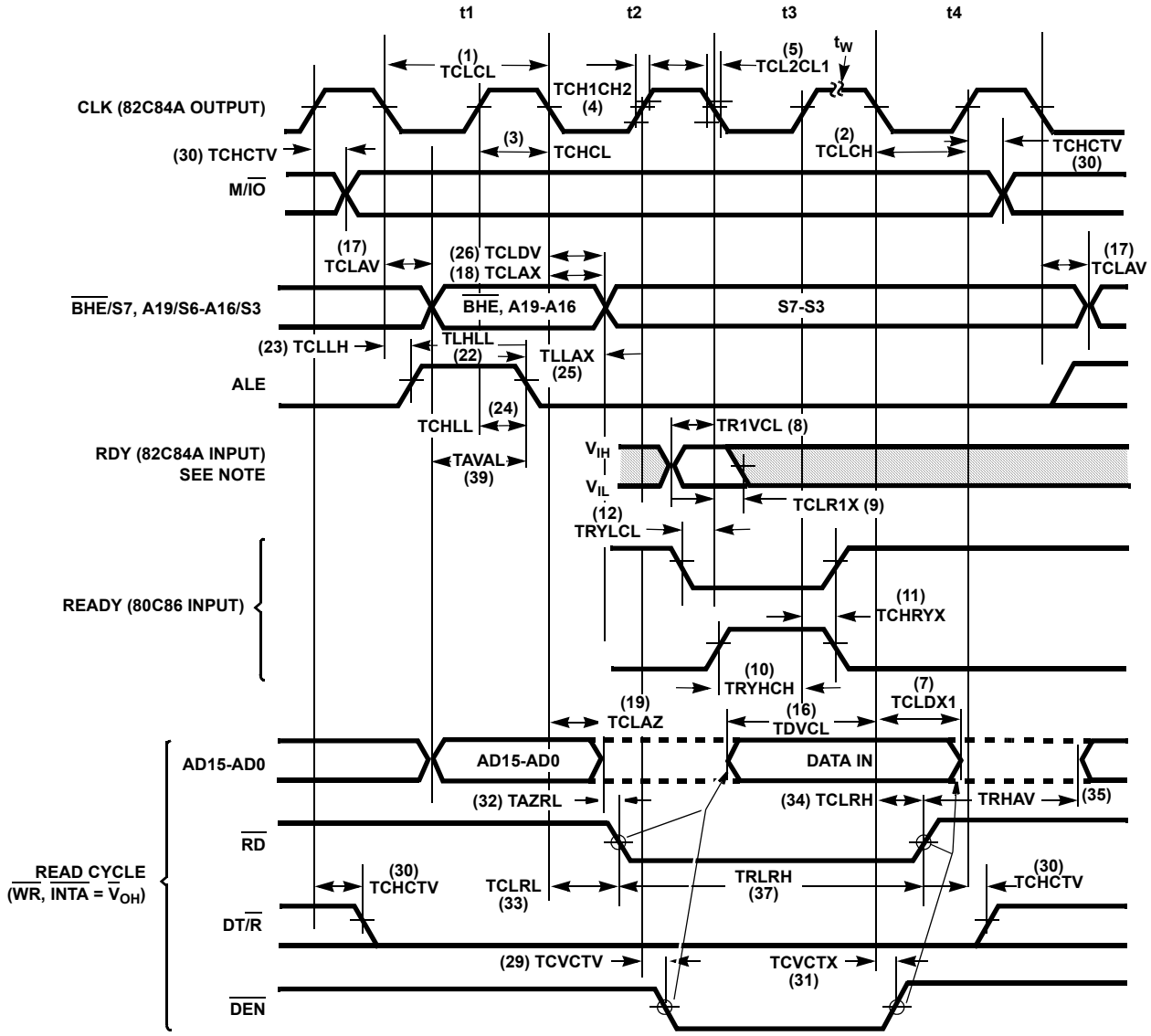


FIGURE 7A. BUS TIMING - MINIMUM MODE SYSTEM

NOTE: Signals at 82C84A are shown for reference only. RDY is sampled near the end of t2, t3, tW to determine if TW machine states are to be inserted.

Waveforms (Continued)

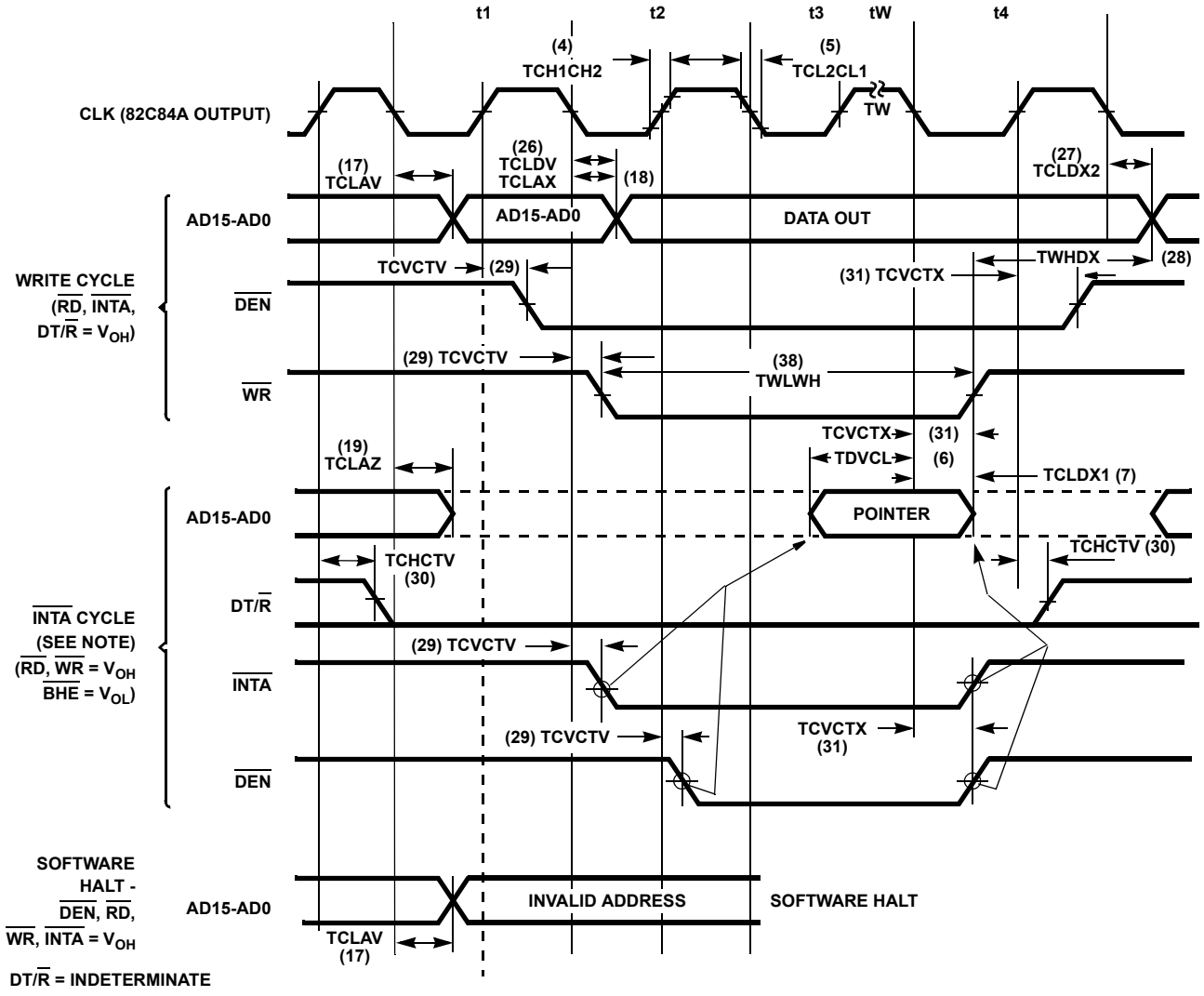


FIGURE 7B. BUS TIMING - MINIMUM MODE SYSTEM

NOTE: Two $\overline{\text{INTA}}$ cycles run back-to-back. The 80C86 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control signals are shown for the second $\overline{\text{INTA}}$ cycle.

AC Electrical Specifications

V_{CC} = 5.0V ±10%T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V ±10%;T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ±5%;T_A = -55°C to +125°C (M80C86-2). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

TIMING REQUIREMENTS				80C86		80C86-2		
SYMBOL		PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNITS
MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)								
Timing Requirements								
(1)	TCLCL	CLK Cycle Period		200		125		ns
(2)	TCLCH	CLK Low Time		118		68		ns
(3)	TCHCL	CLK High Time		69		44		ns
(4)	TCH1CH2	CLK Rise Time	From 1.0V to 3.5V		10		10	ns
(5)	TCL2CL1	CLK Fall Time	From 3.5V to 1.0V		10		10	ns
(6)	TDVCL	Data in Setup Time		30		20		ns
(7)	TCLDX1	Data In Hold Time		10		10		ns
(8)	TR1VCL	RDY Setup Time into 82C84A (Notes 11, 12)		35		35		ns
(9)	TCLR1X	RDY Hold Time into 82C84A (Notes 11, 12)		0		0		ns
(10)	TRYHCH	READY Setup Time into 80C86		118		68		ns
(11)	TCHRYX	READY Hold Time into 80C86		30		20		ns
(12)	TRYLCL	READY Inactive to CLK (Note 13)		-8		-8		ns
(13)	TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) (Note 12)		30		15		ns
(14)	TGVCH	$\overline{RQ}$/$\overline{GT}$ Setup Time		30		15		ns
(15)	TCHGX	$\overline{RQ}$ Hold Time into 80C86 (Note 14)		40	TCHCL + 10	30	TCHCL + 10	ns
(16)	TILIH	Input Rise Time (Except CLK)	From 0.8V to 2.0V		15		15	ns
(17)	TIHIL	Input Fall Time (Except CLK)	From 2.0V to 0.8V		15		15	ns
Timing Responses								
(18)	TCLML	Command Active Delay (Note 11)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	5	35	5	35	ns
(19)	TCLMH	Command Inactive (Note 11)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	5	35	5	35	ns
(20)	TRYHSH	READY Active to Status Passive (Notes 13, 15)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)		110		65	ns
(21)	TCHSV	Status Active Delay	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	10	110	10	60	ns

AC Electrical Specifications

V_{CC} = 5.0V ±10%T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V ±10%;T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ±5%;T_A = -55°C to +125°C (M80C86-2). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

TIMING REQUIREMENTS				80C86		80C86-2		
SYMBOL		PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNITS
(22)	TCLSH	Status Inactive Delay (Note 15)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	10	130	10	70	ns
(23)	TCLAV	Address Valid Delay	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	10	110	10	60	ns
(24)	TCLAX	Address Hold Time	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	10		10		ns
(25)	TCLAZ	Address Float Delay	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	TCLAX	80	TCLAX	50	ns
(26)	TCHSZ	Status Float Delay	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)		80		50	ns
(27)	TSVLH	Status Valid to ALE High (Note 11)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)		20		20	ns
(28)	TSVMCH	Status Valid to MCE High (Note 11)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)		30		30	ns
(29)	TCLLH	CLK low to ALE Valid (Note 11)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)		20		20	ns
(30)	TCLMCH	CLK low to MCE High (Note 11)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)		25		25	ns
(31)	TCHLL	ALE Inactive Delay (Note 11)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	4	18	4	18	ns
(32)	TCLMCL	MCE Inactive Delay (Note 11)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)		15		15	ns
(33)	TCLDV	Data Valid Delay	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	10	110	10	60	ns

AC Electrical Specifications

V_{CC} = 5.0V ±10%T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V ±10%;T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ±5%;T_A = -55°C to +125°C (M80C86-2). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

TIMING REQUIREMENTS				80C86		80C86-2		
SYMBOL		PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNITS
(34)	TCLDX2	Data Hold Time	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	10		10		ns
(35)	TCVNV	Control Active Delay (Note 11)	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)	5	45	5	45	ns
(36)	TCVNX	Control Inactive Delay (Note 11)	C_L = 100pF	10	45	10	45	ns
(37)	TAZRL	Address Float to Read Active	C_L = 100pF	0		0		ns
(38)	TCLRL	$\overline{RD}$ Active Delay	C_L = 100pF	10	165	10	100	ns
(39)	TCLRH	$\overline{RD}$ Inactive Delay	C_L = 100pF	10	150	10	80	ns
(40)	TRHAV	$\overline{RD}$ Inactive to Next Address Active	C_L = 100pF	TCLCL - 45		TCLCL - 40		ns
(41)	TCHDTL	Direction Control Active Delay (Note 11)	C_L = 100pF		50		50	ns
(42)	TCHDTH	Direction Control Inactive Delay (Note 11)	C_L = 100pF		30		30	ns
(43)	TCLGL	$\overline{GT}$ Active Delay	C_L = 100pF	10	85	0	50	ns
(44)	TCLGH	$\overline{GT}$ Inactive Delay	C_L = 100pF	10	85	0	50	ns
(45)	TRLRH	$\overline{RD}$ Width	C_L = 100pF	2TCLCL - 75		2TCLCL - 50		ns
(46)	TOLOH	Output Rise Time	From 0.8V to 2.0V		20		15	ns
(47)	TOHOL	Output Fall Time	From 2.0V to 0.8V		20		15	ns

NOTES:

11. Signal at 82C84A or 82C88 shown for reference only.
12. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
13. Applies only to t2 state (8ns into t3).
14. The 80C86 actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
15. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

Waveforms

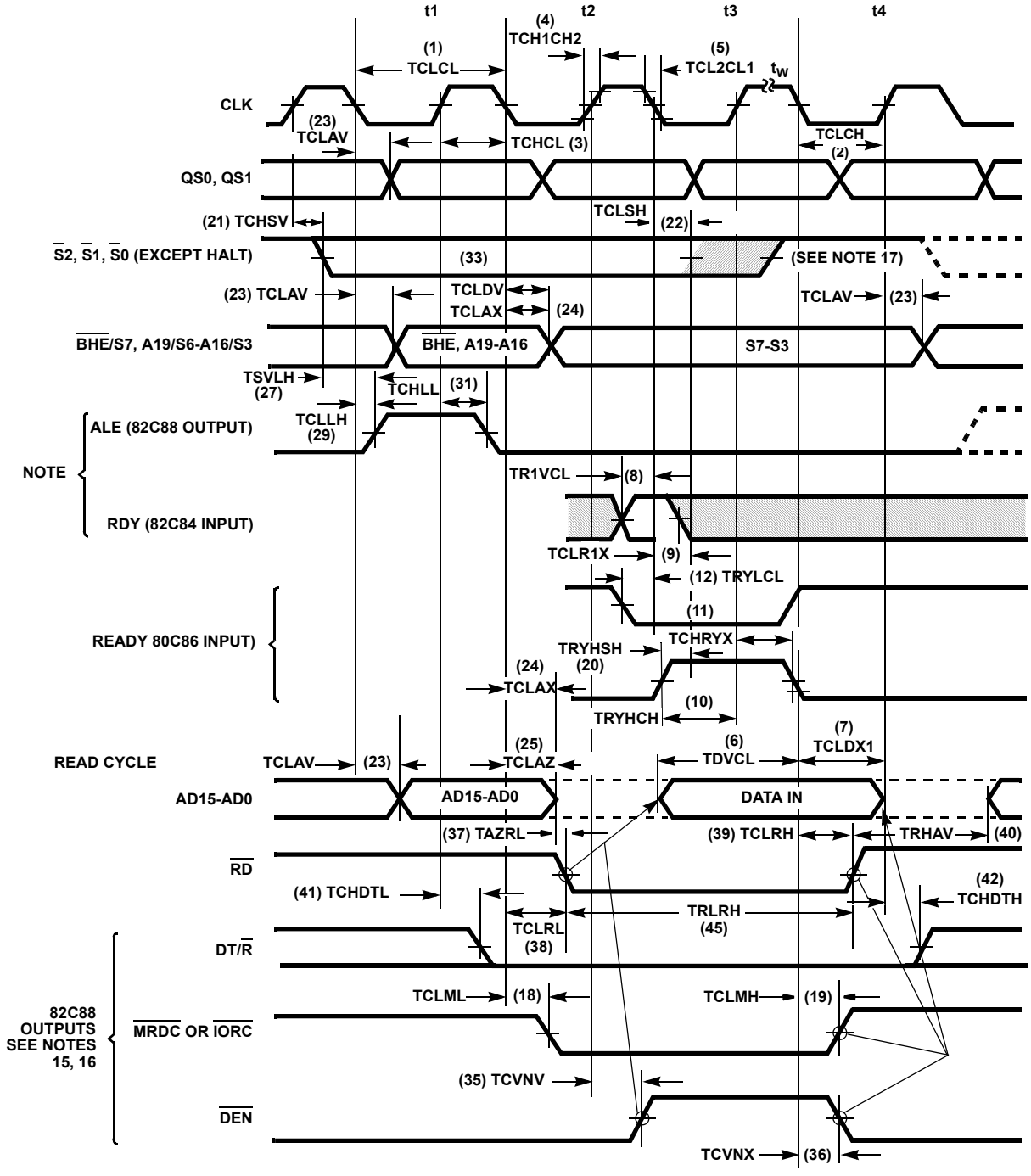


FIGURE 8A. BUS TIMING - MAXIMUM MODE (USING 82C88)

NOTES:

16. Signals at 82C84A or 82C88 are shown for reference only. RDY is sampled near the end of t2, t3, tW to determine if TW machine states are to be inserted.
17. The issuance of the 82C88 command and control signals ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$, and $\overline{\text{DEN}}$) lags the active high 82C88 CEN.
18. Status inactive in state just prior to t4.