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CPC7701

16-Channel High Voltage Analog Switch with Integrated Bleed Resistors

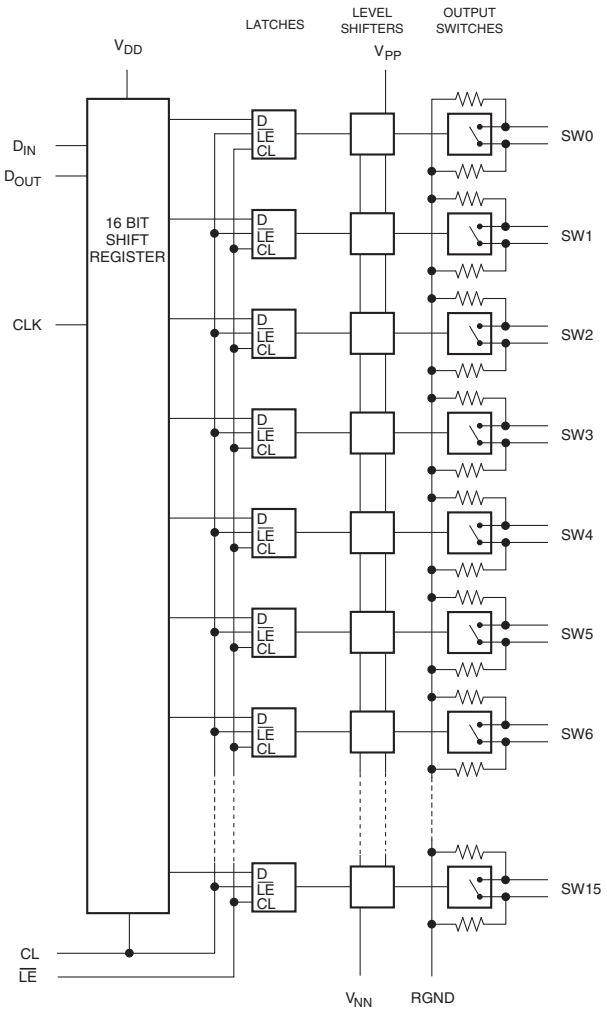
Features

- Processed with BCDMOS on SOI (Silicon on Insulator)
- Flexible High Voltage Supplies up to V_{PP}-V_{NN}=200V
- Internal Output Bleed Resistors
- DC to 10MHz Analog Signal Frequency
- 60dB Minimum Output-Off Isolation at 5MHz
- Low Quiescent Power Dissipation (< 1μA Typical)
- Low Output On-Resistance
- Surface Mount Package

Applications

- Ultrasound Imaging
- Printers
- Industrial Controls and Measurement
- Piezoelectric Transducer Drivers

Figure 1. Block Diagram



Description

The CPC7701 is a low charge injection 16-channel high-voltage analog switch integrated circuit (IC) for use in applications requiring high voltage switching. Bleed resistors are incorporated into both terminals of each output switch. Control of the high voltage switching is via low voltage CMOS logic level inputs for direct connectivity to the system controller.

Switch manipulation is managed by an 16-bit serial to parallel shift register whose outputs are buffered and stored by a 16-bit transparent latch. Level shifters buffer the latch outputs and operate the high voltage switches.

Because the CPC7701 is capable of switching high load voltages and has a flexible load voltage range, e.g. V_{PP}/V_{NN}: +40V/160V or +100V/100V, it is well suited for many medical and industrial applications such as medical ultrasound imaging, printers, and industrial measurement equipment. The bleed resistors enable the discharge of capacitive loads, such as piezoelectric transducers, connected to the output switches of the CPC7701.

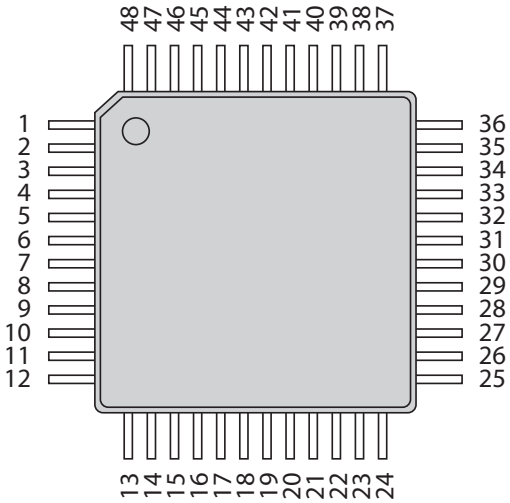
Construction of the high voltage switches using IXYS Integrated Circuits Division's reliable SOI BCDMOS process technology allows the switches to be organized as solid state switches with direct gate drive.

Ordering Information

Part Number	Description
CPC7701K	48-Pin LQFP in Trays (250/Tray)
CPC7701KTR	48-Pin LQFP Tape & Reel (2000/Reel)

1. Specifications

1.1 Package Pinout



1.2 Pin Description

Pin	Name	Description
3	SW4	SW4 Output
4	SW4	SW4 Output
5	SW3	SW3 Output
6	SW3	SW3 Output
7	SW2	SW2 Output
8	SW2	SW2 Output
9	SW1	SW1 Output
10	SW1	SW1 Output
11	SW0	SW0 Output
12	SW0	SW0 Output
13	V_{NN}	Switch Negative High Voltage Supply
15	V_{PP}	Switch Positive High Voltage Supply
17	GND	Ground: All Voltages are Referenced to Ground
18	V_{DD}	Logic Positive Supply Voltage
19	D_{IN}	Serial Data Input
20	CLK	Clock Input, Positive Edge Trigger
21	$\overline{LE}$	Latch Enable, Active Low
22	CL	Latch Clear, Active High, Asynchronously Clears Latches and Opens Switches
23	D_{OUT}	Serial Data Output
24	R_{GND}	Ground for Bleed Resistors, Connect to GND
25	SW15	SW15 Output
26	SW15	SW15 Output
27	SW14	SW14 Output
28	SW14	SW14 Output
29	SW13	SW13 Output
30	SW13	SW13 Output
31	SW12	SW12 Output
32	SW12	SW12 Output
33	SW11	SW11 Output
34	SW11	SW11 Output
37	SW10	SW10 Output
38	SW10	SW10 Output
39	SW9	SW9 Output
40	SW9	SW9 Output
41	SW8	SW8 Output
42	SW8	SW8 Output
43	SW7	SW7 Output
44	SW7	SW7 Output
45	SW6	SW6 Output
46	SW6	SW6 Output
47	SW5	SW5 Output
48	SW5	SW5 Output
1, 2, 14, 16, 35, 36	N/C	No Connection

1.3 Absolute Maximum Ratings

Electrical Absolute Maximum ratings are at 25°C.

All voltages are referenced from ground (GND).

Parameter	Min	Max	Units
V_{DD} Logic Power Supply Voltage	-0.5	7	V
V_{PP} - V_{NN} Supply Voltage	-	220	V
V_{PP} Positive High Voltage Supply	-0.5	V_{NN}+200	V
V_{NN} Negative High Voltage Supply	-0.5	V_{PP}-200	V
R_{GND}-GND Differential	-0.3	+0.3	V
Logic input voltages	-0.5	V_{DD}+0.3	V
Analog signal range	V_{NN}	V_{PP}	V
Peak analog signal current per channel	-	1	A
Power dissipation	-	2.3	W
Storage temperature	- 65	+150	°C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Operating Conditions

Parameter	Symbol	Value
Logic power supply voltage [1]	V_{DD}	3V to 5.5V
Positive high voltage supply [1]	V_{PP}	40V to V_{NN} + 200V
Negative high voltage supply [1]	V_{NN}	-40V to -160V
Analog signal voltage, peak-to-peak [2]	V_{SW}	V_{NN}+10V to V_{PP}-10V
Operating temperature	T_A	0°C to 70°C

[1] Power up/down sequence is arbitrary except that GND must be powered-up first and powered-down last.

[2] V_{SW} must be $V_{NN} \leq V_{SW} \leq V_{PP}$ or floating during power up/down transition.

1.5 Electrical Characteristics

1.5.1 Switch Characteristics

(Over recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions		0°C		+25°C			+70°C		Units
				min	max	min	typ	max	min	max	
Switch on-resistance, Small signal	R_{ONS}	V_{PP}=40V, V_{NN}=-160V	I_{SW}=5mA	-	30	-	27	35	-	48	Ω
			I_{SW}=200mA	-	26	-	22	29	-	40	
		V_{PP}=100V, V_{NN}=-100V	I_{SW}=5mA	-	30	-	27	35	-	48	
			I_{SW}=200mA	-	26	-	22	29	-	40	
		V_{PP}=160V, V_{NN}=-40V	I_{SW}=5mA	-	30	-	27	35	-	48	
			I_{SW}=200mA	-	26	-	22	29	-	40	
Switch on-resistance matching, Small signal	ΔR_{ONS}	V_{PP}=100V, V_{NN}=-100V, I_{SW}=5mA		-	20	-	4	20	-	20	%
Switch on-resistance, Large signal	R_{ONL}	V_{SW}=V_{PP}-10V, I_{SW}=1A		-	-	-	15	-	-	-	Ω
Output bleed resistors	R_{INT}	Output switch to R_{GND}, I_{RINT}=0.5mA		-	-	20	28	50	-	-	kΩ
Switch off leakage, per switch*	I_{SOL}	V_{SW}=V_{PP}-10V and V_{NN}+10V		-	5	-	0.4	10	-	15	µA
DC offset, switch off	V_{OS}	No Load		-	300	-	-	300	-	300	mV
DC offset, switch on	V_{OS}	No Load		-	500	-	-	500	-	500	
Switch output peak current	I_{SW}	V_{SW} duty cycle = 0.1%		-	-	-	-	1	-	-	A
Output switch frequency	f_{SW}	Duty cycle = 50%		-	-	-	-	50	-	-	kHz
Maximum V_{SW} slew rate	dV/dt	V_{PP}=160V, V_{NN}=-40V		-	20	-	-	20	-	20	V/ns
		V_{PP}=100V, V_{NN}=-100V									
		V_{PP}=40V, V_{NN}=-160V									
Off isolation	K_O	f=5MHz, Z_L=1kΩ || 15pF load		30	-	30	-	-	30	-	dB
		f=5MHz, R_L=50Ω load		58	-	58	-	-	58	-	
Switch crosstalk	K_{CR}	f=5MHz, R_L=50Ω load		-60	-	-60	-	-	-60	-	dB
Output switch isolation diode current	I_{ID}	300ns pulse width, 2.0% duty cycle		-	300	-	-	300	-	300	mA
Off capacitance, SW to GND	$C_{SG(OFF)}$	V_{SW}=0V, f=1MHz		5	17	5	-	17	5	17	pF
On capacitance, SW to GND	$C_{SG(ON)}$	V_{SW}=0V, f=1MHz		25	50	20	-	50	25	50	
Output voltage spike	$+V_{SPK}$	V_{PP}=40V, V_{NN}=-160V	R_L=50Ω	-	-	-	-	150	-	-	mV
	$-V_{SPK}$										
	$+V_{SPK}$	V_{PP}=100V, V_{NN}=-100V		-	-	-	-	150	-	-	
	$-V_{SPK}$										
	$+V_{SPK}$	V_{PP}=160V, V_{NN}=-40V		-	-	-	-	150	-	-	
	$-V_{SPK}$										
Charge injection	Q	V_{PP}=100V, V_{NN}=-100V, V_{SW}=0V				-	820	-			pC

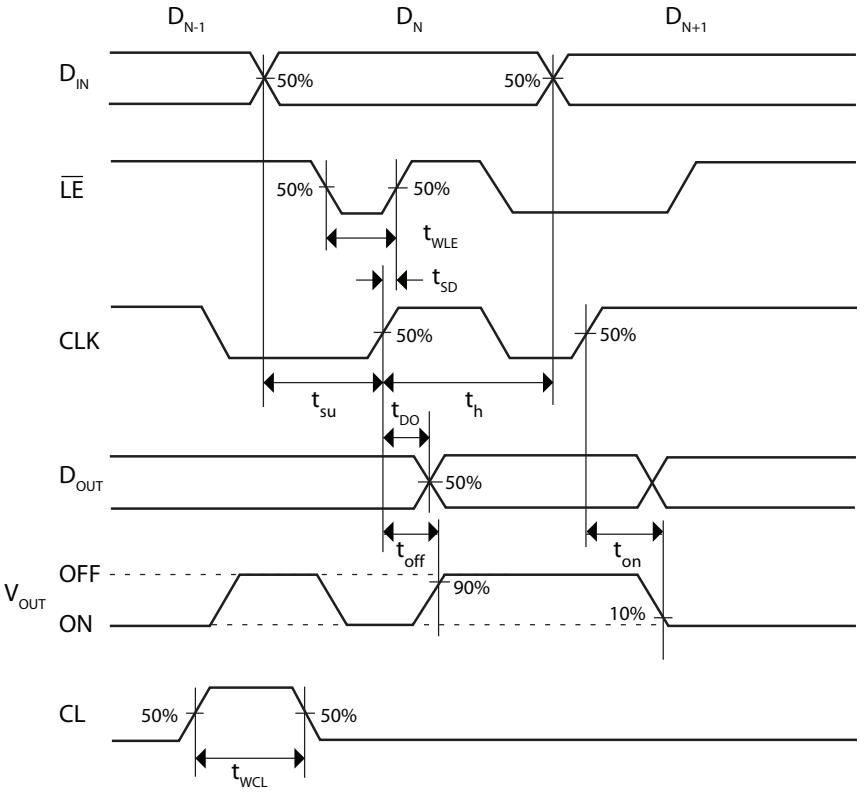
* Does not include the leakage current contribution due to the bleed resistors.

1.5.2 Logic Timing Characteristics

(Over recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions	0°C		+25°C			70°C		Units
			min	max	min	typ	max	min	max	
Setup time before $\overline{LE}$ rises	t_{SD}	-	150	-	150	-	-	150	-	ns
Time width of $\overline{LE}$	t_{WLE}	V_{DD}=3V	56	-	56	-	-	56	-	
		V_{DD}=5V	12	-	12	-	-	12	-	
Clock delay time to Data Out	t_{DO}	V_{DD}=3V	10	100	10	-	100	10	100	
		V_{DD}=5V	5	45	5	-	45	5	45	
Time width of CL	t_{WCL}	-	55	-	55	-	-	55	-	
Setup time, data to clock	t_{su}	V_{DD}=3V	21	-	-	21	-	21	-	
		V_{DD}=5V	7	-	-	7	-	7	-	
Hold time, data from clock	t_h	-	2	-	2	-	-	2	-	
Clock frequency	f_{CLK}	50% duty cycle, f_{DATA}= ½ f_{CLK}, V_{DD}=3V	-	8	-	-	8	-	8	MHz
		50% duty cycle, f_{DATA}= ½ f_{CLK}, V_{DD}=5V	-	20	-	-	20	-	20	
Clock rise and fall times	t_r , t_f	-	-	50	-	-	50	-	50	ns
Turn-on time	t_{on}	V_{SW}=V_{PP}-10V, RL=10kΩ	-	5	-	-	5	-	5	µs
Turn-off time	t_{off}									

1.5.3 Logic Timing Waveforms



1.5.4 Logic DC Characteristics

(Over recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions	0°C		+25°C			+70°C		Units
			min	max	min	typ	max	min	max	
D_{OUT} source capability	V_{OH}	I_{OUT}= -400µA	-	-	V_{DD}-0.7	V_{DD}-0.1	-	-	-	V
D_{OUT} sink capability	V_{OL}	I_{OUT}= +400µA	-	-	-	0.04	0.7	-	-	
Input (Logic) capacitance	C_{IN}	-	-	10	-	-	10	-	10	pF
Input, Logic high	V_{IH}	-	0.9 V_{DD}	-	0.9 V_{DD}	-	-	0.9 V_{DD}	-	V
Input, Logic low	V_{IL}	-	-	0.1 V_{DD}	-	-	0.1 V_{DD}	-	0.1 V_{DD}	

1.5.5 Supply DC Characteristics

(Over recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions		0°C		+25°C			+70°C		Units
				min	max	min	typ	max	min	max	
V_{PP} quiescent supply current	I_{PPQ}	All switches off		-	-	-	0.1	50	-	-	µA
		All switches on, I_{SW}=5mA									
V_{NN} quiescent supply current	I_{NNQ}	All switches off		-	-	-	-0.1	- 50	-	-	
		All switches on, I_{SW}=5mA									
V_{PP} operating supply current	I_{PP}	V_{PP}=40V, V_{NN}=-160V	50kHz output switching frequency with no load	-	6.5	-	-	7	-	8	mA
		V_{PP}=100V, V_{NN}=-100V		-	4	-	-	5.5	-	5.5	
		V_{PP}=160V, V_{NN}=-40V		-	4	-	-	5	-	5.5	
V_{NN} operating supply current	I_{NN}	V_{PP}=40V, V_{NN}=-160V	50kHz output switching frequency with no load	-	6.5	-	-	7	-	8	mA
		V_{PP}=100V, V_{NN}=-100V		-	4	-	-	5.5	-	5.5	
		V_{PP}=160V, V_{NN}=-40V		-	4	-	-	5	-	5.5	
V_{DD} average supply current	I_{DD}	f_{CLK}=5MHz, V_{DD}=5V		-	4	-	-	4	-	4	mA
V_{DD} quiescent supply current	I_{DDQ}	-		-	10	-	0.03	10	-	10	µA

1.5.6 Thermal Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Thermal Resistance (Junction to Ambient)	Free Air	$R_{\theta JA}$	-	-	53	°C/W

2. Functional Description

The CPC7701 takes a serial stream of input data along with a synchronous clock signal. As the clock transits from low to high, the data at the input of each shift register is shifted through from SR(n) to SR(n+1). A high data bit, a “1,” represents an ON switch; a low data bit, a “0,” represents an OFF switch. Data is input and shifted through the internal shift register until all sixteen shift register positions, SR0 through SR15, are in the desired state.

D_{IN}: The data-in line presents data bits to the CPC7701 to be shifted through the internal shift register. The last bit into the shift register is the SW0 control bit.

CLK: The clock signal's rising edge is associated only with shifting data into and through the shift register.

CL: The clear line overrides all other inputs. When CL is high, the shift register is asynchronously cleared to all 0s and all latches are set low, which causes all output switches to be turned OFF immediately. When CL is low, all output switches remain in whatever state they are in, ON or OFF, in response to CLK, latch inputs, and the $\overline{LE}$ signal.

$\overline{LE}$: latch enable controls the state of the latches and the state of the sixteen switches. If $\overline{LE}$ is high, then the latches do not change states, but retain their most recent status: either ON or OFF. With $\overline{LE}$ high, input data and CLK have no effect on the state of the output switches. If $\overline{LE}$ is low, then all latch outputs and their switch states follow the inputs from the shift register. $\overline{LE}$ is overridden by CL: no matter what state $\overline{LE}$ is in, CL clears the latches. See **“Truth Table” on page 9**. Note that holding $\overline{LE}$ active while clocking in new data will cause the outputs to toggle with the shifting data.

D_{OUT}: The data-out pin is the output of SR15. After sixteen clock pulses, the first bit of sixteen shifted input data bits is output at SR15, and appears on D_{OUT}.

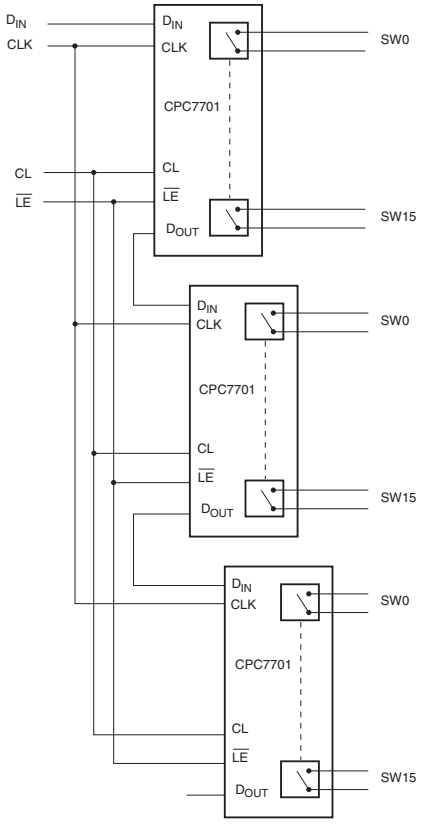
SW0 - SW15: The CPC7701 provides sixteen high-voltage SPST output switches with a nominal small signal on-resistance of 25Ω. The two connections of each switch are not polarity-sensitive. As can be seen in **“Block Diagram” on page 1**, integrated bleed resistors are provided to facilitate charge dissipation for capacitive load applications.

V_{PP} and V_{NN}: Voltage inputs to the level shifters for each switch channel that translate the voltage level of the latch output signals to an appropriate level for the voltages being switched.

The high-voltage output switches are turned on and off in response to the data sent into the latches from the shift register: data 0 turns a switch OFF, data 1 turns a switch ON.

Two or more CPC7701 devices can be cascaded to form an n-switch arrangement. The D_{OUT} pin of the first is connected to the D_{IN} pin of the next in the series. All devices are connected to the same clock (CLK) signal. $\overline{LE}$ of all devices would normally be connected, as would CL, but this is not necessary.

The first data bit applied to D_{IN} of the CPC7701, whether it's a single device or several cascaded devices, ripples through to the last switch output in line after the application of a full clocking sequence of 16 clock pulses. Setting the serial I/O device to output the most significant bit (MSB) first, results in the MSB appearing on SW15 of the last device in line after a full clocking sequence.



2.1 Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	$\overline{LE}$	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15
L																L	L	OFF															
H																L	L	ON															
	L															L	L		OFF														
	H															L	L		ON														
		L														L	L			OFF													
		H														L	L			ON													
			L													L	L				OFF												
			H													L	L				ON												
				L												L	L					OFF											
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													H			L	L														ON		
														L		L	L															OFF	
														H		L	L															ON	
															L	L	L																OFF
															H	L	L																ON
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE															
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

1. The sixteen switches operate independently.
2. Serial data is clocked in on the rising edge of the CLK signal.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the shift register data flows through the latch.
4. D_{OUT} is high when switch SW15 is on.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.
6. The clear input overrides all other inputs.

3. Manufacturing Information

3.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC7701K	MSL 3

3.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Reflow Profile

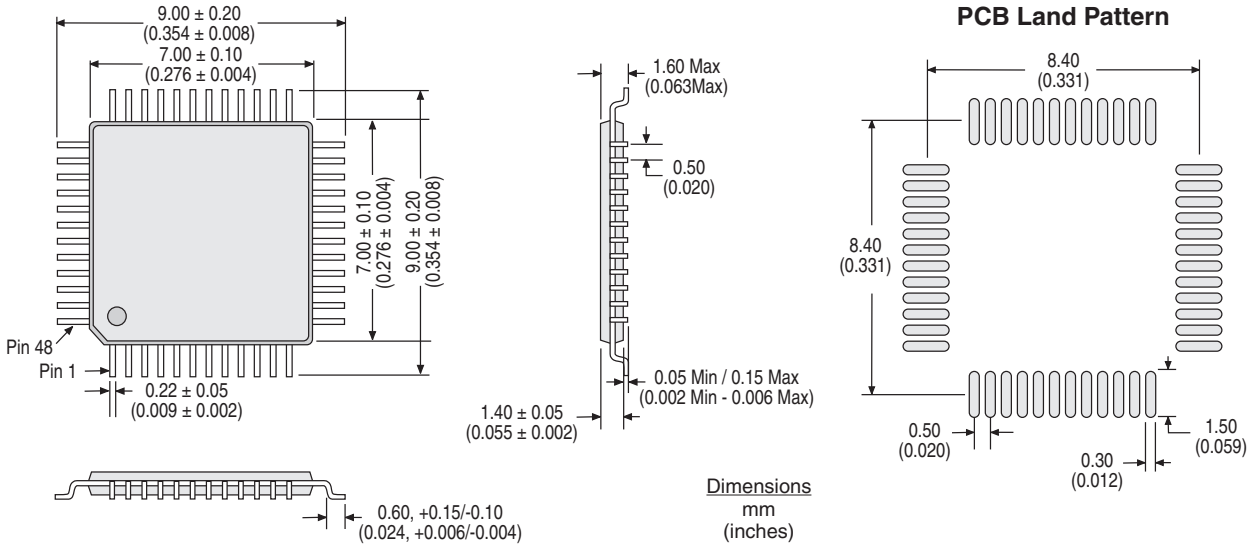
This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC7701K	260°C for 30 seconds

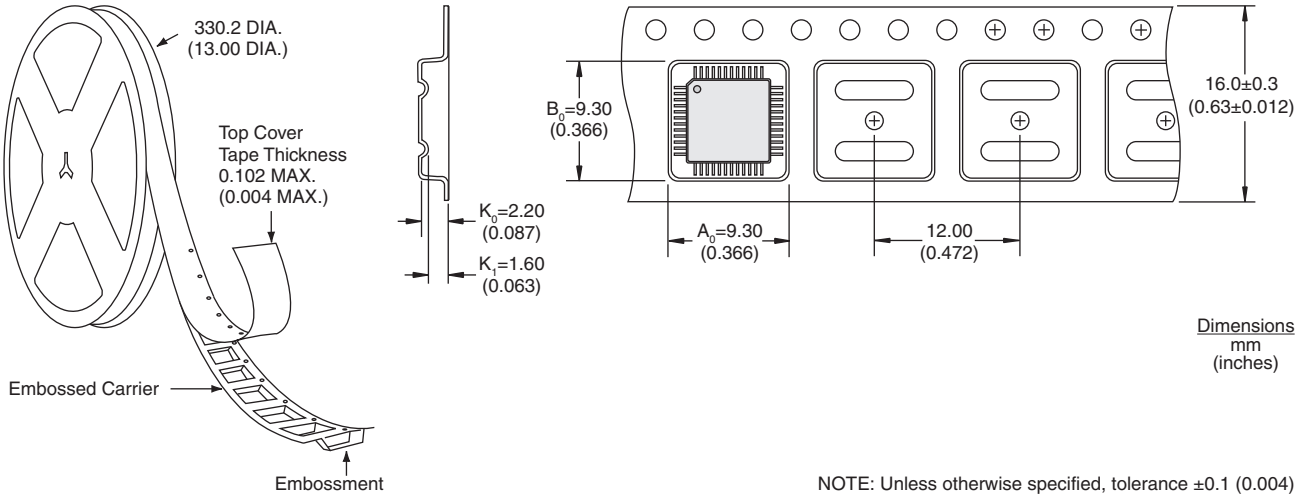
3.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

3.5 Mechanical Dimensions



3.6 Tape and Reel Specifications



NOTE: Unless otherwise specified, tolerance ±0.1 (0.004)

For additional information please visit www.ixysic.com

Specification: DS-CPC7701-R03

12/18/2012