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LatticeCORE

CPRI IP Core User Guide

IPUG56 Version 2.7, October 2016

Introduction

This document provides technical information about the Lattice Common Public Radio Interface (CPRI) IP core. This IP core together with SERDES and Physical Coding Sublayer (PCS) functionality integrated in the LatticeECP3™ and ECP5™ LFE5UM FPGAs implements the physical layer of the CPRI specification and interleaves IQ data with synchronization, control and management information. It can be used to connect Radio Equipment Control (REC) and Radio Equipment (RE) modules.

The CPRI IP core implements not only all of the capabilities required to support the physical layer of the CPRI specification (basic function), but also specific requirements related to link delay accuracy (low latency character).

One CPRI core configuration for 5G version (4.9152 Gbps) is also supported. It is similar to the "low latency" one for 3G version except the data rate. The remainder of this document focuses on the detailed specifications associated with implementing and using the basic function. The LatticeECP3 and ECP5 LFE5UM FPGAs optimize PCS/SERDES architecture for low latency control. Complete details on the implementation and use of the low latency configuration are included in IPUG74, CPRI IP Core Low Latency Variation Design Considerations User's Guide.

The CPRI soft-core comes with the following documentation and files:

- Data sheet
- Protected netlist/database
- Behavioral RTL simulation model
- Source files for instantiating and evaluating the core

The CPRI IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core that operate in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. It may also be used to evaluate the core in hardware in user-defined designs. Details for using the hardware evaluation capability are described in the Hardware Evaluation section of this document.

In the following text, transmit refers to data flow from the user application logic to the CPRI link. Receive refers to data flow from the CPRI link to the user application logic. Downlink refers to the direction of data flow from REC to RE, and uplink refers to the direction of data flow from RE to REC.

The Lattice CPRI core is compliant with the version 5.0 CPRI specification. Note however that the core does not directly support requirement R-31 (line-rate autonegotiation). For the 3G version, Lattice supports dynamic switching between full and half rate line settings (i.e., 614M/1.2G or 1.2/2.4G). However, switching dynamically between all line rates is not supported since some PCS/SERDES bit settings need to be re-programmed through the SCI to support reliable data transfer. It is anticipated that in most network applications, line rate negotiation will be established/managed at the system level and there is nothing in the IP core that precludes supporting such capability.

Quick Facts

Table 1-1 provides quick facts about the CPRI IP core 3G version.

Table 1-1. CPRI IP Core Quick Facts (3G Version)

		CPRI IP Core (3G Version)	
		Across All IP Configurations	
Core Requirements	FPGA Families Supported	LatticeECP3, ECP5	
	Minimal Device Supported	LFE3-35E-6FTN256C	LFE5UM-85F-7MG381C
Resource Utilization	Data Path Width	8-40 bits	
	LUTs	1400-1600	1600-2000
	sysMEM EBRs	2-6	
	Registers	1500-1700	1500-1700
Design Tool Support	Lattice Implementation	Lattice Diamond® 3.2	
	Synthesis	Synopsys® Synplify Pro® for I-2013.09L-SP1-1	
	Simulation	Aldec® Active-HDL™ 9.3 Lattice Edition	
		Mentor Graphics® ModelSim® SE 10.1C	

Table 1-2 provides quick facts about the CPRI IP core 5G version.

Table 1-2. CPRI IP Core Quick Facts (5G Version)

		CPRI IP Core (5G Version)
		Across All IP Configurations
Core Requirements	FPGA Families Supported	ECP5-5G
	Minimal Device Supported	LFE5UM5G-45F-8BG381C
Resource Utilization	Data Path Width	64 bits
	LUTs	1100~1300
	sysMEM EBRs	1~2
	Registers	1000
Design Tool Support	Lattice Implementation	Lattice Diamond® 3.8
	Synthesis	Lattice Synthesis Engine
	Simulation	Aldec® Active-HDL™ 10.2 Lattice Edition
		Mentor Graphics® ModelSim® 6.6e SE

Features

The following features apply to the basic CPRI core configuration for 3G version:

- Supports the physical link layer (Layer 1) of the CPRI specification
- Supports four standard bit rates of the CPRI specification
  - 614.4 Mbps
  - 1228.8 Mbps
  - 2457.6 Mbps
  - 3072 Mbps
- Supports 8b/10b encoding/decoding performed in the PCS/SERDES
- Supports code-violation detection performed in the PCS/SERDES

- Performs CPRI Hyperframe Framing
  - Performs interleaving of IQ data, sync, C&M data, and vendor specific information
  - Provides an 8-, 16-, 32- or 40-bit parallel interface for IQ data
- Performs subchannel mapping:
  - Supports a slow C&M channel based on a serial HDLC interface at standard bit rates (240 Kbps, 480 Kbps, 960 Kbps, and 1920 Kbps). The HDLC framer, if needed, must be implemented in the user logic.
  - Supports a fast C&M channel based on a serial Ethernet interface (84.48 Mbps max.) to the user logic, a non-standard rate MII Ethernet interface to a MAC, or a 100 Mbps MII interface to a PHY device. Accepts a user-selected pointer to the CPRI subchannel where the Ethernet link starts. The Ethernet MAC function is provided as a separate IP core.
- Performs synchronization and timing as defined in section 4.2.8 of CPRI Specification v5.0
- Supports the L1 Inband Protocol
- Provides a parallel interface for merging vendor specific data into the CPRI frame
- Provides a start-up sequence state machine in hardware for both REC and RE nodes which performs:
  - Synchronization and Rate Negotiation
  - C&M Plane setup
- Performs Link Maintenance as defined in section 4.2.10 of CPRI Specification v5.0:
  - LOS detection
  - LOF detection
  - RAI indication
- Optional top-level template that implements user registers for control and status management
- Optional 8-bit register interface through SCI bus

The low latency CPRI core configuration for 3G version supports all of the features specified for the basic core configuration with the following key exceptions/modifications:

- Supported for LatticeECP3 and ECP5 FPGA families only
- Supports 1228.8 Mbps, 2457.6 Mbps, and 3072 Mbps line bit rates only.
- FPGA bridge FIFOs in the SERDES/PCS (DCU in ECP5) block are bypassed in both the receive and transmit directions
- Logic blocks supporting receive direction 10b word alignment, 10b/8b decoding and core-violation detection in the SERDES/PCS (DCU in ECP5) block are bypassed and the corresponding functions are implemented in FPGA gates.

The low latency CPRI core configuration for 5G version is similar to the low latency core configuration for 3G version with the following key exceptions/modifications:

- Supported for ECP5 FPGA family only.
- Supports 4915.2 Mbps only.
- Provides 64-bit parallel interface for IQ data only.
- Supports a slow C&M channel based on a serial HDLC interface at standard bit rates (240 Kbps, 480 Kbps, 960 Kbps, 1920 Kbps, 2400Kbps, and 3840Kbps).
- No 8-bit register interface through the JTAG port

The low latency CPRI core implementation is different between LatticeECP3 and ECP5 for 3G version:

- FPGA bridge FIFOs in the SERDES/PCS block are bypassed in both the receive and transmit directions for LatticeECP3 FPGA, but enabled with synchronous WR/RD clocks for ECP5 LFE5UM FPGA
- The latency variability from 10-bit word alignment is the key for low latency control. For LatticeECP3, CPRI implements a PLL to eliminate the latency variation associated with the SERDES de-serializer 10-bit word alignment function by reading word align offset status registers. (The value can be read at channel register 0x22 with the base address.) For the LFE5UM device, the SERDES includes a new function that allows the de-serializer to slip the location of the bits in the parallel output by one bit at a time. This is done one bit at a time under control of a signal from the PCS and can be done multiple times as needed in order to align the data word as needed. This can be used by the word aligner in the PCS to ensure that the parallel word is aligned on a comma character boundary and is important to do in applications for CPRI that require that the latency variation through the SERDES block be as small as possible.

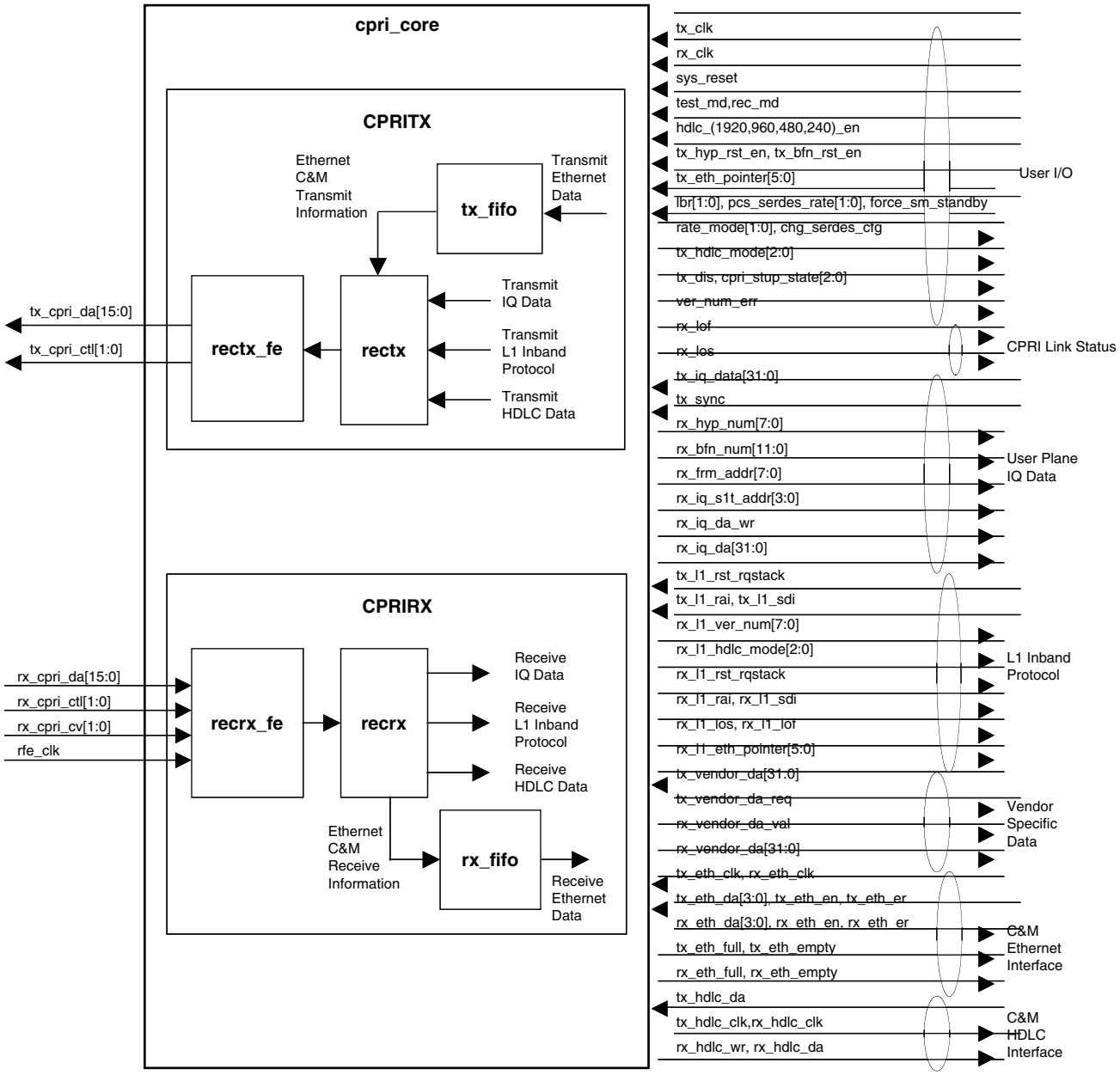
This chapter provides a functional description of the CPRI IP core.

Block Diagram

The complete CPRI IP core includes two key components, the CPRI IP logic core and separate logic blocks that support the interface between the logic core and the integrated PCS/SERDES block.

A block diagram of the CPRI IP logic core for 3G version is shown in Figure 2-1. For 5G version, higher HDLC rate(hdlc_2400_en) is also supported. And 64-bit parallel interfaces (tx/rx_iq_da[63:0], tx/rx_vendor_da[63:0]) are implemented instead.

Figure 2-1. CPRI IP Logic Core Block Diagram



General Description

The complete CPRI IP core includes two key components, the CPRI IP logic core and separate logic blocks that support the interface between the logic core and the SERDES/PCS (DCU for LFE5UM) functions integrated in the FPGA. Figure 2-1 shows a block diagram of the CPRI IP logic core. For 3G version, control and status parameters specifying core functionality are managed via bit-mapped I/O that may be hard-wired or interfaced to programmable registers, providing users with optimal flexibility in defining static and/or dynamic management of the various functional parameters needed for their particular applications.

The CPRI IP Core supports a parallel user IQ data interface, a serial HDLC interface, a serial Ethernet interface, a parallel interface for vendor specific information, and provides individual signals which allow the user to insert/receive L1 Inband Protocol information to/from the CPRI link. The interfaces to the user application are by design very simple to allow the CPRI IP Core to be as flexible as possible. All higher-level functions such as Ethernet MAC functions, HDLC framing, etc. are all intended to be done outside of the CPRI IP Core in user logic or in other Lattice IP Modules.

Figure 2-2 and Figure 2-3 show a system level block diagram of CPRI IP core instantiated in an LatticeECP3 or LFE5UM series FPGA. As indicated in Figure 2-2 and Figure 2-3, additional IP cores may be instantiated to support multiple RP3 data links. Also shown in Figure 2-2 and Figure 2-3 are RXFE and TXFE logic blocks that support the interface between IP logic core and the integrated SERDES/PCS (DCU for LFE5UM) block.

Figure 2-2. CPRI IP Core System Block Diagram in LatticeECP3

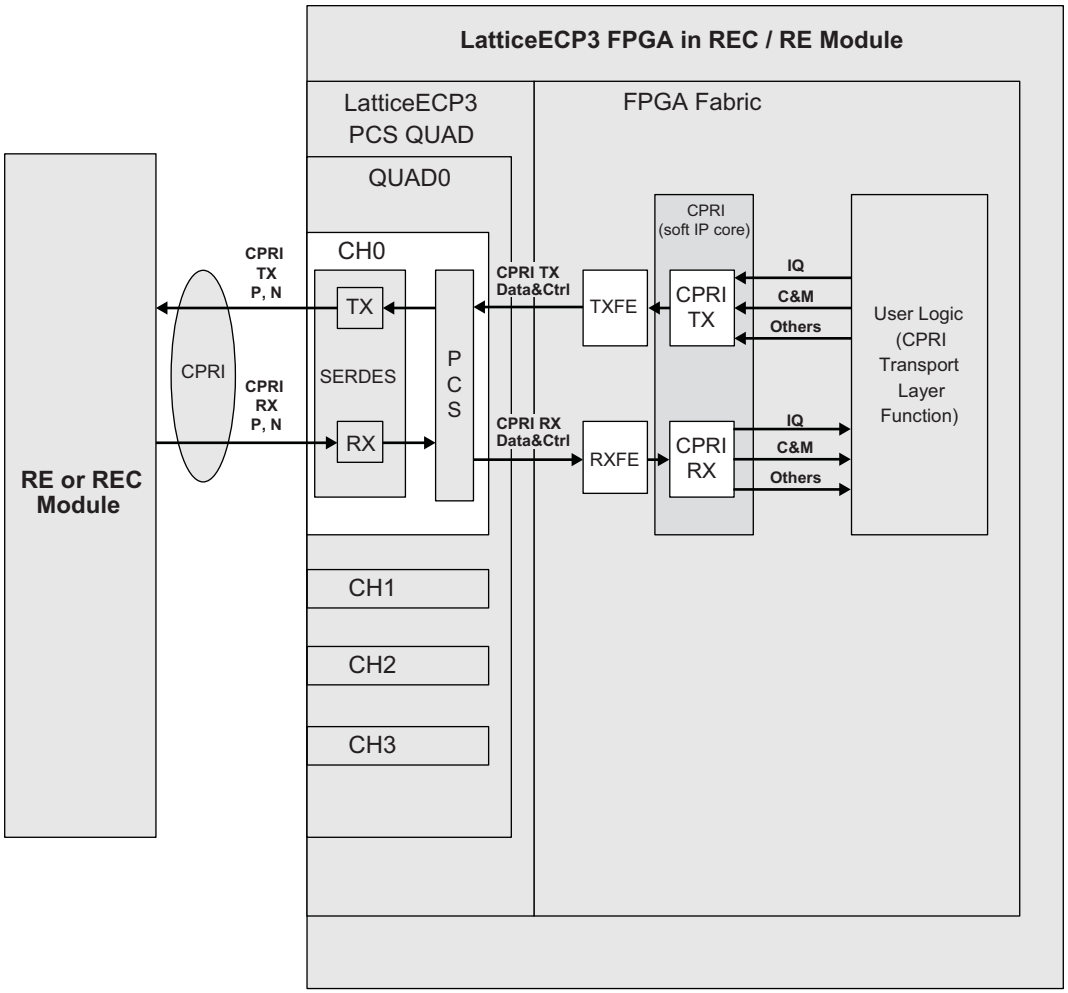
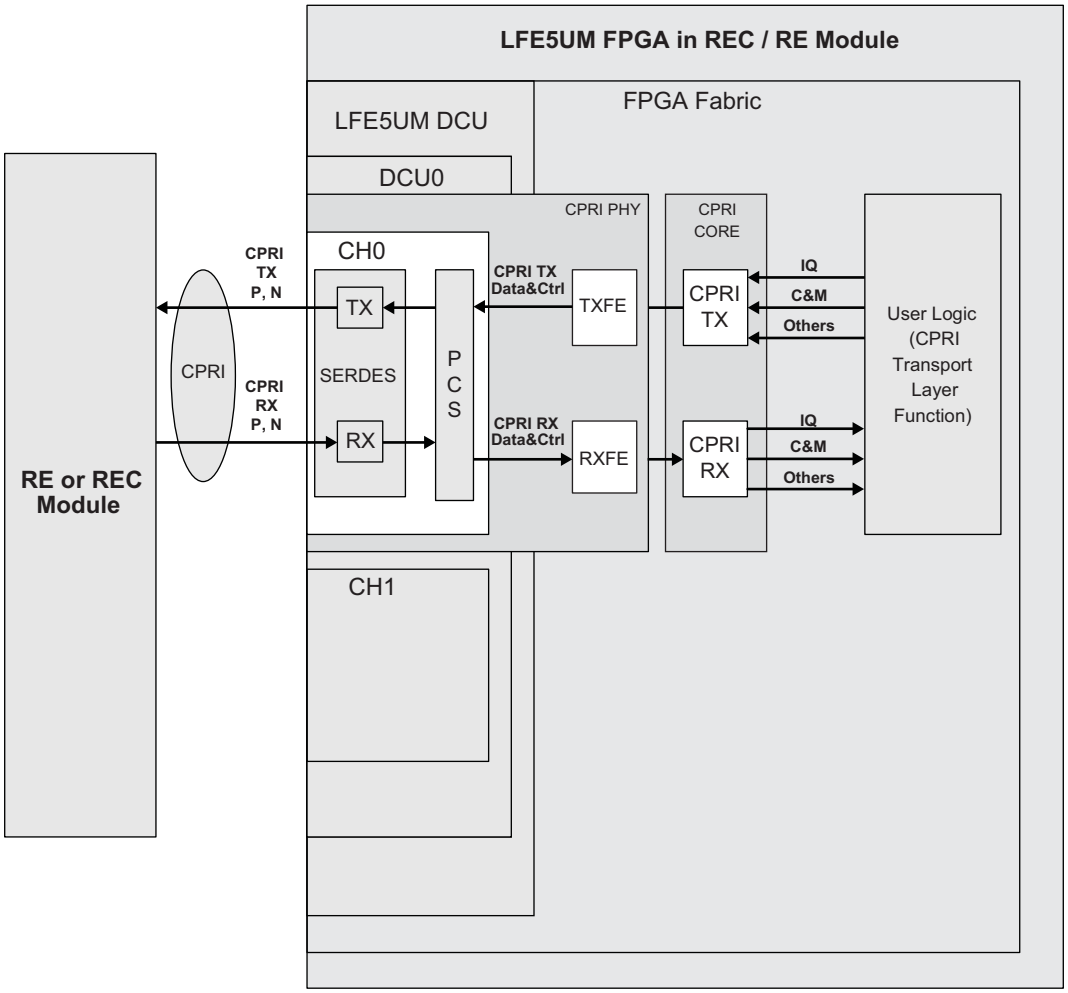
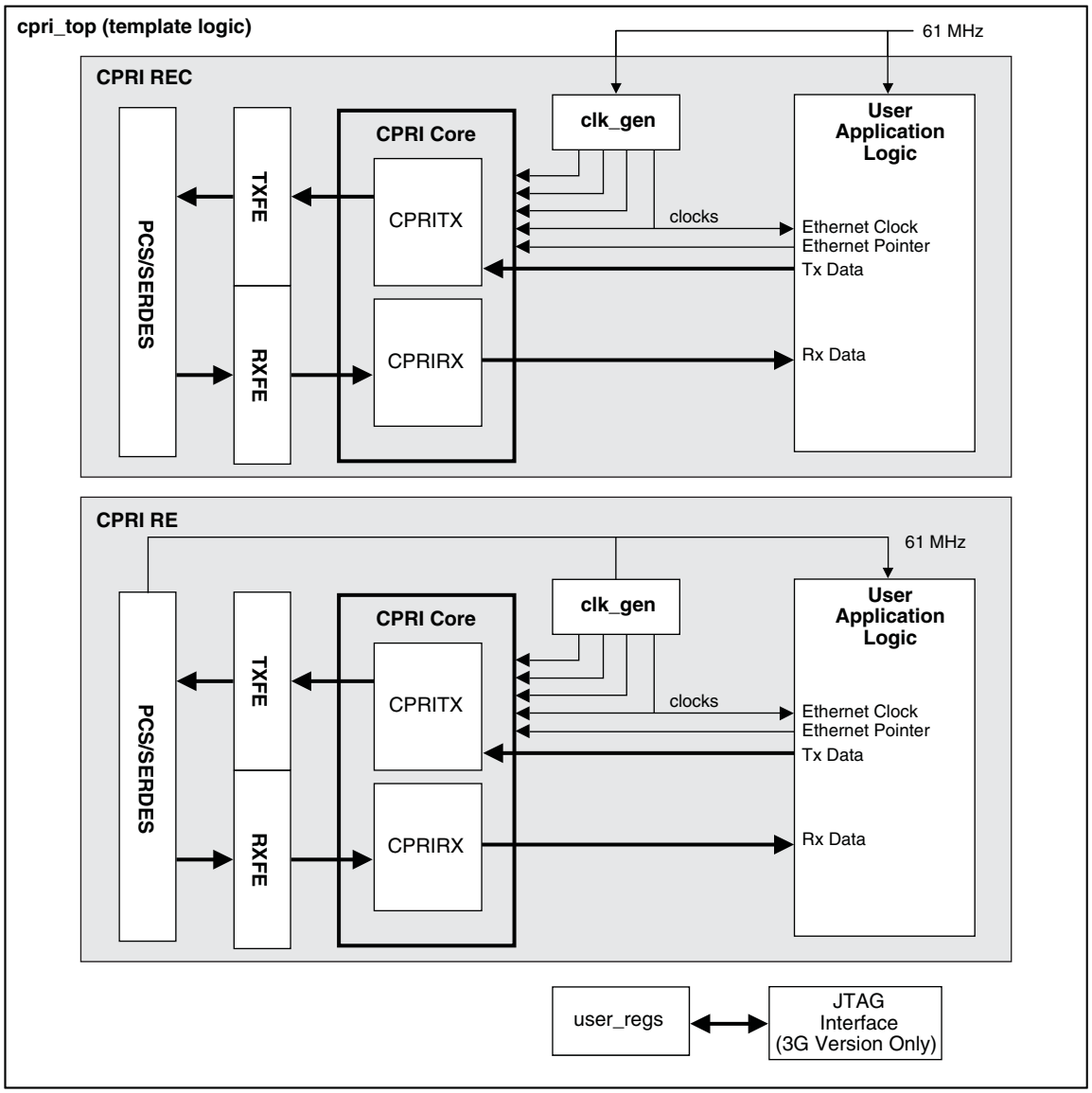


Figure 2-3. CPRI IP Core System Block Diagram in ECP5 LFE5UM



Included in the CPRI IP core evaluation package is a reference module that provides an example of how the IP core is instantiated at the top level, as shown in Figure 2-4. This top-level template is provided in RTL format and provides a good starting point from which the user can begin to add custom logic to a design.

Figure 2-4. Top-Level Template Included with CPRI IP Core (Includes Example Connections for using IP Core in REC and RE Modes)



The CPRI IP logic core is provided in NGO format. For LatticeECP3 CPRI IP core, the rxfe and txfe blocks are RTL templates. For LFE5UM, PCS/SERDES, the rxfe and txfe blocks are packaged as CPRI PHY.

Also included in the reference top file is a user side driver/monitor module and register implementation module for optional use. These included modules are used in the evaluation simulation capability. The driver/monitor module is used to provide data in the transmit direction and verify data in the receive direction. The register implementation module is used to control the IP core. The overall top-level design can be used without modification in the debugging phase on physical hardware needing only a CPRI source/sink capability to verify IP core operation.

Signal Descriptions

Table 2-1. CPRI I/O Signal Descriptions

Signal Name	Direction Input/Output	Width (Bits)	Description
System Clock and Reset			
tx_clk	I	1	61 MHz system clock input
rx_clk	I	1	61 MHz receive side clock input
sys_reset	I	1	Active low reset
txrst	I	1	Active high Ethernet FIFO reset (in TX CPRI)
rxrst	I	1	Active high Ethernet FIFO reset (in RX CPRI)
User Interface			
rec_md	I	1	Select between REC or RE mode, REC = 1
test_md	I	1	test_mod = 1, speed up the timer for simulation
hdlc_240_en	I	1	240 KHz HDLC frequency enable
hdlc_480_en	I	1	480 KHz HDLC frequency enable
hdlc_960_en	I	1	960 KHz HDLC frequency enable
hdlc_1920_en	I	1	1920 KHz HDLC frequency enable
hdlc_2400_en	I	1	2400 KHz HDLC frequency enable (only available in 3G)
auto_cnt	I	1	For master CPRI TX only, update Z64, Z128, Z192 with hyp_cnt_init and bfn_cnt_init when low. When it is high, control words are updated by internal counter.
hyn_cnt_init	I	8	For master CPRI TX only, used for two purposes: Auto_cnt = 0: update Z64 Auto_cnt = 1: update internal hfn counter when tx_sync = 1 and tx_hyp_rst_en = 1
bfn_cnt_init	I	12	For master CPRI TX only, used for two purposes: Auto_cnt = 0: update Z128, Z192 Auto_cnt = 1: update internal bfn counter when tx_sync = 1 and tx_bfn_rst_en = 1
tx_hyp_rst_en	I	1	Transmit side hype frame counter reset enable during tx_sync active
tx_bfn_rst_en	I	1	Transmit side bfn counter reset enable during tx_sync active
tx_eth_pointer	I	6	Transmit Ethernet pointer value, the value is 0, 20~63.
lbr_en	I	2 (3 for 5G)	[1:0] – Maximum CPRI Line bit rate enabled by user
force_sm_standby	I	1	Force startup state machine to standby
pcs_serdes_rate	I	2	CPRI line rate supported by PCS/SERDES
rate_mode	O	2	Final negotiated CPRI Line bit rate after start-up sequence completes
chg_serdes_cfg	O	1	Indicator to program the SERDES for different rate
tx_hdlc_mode	O	3	Transmit side HDLC negotiated bit rate
tx_dis	O	1	For RE mode disable transmit side active high
cpri_stup_stat	O	3	Start up sequence state state 1 = synchronization state 2 = protocol setup state 3 = c/m plane setup state 4 = interface and vendor negotiation state 5 = operation
ver_num_err	O	1	Version number error
CPRI Link Status			
rx_lof	O	1	Receive side Loss of Frame

Table 2-1. CPRI I/O Signal Descriptions (Continued)

Signal Name	Direction Input/Output	Width (Bits)	Description
rx_los	O	1	Receive side Loss of Signal
User Plane IQ Data Signals			
tx_iq_da	I	32 (40 for 3G, 64 for 5G)	Transmit side IQ data
tx_sync	I	1	Transmit side IQ data sync
rx_hyp_num	O	8	Receive side hyper frame number
rx_bfn_num	O	12	Receive side basic frame number
rx_frm_addr	O	8	Receive side frame address
rx_iq_slt_addr	O	4	Receive side IQ data slot address
rx_iq_da_wr	O	1	Receive side IQ data write enable
rx_iq_da	O	32 (40 for 3G, 64 for 5G)	Receive side IQ data
L1 Inband Protocol Signals			
tx_l1_rst_rqstack	I	1	Transmit reset request or acknowledge
tx_l1_rai	I	1	Transmit Remote Alarm indication
tx_l1_sdi	I	1	Transmit SAP Defect Indication
rx_l1_ver_num	O	8	Received version number
rx_l1_hdlc_mode	O	3	Receive side HDLC negotiated bit rate
rx_l1_rst_rqstack	O	1	Receive reset request or acknowledge
rx_l1_rai	O	1	Receive Remote Action Indication
rx_l1_sdi	O	1	Receive SAP Defect Indication
rx_l1_los	O	1	Receive Loss of Signal
rx_li_lof	O	1	Receive Loss of Frame
rx_l1_eth_pointer	O	6	Receive side Ethernet pointer value
Vendor-Specific Data Interface Signals			
tx_vendor_da	I	32 (40 for 3G, 64 for 5G)	Vendor-specific transmit data
tx_vendor_da_req	O	1	Vendor-specific transmit data request
rx_vendor_da_val	O	1	Vendor-specific receive data valid
rx_vendor_da	O	32 (40 for 3G, 64 for 5G)	Vendor-specific receive data
CPRI to SERDES Signals			
tx_cpri_ctl	O	2	Transmit side CPRI control to SERDES
tx_cpri_da	O	16 (40 for 3G and 64 for 5G, applies to tx-cpri_da and rx_cpri_da) (5 for 3G and 8 for 5G, applies to tx_cpri_ctl, rx_cpri_ctl and rx_cpri_cv)	Transmit side CPRI data to SERDES

Table 2-1. CPRI I/O Signal Descriptions (Continued)

Signal Name	Direction Input/Output	Width (Bits)	Description
rx_cpri_ctl	I	2	Receive side CPRI control from SERDES
rx_cpri_da	I	16	Receive side CPRI data from SERDES
rx_cpri_cv	I	2	Receive side CPRI code violation from SERDES
slip_rxfe	O	1	Receive side slip to get “BC” in low byte
C&M Ethernet Interface Signals			
tx_eth_clk, rx_eth_clk	I	1	Transmit Ethernet clock, Receive Ethernet clock
tx_eth_da	I	4	Transmit Ethernet data (1 bit wide in Serial mode)
tx_eth_en	I	1	Transmit Ethernet data enable (not equipped in Serial mode)
tx_eth_er	I	1	Transmit Ethernet error (not equipped in Serial mode)
rx_eth_da	O	4	Receive Ethernet data (1 bit wide in Serial mode)
rx_eth_en	I	1	Receive Ethernet data enable (not equipped in Serial mode)
rx_eth_er	I	1	Receive Ethernet error (not equipped in Serial mode)
tx_eth_almost_full	O	1	Transmit Ethernet FIFO almost full. This is for user flow control.
tx_eth_empty	O	1	Transmit Ethernet FIFO empty
rx_eth_full	O	1	Receive Ethernet FIFO full
rx_eth_empty	O	1	Receive Ethernet FIFO empty
rx_eth_fifo_err	O	2	Receive Ethernet FIFO error flag (only for Fixed mode)
C&M HDLC Interface Signals			
tx_hdlc_da	I	1	Transmit HDLC data
tx_hdlc_clk	O	1	Transmit HDLC clock
rx_hdlc_clk	O	1	Receive HDLC clock
rx_hdlc_wr	O	1	Receive HDLC write
rx_hdlc_da	O	1	Receive HDLC data

Timing Specifications

Refer to DS1021, LatticeECP3 Family Data Sheet and DS1044, ECP5 Family Data Sheet for detailed SERDES and FPGA interface timing and electrical specifications.

CPRI Overview

Figure 2-5 shows the CPRI layer 1 and layer 2 protocols. The CPRI IP core interleaves user IQ (in-phase and quadrature) data with control and management (C&M) data into the frame and hyperframe formats specified by the CPRI Specification and shown in Figure 2-6 and Figure 2-7, respectively.

Figure 2-5. CPRI Protocol Overview

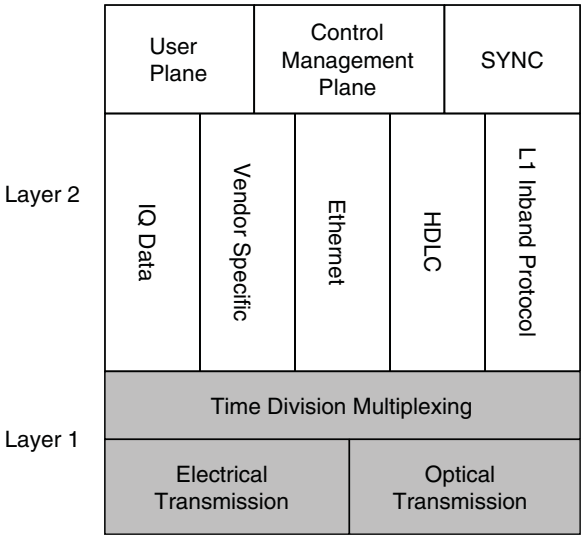


Figure 2-6. CPRI Frame (Shown for 614.4 Mbps, 1228.8 Mbps, 2457.6 Mbps, and 3072 Mbps Line Rates)

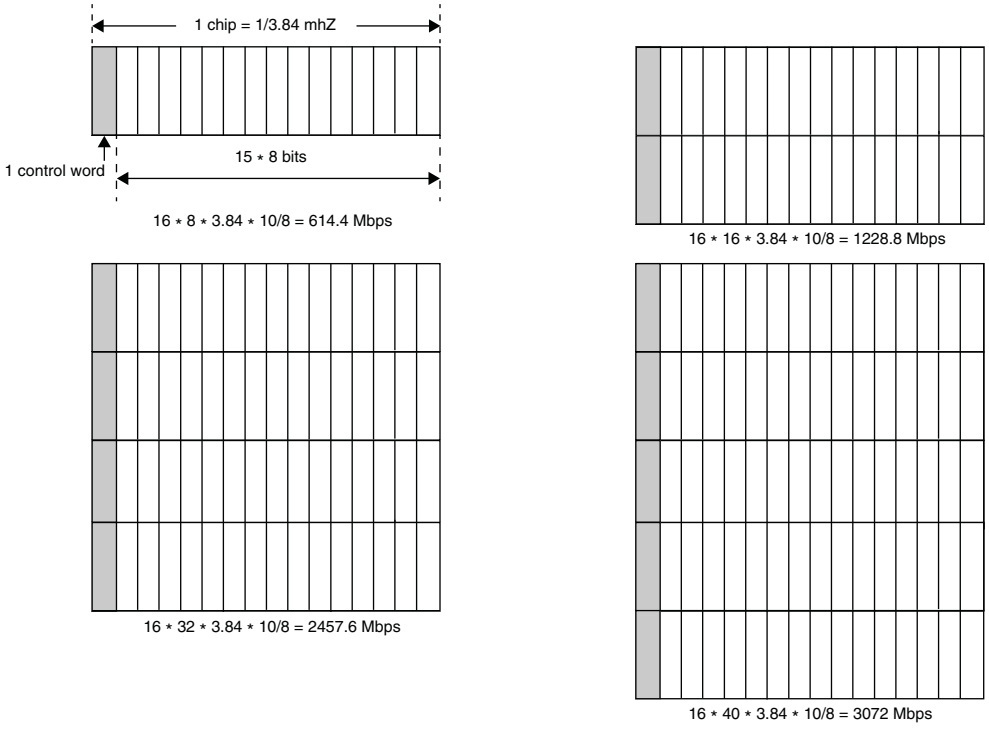
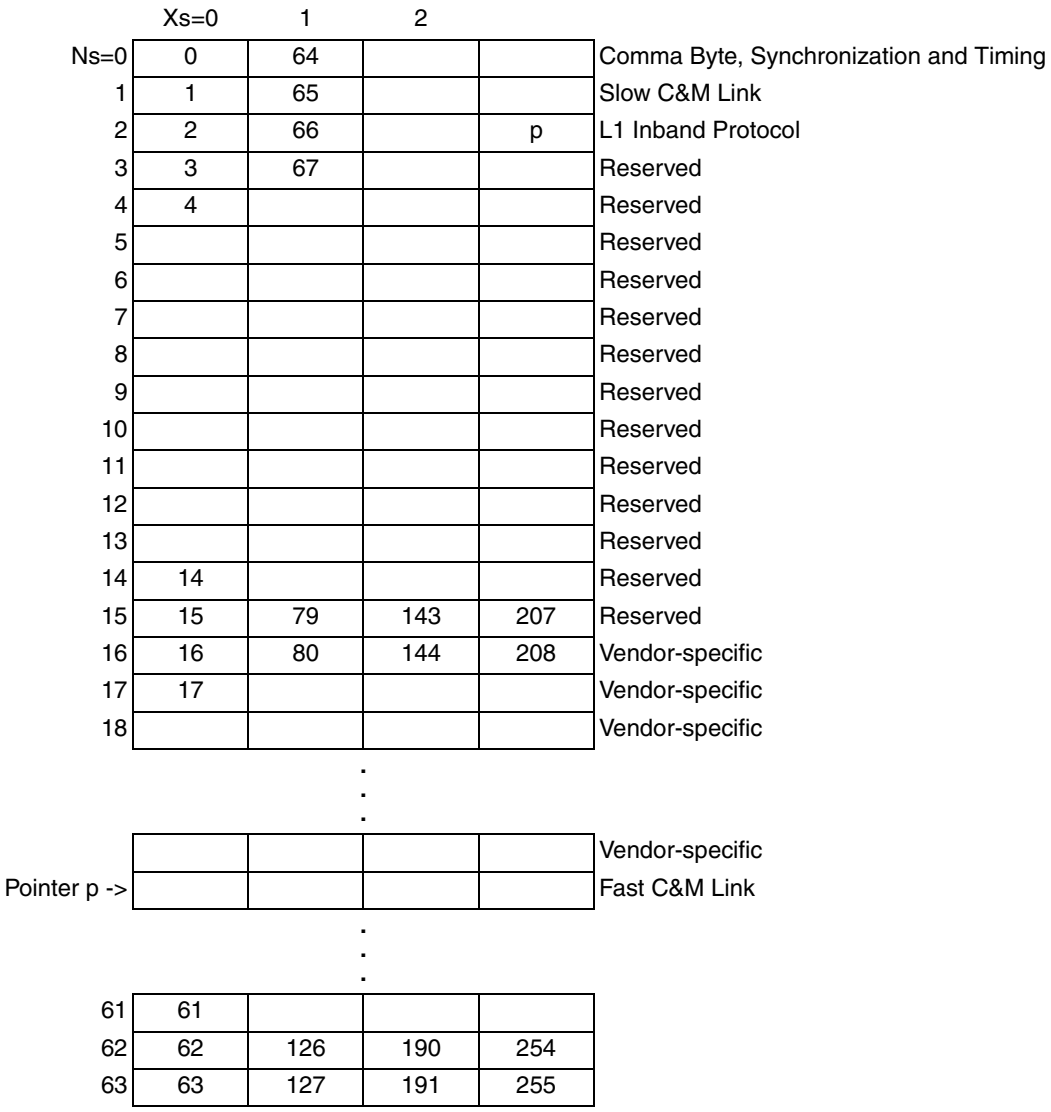


Figure 2-7. CPRI Hyperframe Format



Four possible line rates for the CPRI frame are supported, as shown in Table 2-2. The maximum line bit rate that the core must support is selected by setting the lbr_en input signals. Once the maximum line bit rate has been selected, all lower line bit rates are automatically enabled. The bit rate between the REC and RE is then negotiated between the transmitting and receiving ends by the start-up sequence state machine within the CPRI IP core.

Table 2-2. CPRI Line Rates

CPRI Line Bit Rate	Rate (Mbps)	lbr_en[1:0] (lbr_en[2:0] for 5G)
Option 1	614.4	00
Option 2	1228.8	01
Option 3	2457.6	1X or 10 (LatticeECP3 only)
Option 4	3072	11 (LatticeECP3 only)
Option 5 (for 5G version)	4915.2	100 (LatticeECP5 only)

Functional Overview

A block diagram of a typical LatticeECP3 CPRI application is shown in Figure 2-2 and a block diagram of a typical LFE5UM CPRI application is shown in Figure 2-3. These examples show four CPRI link transceivers implemented in a LatticeECP3 and an LFE5UM device. The major functional blocks in the example are the CPRI Soft IP core, the PCS/SERDES block, and the user application logic. The CPRI IP Core (cpri_core), shown in Figure 2-1, consists of two major functional blocks, the transmitter (CPRITX) and the receiver (CPRIRX). One side of each of these two blocks interfaces to the PCS/SERDES module, and the other side interfaces to the user logic that implements the data link and higher layers of the CPRI protocol.

The CPRI IP Core multiplexes user IQ data with synchronization and C&M data. The IP core is being designed with very simple and versatile interfaces for transferring data to the user application logic.

IQ data is transferred between the IP core and the user logic using a parallel data interface. In the transmit direction, the user application provides a sync pulse which determines the start of a CPRI BFN (every 150 hyperframes) frame. In the receive direction, the IP core transfers IQ data to the user application along with framing information recovered from the CPRI link.

In the transmit direction, the CPRI IP core accepts user C&M data at either the HDLC and/or the Ethernet interface and interleaves that data with the user IQ data into the CPRI frame. In the receive direction, C&M data received on the CPRI link is disinterleaved from the user IQ data, and the HDLC or Ethernet encapsulated data is presented to the user at either the HDLC or Ethernet interfaces of the CPRI IP core.

The C&M data can be encapsulated in either HDLC (slow channel) or Ethernet (fast channel) as desired by the user. For HDLC, the CPRI IP Core only performs the interleaving of the C&M data with user IQ data. It does not provide any of the HDLC Level 2 functions such as framing and serial to parallel conversion. These functions must be done in the user application logic or in another IP module. For Ethernet, three modes are provided. In mode 1, the core does not provide the serial to parallel and 4B/5B conversion. The interface is a serial bitstream that contains 5B encoded nibbles. In mode 2, the core provides a standard MII interface that can be connected to a standard Ethernet MAC. In mode 3, the core provides an MII like interface that has the clocks as inputs instead of outputs. This interface can be connected to a PHY that is operating at the 100 Mbps standard rate.

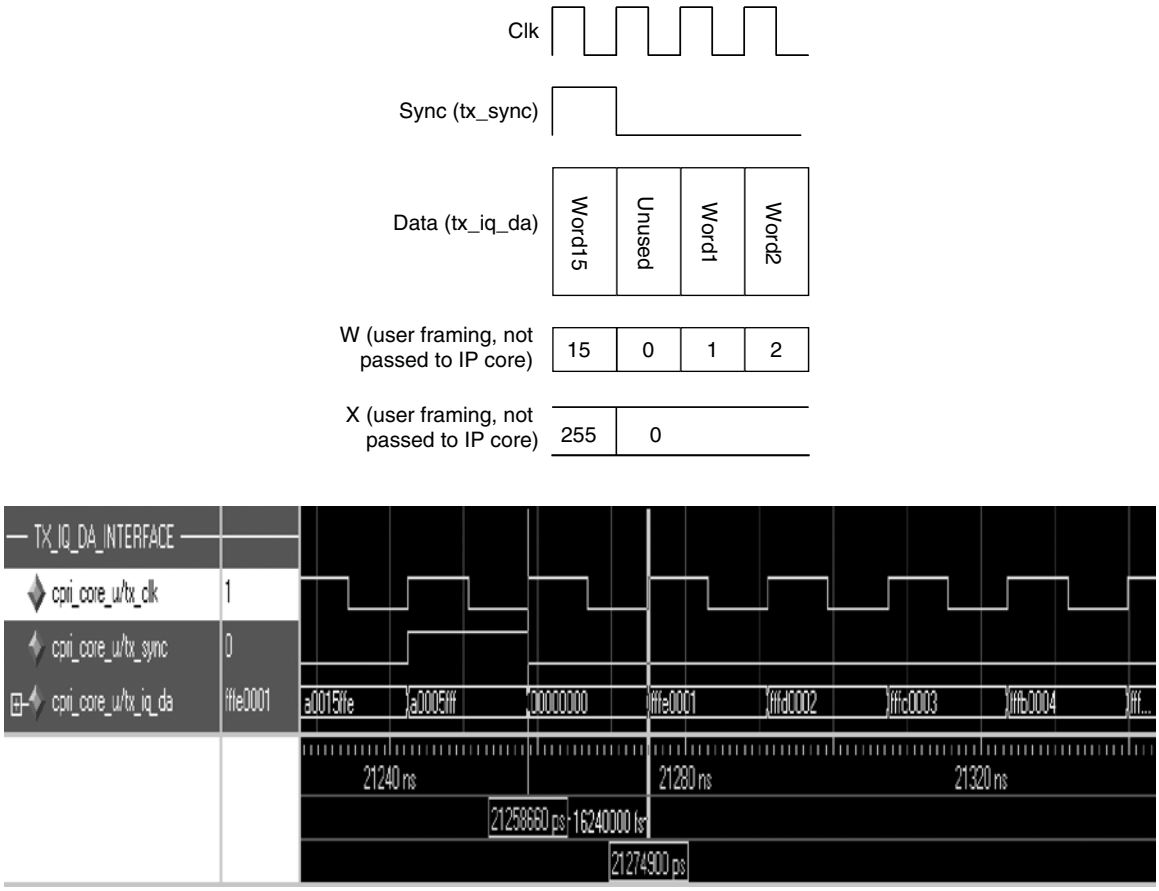
The following sections discuss the interfaces of the IQ data, HDLC, Ethernet, and vendor information interfaces of the CPRI IP core.

User Plane IQ Data Interface

The user IQ data interface supports the five line rates shown in Table 2-2. For 3G version, both the transmit and receive directions provide a 40-bit IQ data bus. However, the number of bits used depends on the line rate selected by the user. For the 614.4 Mbps line rate, 8 of the 32 bits on the IQ data interface are used (bits 7:0). For 1228.8 Mbps, bits 15:0 are used, and for a line rate of 2457.6 Mbps, 32 bits are used. For a line rate of 3072 Mbps, all 40 bits are used. For 5G version (4.9152 Gbps line rate), 64-bit IQ data bus is used for both the transmitter and the receiver.

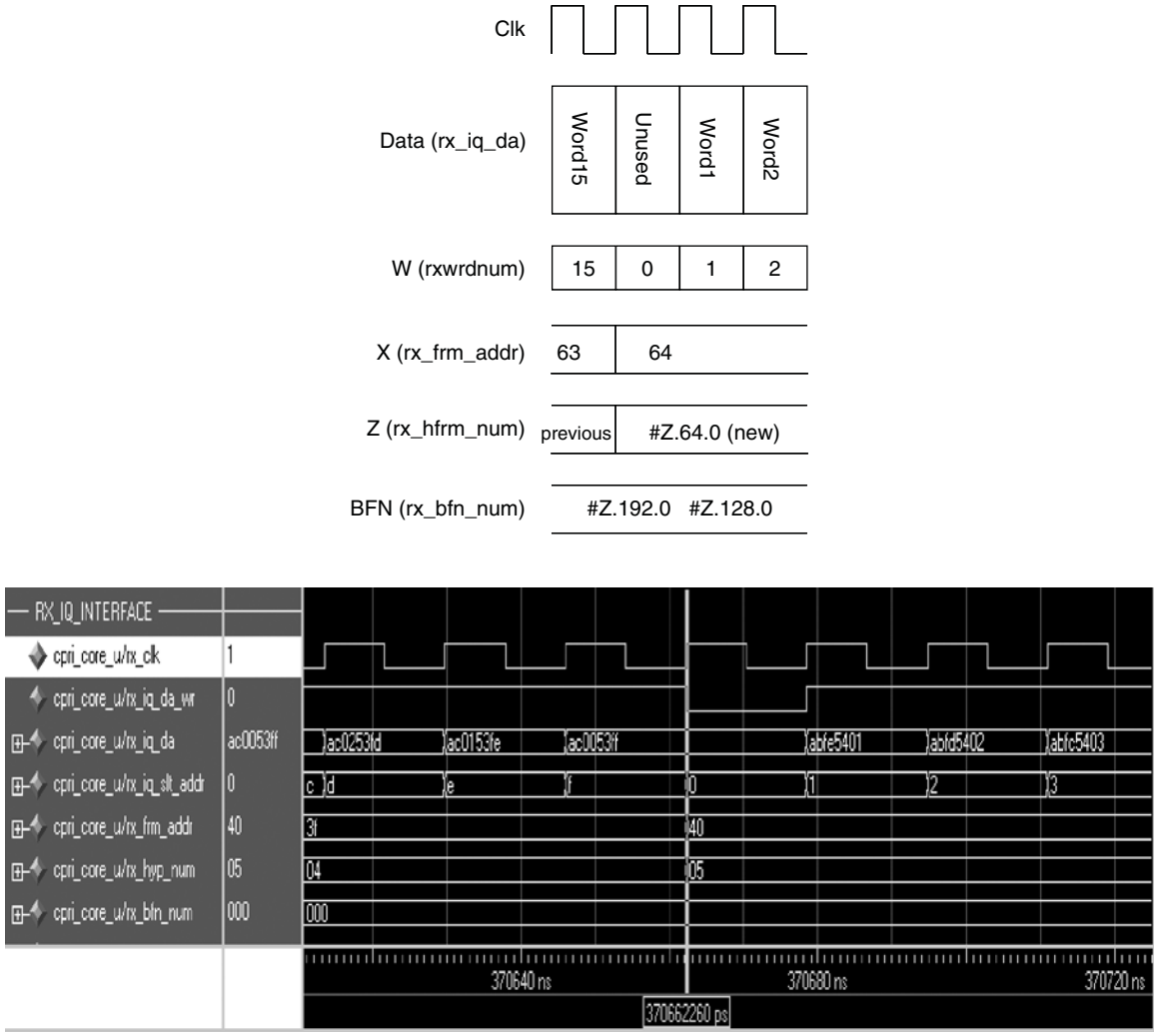
In the transmit direction, the user application must provide a sync pulse to the CPRI IP core to indicate the start of each CPRI BFN (every 150 hyperframes) frame. This sync pulse must be aligned with the IQ data, as shown in Figure 2-8.

Figure 2-8. Tx User IQ Interface Sync Pulse Alignment



In the receive direction, the CPRI IP Core provides IQ data to the user interface along with a word number (W), frame number (X), hyperframe number (Z), and a BFN number, as shown in Figure 2-9.

Figure 2-9. Rx IQ Interface Data and Frame Number Alignment



Ethernet Interface

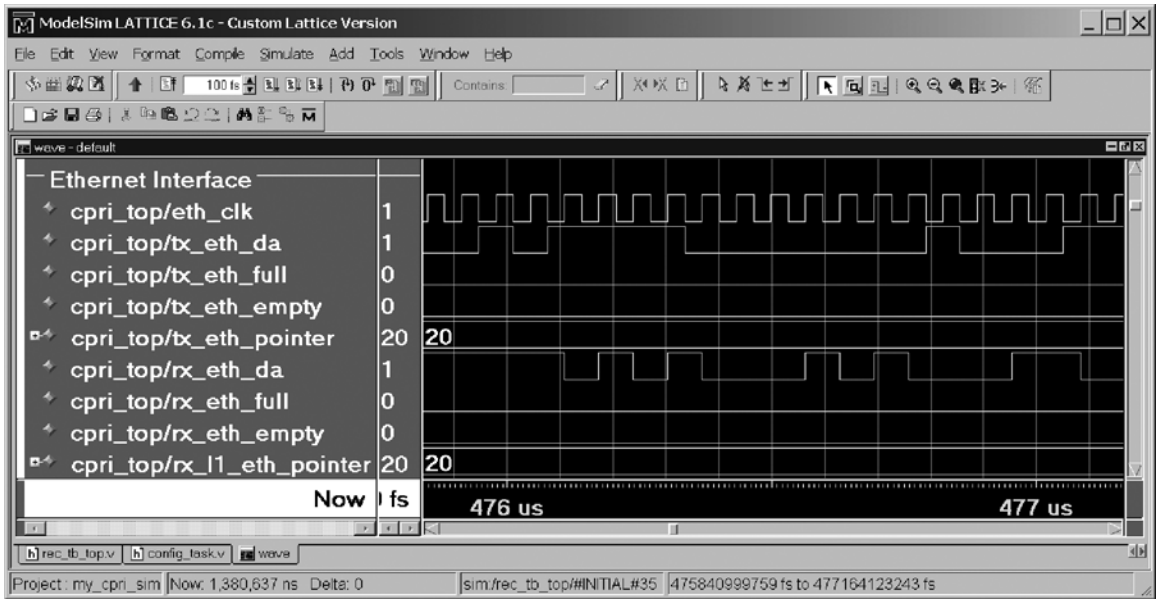
Mode 1 (Serial)

The CPRI IP Core Ethernet Interface transmits and receives Ethernet data to/from the user application logic using a simple serial data connection. The amount of bandwidth on the CPRI link which is allocated to Ethernet (fast C&M) data is determined by the pointer value (Z.194.0) which in turn determines which subchannel number the Ethernet data starts at within the CPRI hyperframe. The pointer value is set by the user using the tx_eth_pointer[7:0] inputs to the IP core. The transmitter and receiver of the REC and RE ends must be able to use the same pointer value.

Since a buffer is provided within the IP core for Ethernet data, the Ethernet interface clock between the IP core and the user application logic must be chosen such that the correct number of words are transferred between the IP core and the user's logic each frame or else the internal buffer may overrun or underrun. Due to the large number of possible pointer values available it is not practical for the IP core to generate the Ethernet interface clock. Instead, the IP core is designed such that the pointer value and the Ethernet interface clock are provided as inputs to the Core, giving the user the maximum flexibility. The template logic (cpri_top) shown in Figure 2-10, which will be delivered with the IP core, will include an example of how to generate and connect an Ethernet interface clock frequency of 61.44 MHz. Additional clock frequencies and pointer values may be set by the user by modifying the template logic. The difficulty which will be encountered in generating various Ethernet clock frequencies and pointer values will be entirely dependent on the clock frequencies available in the user's system. This is why the

generation of the Ethernet clock frequency, and the assignment of the pointer value, must be done in the template logic and not within the IP core.

Figure 2-10. Ethernet C&M Interface



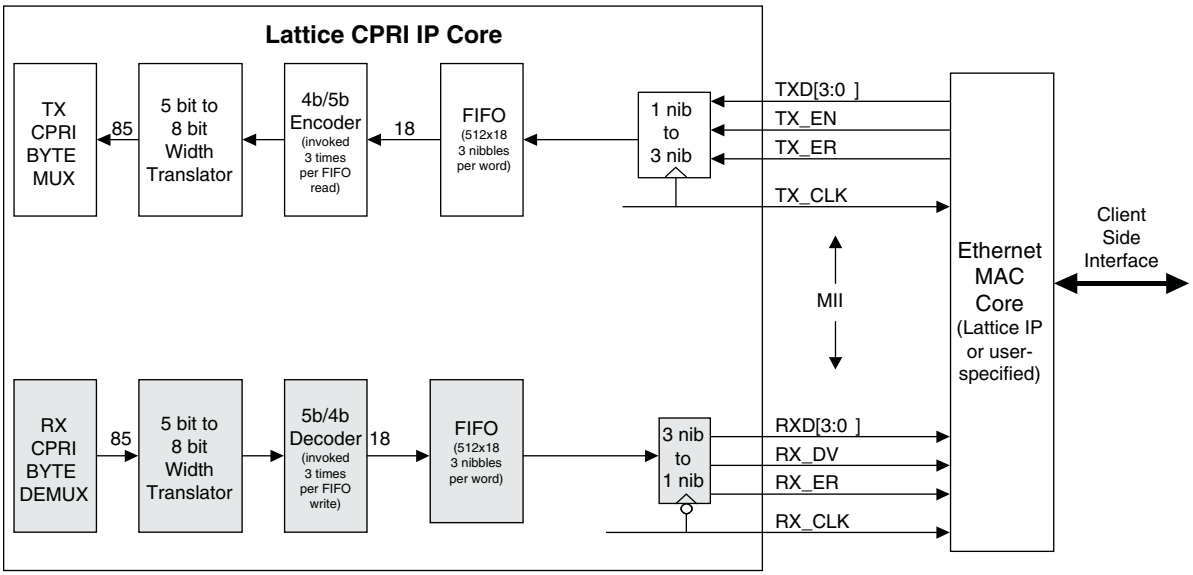
Mode 2 (Matched Rate MII)

The CPRI IP Core Ethernet Interface transmits and receives Ethernet data to/from the user application logic using a non-standard rate MII interface. The amount of bandwidth on the CPRI link which is allocated to Ethernet (fast C&M) data is determined by the pointer value (Z.194.0) which in turn determines which subchannel number the Ethernet data starts at within the CPRI hyperframe. The pointer value is set by the user using the tx_eth_pointer[7:0] inputs to the IP core.

Since a buffer is provided within the IP core for Ethernet data, the Ethernet interface clock between the IP core and the user application logic must be chosen such that the correct number of words are transferred between the IP core and the user's logic each frame or else the internal buffer may overrun or underrun. Due to the large number of possible pointer values available it is not practical for the IP Core to generate a periodic interface clock. Instead, the IP core is designed to produce a gapped clock. The Ethernet pointer and CPRI line rate are used to index a two parameter table that specifies the frequency and number of pulses contained in the gapped clock. The transmit Ethernet clock is based on the negotiated rate and transmit pointer. The receive Ethernet clock is based on the negotiated rate and the received L1 inband pointer in Z.194.0.

The core provides the 4B/5B code conversion required by the CPRI specification. The logic that interfaces the MII to CPRI byte mux/demux is shown in Figure 2-11.

Figure 2-11. Matched Rate MII CPRI Ethernet Interface



Note 1: TX_CLK and RX_CLK are gapped clocks with transition rates matching the effective data rate of the Fast C&M Channel specified by the pointer value in control byte #Z.194.0 and the CPRI line rate.
Note 2: Both FIFOs are read and written as needed to source and sink data/control from/to the MII and CPRI mux/demux.

Mode 3 (100 Mb/s Fixed Rate MII)

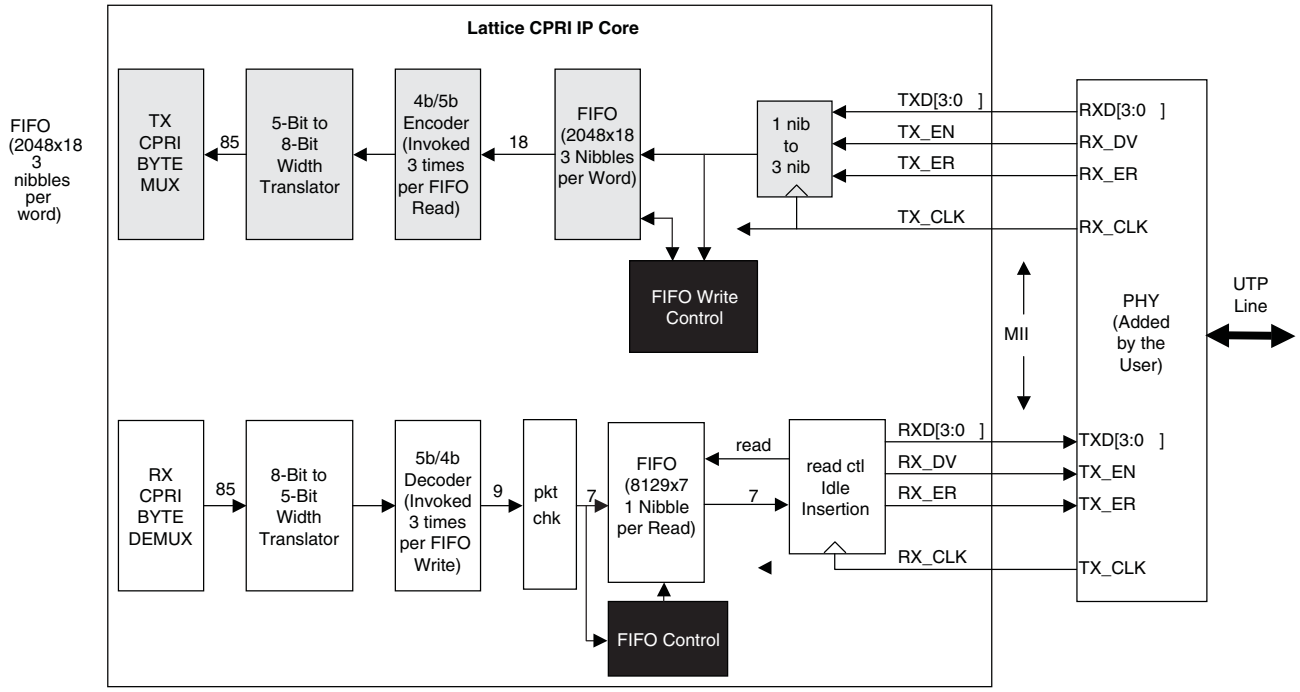
The CPRI IP Core Ethernet Interface transmits and receives Ethernet data to/from the user application logic using a 100 Mbps rate MII interface. The amount of bandwidth on the CPRI link which is allocated to Ethernet (fast C&M) data is determined by the pointer value (Z.194.0) which in turn determines which subchannel number the Ethernet data starts at within the CPRI hyperframe. The pointer value is set by the user using the tx_eth_pointer[7:0] inputs to the IP core.

The logic needed to support mode 3 is similar to that required for mode 2 with the exception of handling the reading and writing of the FIFOs. On the transmit side, the FIFO is always written at a faster rate than it is read. This means that the reading of this FIFO is the same as mode 2. Interframe gap is only written into the FIFO if the almost empty threshold is not maintained. This prevents the FIFO from being filled with idle information. It is the responsibility of the driver of the 100 Mbps link to not over run the FIFO. There is no flow control provided to accommodate the rate mismatch between the 100Mbps link and the CPRI link. Packets must be spaced to allow enough time for the CPRI to transmit packets. On the receive side, the FIFO is always read at a faster rate than it is written. When the FIFO input data is not idle and passes basic SSD and ESD checks, it is written to the FIFO. When idle is detected on the FIFO input the FIFO is not written. When an end of packet is detected, a request is sent to the FIFO Read Control to send the packet on to the MII. A complete packet is received before it is read from the FIFO. FIFO reads begin when a request is received from the FIFO Write Control. FIFO reads continue until an end of packet is detected. When an end of packet is detected, FIFO reads stop and a minimum of 24 nibble IDLEs are supplied to the MII interface.

For 3.072 Gbps CPRI link, the MAC Ethernet MAX bandwidth is 3.84M/64*(64-20)*40, that is 105.6 Mbps (when Ethernet pointer p is set to 20), and MIN bandwidth is 2.4 Mbps (when Ethernet pointer p is set to 63). For example, if your Ethernet bandwidth requirement is 10 Mbps, please set Ethernet pointer p as 60~61, the corresponding bandwidth is 7.2~9.6 Mbps. If Ethernet pointer p is set too small, the TX FIFO for Ethernet may be empty, and the Ethernet package may be inserted by duplicated data of the partial package. If Ethernet pointer p is set too large, the TX FIFO for Ethernet may be full. If no Ethernet bandwidth is needed, please set Ethernet pointer p to 0.

The core provides the 4B/5B code conversion required by the CPRI specification. The logic that interfaces the MII to CPRI byte mux/demux is shown in Figure 2-12.

Figure 2-12. 100 Mbps Fixed Rate MII CPRI Ethernet Interface



1. TX_CLK and RX_CLK are supplied by the external PHY device and assumed to be 25MHz.
2. The transmit FIFO is read as needed to supply data/control to the CPRI mux.
3. The transmit FIFO is written as needed to sink packets from the MII and supply idle.
4. The receive FIFO is read and written as needed to source and sink packets from/to the MII and CPRI demux. Idle is supplied seperately.

HDLC Interface

A timing diagram for the Ethernet C&M interface is given in Figure 2-13. The CPRI IP Core HDLC interface transmits and receives HDLC data to/from the user application logic using a serial data connection. The user selects the desired frequencies which the IP core will support by setting the hdlc_(240,480,960,1920,2400)_en input signals. The HDLC data rates shown in Table 2-3 are supported.

The CPRI IP core HDLC Interface does not perform any HDLC framing or processing. This must be performed in the user application logic or in another IP module. The transmitter of the IP core will negotiate with the receiver of the end of the CPRI link to achieve the maximum HDLC rate possible.

Figure 2-13. HDLC C&M Interface

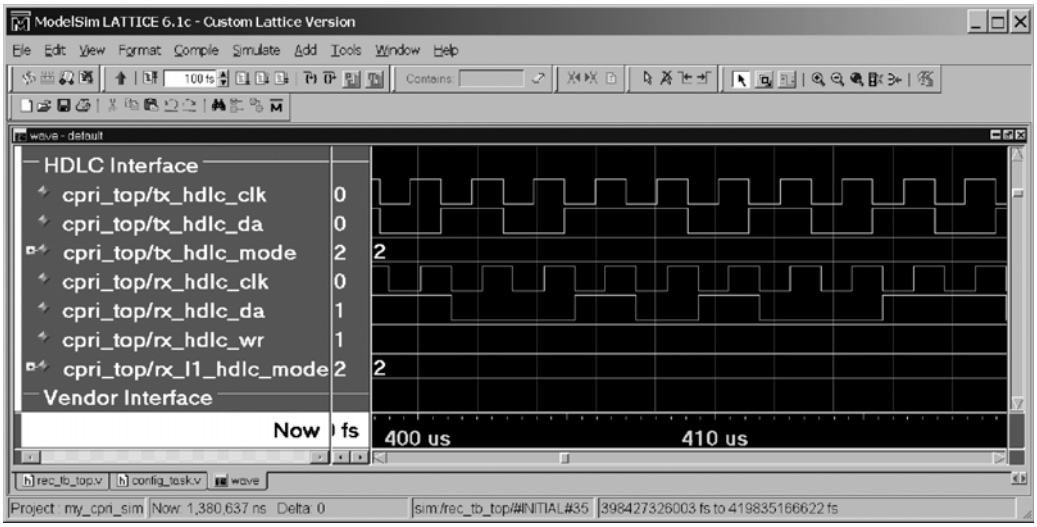


Table 2-3. HDLC Frequencies Supported

HDLC Option	Input Signal	HDLC Data Rate (Kbps)
0	None selected	HDLC disabled
1	hdlc_240_en = 1	240
2	hdlc_480_en = 1	480
3	hdlc_960_en = 1	960
4	hdlc_1920_en = 1	1920
5	hdlc_2400_en = 1	2400

L1 Inband Protocol Interface

The L1 Inband Protocol Interface provides signals that allow the user application logic to populate the control words listed in the CPRI specification, and to read the value of the L1 Inband Protocol control words that are received from the CPRI link.

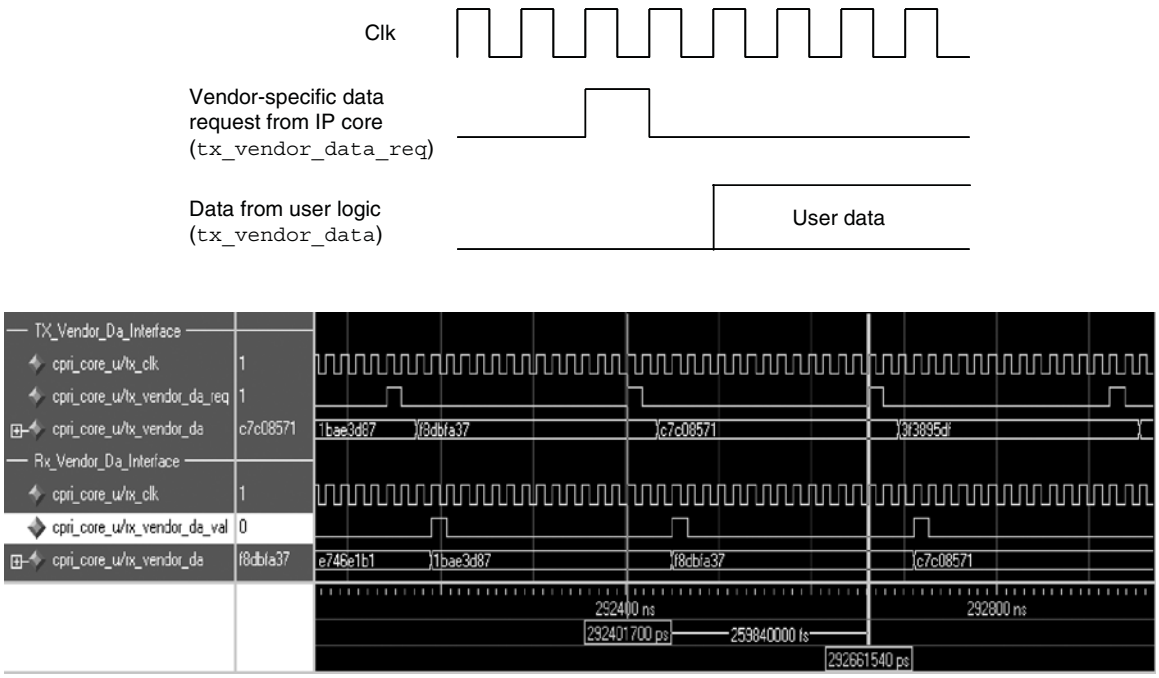
Vendor Specific Information

Figure 2-14 illustrates the timing of the vendor-specific information interface between the IP core and the user application logic. The IP core provides a simple parallel interface for merging vendor-specific information into the CPRI frame. The number of bytes available in the CPRI frame for vendor-specific information is dependent on the pointer value chosen. Any FIFOs required to support the bandwidth allocated to vendor-specific information must be implemented in the user logic.

The IP core provides a data request signal to the user application logic called tx_vendor_data_req. When this signal goes high, the user logic must return the vendor-specific data to the IP core within six clock cycles. The user logic must continue to provide vendor-specific data until the tx_vendor_data_req signal is once again asserted. If the user does not have any data to send in the vendor-specific bytes, then it must insert idle code.

In the receive direction, incoming vendor-specific information which is recovered from the CPRI link is presented to the user application logic along with a rx_vendor_da_val signal. The vendor-specific information interface uses either 8, 16, or 32 (40 for 3G, 64 for 5G) of the available data bits, depending on which CPRI line bit rate has been selected. This is similar to the IQ data interface described previously.

Figure 2-14. Timing for Vendor-Specific Information Interface



Start-up Sequence

The CPRI IP Core provides a start-up state machine which executes the startup state transitions as shown in Figure 30 in the CPRI Specification (Reference 2). This state machine will automatically perform the synchronization of Layer 1, and it will align the capabilities of the REC and the RE (line bit rate, protocol, C&M link speed, C&M protocol, and vendor specific signaling). For 3G version, the CPRI IP Core depends on software to program the correct data bus width into the LatticeECP3/LFE5UM SERDES through the SCI Bus. For a 1228.8 or 2457.6 Mbps CPRI line bit rate, the SERDES must be provisioned for a 16-bit interface to the FPGA logic. For all CPRI line bit rate, the SERDES must be provisioned for an 8-bit interface to the FPGA logic to achieve low latency purpose. Since the provisioned mode of the SERDES may need to change while the start-up sequence is negotiating the CPRI line rate, a signal (chg_serdes_cfg) is provided to the user application logic indicating that the mode the SERDES should be programmed for needs to be changed. The user application must monitor this signal and program the SERDES to the correct mode while the REC and RE are attempting to match line bit rates. When the application has finished programming the PCS/SERDES it writes the rate that is being supported to lbr_en[4:3]. For 5G version, there is not JTAG interface to update parameters.

The IPexpress ™ and the Clarity Designer tools are used to create IP and architectural modules in the Diamond software. IPexpress is for LatticeECP3 CPRI IP Core and Clarity Designer is for LFE5UM CPRI IP Core. Refer to "IP Core Generation" on page 28 for a description on how to generate the IP.

Table 3-1 provides the list of user configurable parameters for the CPRI IP core for 3G version. The parameter settings are specified using the CPRI IP core Configuration GUI in IPexpress.

Table 3-1. IP Core Parameters

Parameters	Range/Options	Default
General Options		
Design Entry	Low Latency	Low Latency
Ethernet Mode	100 Mb/s, Matched, Serial	100 Mb/s
Eval Configuration		
Synthesis Tool	Synplify	Synplify

CPRI Configuration Dialog Box

Figure 3-1 shows the CPRI Configuration dialog box.

Figure 3-1. CPRI Configuration Dialog Box

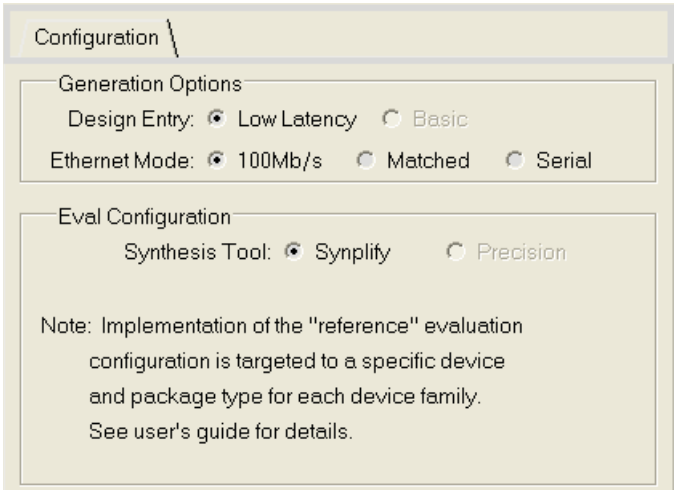
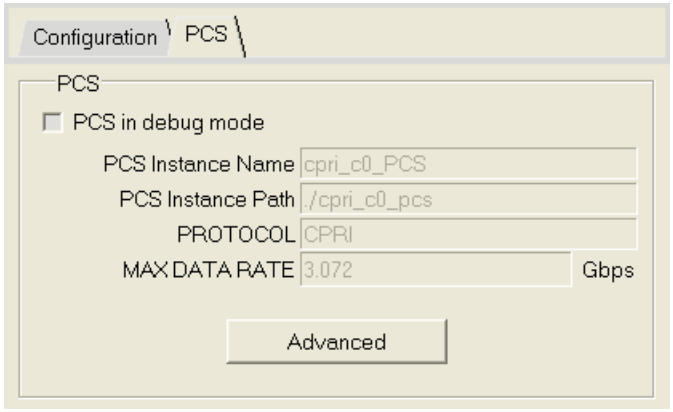


Figure 3-2 shows the CPRI PCS Configuration dialog box, it is for LFE5UM CPRI IP Core only. The page 'PCS' is for ECP5UM PCS/SERDES settings. If the **PCS in debug mode** option is selected, the LFE5UM DCU interface is displayed in <username>_phy_bb.v for debug. For further PCS configuration, click the **Advanced** button.

Figure 3-2. CPRI PCS Configuration Dialog Box

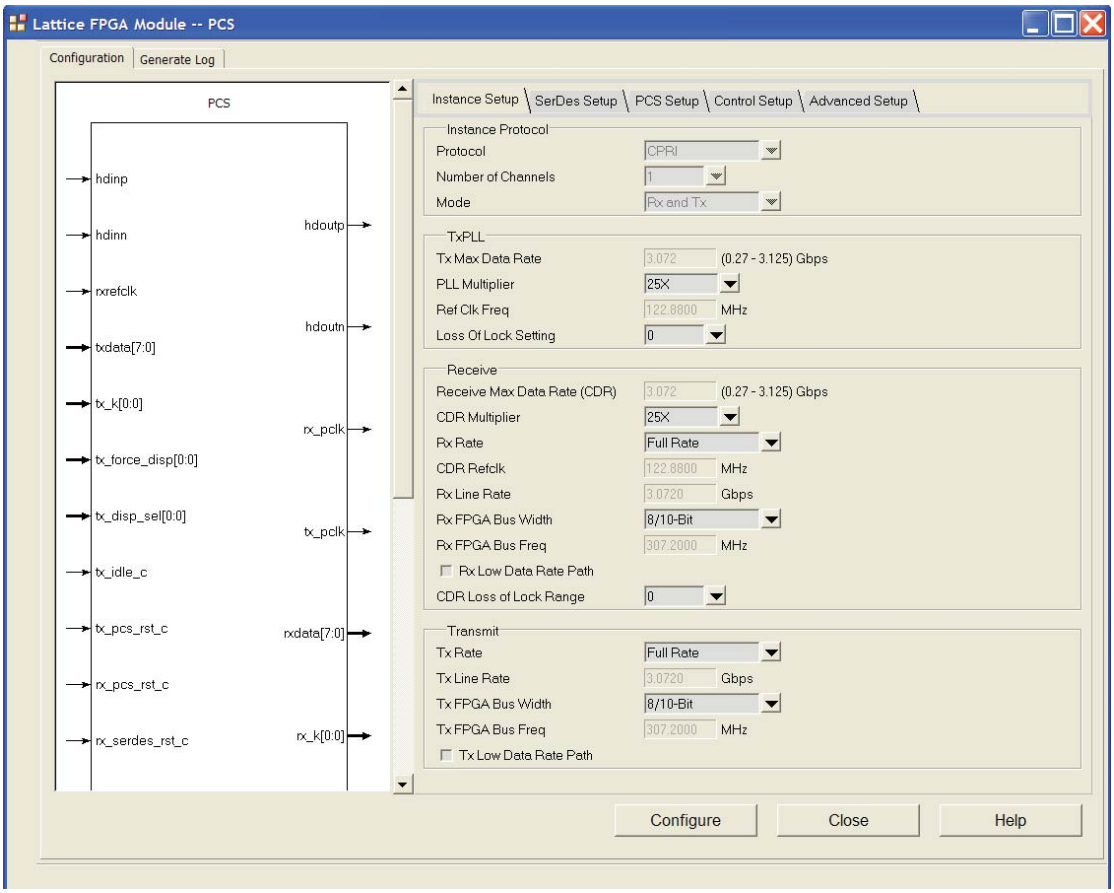


Clicking the **Advanced** button opens the CPRI PCS Advanced Configuration Dialog Box shown in Figure 3-3.

If only one PCS is used in the project, it is recommended to select the **Reset Sequence Select** option in Control Setup tab.

If you want to revise the SERDES electric character, change the parameters on the SerDes Setup tab. Refer to TN1261, ECP5 SERDES/PCS Usage Guide.

Figure 3-3. CPRI PCS Advanced Configuration Dialog Box



Generation Options

Design Entry

Lattice CPRI IP core only supports low latency character. The 'basic' option is not supported.

Ethernet Mode

This option allows the user to specify the Ethernet mode supported by the IP core, either Serial, Matched Rate MII or 100Mb/s Fixed Rate MII. See “Ethernet Interface” on page 19 for a detailed description of these different modes.

Eval Configuration

Synthesis Tool

This option specifies evaluation configuration synthesis tool support for Synplify.

Programmable Parameters

The configuration settings listed in Table 3-2 are controlled via user-specified input signals to the IP core.

Table 3-2. CPRI Parameters Controlled via Input Signals to the IP Core

Input Signal	Values	Function
lbr_en[1:0](for 3G) lbr_en[2:0](for 5G)	0, 1, 2, 3, 4	Selects the maximum line bit rate which the IP core will support: 0 – 614.4 Mbps maximum 1 – 1228.8 Mbps maximum 2, 3 – 2457.6 Mbps maximum 3 – 3072 Mbps in 3G version 4 - 4915.2 Mbps in 5G version
force_sm_standby	0, 1	A zero-to-one transition forces the startup state machine to the Standby state.
pcs_serdes_rate[1:0] (for 3G) pcs_serdes_rate[2:0] (for 5G)	0, 1, 2, 3, 4	Selects the line bit rate which the PCS/SERDES will support: 0 – 614.4 Mbps maximum 1 – 1228.8 Mbps maximum 2 – 2457.6 Mbps maximum 3 – 3072 Mbps in 3G version 4 - 4915.2 Mbps in 5G version
tx_eth_pointer[7:0]	0-63	Selects fast C&M pointer value
hdlc_240_en	0, 1	Enables 240 KHz as the maximum HDLC interface frequency
hdlc_480_en	0, 1	Enables 480 KHz as the maximum HDLC interface frequency
hdlc_960_en	0, 1	Enables 960 KHz as the maximum HDLC interface frequency
hdlc_1920_en	0, 1	Enables 1920 KHz as the maximum HDLC interface frequency
hdlc_2400_en	0, 1	Enables 2400 KHz as the maximum HDLC interface frequency
auto_cnt	0, 1	Enable master CPRI tx hfn and bfn updating. Default 1.
hyp_cnt_init	0-255	hfn used to update the control words or initialize the internal hfn counter. Default 0.
bfn_cnt_init	0-4095	bfn used to update the control words or initialize the internal bfn counter. Default 0.
tx_hyp_rst_en	0, 1	Enables tx_sync to reset tx_hyp_num
tx_bfn_rst_en	0, 1	Enables tx_sync to reset tx_bfn_num
test_md	0, 1	Speeds up timer to reduce test time: 0 – Normal 1 – Test
rec_md	0, 1	Sets core to REC or RE: 0 – RE 1 – REC