



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



30 W Digital Audio Amplifier with Integrated ADC

Digital Amplifier Features

- ◆ Fully Integrated Power MOSFETs
- ◆ No Heatsink Required
 - Programmable Power Foldback on Thermal Warning
 - High Efficiency
- ◆ > 100 dB Dynamic Range
- ◆ < 0.1% THD+N @ 1 W
- ◆ Configurable Outputs (10% THD+N)
 - 1 x 30 W into 4 Ω, Parallel Full-Bridge
 - 2 x 15 W into 8 Ω, Full-Bridge
 - 2 x 7 W into 4 Ω, Half-Bridge + 1 x 15 W into 8 Ω, Full-Bridge
- ◆ Built-In Protection with Error Reporting
 - Overcurrent/Undervoltage/Thermal Overload Shutdown
 - Thermal Warning Reporting
- ◆ PWM Popguard® for Half-Bridge Mode
- ◆ Click-Free Start-Up
- ◆ Programmable Channel Delay for System Noise & Radiated Emissions Management

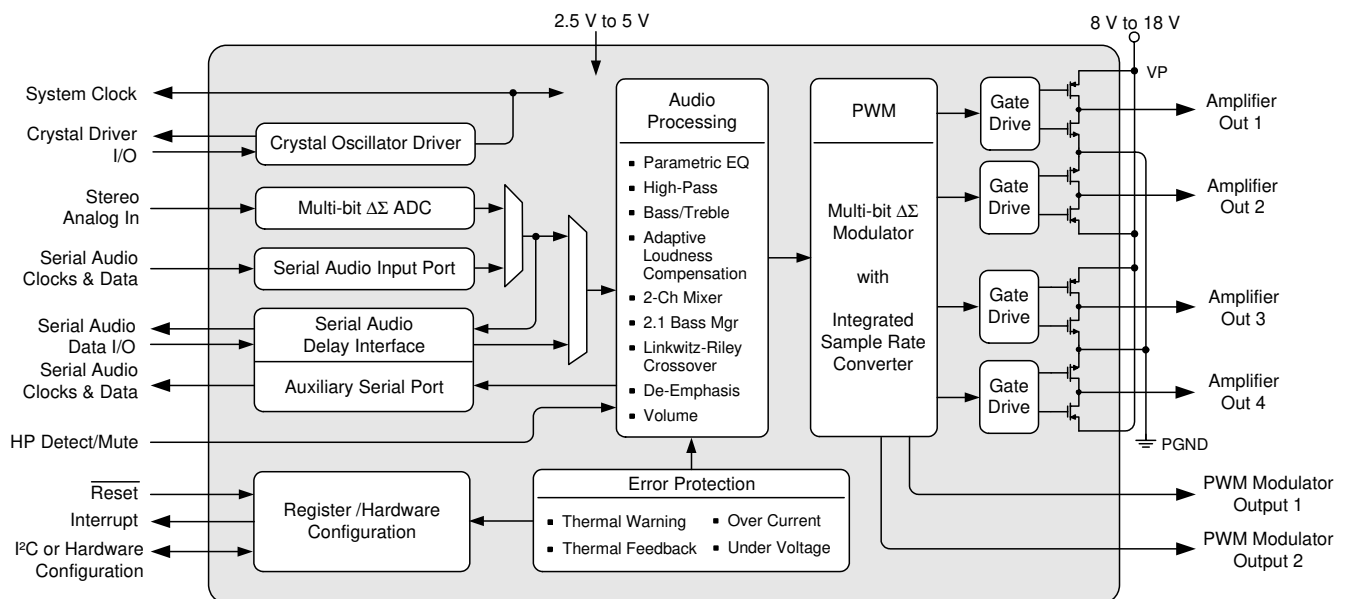
ADC Features

- ◆ Stereo, 24-bit, 48 kHz Conversion
- ◆ Multi-bit Architecture
- ◆ 95 dB Dynamic Range (A-wtd)
- ◆ -86 dB THD+N
- ◆ Supports 2 Vrms Input with Passive Components

System Features

- ◆ Asynchronous 2-Channel Digital Serial Port
- ◆ 32 kHz to 96 kHz Input Sample Rates
- ◆ Operation with On-Chip Oscillator Driver or Applied SYS_CLK at 18.432, 24.576 or 27.000 MHz
- ◆ Integrated Sample Rate Converter (SRC)
 - Eliminates Clock-Jitter Effects
 - Input Sample Rate Independent Operation
 - Simplifies System Integration
- ◆ Spread Spectrum PWM Modulation
 - Reduces EMI Radiated Energy
- ◆ Low Quiescent Current

(Features continued on page 2)



Preliminary Product Information

This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

Software Mode System Features

- ◆ Digital Audio Processing
 - 5 Programmable Parametric EQ Filters
 - Selectable High-Pass Filter
 - Bass/Treble Tone Control
 - Adaptive Loudness Compensation
 - 2-Channel Mixer
 - 2.1 Bass Management
 - 24 dB/octave Linkwitz-Riley Crossover Filters
 - De-emphasis Filter
- ◆ Selectable Serial Audio Interface Formats
 - Left-Justified up to 24-bit
 - I²S up to 24-bit
 - Right-Justified 16-, 18-, 20-, 24-bits
- ◆ Digital Serial Connection to Additional CS4525 or DACs for Subwoofer
- ◆ Digital Interface to External Lip-Sync Delay
- ◆ PWM Switch Rate Shifting Eliminates AM Frequency Interference
- ◆ Digital Volume Control with Soft ramp
 - +24 to -103 dB in 0.5 dB steps
- ◆ Programmable Peak Detect and Limiter
- ◆ 2-Channel Logic-Level PWM Output
 - Programmable Channel Mapping
 - Can Drive an External PWM Amplifier, Headphone Amplifier, or Line-Out Amplifier
 - Integrated Headphone Detection
- ◆ Flexible Power Output Configurations
- ◆ Thermal Foldback for Interruption-Free Power-Stage Protection
 - Supports Internal and External Power Stages
- ◆ Operation from On-Chip Oscillator Driver or Applied Systems Clock
- ◆ Supports I²C[®] Host Control Interface

Hardware Mode System Features

- ◆ 2-Channel Stereo Full-Bridge Power Outputs
- ◆ Analog and Digital Inputs
- ◆ I²S and Left-Justified Serial Input Formats
- ◆ Thermal Foldback for Interruption-Free Protection of Internal Power Stage
- ◆ Operation from Applied Systems Clock
- ◆ External Mute Input

Common Applications

- ◆ Integrated Digital TV's
- ◆ Flat Panel TV Monitors
- ◆ Computer/TV Monitors
- ◆ Mini/Micro Shelf Systems
- ◆ Digital Powered Speakers
- ◆ Portable Docking Stations
- ◆ Computer Desktop Audio

General Description

The CS4525 is a stereo analog or digital input PWM high efficiency Class D amplifier audio system with an integrated stereo analog-to-digital (A/D) converter. The stereo power amplifiers can deliver up to 15 W per channel into 8 Ω speakers from a small space-saving 48-pin QFN package. The PWM amplifier can achieve greater than 85% efficiency. The package is thermally enhanced for optimal heat dissipation which eliminates the need for a heatsink.

The power stage outputs can be configured as two full-bridge channels for 2 x 15 W operation, two half-bridge channels and one full-bridge channel for 2 x 7 W + 1 x 15 W operation, or one parallel full-bridge channel for 1 x 30 W operation. The CS4525 integrates on-chip over-current, under-voltage, and over-temperature protection and error reporting as well as a thermal warning indicator and programmable foldback of the output power to allow cooling.

The main digital serial port on the CS4525 can support asynchronous operation with the integrated on-chip sample rate converter (SRC) which eases system integration. The SRC allows for a fixed PWM switching frequency regardless of incoming sample rate as well as optimal clocking for the A/D modulators.

An on-chip oscillator driver eliminates the need for an external crystal oscillator circuit, reducing overall design cost and conserving circuit board space. The CS4525 automatically uses the on-chip oscillator driver in the absence of an applied master clock.

The CS4525 is available in a 48-pin QFN package in Commercial grade (-10° to +70° C). The CRD4525-Q1 4-layer, 1 oz. copper and CRD4525-D1 2-layer, 1 oz. copper customer reference designs are also available.

Please refer to [“Ordering Information” on page 97](#) for complete ordering information.

TABLE OF CONTENTS

1. PIN DESCRIPTIONS - SOFTWARE MODE	8
2. PIN DESCRIPTIONS - HARDWARE MODE	10
2.1 Digital I/O Pin Characteristics	12
3. TYPICAL CONNECTION DIAGRAMS	13
4. TYPICAL SYSTEM CONFIGURATION DIAGRAMS	15
5. CHARACTERISTICS AND SPECIFICATIONS	18
6. APPLICATIONS	26
6.1 Software Mode	26
6.1.1 System Clocking	26
6.1.1.1 SYS_CLK Input Clock Mode	26
6.1.1.2 Crystal Oscillator Mode	27
6.1.2 Power-Up and Power-Down	28
6.1.2.1 Recommended Power-Up Sequence	28
6.1.2.2 Recommended Power-Down Sequence	28
6.1.3 Input Source Selection	29
6.1.4 Digital Sound Processing	29
6.1.4.1 Pre-Scaler	30
6.1.4.2 Digital Signal Processing High-Pass Filter	30
6.1.4.3 Channel Mixer	30
6.1.4.4 De-Emphasis	31
6.1.4.5 Tone Control	31
6.1.4.6 Parametric EQ	33
6.1.4.7 Adaptive Loudness Compensation	34
6.1.4.8 Bass Management	35
6.1.4.9 Volume and Muting Control	36
6.1.4.10 Peak Signal Limiter	37
6.1.4.11 Thermal Limiter	39
6.1.4.12 Thermal Foldback	40
6.1.4.13 2-Way Crossover & Sensitivity Control	41
6.1.5 Auxiliary Serial Output	43
6.1.6 Serial Audio Delay & Warning Input Port	44
6.1.6.1 Serial Audio Delay Interface	44
6.1.6.2 External Warning Input Port	44
6.1.7 Powered PWM Outputs	45
6.1.7.1 Output Channel Configurations	45
6.1.7.2 PWM Popguard Transient Control	45
6.1.8 Logic-Level PWM Outputs	46
6.1.8.1 Recommended PWM_SIG Power-Up Sequence for an External PWM Amplifier	47
6.1.8.2 Recommended PWM_SIG Power-Down Sequence for an External PWM Amplifier	47
6.1.8.3 Recommended PWM_SIG Power-Up Sequence for Headphone & Line-Out	48
6.1.8.4 Recommended PWM_SIG Power-Down Sequence for Headphone & Line-Out	48
6.1.8.5 PWM_SIG Logic-Level Output Configurations	49
6.1.9 PWM Modulator Configuration	50
6.1.9.1 PWM Channel Delay	50
6.1.9.2 PWM AM Frequency Shift	51
6.1.10 Headphone Detection & Hardware Mute Input	51
6.1.11 Interrupt Reporting	53
6.1.12 Automatic Power Stage Shut-Down	53
6.2 Hardware Mode	54
6.2.1 System Clocking	54
6.2.2 Power-Up and Power-Down	54
6.2.2.1 Recommended Power-Up Sequence	54

6.2.2.2 Recommended Power-Down Sequence	55
6.2.3 Input Source Selection	55
6.2.4 PWM Channel Delay	55
6.2.5 Digital Signal Flow	56
6.2.5.1 High-Pass Filter	56
6.2.5.2 Mute Control	56
6.2.5.3 Warning and Error Reporting	56
6.2.6 Thermal Foldback	57
6.2.7 Automatic Power Stage Shut-Down	58
6.3 PWM Modulators and Sample Rate Converters	58
6.4 Output Filters	59
6.4.1 Half-Bridge Output Filter	59
6.4.2 Full-Bridge Output Filter (Stereo or Parallel)	60
6.5 Analog Inputs	61
6.6 Serial Audio Interfaces	62
6.6.1 I ² S Data Format	62
6.6.2 Left-Justified Data Format	62
6.6.3 Right-Justified Data Format	63
6.7 Integrated VD Regulator	63
6.8 I ² C Control Port Description and Timing	64
7. PCB LAYOUT CONSIDERATIONS	65
7.1 Power Supply, Grounding	65
7.2 QFN Thermal Pad	65
8. REGISTER QUICK REFERENCE	66
9. REGISTER DESCRIPTIONS	69
9.1 Clock Configuration (Address 01h)	69
9.1.1 SYS_CLK Output Enable (EnSysClk)	69
9.1.2 SYS_CLK Output Divider (DivSysClk)	69
9.1.3 Clock Frequency (ClkFreq[1:0])	69
9.1.4 HP_Detect/Mute Pin Active Logic Level (HP/MutePol)	70
9.1.5 HP_Detect/Mute Pin Mode (HP/Mute)	70
9.1.6 Modulator Phase Shifting (PhaseShift)	70
9.1.7 AM Frequency Shifting (FreqShift)	70
9.2 Input Configuration (Address 02h)	71
9.2.1 Input Source Selection (ADC/SP)	71
9.2.2 ADC High-Pass Filter Enable (EnAnHPF)	71
9.2.3 Serial Port Sample Rate (SPRate[1:0]) - Read Only	71
9.2.4 Input Serial Port Digital Interface Format (DIF [2:0])	71
9.3 AUX Port Configuration (Address 03h)	72
9.3.1 Enable Aux Serial Port (EnAuxPort)	72
9.3.2 Delay & Warning Port Configuration (DlyPortCfg[1:0])	72
9.3.3 Aux/Delay Serial Port Digital Interface Format (AuxI ² S/LJ)	72
9.3.4 Aux Serial Port Right Channel Data Select (RChDSel[1:0])	72
9.3.5 Aux Serial Port Left Channel Data Select (LChDSel[1:0])	73
9.4 Output Configuration (Address 04h)	73
9.4.1 Output Configuration (OutputCfg[1:0])	73
9.4.2 PWM Signals Output Data Select (PWMDSel[1:0])	73
9.4.3 Channel Delay Settings (OutputDly[3:0])	73
9.5 Foldback and Ramp Configuration (Address 05h)	74
9.5.1 Select VP Level (SelectVP)	74
9.5.2 Enable Thermal Foldback (EnTherm)	74
9.5.3 Lock Foldback Adjust (LockAdj)	74
9.5.4 Foldback Attack Delay (AttackDly[1:0])	75
9.5.5 Enable Foldback Floor (EnFloor)	75

9.5.6 Ramp Speed (RmpSpd[1:0])	75
9.6 Mixer / Pre-Scale Configuration (Address 06h)	75
9.6.1 Pre-Scale Attenuation (PreScale[2:0])	75
9.6.2 Right Channel Mixer (RChMix[1:0])	76
9.6.3 Left Channel Mixer (LChMix[1:0])	76
9.7 Tone Configuration (Address 07h)	76
9.7.1 De-Emphasis Control (DeEmph)	76
9.7.2 Adaptive Loudness Compensation Control (Loudness)	76
9.7.3 Digital Signal Processing High-Pass Filter (EnDigHPF)	77
9.7.4 Treble Corner Frequency (TrebFc[1:0])	77
9.7.5 Bass Corner Frequency (BassFc[1:0])	77
9.7.6 Tone Control Enable (EnToneCtrl)	77
9.8 Tone Control (Address 08h)	78
9.8.1 Treble Gain Level (Treb[3:0])	78
9.8.2 Bass Gain Level (Bass[3:0])	78
9.9 2.1 Bass Manager/Parametric EQ Control (Address 09h)	78
9.9.1 Freeze Controls (Freeze)	78
9.9.2 Hi-Z PWM_SIG Outputs (HiZPSig)	79
9.9.3 Bass Cross-Over Frequency (BassMgr[2:0])	79
9.9.4 Enable Channel B Parametric EQ (EnChBPPEq)	79
9.9.5 Enable Channel A Parametric EQ (EnChAPEq)	79
9.10 Volume and 2-Way Cross-Over Configuration (Address 55h)	80
9.10.1 Soft Ramp and Zero Cross Control (SZCMode[1:0])	80
9.10.2 Enable 50% Duty Cycle for Mute Condition (Mute50/50)	80
9.10.3 Auto-Mute (AutoMute)	80
9.10.4 Enable 2-Way Crossover (En2Way)	81
9.10.5 2-Way Cross-Over Frequency (2WayFreq[2:0])	81
9.11 Channel A & B: 2-Way Sensitivity Control (Address 56h)	81
9.11.1 Channel A and Channel B Low-Pass Sensitivity Adjust (LowPass[3:0])	81
9.11.2 Channel A and Channel B High-Pass Sensitivity Adjust (HighPass[3:0])	82
9.12 Master Volume Control (Address 57h)	82
9.12.1 Master Volume Control (MVol[7:0])	82
9.13 Channel A and B Volume Control (Address 58h & 59h)	83
9.13.1 Channel X Volume Control (ChXVol[7:0])	83
9.14 Sub Channel Volume Control (Address 5Ah)	83
9.14.1 Sub Channel Volume Control (SubVol[7:0])	83
9.15 Mute/Invert Control (Address 5Bh)	84
9.15.1 ADC Invert Signal Polarity (InvADC)	84
9.15.2 Invert Channel PWM Signal Polarity (InvChX)	84
9.15.3 Invert Sub PWM Signal Polarity (InvSub)	84
9.15.4 ADC Channel Mute (MuteADC)	84
9.15.5 Independent Channel A & B Mute (MuteChX)	84
9.15.6 Sub Channel Mute (MuteSub)	85
9.16 Limiter Configuration 1 (Address 5Ch)	85
9.16.1 Maximum Threshold (Max[2:0])	85
9.16.2 Minimum Threshold (Min[2:0])	85
9.16.3 Peak Signal Limit All Channels (LimitAll)	86
9.16.4 Peak Detect and Limiter Enable (EnLimiter)	86
9.17 Limiter Configuration 2 (Address 5Dh)	87
9.17.1 Limiter Release Rate (RRate[5:0])	87
9.18 Limiter Configuration 3 (Address 5Eh)	87
9.18.1 Enable Thermal Limiter (EnThLim)	87
9.18.2 Limiter Attack Rate (ARate[5:0])	87
9.19 Power Control (Address 5Fh)	88

9.19.1 Automatic Power Stage Retry (AutoRetry)	88
9.19.2 Enable Over-Current Protection (EnOCProt)	88
9.19.3 Select VD Level (SelectVD)	88
9.19.4 Power Down ADC (PDnADC)	88
9.19.5 Power Down PWM Power Output X (PDnOutX)	88
9.19.6 Power Down (PDnAll)	89
9.20 Interrupt (Address 60h)	89
9.20.1 SRC Lock State Transition Interrupt (SRCLock)	89
9.20.2 ADC Overflow Interrupt (ADCOvfl)	90
9.20.3 Channel Overflow Interrupt (ChOvfl)	90
9.20.4 Amplifier Error Interrupt Bit (AmpErr)	90
9.20.5 Mask for SRC State (SRCLockM)	91
9.20.6 Mask for ADC Overflow (ADCOvflM)	91
9.20.7 Mask for Channel X and Sub Overflow (ChOvflM)	91
9.20.8 Mask for Amplifier Error (AmpErrM)	92
9.21 Interrupt Status (Address 61h) - Read Only	92
9.21.1 SRC State Transition (SRCLockSt)	92
9.21.2 ADC Overflow (ADCOvflSt)	92
9.21.3 Sub Overflow (SubOvflSt)	92
9.21.4 Channel X Overflow (ChXOvflSt)	93
9.21.5 Ramp-Up Cycle Complete (RampDone)	93
9.22 Amplifier Error Status (Address 62h) - Read Only	93
9.22.1 Over-Current Detected On Channel X (OverCurrX)	93
9.22.2 External Amplifier State (ExtAmpSt)	93
9.22.3 Under Voltage / Thermal Error State (UVTE[1:0])	94
9.23 Device I.D. and Revision (Address 63h) - Read Only	94
9.23.1 Device Identification (DeviceID[4:0])	94
9.23.2 Device Revision (RevID[2:0])	94
10. PARAMETER DEFINITIONS	95
11. REFERENCES	95
12. PACKAGE DIMENSIONS	96
13. THERMAL CHARACTERISTICS	97
13.1 Thermal Flag	97
14. ORDERING INFORMATION	97
15. REVISION HISTORY	98

LIST OF FIGURES

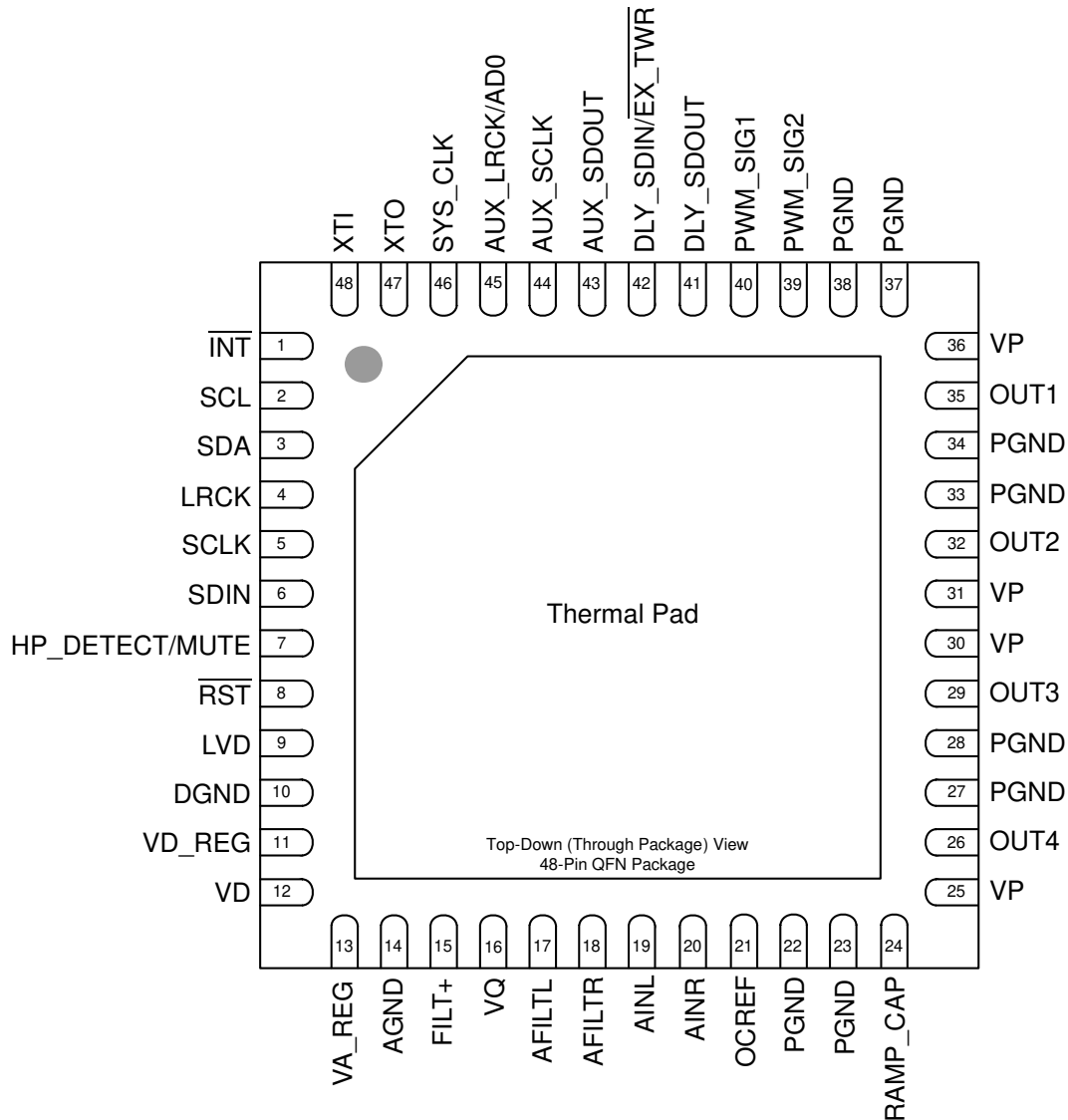
Figure 1. Typical Connection Diagram - Software Mode	13
Figure 2. Typical Connection Diagram - Hardware Mode	14
Figure 3. Typical System Configuration 1	15
Figure 4. Typical System Configuration 2	15
Figure 5. Typical System Configuration 3	16
Figure 6. Typical System Configuration 4	17
Figure 7. Serial Audio Input Port Timing	21
Figure 8. AUX Serial Port Interface Master Mode Timing	22
Figure 9. SYS_CLK Timing from Reset	23
Figure 10. PWM_SIGX Timing	23
Figure 11. Control Port Timing - I ² C	24
Figure 12. Typical SYS_CLK Input Clocking Configuration	26
Figure 13. Typical Crystal Oscillator Clocking Configuration	27
Figure 14. Digital Signal Flow	29
Figure 15. De-Emphasis Filter	31
Figure 16. Bi-Quad Filter Architecture	33

Figure 17. Peak Signal Detection & Limiting	37
Figure 18. Foldback Process	40
Figure 19. Popguard Connection Diagram	46
Figure 20. 2-Channel Full-Bridge PWM Output Delay	50
Figure 21. 3-Channel PWM Output Delay	50
Figure 22. Typical SYS_CLK Input Clocking Configuration	54
Figure 23. Hardware Mode PWM Output Delay	55
Figure 24. Hardware Mode Digital Signal Flow	56
Figure 25. Foldback Process	57
Figure 26. Output Filter - Half-Bridge	59
Figure 27. Output Filter - Full-Bridge	60
Figure 28. Recommended Unity Gain Input Filter	61
Figure 29. Recommended 2 V _{RMS} Input Filter	61
Figure 30. I ² S Serial Audio Formats	62
Figure 31. Left-Justified Serial Audio Formats	62
Figure 32. Right-Justified Serial Audio Formats	63
Figure 33. Control Port Timing, I ² C Write	64
Figure 34. Control Port Timing, I ² C Read	64

LIST OF TABLES

Table 1. I/O Power Rails	12
Table 2. Bass Shelving Filter Corner Frequencies	31
Table 3. Treble Shelving Filter Corner Frequencies	32
Table 4. Bass Management Cross-Over Frequencies	35
Table 5. 2-Way Cross-Over Frequencies	41
Table 6. Auxiliary Serial Port Data Output	43
Table 7. Nominal Switching Frequencies of the Auxiliary Serial Output	43
Table 8. PWM Power Output Configurations	45
Table 9. Typical Ramp Times for Various VP Voltages	46
Table 10. PWM Logic-Level Output Configurations	49
Table 11. PWM Output Switching Rates and Quantization Levels	51
Table 12. Output of PWM_SIG Outputs	52
Table 13. SYS_CLOCK Frequency Selection	54
Table 14. Input Source Selection	55
Table 15. Serial Audio Interface Format Selection	55
Table 16. Thermal Foldback Enable Selection	57
Table 17. PWM Output Switching Rates and Quantization Levels	58
Table 18. Low-Pass Filter Components - Half-Bridge	59
Table 19. DC-Blocking Capacitors Values - Half-Bridge	59
Table 20. Low-Pass Filter Components - Full-Bridge	60
Table 21. Power Supply Configuration and Settings	63

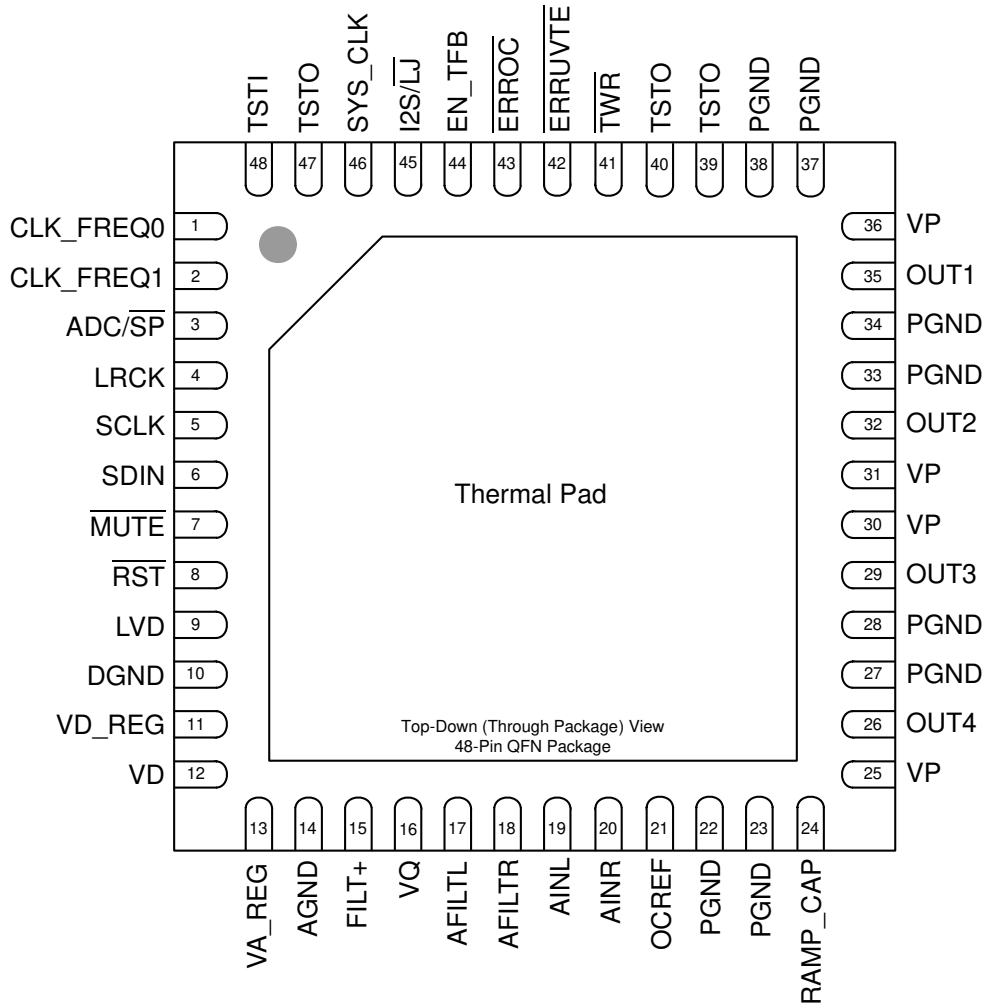
1. PIN DESCRIPTIONS - SOFTWARE MODE



Pin Name	Pin #	Pin Description
$\overline{\text{INT}}$	1	Interrupt (Output) - Indicates an interrupt condition has occurred.
SCL	2	Serial Control Port Clock (Input) - Serial clock for the I ² C control port.
SDA	3	Serial Control Data (Input/Output) - Bi-directional data I/O for the I ² C control port.
LRCK	4	Left Right Clock (Input) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	5	Serial Clock (Input) - Serial bit clock for the serial audio interface.
SDIN	6	Serial Audio Data Input (Input) - Input for two's complement serial audio data.
HP_DETECT/ MUTE	7	Headphone Detect / Mute (Input) - Headphone detection or mute input signal as configured via the I ² C control port.
$\overline{\text{RST}}$	8	Reset (Input) - The device enters a low power mode and all internal registers are reset to their default settings when this pin is driven low.

LVD	9	VD Voltage Level Indicator (Input) - Identifies the voltage level attached to VD. When applying 5.0 V to VD, LVD must be connected to VD. When applying 2.5 V or 3.3 V to VD, LVD must be DGND.
DGND	10	Digital Ground (Input) - Ground for the internal logic and digital I/O.
VD_REG	11	Core Logic Power (Output) - Internally generated low voltage power supply for digital logic.
VD	12	Power (Input) - Positive power supply for the internal regulators and digital I/O.
VA_REG	13	Analog Power (Output) - Internally generated positive power for the analog section and I/O.
AGND	14	Analog Ground (Input) - Ground reference for the internal analog section and I/O.
FILT+	15	Positive Voltage Reference (Output) - Positive reference voltage for the internal ADC sampling circuits.
VQ	16	Common Mode Voltage (Output) - Filter connection for internal common mode voltage.
AFILT	17	Antialias Filter Connection (Output) - Antialias filter connection for ADC inputs.
AFILTR	18	
AINL	19	Analog Input (Input) - The full-scale input level is specified in the ADC Analog Characteristics specification table.
AINR	20	
OCREF	21	Over Current Reference Setting (Input) - Sets the reference for over current detection.
PGND	22,23 27,28 33,34 37,38	Power Ground (Input) - Ground for the individual output power half-bridge devices.
RAMP_CAP	24	Output Ramp Capacitor (Input) - Used by the PWM Popguard Transient Control to suppress the initial pop in half-bridge-configured outputs.
VP	25,30, 31,36	High Voltage Power (Input) - High voltage power supply for the individual half-bridge devices.
OUT4	26	PWM Output (Output) - Amplified PWM power outputs.
OUT3	29	
OUT2	32	
OUT1	35	
PWM_SIG2	39	Logic Level PWM Output (Output) - Logic Level PWM switching signals.
PWM_SIG1	40	
DLY_SDOOUT	41	Delay Serial Audio Data Out (Output) - Output for two's complement serial audio data.
DLY_SDIN/ EX_TWR	42	Delay Serial Audio Data Input (Input) - Input for two's complement serial audio data. External Thermal Warning (Input) - Input for an external thermal warning signal. Configurable via the I ² C control port.
AUX_SDOOUT	43	Auxiliary Port Serial Audio Data Out (Output) - Output for two's complement auxiliary port serial data.
AUX_SCLK	44	Auxiliary Port Serial Clock (Output) - Serial clock for the auxiliary port serial interface.
AUX_LRCK/ AD0	45	Auxiliary Port Left Right Clock (Output) - Determines which channel, Left or Right, is currently active on the serial audio data line. AD0 (Input) - Sets the LSB of the I ² C device address. Sensed on the release of $\overline{\text{RST}}$.
SYS_CLK	46	System Clock (Input/Output) - Clock source for the internal logic, processing, and modulators. This pin should be connected to through a 10k Ω to ground when unused.
XTO	47	Crystal Oscillator Output (Output) - Crystal oscillator driver output.
XTI	48	Crystal Oscillator Input (Input) - Crystal oscillator driver input.
Thermal Pad	-	Thermal Pad - Thermal relief pad for optimized heat dissipation. See "QFN Thermal Pad" on page 65 for more information.

2. PIN DESCRIPTIONS - HARDWARE MODE



Pin Name	Pin #	Pin Description
CLK_FREQ0	1	Clock Frequency (Input) - Determines the frequency of the clock expected to be driven into the SYS_CLK pin.
CLK_FREQ1	2	
ADC/SP	3	ADC/Serial Port (Input) - Selects between the Analog to Digital Converter and the Serial Port for audio input. Selects the ADC when high or the serial port when low.
LRCK	4	Left Right Clock (Input) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	5	Serial Clock (Input) - Serial bit clock for the serial audio interface.
SDIN	6	Serial Audio Data Input (Input) - Input for two's complement serial audio data.
MUTE	7	Mute (Input) - The PWM outputs will output silence as a 50% duty cycle signal when this pin is driven low.
RST	8	Reset (Input) - The device enters a low power mode and all internal registers are reset to their default settings when this pin is driven low.

LVD	9	VD Voltage Level Indicator (Input) - Identifies the voltage level attached to VD. When applying 5.0 V to VD, LVD must be connected to VD. When applying 2.5 V or 3.3 V to VD, LVD must be connected to DGND.
DGND	10	Digital Ground (Input) - Ground for the internal logic and I/O.
VD_REG	11	Core Logic Power (Output) - Internally generated low voltage power supply for digital logic.
VD	12	Digital Power (Input) - Positive power supply for the internal regulators and digital I/O.
VA_REG	13	Analog Power (Output) - Internally generated positive power for the analog section and I/O.
AGND	14	Analog Ground (Input) - Ground reference for the internal analog section and I/O.
FILT+	15	Positive Voltage Reference (Output) - Positive reference voltage for the internal ADC sampling circuits.
VQ	16	Common Mode Voltage (Output) - Filter connection for internal common mode voltage.
AFILT	17	Antialias Filter Connection (Output) - Antialias filter connection for ADC inputs.
AFILTR	18	
AINL	19	Analog Input (Input) - The full-scale input level is specified in the ADC Analog Characteristics specification table.
AINR	20	
OCREF	21	Over Current Reference Setting (Input) - Sets the reference for over current detection.
PGND	22,23 27,28 33,34 37,38	Power Ground (Input) - Ground for the individual output power half-bridge devices.
RAMP_CAP	24	Output Ramp Capacitor (Input) - This pin should be connected directly to VP in hardware mode.
VP	25,30, 31,36	High Voltage Power (Input) - High voltage power supply for the individual half-bridge devices.
OUT4	26	PWM Output (Output) - Amplified PWM power outputs.
OUT3	29	
OUT2	32	
OUT1	35	
TSTO	39 40	Test Output (Output) - These pins are outputs used for the Logic Level PWM switching signals available only in software mode. They must be left unconnected for hardware mode operation.
TWR	41	Thermal Warning Output (Output) - Thermal warning output.
$\overline{\text{ERRUVTE}}$	42	Thermal and Undervoltage Error Output (Output) - Error flag for thermal shutdown and undervoltage.
$\overline{\text{ERROC}}$	43	Overcurrent Error Output (Output) - Overcurrent error flag.
EN_TFB	44	Enable Thermal Feedback (Input) - Enables the thermal foldback feature when high.
I2S/LJ	45	I²S/Left Justified (Input) - Selects between I ² S and Left-Justified data format for the serial input port. Selects I ² S when high and LJ when low.
SYS_CLK	46	System Clock (Input/Output) - Clock source for the delta-sigma modulators.
TSTO	47	Test Output (Output) - This pin is an output used for the crystal oscillator driver available only in software mode. It must be left unconnected for normal hardware mode operation.
TSTI	48	Test Input (Input) - This pin is an input used for the crystal oscillator driver available only in software mode. It must be tied to digital ground for normal hardware mode operation.
Thermal Pad	-	Thermal Pad - Thermal relief pad for optimized heat dissipation. See “QFN Thermal Pad” on page 65 for more information.

2.1 Digital I/O Pin Characteristics

The logic level for each input is set by its corresponding power supply and should not exceed the maximum ratings.

Power Supply	Pin Number	Pin Name	I/O	Driver	Receiver	
Software Mode						
VD	1	INT	Output	2.5 V-5.0 V, Open Drain		
	2	SCL	Input	-	2.5 V-5.0 V, with Hysteresis	
	3	SDA	Input/Output	2.5 V-5.0 V, Open Drain	2.5 V-5.0 V, with Hysteresis	
	7	HP_DETECT	Input	-	2.5 V-5.0 V	
		MUTE	Input	-	2.5 V-5.0 V	
	41	DLY_SDOOUT	Output	2.5 V-5.0 V, CMOS	-	
	42	DLY_SDIN	Input	-	2.5 V-5.0 V	
		EX_TWR	Input	-	2.5 V-5.0 V	
VD	43	AUX_SDOOUT	Output	2.5 V-5.0 V, CMOS	-	
	44	AUX_SCLK	Output	2.5 V-5.0 V, CMOS	-	
	45	AUX_LRCK	Output	2.5 V-5.0 V, CMOS	-	
	VD_REG	39	PWM_SIG2	Output	2.5 V, CMOS	-
		40	PWM_SIG1	Output	2.5 V, CMOS	-
	Hardware Mode					
	VD	1	SEL_OSC0	Input	-	2.5 V-5.0 V
2		SEL_OSC1	Input	-	2.5 V-5.0 V	
3		ADC/SP	Input	-	2.5 V-5.0 V	
7		MUTE	Input	-	2.5 V-5.0 V	
41		TWR	Output	2.5 V-5.0 V, Open Drain	-	
42		ERRUVTE	Output	2.5 V-5.0 V, Open Drain	-	
43		ERROC	Output	2.5 V-5.0 V, Open Drain	-	
44		EN_TFB	Input	-	2.5 V-5.0 V	
	45	I ² S/LJ	Input	-	2.5 V-5.0 V	
All Modes						
VD	4	LRCK	Input	-	2.5 V-5.0 V	
	5	SCLK	Input	-	2.5 V-5.0 V	
	6	SDIN	Input	-	2.5 V-5.0 V	
	8	RST	Input	-	2.5 V-5.0 V	
	9	LVD	Input	-	2.5 V-5.0 V	
	46	SYS_CLK	Input/Output	2.5 V-5.0 V, CMOS	2.5 V-5.0 V	
VP	26	OUT4	Output	8.0 V-18.0 V Power MOSFET	-	
	29	OUT3	Output	8.0 V-18.0 V Power MOSFET	-	
	32	OUT2	Output	8.0 V-18.0 V Power MOSFET	-	
	35	OUT1	Output	8.0 V-18.0 V Power MOSFET	-	

Table 1. I/O Power Rails

3. TYPICAL CONNECTION DIAGRAMS

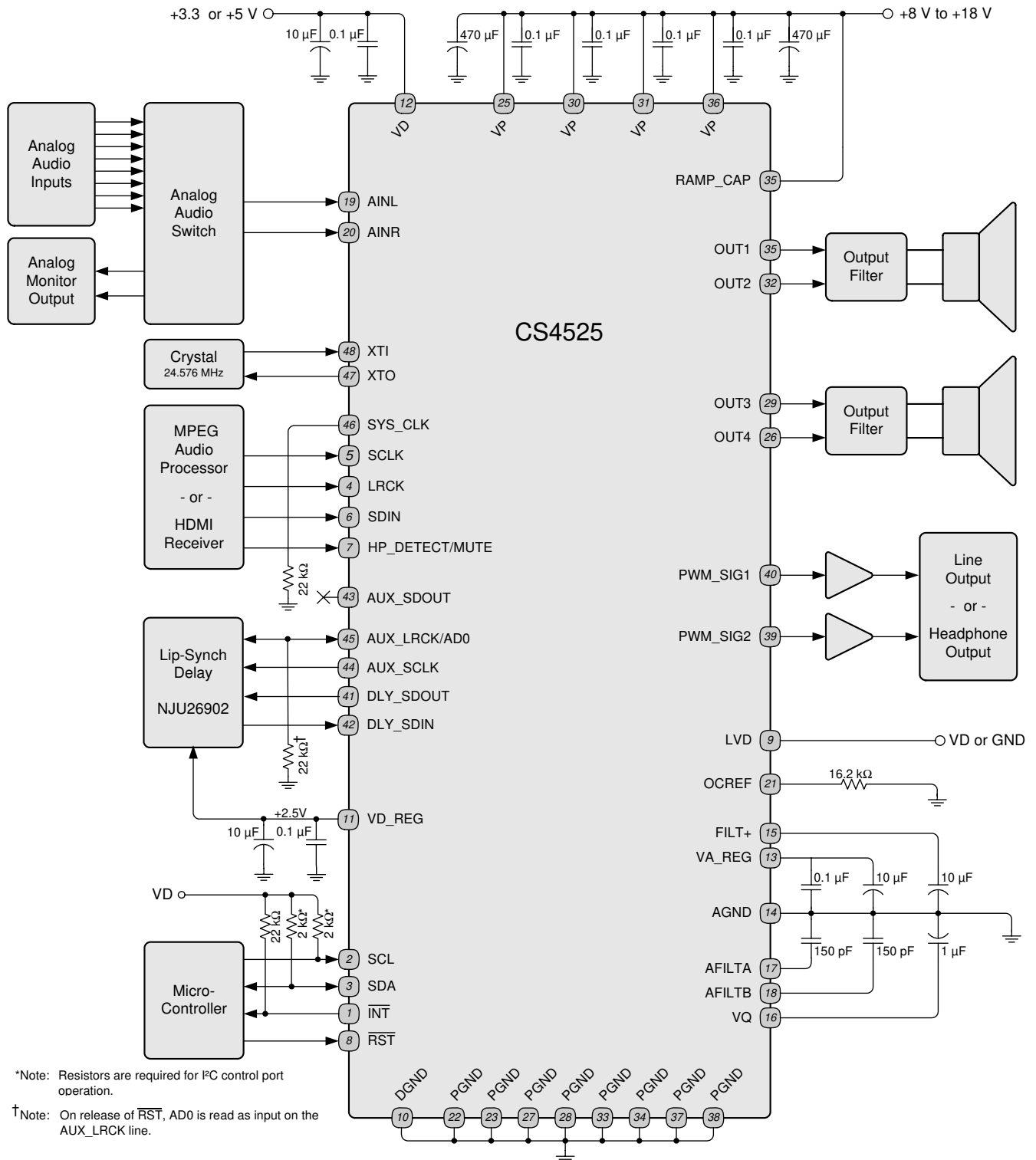
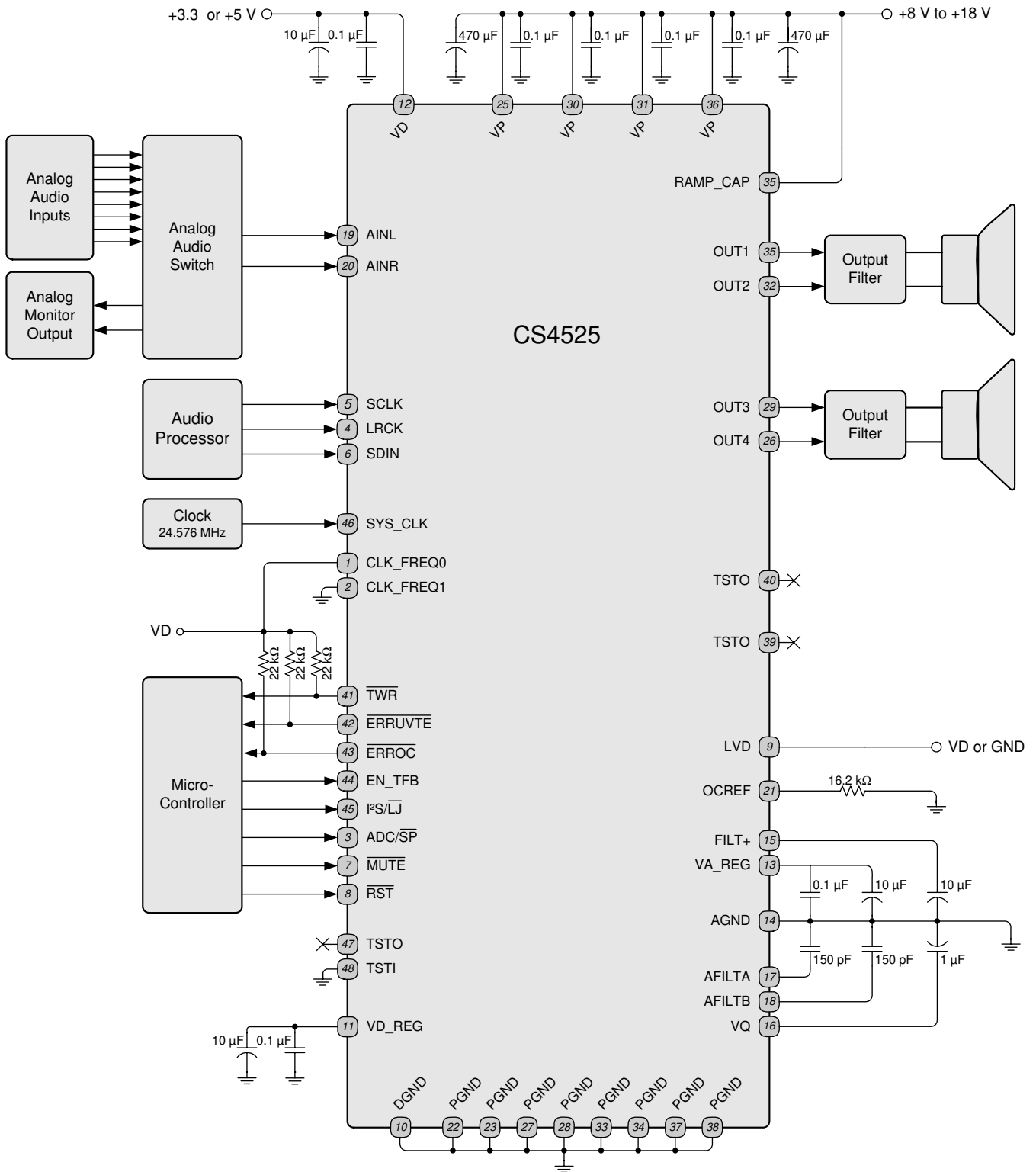


Figure 1. Typical Connection Diagram - Software Mode


Figure 2. Typical Connection Diagram - Hardware Mode

4. TYPICAL SYSTEM CONFIGURATION DIAGRAMS

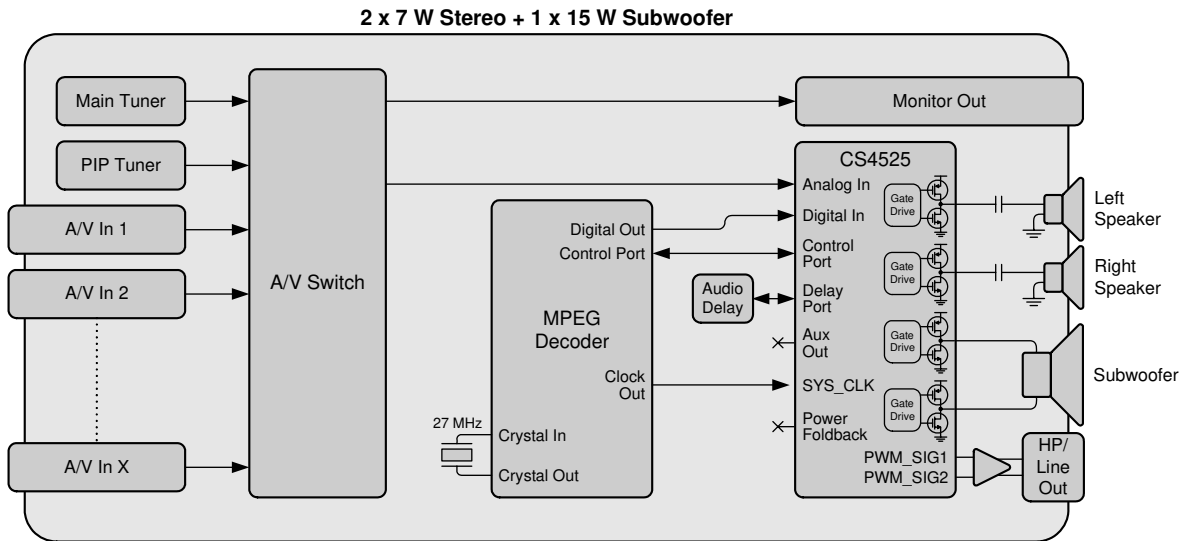


Figure 3. Typical System Configuration 1

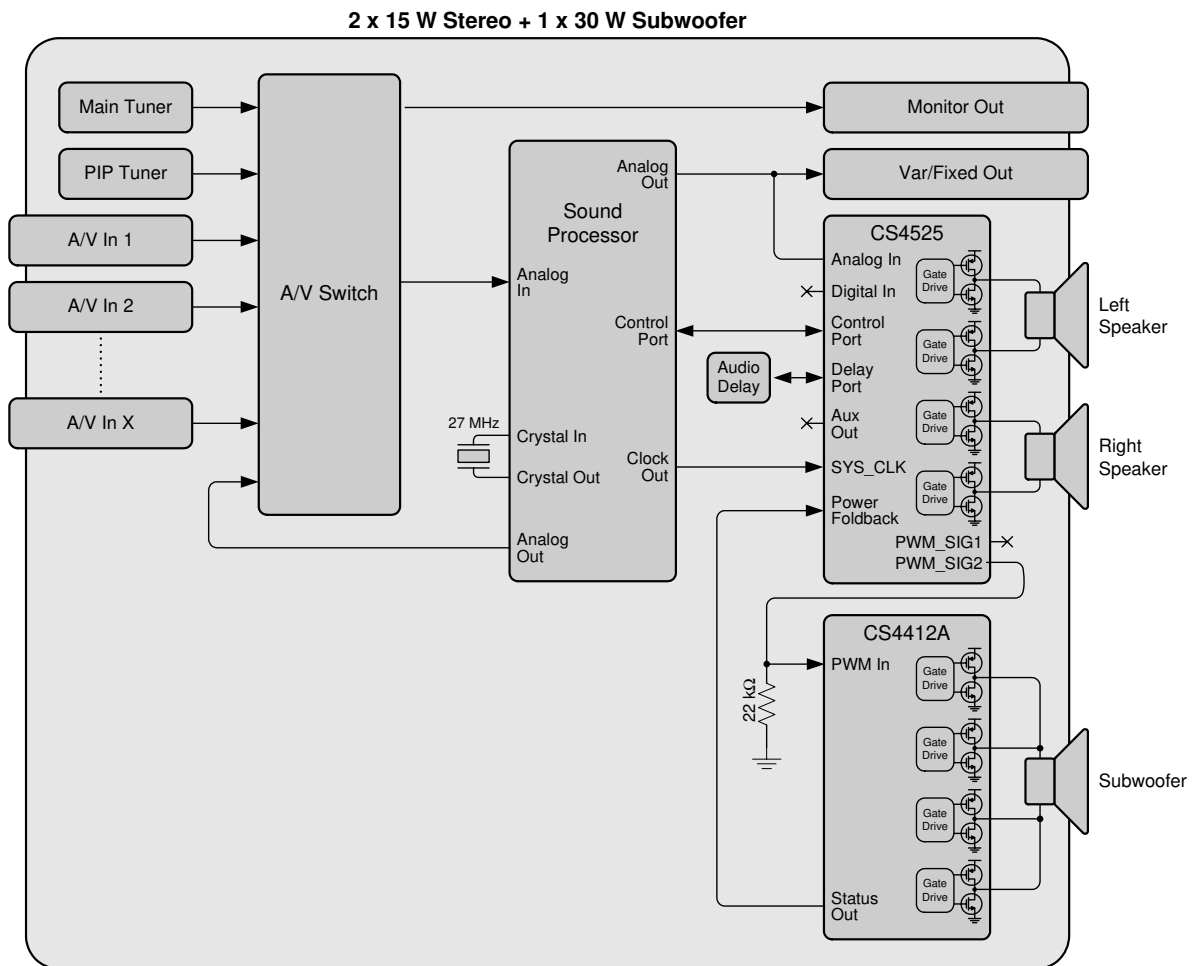


Figure 4. Typical System Configuration 2

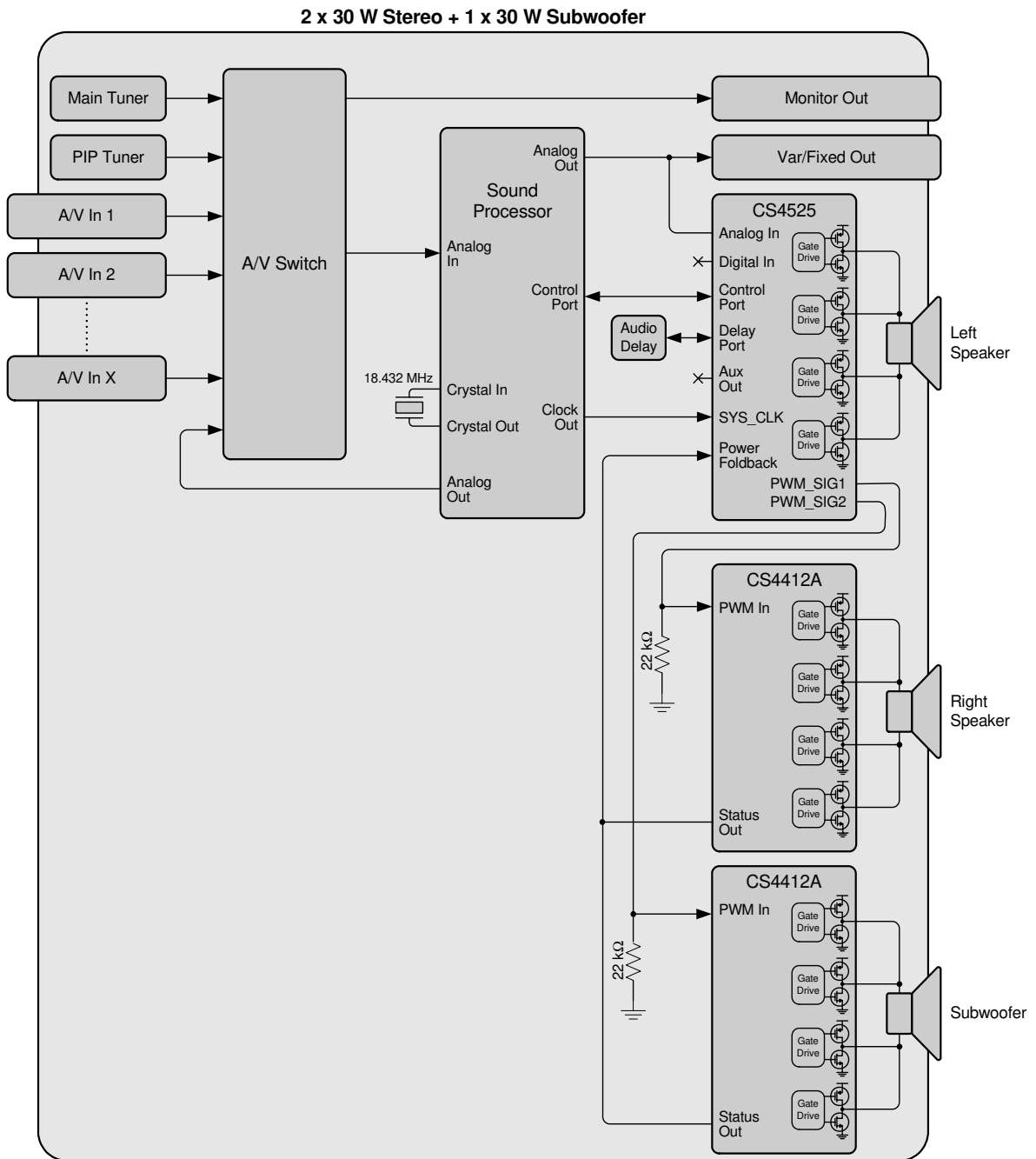


Figure 5. Typical System Configuration 3

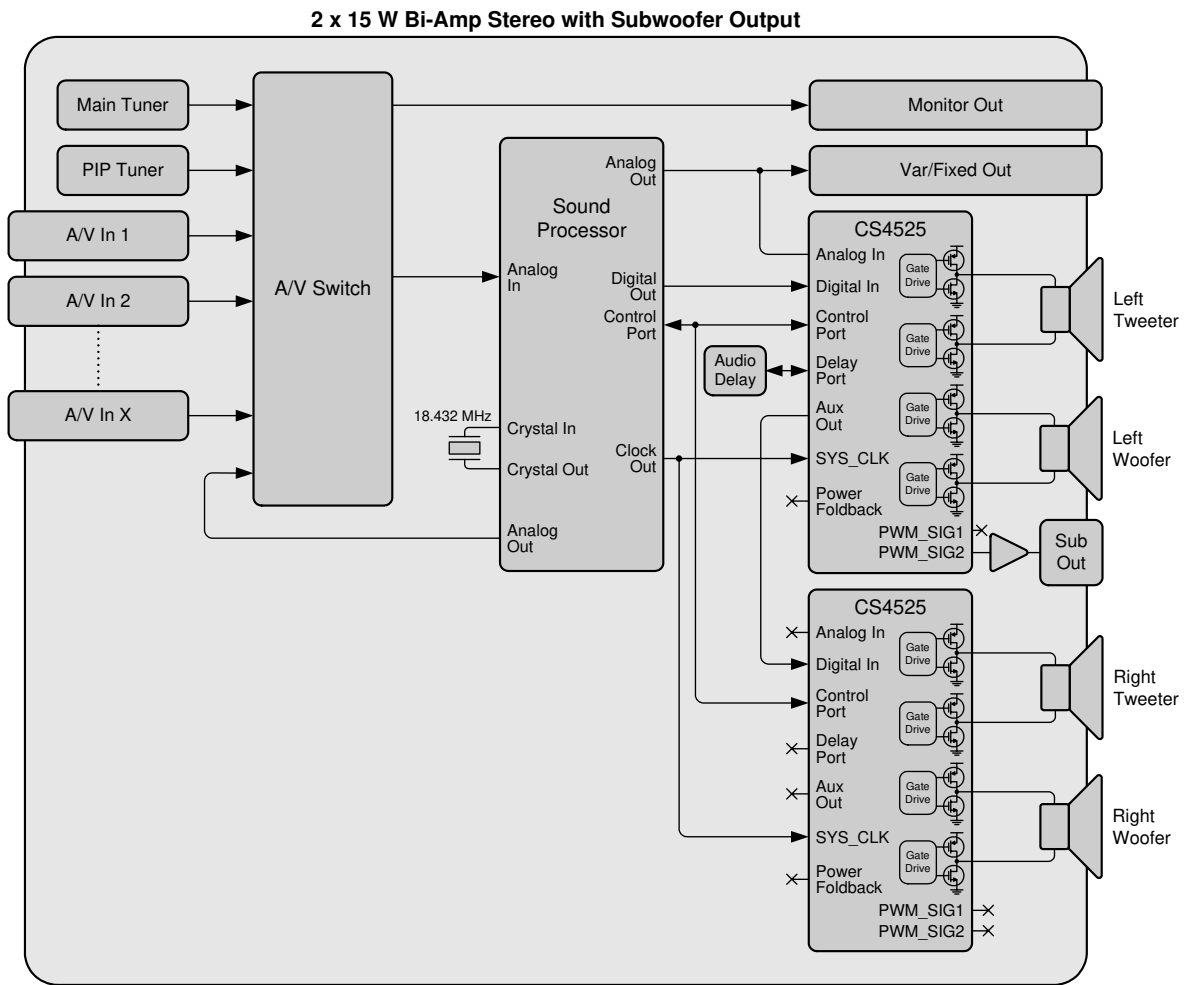


Figure 6. Typical System Configuration 4

5. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

AGND = DGND = PGND = 0 V; all voltages with respect to ground.

Parameters	Symbol	Min	Nom	Max	Units
DC Power Supply					
Digital and Analog Core (Note 1)	VD	2.375	2.5	2.625	V
	VD	3.135	3.3	3.465	V
	VD	4.75	5.0	5.25	V
Amplifier Outputs	VP	8.0	-	18.0	V
Temperature					
Ambient Temperature Commercial	T _A	-10	-	+70	°C
Junction Temperature	T _J	-10	-	+125	°C

Notes: 1. For VD = 2.5 V, VA_REG and VD_REG must be connected to VD. See [section 6.7 on page 63](#) for details.

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = PGND = 0 V; all voltages with respect to ground.

Parameters	Symbol	Min	Max	Units
DC Power Supply				
Power Stage Outputs Switching and Under Load	VP	-0.3	19.8	V
Power Stage No Output Switching	VP	-0.3	23.0	V
Digital and Analog Core	VD	-0.3	6.0	V
Inputs				
Input Current (Note 2)	I _{in}	-	±10	mA
Analog Input Voltage (Note 3)	V _{INA}	AGND - 0.7	VA_REG + 0.7	V
Digital Input Voltage (Note 3)	V _{IND}	-0.3	VD + 0.4	V
Temperature				
Ambient Operating Temperature - Power Applied Commercial	T _A	-20	+85	°C
Storage Temperature	T _{stg}	-65	+150	°C

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): AGND = DGND = PGND = 0 V; All voltages with respect to ground; $T_A = 25^\circ\text{C}$; $V_D = 3.3\text{ V}$; Input Signal: 1 kHz sine wave through the recommended passive input filter shown in [Figure 28 on page 61](#); Capacitor values connected to AFILTA, AFILTB, FILT+, VQ, VD_REG, and VA_REG as shown in [Figure 1 on page 13](#); Sample Frequency = 48 kHz; 10 Hz to 20 kHz Measurement Bandwidth; Power outputs in power-down state (PDnOut1 = 1, PDnOut2 = 1, PDnOut3/4 = 1).

Parameter		Min	Typ	Max	Unit
Dynamic Range (Note 4)	A-weighted	90	95	-	dB
	unweighted	87	92	-	dB
Total Harmonic Distortion + Noise	-1 dB	-	-86	-77	dB
	-20 dB	-	-72	-	dB
	-60 dB	-	-32	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.05	-	dB
Gain Drift		-	± 100	-	ppm/ $^\circ\text{C}$
Interchannel Isolation		-	90	-	dB
Full-scale Input Voltage	$V_D = 2.5\text{ V}$ (Note 5)	$0.786 \cdot V_D$	$0.827 \cdot V_D$	$0.868 \cdot V_D$	V _{pp}
	$V_D = 3.3\text{ V}$	$0.590 \cdot V_D$	$0.621 \cdot V_D$	$0.652 \cdot V_D$	V _{pp}
	$V_D = 5.0\text{ V}$	$0.398 \cdot V_D$	$0.419 \cdot V_D$	$0.440 \cdot V_D$	V _{pp}
Input Impedance	(Note 6)	40	-	-	k Ω

- Notes:**
4. Referred to the typical full-scale voltage
 5. For $V_D = 2.5\text{ V}$, VA_REG and VD_REG must be connected to VD. See [section 6.7 on page 63](#) for details.
 6. Measured between AINx and AGND.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter		Min	Typ	Max	Unit
Passband (Frequency Response) (Note 7)	to -0.1 dB corner	0	-	0.4948	F _s
Passband Ripple		-0.09	-	0	dB
Stopband	(Note 7)	0.6677	-	-	F _s
Stopband Attenuation		48.4	-	-	dB
Total Group Delay		-	$2.7/F_s$	-	s
High-Pass Filter Characteristics					
Frequency Response	-3.0 dB	-	3.7	-	Hz
	-0.13 dB	-	24.2	-	Hz
Phase Deviation	20 Hz	-	10	-	Deg
Passband Ripple		-	-	0.17	dB
Filter Settling Time		-	$10^5/F_s$	-	s

- Notes:**
7. Filter response is clock dependent and scales with the ADC sampling frequency (F_s). With a 27.000 MHz or 24.576 MHz XTAL/SYS_CLK, F_s is equal to the applied clock divided by 512. With an 18.432 MHz XTAL/SYS_CLK, F_s is equal to the applied clock divided by 384.

PWM POWER OUTPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): AGND = DGND = PGND = 0 V; All voltages with respect to ground; $T_A = 25^\circ\text{C}$; $V_D = 3.3\text{ V}$; $V_P = 18\text{ V}$; $R_L = 8\ \Omega$ for full-bridge, $R_L = 4\ \Omega$ for half-bridge and parallel full-bridge; $\text{OutputDly}[3:0] = 1111$; $\text{PhaseShift} = 1$ for half-bridge, $\text{PhaseShift} = 0$ for full-bridge and parallel full-bridge; Input Signal: full-scale 997 Hz sine wave through serial audio input port, 48 kHz sample rate; Capacitor values connected to AFILTA, AFILTB, FILT+, VQ, VD_REG, and VA_REG as shown in [Figure 1 on page 13](#); PWM Switch Rate = 384 kHz; 10 Hz to 20 kHz Measurement Bandwidth; Performance measurements taken through AES17 filter.

Parameters	Symbol	Conditions	Min	Typ	Max	Units	
Power Output per Channel	Stereo Full-Bridge	THD+N < 10%	-	15	-	W	
		THD+N < 1%	-	12	-	W	
		Half-Bridge	THD+N < 10%	-	7	-	W
			THD+N < 1%	-	5.5	-	W
		Parallel Full-Bridge	THD+N < 10%	-	30	-	W
			THD+N < 1%	-	23.5	-	W
Total Harmonic Distortion + Noise	THD+N	$P_O = 1\text{ W}$	-	0.05	-	%	
		$P_O = 0\text{ dBFS} = 11.3\text{ W}$	-	0.10	-	%	
		Stereo Full-Bridge	$P_O = 1\text{ W}$	-	0.12	-	%
			$P_O = 0\text{ dBFS} = 5.0\text{ W}$	-	0.28	-	%
		Half-Bridge	$P_O = 1\text{ W}$	-	0.1	-	%
			$P_O = 0\text{ dBFS} = 22.6\text{ W}$	-	0.3	-	%
Dynamic Range	DYR	$P_O = -60\text{ dBFS}$, A-Weighted	-	102	-	dB	
		$P_O = -60\text{ dBFS}$, Unweighted	-	99	-	dB	
		Stereo Full-Bridge	$P_O = -60\text{ dBFS}$, A-Weighted	-	99	-	dB
			$P_O = -60\text{ dBFS}$, Unweighted	-	96	-	dB
		Half-Bridge	$P_O = -60\text{ dBFS}$, A-Weighted	-	102	-	dB
			$P_O = -60\text{ dBFS}$, Unweighted	-	99	-	dB
Parallel Full-Bridge	$P_O = -60\text{ dBFS}$, A-Weighted	-	102	-	dB		
	$P_O = -60\text{ dBFS}$, Unweighted	-	99	-	dB		
MOSFET On Resistance	$R_{DS(ON)}$	$I_d = 0.5\text{ A}$, $T_J = 50^\circ\text{C}$	-	280	-	m Ω	
Efficiency	h	$P_O = 2 \times 15\text{ W}$, $R_L = 8\ \Omega$	-	85	-	%	
Minimum Output Pulse Width	PW_{min}	No Load	-	50	-	ns	
Rise Time of OUTx	t_r	Resistive Load	-	20	-	ns	
Fall Time of OUTx	t_f	Resistive Load	-	20	-	ns	
PWM Output Over-Current Error Trigger Point	I_{CE}	$T_A = 25^\circ\text{C}$, $OCREF = 16.2\text{ k}\Omega$	-	2.5	-	A	
		$T_A = 25^\circ\text{C}$, $OCREF = 18\text{ k}\Omega$	-	2.1	-	A	
		$T_A = 25^\circ\text{C}$, $OCREF = 22\text{ k}\Omega$	-	1.7	-	A	
Junction Thermal Warning Trigger Point	T_{TW}		-	105	-	$^\circ\text{C}$	
Junction Thermal Error Trigger Point	T_{TE}		-	125	-	$^\circ\text{C}$	
VP Under-Voltage Error Falling Trigger Point	V_{UVFALL}	$T_A = 25^\circ\text{C}$	-	4.7	4.9	V	
VP Under-Voltage Error Rising Trigger Point	V_{UVRISE}	$T_A = 25^\circ\text{C}$	-	4.95	5.4	V	

SERIAL AUDIO INPUT PORT SWITCHING SPECIFICATIONS

AGND = DGND = PGND = 0 V; $T_A = 25^\circ\text{C}$; $V_D = 3.3\text{ V}$; Inputs: Logic 0 = DGND; Logic 1 = V_D .

Parameters	Symbol	Min	Nominal	Max	Units
Supported Input Sample Rates	F_{SI}	28.5	32	35.2	kHz
		39.5	44.1	52.8	kHz
		39.5	48	52.8	kHz
		86.4	96	105.6	kHz
LRCK Duty Cycle		45	-	55	%
SCLK Frequency	(Note 8),(Note 9) $1/t_p$	$F_{SI} * 2 * N_{bits}$	-	$F_{CLK}/3$	Hz
SCLK Duty Cycle		45	-	55	%
LRCK Setup Time Before SCLK Rising Edge	$t_{s(LK-SK)}$	40	-	-	ns
SDIN Setup Time Before SCLK Rising Edge	$t_{s(SD-SK)}$	25	-	-	ns
SDIN Hold Time After SCLK Rising Edge	t_h	10	-	-	ns
RST pin Low Pulse Width	(Note 10)	1	-	-	ms

- Notes:**
8. F_{CLK} is the frequency of the crystal connected to the XTI/XTO pins or the input SYS_CLK signal.
 9. N_{bits} is the number of bits per sample of the serial digital input.
 10. After powering up the CS4525, \overline{RST} should be held low until the power supplies and clocks are stable.

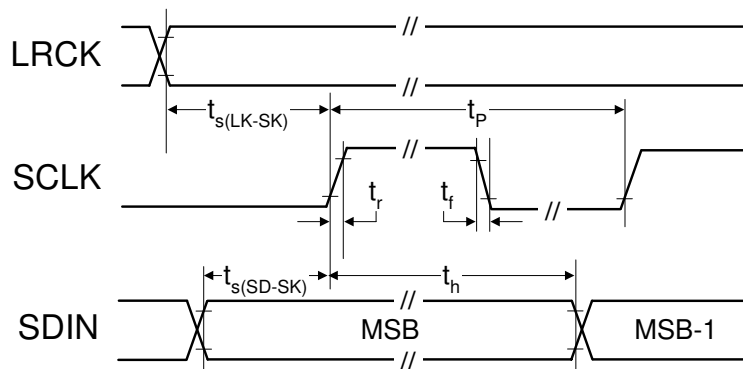


Figure 7. Serial Audio Input Port Timing

AUX SERIAL AUDIO I/O PORT SWITCHING SPECIFICATIONS

AGND = DGND = PGND = 0 V; $T_A = 25^\circ\text{C}$; $V_D = 3.3\text{ V}$; AUX_SDOOUT & DLY_SDOOUT $C_L = 15\text{ pF}$; Inputs: Logic 0 = DGND; Logic 1 = VD; (Note 11).

Parameters	Symbol	Min	Typ	Max	Units	
Input Source: Analog Inputs (Internal ADC)						
Output Sample Rate	ClkFreq[1:0] = '00' ClkFreq[1:0] = '01' ClkFreq[1:0] = '10'	F_{SO}	-	$F_{CLK}/384$	-	Hz
			-	$F_{CLK}/512$	-	Hz
			-	$F_{CLK}/512$	-	Hz
AUX_LRCK Duty Cycle		-	50	-	%	
AUX_LRCK Period		-	$1/F_{SO}$	-	s	
AUX_SCLK Frequency	ClkFreq[1:0] = '00' ClkFreq[1:0] = '01' ClkFreq[1:0] = '10'	F_{SCLKO}	-	$48 \cdot F_{SO}$	-	Hz
			-	$64 \cdot F_{SO}$	-	Hz
			-	$64 \cdot F_{SO}$	-	Hz
AUX_SCLK Duty Cycle		-	50	-	%	
AUX_SCLK Period		-	$1/F_{SCLKO}$	-	s	
Input Source: Serial Audio Input Port						
Output Sample Rate	$F_{S-In} = 32\text{ kHz}, 44.1\text{ kHz}, 48\text{ kHz}$ $F_{S-In} = 96\text{ kHz}$	F_{SO}	-	F_{SI}	-	Hz
			-	$F_{SI}/2$	-	Hz
AUX_LRCK Duty Cycle	(Note 13)		45	-	55	%
AUX_LRCK Period	(Note 12, 13)		$T_{SI} - T_{CLK}$	T_{SI}	$T_{SI} + T_{CLK}$	s
AUX_SCLK Frequency	$F_{S-In} = 32\text{ kHz}, 44.1\text{ kHz}, 48\text{ kHz}$ (Note 14) $F_{S-In} = 96\text{ kHz}$		-	F_{SCLKI}	-	Hz
			-	$F_{SCLKI}/2$	-	Hz
AUX_SCLK Duty Cycle			30	-	70	%
AUX_SCLK Period	$F_{S-In} = 32\text{ kHz}, 44.1\text{ kHz}, 48\text{ kHz}$ (Note 13, 14) $F_{S-In} = 96\text{ kHz}$		$T_{SCLKI} - T_{CLK}$	T_{SCLKI}	$T_{SCLKI} + T_{CLK}$	s
			$2 \cdot T_{SCLKI} - T_{CLK}$	$2 \cdot T_{SCLKI}$	$2 \cdot T_{SCLKI} + T_{CLK}$	s
Input Source: Analog Inputs or Serial Audio Input Port						
AUX_LRCK Rising Edge to AUX_SCLK Falling Edge		t_{LTSF}	-	-	20	ns
AUX_SCLK Rising Edge to Data Output Valid		t_{SRDV}	-	-	$T_{CLK} + 20$	ns
DLY_SDIN Setup Time Before AUX_SCLK Rising Edge		t_{DIS}	25	-	-	ns
DLY_SDIN Hold Time After AUX_SCLK Rising Edge		t_{DIH}	10	-	-	ns

- Notes:**
- F_{CLK} is the frequency of the crystal connected to the XT1/XTO pins or the input SYS_CLK signal.
 $T_{CLK} = 1/F_{CLK}$.
 - F_{SI} is the frequency of the input LRCK signal. $T_{SI} = 1/F_{SI}$
 - May vary during normal operation.
 - F_{SCLKI} is the frequency of the input SCLK signal. $T_{SCLKI} = 1/F_{SCLKI}$.

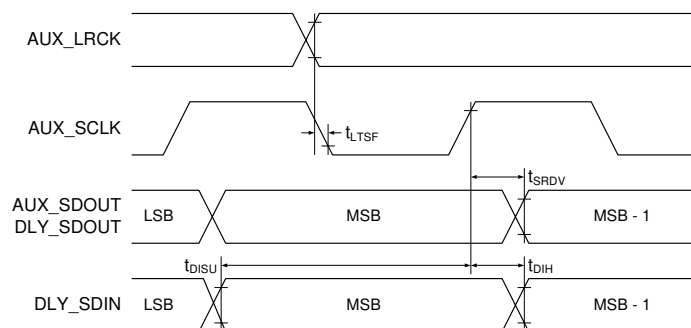


Figure 8. AUX Serial Port Interface Master Mode Timing

XTI SWITCHING SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
External Crystal Operating Frequency (Note 15)	ClkFreq[1:0] = '00'	18.240	18.432	18.617	MHz
	ClkFreq[1:0] = '01'	24.330	24.576	24.822	MHz
	ClkFreq[1:0] = '10'	26.730	27.000	27.270	MHz
XTI Duty Cycle		45	50	55	%

Notes: 15. See “Clock Frequency (ClkFreq[1:0])” on page 69.

SYS_CLK SWITCHING SPECIFICATIONS

AGND = DGND = PGND = 0 V; $T_A = 25^\circ\text{C}$; VD = 3.3 V; Input: Logic 0 = DGND; Logic 1 = VD, SYS_CLK Output: $C_L = 20$ pF.

Parameter	Symbol	Min	Typ	Max	Unit
External Clock Operating Frequency (Note 15)	ClkFreq[1:0] = '00'	18.240	18.432	18.617	MHz
	ClkFreq[1:0] = '01'	24.330	24.576	24.822	MHz
	ClkFreq[1:0] = '10'	26.730	27.000	27.270	MHz
Rising Edge $\overline{\text{RST}}$ to start of SYS_CLK	t_{sclko}	-	$1024 \cdot t_{\text{sclki}}$	-	
SYS_CLK Period	t_{sclki}	37.04	-	54.25	ns
SYS_CLK Duty Cycle		45	50	55	%
SYS_CLK high time	t_{clkih}	16.67	-	29.84	ns
SYS_CLK low time	t_{clkil}	16.67	-	29.84	ns

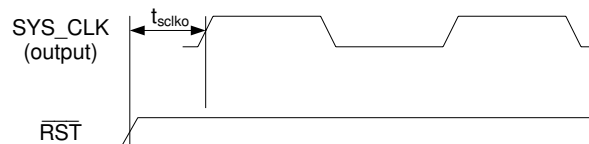


Figure 9. SYS_CLK Timing from Reset

PWM_SIGX SWITCHING SPECIFICATIONS

AGND = DGND = PGND = 0 V; $T_A = 25^\circ\text{C}$; VD = 3.3 V; Load = 10 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time of PWM_SIGx	t_r	-	2.1	-	ns
Fall Time of PWM_SIGx	t_f	-	1.4	-	ns

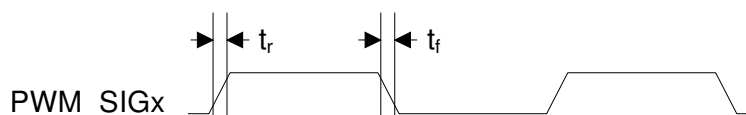


Figure 10. PWM_SIGX Timing

I²C CONTROL PORT SWITCHING SPECIFICATIONS

AGND = DGND = PGND = 0 V; T_A = 25°C; V_D = 3.3 V; Inputs: Logic 0 = DGND; Logic 1 = V_D; SDA C_L = 30 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f _{scl}	-	100	kHz
RST Rising Edge to Start	t _{irs}	500	-	ns
Bus Free Time Between Transmissions	t _{buf}	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t _{hdst}	4.0	-	μs
Clock Low time	t _{low}	4.7	-	μs
Clock High Time	t _{high}	4.0	-	μs
Setup Time for Repeated Start Condition	t _{sust}	4.7	-	μs
SDA Hold Time from SCL Falling (Note 16)	t _{hdd}	10	-	ns
SDA Setup time to SCL Rising	t _{sud}	250	-	ns
Rise Time of SCL and SDA	t _{rc}	-	1	μs
Fall Time SCL and SDA	t _{fc}	-	300	ns
Setup Time for Stop Condition	t _{susp}	4.7	-	μs
Acknowledge Delay from SCL Falling	t _{ack}	300	1000	ns

Notes: 16. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

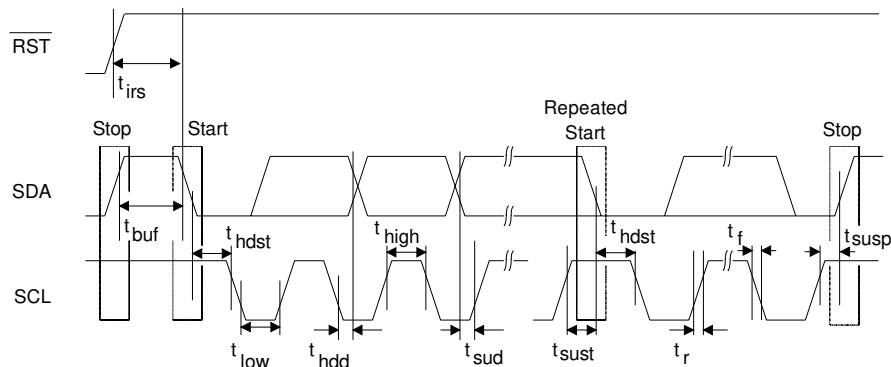


Figure 11. Control Port Timing - I²C

DC ELECTRICAL CHARACTERISTICS

AGND = DGND = PGND = 0 V; All voltages with respect to ground; PWM switch rate = 384 kHz; Unless otherwise specified.

Parameters		Min	Typ	Max	Units
Normal Operation (Note 17)					
Power Supply Current	VD = 3.3 V	-	54	-	mA
Power Dissipation	VD = 3.3 V	-	180	-	mW
Power-Down Mode (Note 18)					
Power Supply Current	VD = 3.3 V	-	2.8	-	mA
VD_REG Characteristics					
Nominal Voltage		2.25	2.5	2.75	V
DC current source		-	-	3	mA
VA_REG Characteristics					
Nominal Voltage		2.25	2.5	2.75	V
DC current source		-	-	1	mA
VQ Characteristics					
Nominal Voltage		-	0.5*VA_REG	-	V
Output Impedance		-	23	-	kΩ
DC current source/sink	(Note 19)	-	-	10	μA
Filt+ Nominal Voltage		-	VA_REG	-	V
Power Supply Rejection Ratio (Note 20)	1 kHz	-	60	-	dB
	60 Hz	-	40	-	dB

- Notes:**
- Normal operation is defined as $\overline{RST} = HI$.
 - Power-Down Mode is defined as $\overline{RST} = LOW$ with all input lines held static.
 - The DC current drain represents the allowed current from the VQ pin due to typical leakage through the electrolytic de-coupling capacitors.
 - Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will increase the PSRR.

DIGITAL INTERFACE SPECIFICATIONS

AGND = DGND = PGND = 0 V; All voltages with respect to ground; Unless otherwise specified.

Parameters		Symbol	Min	Max	Units
Digital Interface Signal Characteristics (Note 21)					
High-Level Input Voltage		V _{IH}	0.75*VD_REG	-	V
Low-Level Input Voltage		V _{IL}	-	0.20*VD_REG	V
High-Level Output Voltage	I _o =2 mA	V _{OH}	0.90*VD	-	V
Low-Level Output Voltage	I _o =2 mA	V _{OL}	-	0.2	V
Input Leakage Current		I _{in}	-	±10	uA
Input Capacitance			-	8	pF
PWM_SIGx Characteristics					
High-Level PWM_SIGx Output Voltage	I _o =2 mA	V _{OHPS}	0.90*VD_REG	-	V
Low-Level PWM_SIGx Output Voltage	I _o =2 mA	V _{OLPS}	-	0.2	V

- Notes:**
- Digital interface signals include all pins sourced from the VD supply as shown in “Digital I/O Pin Characteristics” on page 12.