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CS4525

30 W Digital Audio Amplifier with Integrated ADC

Digital Amplifier Features

- Fully Integrated Power MOSFETs
- No Heatsink Required
  - Programmable Power Foldback on Thermal Warning
  - High Efficiency
- > 100 dB Dynamic Range
- < 0.1% THD+N @ 1 W
- Configurable Outputs (10% THD+N)
  - 1 x 30 W into 4 Ω, Parallel Full-Bridge
  - 2 x 15 W into 8 Ω, Full-Bridge
  - 2 x 7 W into 4 Ω, Half-Bridge + 1 x 15 W into 8 Ω, Full-Bridge
- Built-In Protection with Error Reporting
  - Overcurrent/Undervoltage/Thermal Overload Shutdown
  - Thermal Warning Reporting
- PWM Popguard® for Half-Bridge Mode
- Click-Free Start-Up
- Programmable Channel Delay for System Noise & Radiated Emissions Management

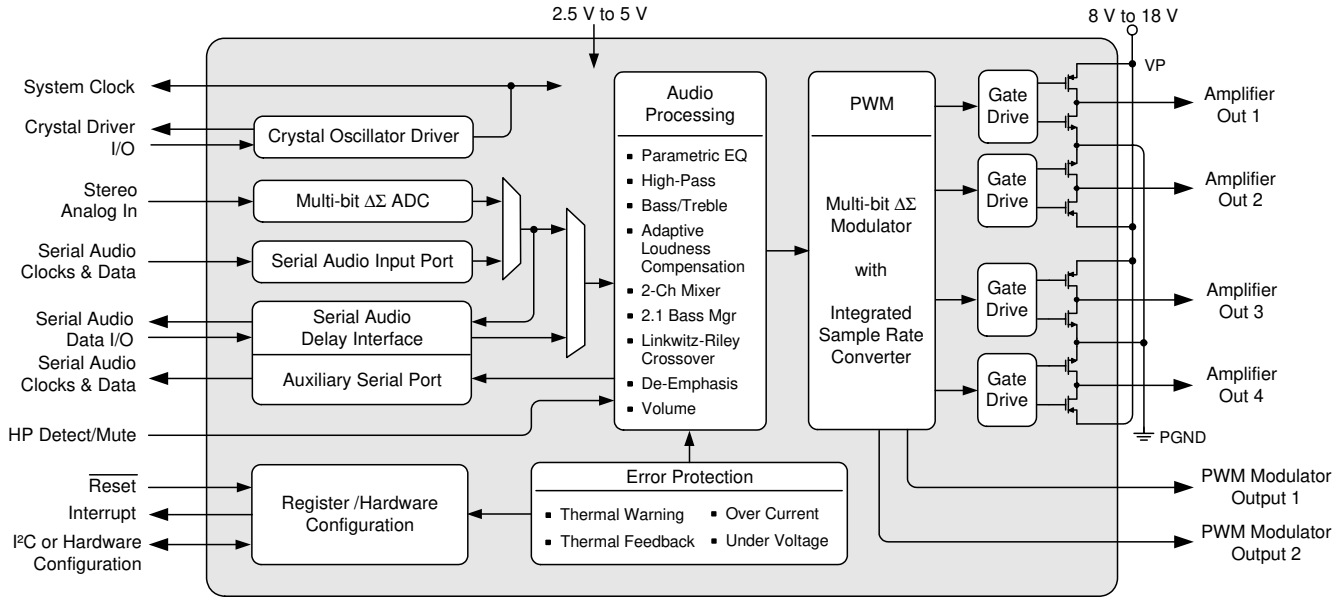
ADC Features

- Stereo, 24-bit, 48 kHz Conversion
- Multi-bit Architecture
- 95 dB Dynamic Range (A-wtd)
- -86 dB THD+N
- Supports 2 Vrms Input with Passive Components

System Features

- Asynchronous 2-Channel Digital Serial Port
- 32 kHz to 96 kHz Input Sample Rates
- Operation with On-Chip Oscillator Driver or Applied SYS_CLK at 18.432, 24.576 or 27.000 MHz
- Integrated Sample Rate Converter (SRC)
  - Eliminates Clock-Jitter Effects
  - Input Sample Rate Independent Operation
  - Simplifies System Integration
- Spread Spectrum PWM Modulation
  - Reduces EMI Radiated Energy
- Low Quiescent Current

(Features continued on page 2)



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Software Mode System Features

- Digital Audio Processing
  - 5 Programmable Parametric EQ Filters
  - Selectable High-Pass Filter
  - Bass/Treble Tone Control
  - Adaptive Loudness Compensation
  - 2-Channel Mixer
  - 2.1 Bass Management
  - 24 dB/octave Linkwitz-Riley Crossover Filters
  - De-emphasis Filter
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I²S up to 24-bit
  - Right-Justified 16-, 18-, 20-, 24-bits
- Digital Serial Connection to Additional CS4525 or DACs for Subwoofer
- Digital Interface to External Lip-Sync Delay
- PWM Switch Rate Shifting Eliminates AM Frequency Interference
- Digital Volume Control with Soft ramp
  - +24 to -103 dB in 0.5 dB steps
- Programmable Peak Detect and Limiter
- 2-Channel Logic-Level PWM Output
  - Programmable Channel Mapping
  - Can Drive an External PWM Amplifier, Headphone Amplifier, or Line-Out Amplifier
  - Integrated Headphone Detection
- Flexible Power Output Configurations
- Thermal Foldback for Interruption-Free Power-Stage Protection
  - Supports Internal and External Power Stages
- Operation from On-Chip Oscillator Driver or Applied Systems Clock
- Supports I²C® Host Control Interface

Hardware Mode System Features

- 2-Channel Stereo Full-Bridge Power Outputs
- Analog and Digital Inputs
- I²S and Left-Justified Serial Input Formats
- Thermal Foldback for Interruption-Free Protection of Internal Power Stage
- Operation from Applied Systems Clock
- External Mute Input

Common Applications

- Integrated Digital TV's
- Flat Panel TV Monitors
- Computer/TV Monitors
- Mini/Micro Shelf Systems
- Digital Powered Speakers
- Portable Docking Stations
- Computer Desktop Audio

General Description

The CS4525 is a stereo analog or digital input PWM high efficiency Class D amplifier audio system with an integrated stereo analog-to-digital (A/D) converter. The stereo power amplifiers can deliver up to 15 W per channel into 8 Ω speakers from a small space-saving 48-pin QFN package. The PWM amplifier can achieve greater than 85% efficiency. The package is thermally enhanced for optimal heat dissipation which eliminates the need for a heatsink.

The power stage outputs can be configured as two full-bridge channels for 2 x 15 W operation, two half-bridge channels and one full-bridge channel for 2 x 7 W + 1 x 15 W operation, or one parallel full-bridge channel for 1 x 30 W operation. The CS4525 integrates on-chip over-current, under-voltage, and over-temperature protection and error reporting as well as a thermal warning indicator and programmable foldback of the output power to allow cooling.

The main digital serial port on the CS4525 can support asynchronous operation with the integrated on-chip sample rate converter (SRC) which eases system integration. The SRC allows for a fixed PWM switching frequency regardless of incoming sample rate as well as optimal clocking for the A/D modulators.

An on-chip oscillator driver eliminates the need for an external crystal oscillator circuit, reducing overall design cost and conserving circuit board space. The CS4525 automatically uses the on-chip oscillator driver in the absence of an applied master clock.

The CS4525 is available in a 48-pin QFN package in Commercial grade (-10° to +70° C). The CRD4525-Q1 4-layer, 1 oz. copper and CRD4525-D1 2-layer, 1 oz. copper customer reference designs are also available.

Please refer to "Ordering Information" on page 97 for complete ordering information.

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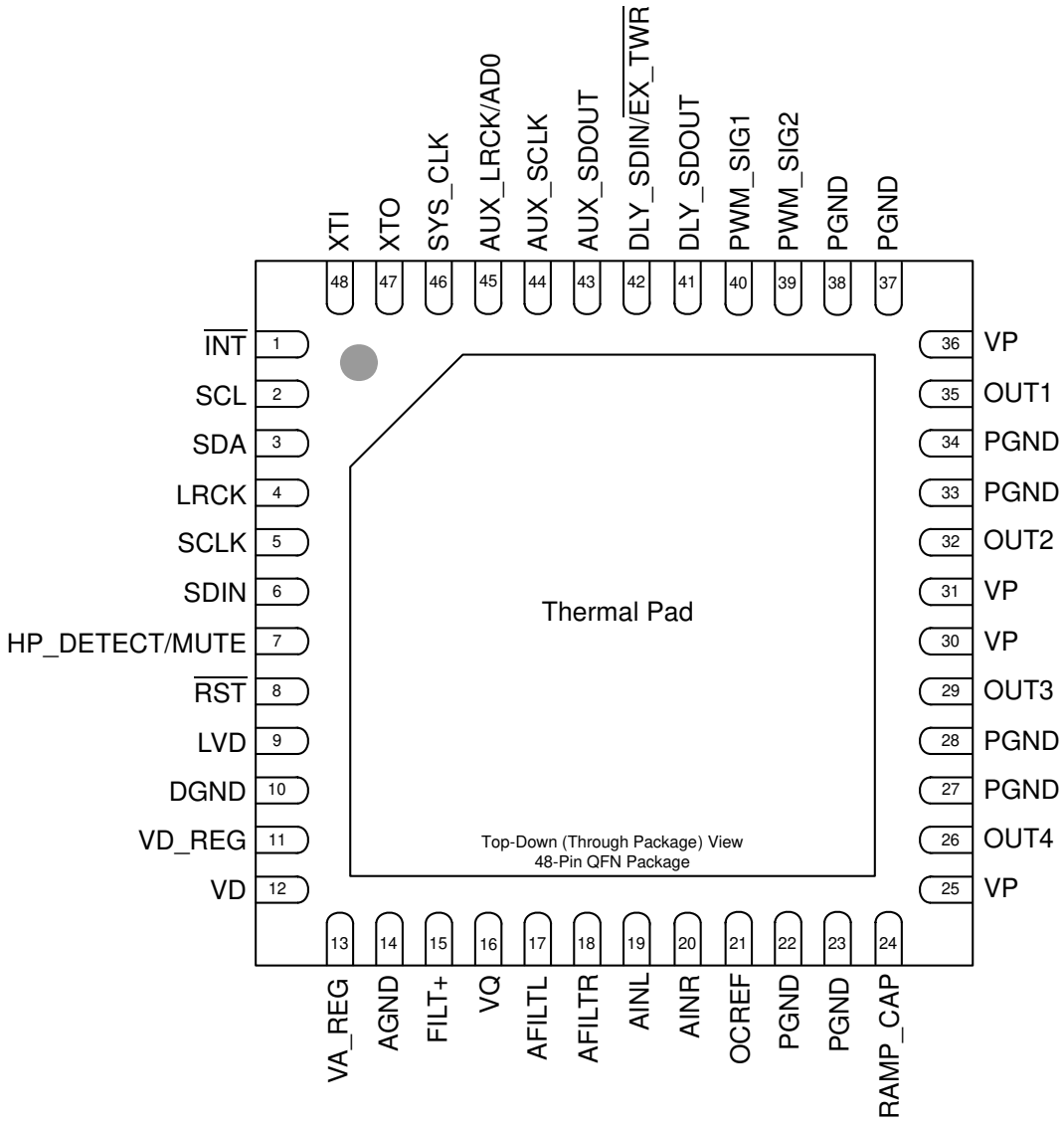
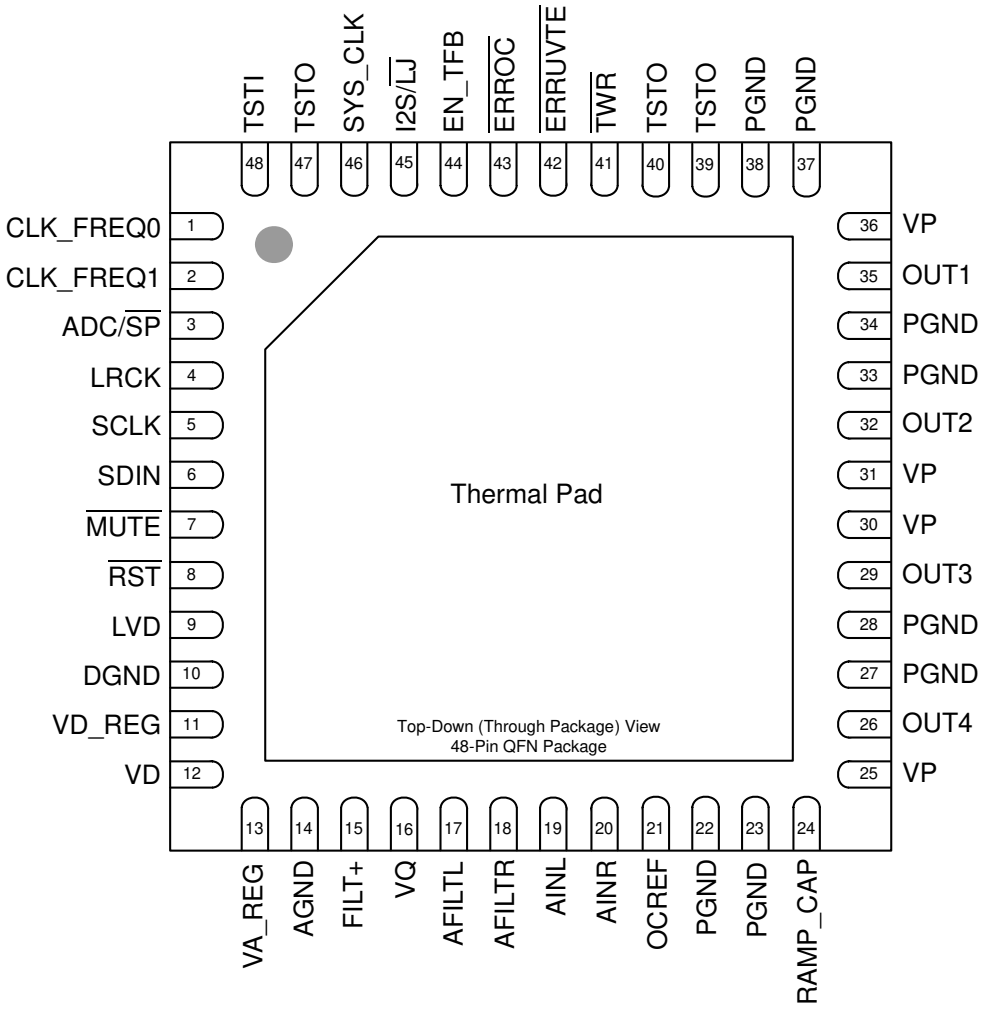
1. PIN DESCRIPTIONS - SOFTWARE MODE



Pin Name	Pin #	Pin Description
$\overline{\text{INT}}$	1	**Interrupt** *(Output)* - Indicates an interrupt condition has occurred.
SCL	2	**Serial Control Port Clock** (*Input*) - Serial clock for the I²C control port.
SDA	3	**Serial Control Data** (*Input/Output*) - Bi-directional data I/O for the I²C control port.
LRCK	4	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	5	**Serial Clock** (*Input*) **-** Serial bit clock for the serial audio interface.
SDIN	6	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
HP_DETECT/ MUTE	7	**Headphone Detect** / **Mute** (*Input*) - Headphone detection or mute input signal as configured via the I²C control port.
$\overline{\text{RST}}$	8	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when this pin is driven low.

LVD	9	**VD Voltage Level Indicator** (*Input*) - Identifies the voltage level attached to VD. When applying 5.0 V to VD, LVD must be connected to VD. When applying 2.5 V or 3.3 V to VD, LVD must be DGND.
DGND	10	**Digital Ground** (*Input*) - Ground for the internal logic and digital I/O.
VD_REG	11	**Core Logic Power** (*Output*) - Internally generated low voltage power supply for digital logic.
VD	12	**Power** (*Input*) - Positive power supply for the internal regulators and digital I/O.
VA_REG	13	**Analog Power** *(Output)* - Internally generated positive power for the analog section and I/O.
AGND	14	**Analog Ground** (*Input*) - Ground reference for the internal analog section and I/O.
FILT+	15	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal ADC sampling circuits.
VQ	16	**Common Mode Voltage** (*Output*) - Filter connection for internal common mode voltage.
AFILTL AFILTR	17 18	**Antialias Filter Connection** (*Output*) - Antialias filter connection for ADC inputs.
AINL AINR	19 20	**Analog Input** (*Input*) - The full-scale input level is specified in the ADC Analog Characteristics specification table.
OCREF	21	**Over Current Reference Setting** (*Input*) - Sets the reference for over current detection.
PGND	22,23 27,28 33,34 37,38	**Power Ground** (*Input*) - Ground for the individual output power half-bridge devices.
RAMP_CAP	24	**Output Ramp Capacitor** (*Input*) - Used by the PWM Popguard Transient Control to suppress the initial pop in half-bridge-configured outputs.
VP	25,30, 31,36	**High Voltage Power** (*Input*) - High voltage power supply for the individual half-bridge devices.
OUT4 OUT3 OUT2 OUT1	26 29 32 35	**PWM Output** (*Output*) - Amplified PWM power outputs.
PWM_SIG2 PWM_SIG1	39 40	**Logic Level PWM Output** (*Output*) - Logic Level PWM switching signals.
DLY_SDOUT	41	**Delay Serial Audio Data Out** (*Output*) - Output for two's complement serial audio data.
$\overline{\text{DLY\_SDIN}}$/ $\overline{\text{EX\_TWR}}$	42	**Delay Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data. **External Thermal Warning** (*Input*) - Input for an external thermal warning signal. Configurable via the I²C control port.
AUX_SDOUT	43	**Auxiliary Port Serial Audio Data Out** (*Output*) - Output for two's complement auxiliary port serial data.
AUX_SCLK	44	**Auxiliary Port Serial Clock** *(Output)* - Serial clock for the auxiliary port serial interface.
AUX_LRCK/ AD0	45	**Auxiliary Port Left Right Clock** *(Output)* - Determines which channel, Left or Right, is currently active on the serial audio data line. **AD0** *(Input)* - Sets the LSB of the I²C device address. Sensed on the release of $\overline{\text{RST}}$.
SYS_CLK	46	**System Clock** (*Input/Output*) -Clock source for the internal logic, processing, and modulators. This pin should be connected to through a 10kΩ to ground when unused.
XTO	47	**Crystal Oscillator Output** *(Output)* - Crystal oscillator driver output.
XTI	48	**Crystal Oscillator Input** (*Input*) - Crystal oscillator driver input.
Thermal Pad	-	**Thermal Pad** - Thermal relief pad for optimized heat dissipation. See "QFN Thermal Pad" on page 65 for more information.

2. PIN DESCRIPTIONS - HARDWARE MODE



Pin Name	Pin #	Pin Description
CLK_FREQ0 CLK_FREQ1	1 2	**Clock Frequency** *(Input)* - Determines the frequency of the clock expected to be driven into the SYS_CLK pin.
ADC/$\overline{SP}$	3	**ADC/Serial Port** *(Input)* - Selects between the Analog to Digital Converter and the Serial Port for audio input. Selects the ADC when high or the serial port when low.
LRCK	4	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	5	**Serial Clock** (*Input*) - Serial bit clock for the serial audio interface.
SDIN	6	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
$\overline{MUTE}$	7	**Mute** (*Input*) - The PWM outputs will output silence as a 50% duty cycle signal when this pin is driven low.
$\overline{RST}$	8	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when this pin is driven low.

LVD	9	**VD Voltage Level Indicator** (*Input*) - Identifies the voltage level attached to VD. When applying 5.0 V to VD, LVD must be connected to VD. When applying 2.5 V or 3.3 V to VD, LVD must be connected to DGND.
DGND	10	**Digital Ground** (*Input*) - Ground for the internal logic and I/O.
VD_REG	11	**Core Logic Power** (*Output*) - Internally generated low voltage power supply for digital logic.
VD	12	**Digital Power** (*Input*) - Positive power supply for the internal regulators and digital I/O.
VA_REG	13	**Analog Power** *(Output)* - Internally generated positive power for the analog section and I/O.
AGND	14	**Analog Ground** (*Input*) - Ground reference for the internal analog section and I/O.
FILT+	15	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal ADC sampling circuits.
VQ	16	**Common Mode Voltage** (*Output*) - Filter connection for internal common mode voltage.
AFILTL AFILTR	17 18	**Antialias Filter Connection** (*Output*) - Antialias filter connection for ADC inputs.
AINL AINR	19 20	**Analog Input** (*Input*) - The full-scale input level is specified in the ADC Analog Characteristics specification table.
OCREF	21	**Over Current Reference Setting** (*Input*) - Sets the reference for over current detection.
PGND	22,23 27,28 33,34 37,38	**Power Ground** (*Input*) - Ground for the individual output power half-bridge devices.
RAMP_CAP	24	**Output Ramp Capacitor** (*Input*) - This pin should be connected directly to VP in hardware mode.
VP	25,30, 31,36	**High Voltage Power** (*Input*) - High voltage power supply for the individual half-bridge devices.
OUT4 OUT3 OUT2 OUT1	26 29 32 35	**PWM Output** (*Output*) - Amplified PWM power outputs.
TSTO	39 40	**Test Output** *(Output)* - These pins are outputs used for the Logic Level PWM switching signals available only in software mode. They must be left unconnected for hardware mode operation.
$\overline{\text{TWR}}$	41	**Thermal Warning Output** (*Output*) - Thermal warning output.
$\overline{\text{ERRUVTE}}$	42	**Thermal and Undervoltage Error Output** (*Output*) - Error flag for thermal shutdown and undervoltage.
$\overline{\text{ERROC}}$	43	**Overcurrent Error Output** *(Output)* - Overcurrent error flag.
EN_TFB	44	**Enable Thermal Feedback** *(Input)* - Enables the thermal foldback feature when high.
I2S/$\overline{\text{LJ}}$	45	**I²S/Left Justified** *(Input)* - Selects between I²S and Left-Justified data format for the serial input port. Selects I²S when high and LJ when low.
SYS_CLK	46	**System Clock** (*Input/Output*) -Clock source for the delta-sigma modulators.
TSTO	47	**Test Output** *(Output)* - This pin is an output used for the crystal oscillator driver available only in software mode. It must be left unconnected for normal hardware mode operation.
TSTI	48	**Test Input** (*Input*) - This pin is an input used for the crystal oscillator driver available only in software mode. It must be tied to digital ground for normal hardware mode operation.
Thermal Pad	-	**Thermal Pad** - Thermal relief pad for optimized heat dissipation. See "QFN Thermal Pad" on page 65 for more information.

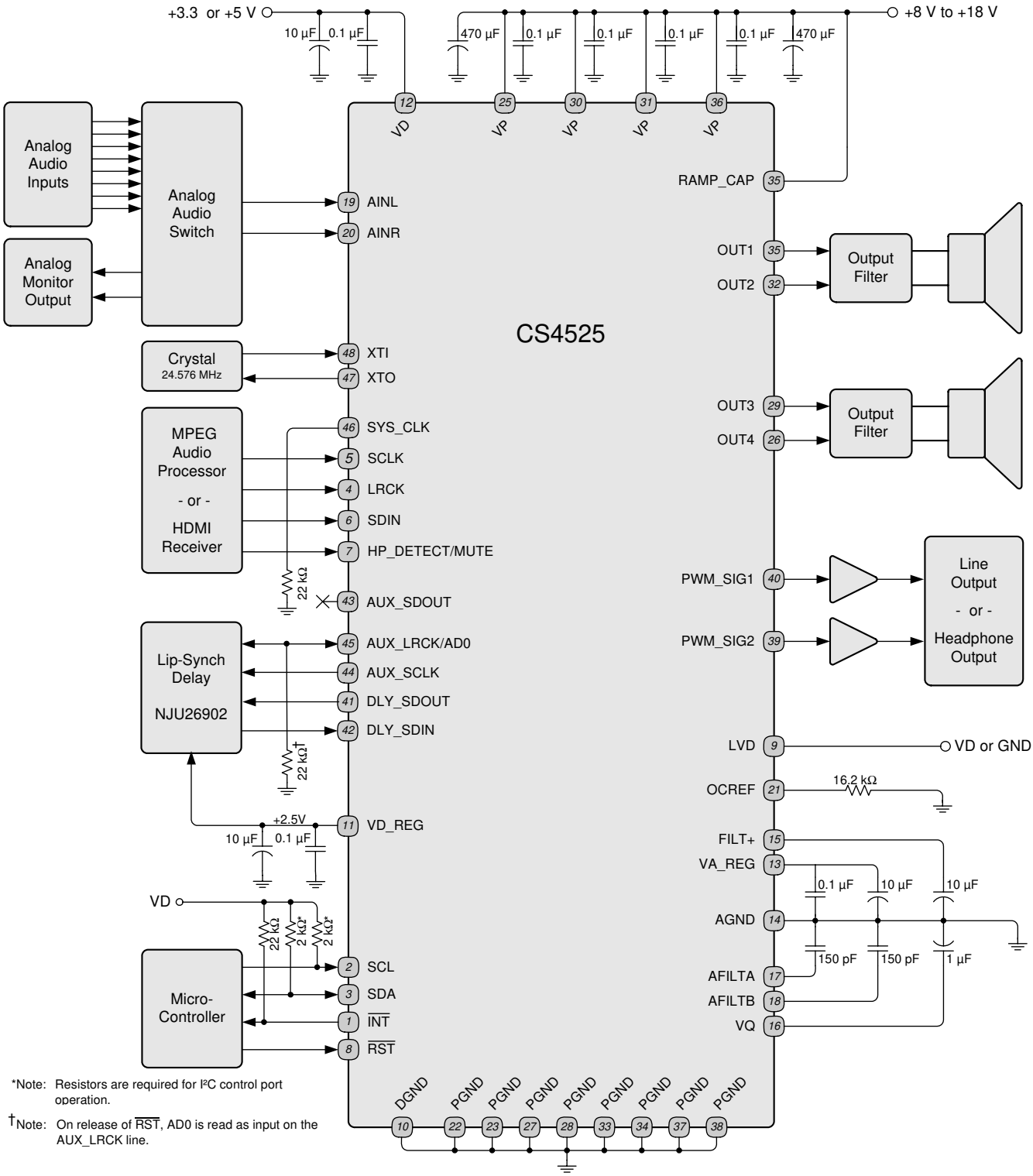
2.1 Digital I/O Pin Characteristics

The logic level for each input is set by its corresponding power supply and should not exceed the maximum ratings.

Power Supply	Pin Number	Pin Name	I/O	Driver	Receiver
Software Mode					
VD	1	INT	Output	2.5 V-5.0 V, Open Drain	
	2	SCL	Input	-	2.5 V-5.0 V, with Hysteresis
	3	SDA	Input/Output	2.5 V-5.0 V, Open Drain	2.5 V-5.0 V, with Hysteresis
	7	HP_DETECT MUTE	Input Input	- -	2.5 V-5.0 V 2.5 V-5.0 V
	41	DLY_SDOUT	Output	2.5 V-5.0 V, CMOS	-
	42	DLY_SDIN $\overline{\text{EX\_TWR}}$	Input Input	- -	2.5 V-5.0 V 2.5 V-5.0 V
	43	AUX_SDOUT	Output	2.5 V-5.0 V, CMOS	-
	44	AUX_SCLK	Output	2.5 V-5.0 V, CMOS	-
	45	AUX_LRCK	Output	2.5 V-5.0 V, CMOS	-
VD_REG	39	PWM_SIG2	Output	2.5 V, CMOS	-
	40	PWM_SIG1	Output	2.5 V, CMOS	-
Hardware Mode					
VD	1	SEL_OSC0	Input	-	2.5 V-5.0 V
	2	SEL_OSC1	Input	-	2.5 V-5.0 V
	3	ADC/$\overline{\text{SP}}$	Input	-	2.5 V-5.0 V
	7	$\overline{\text{MUTE}}$	Input	-	2.5 V-5.0 V
	41	$\overline{\text{TWR}}$	Output	2.5 V-5.0 V, Open Drain	-
	42	$\overline{\text{ERRUVTE}}$	Output	2.5 V-5.0 V, Open Drain	-
	43	$\overline{\text{ERROC}}$	Output	2.5 V-5.0 V, Open Drain	-
	44	EN_TFB	Input	-	2.5 V-5.0 V
	45	I²S/$\overline{\text{LJ}}$	Input	-	2.5 V-5.0 V
All Modes					
VD	4	LRCK	Input	-	2.5 V-5.0 V
	5	SCLK	Input	-	2.5 V-5.0 V
	6	SDIN	Input	-	2.5 V-5.0 V
	8	RST	Input	-	2.5 V-5.0 V
	9	LVD	Input	-	2.5 V-5.0 V
	46	SYS_CLK	Input/Output	2.5 V-5.0 V, CMOS	2.5 V-5.0 V
VP	26	OUT4	Output	8.0 V-18.0 V Power MOSFET	-
	29	OUT3	Output	8.0 V-18.0 V Power MOSFET	-
	32	OUT2	Output	8.0 V-18.0 V Power MOSFET	-
	35	OUT1	Output	8.0 V-18.0 V Power MOSFET	-

Table 1. I/O Power Rails

3. TYPICAL CONNECTION DIAGRAMS



*Note: Resistors are required for I²C control port operation.

†Note: On release of $\overline{\text{RST}}$, AD0 is read as input on the AUX_LRCK line.

Figure 1. Typical Connection Diagram - Software Mode

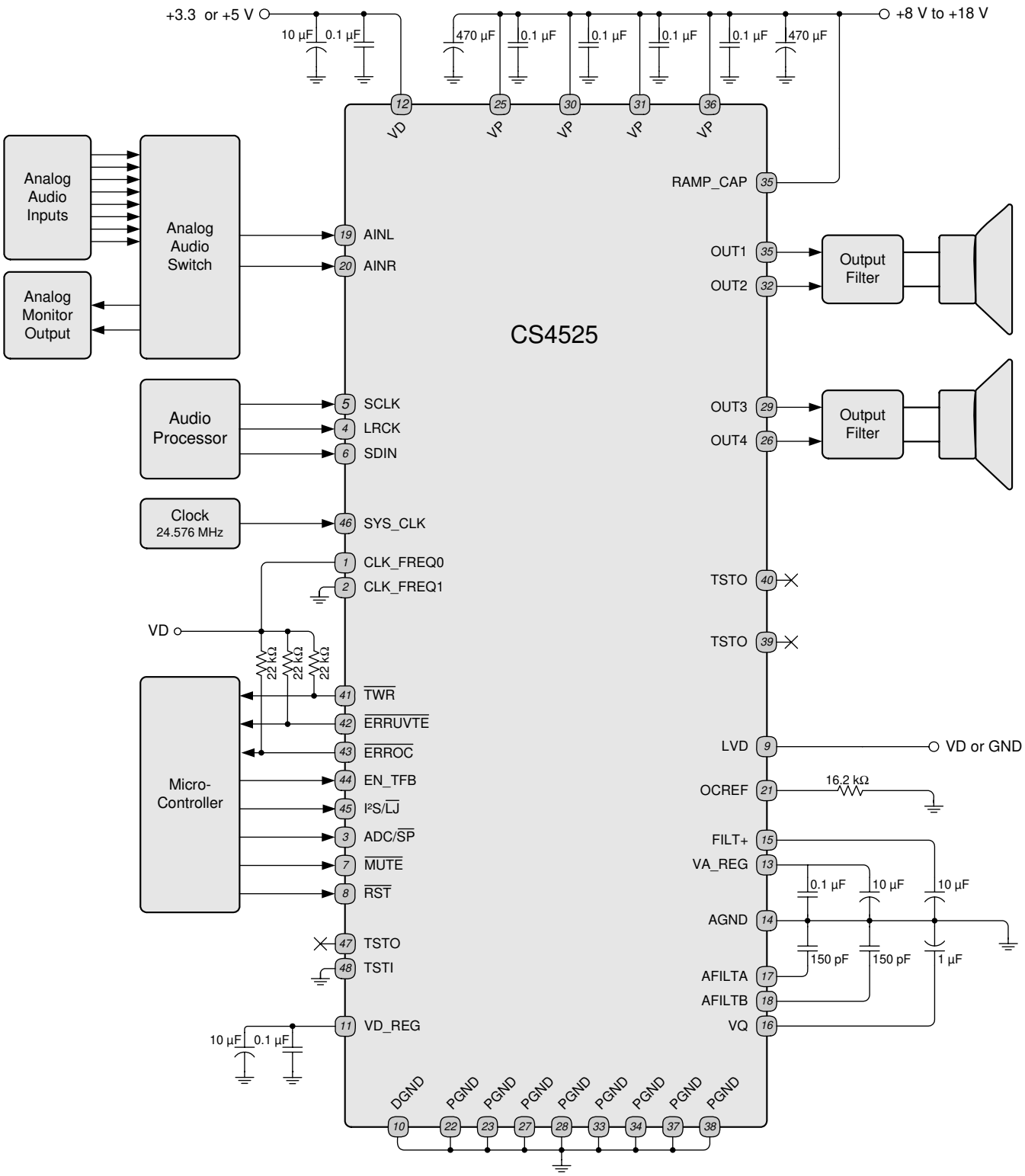


Figure 2. Typical Connection Diagram - Hardware Mode

4. TYPICAL SYSTEM CONFIGURATION DIAGRAMS

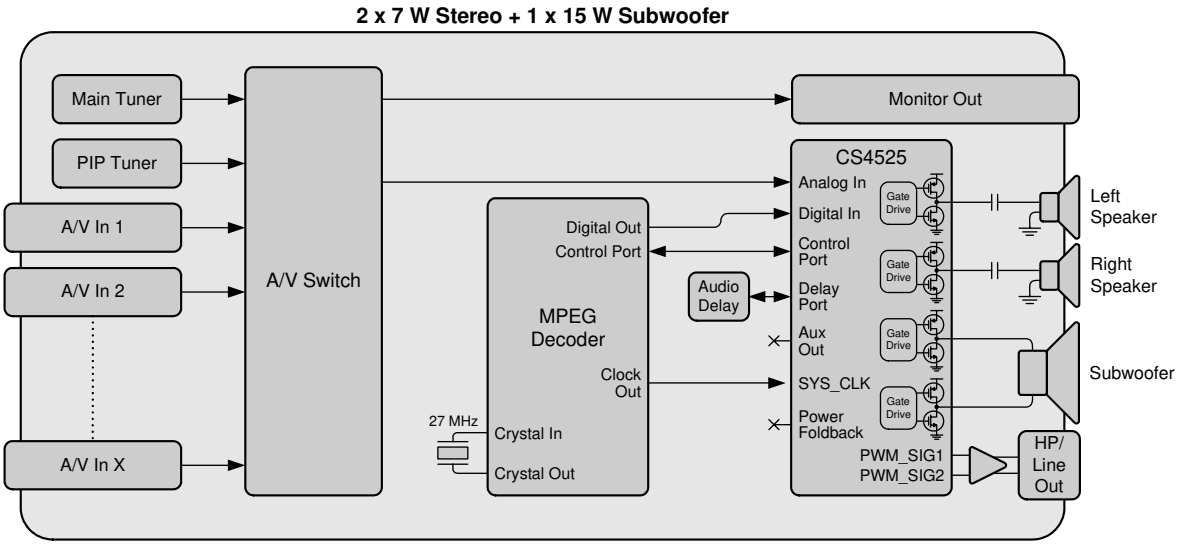


Figure 3. Typical System Configuration 1

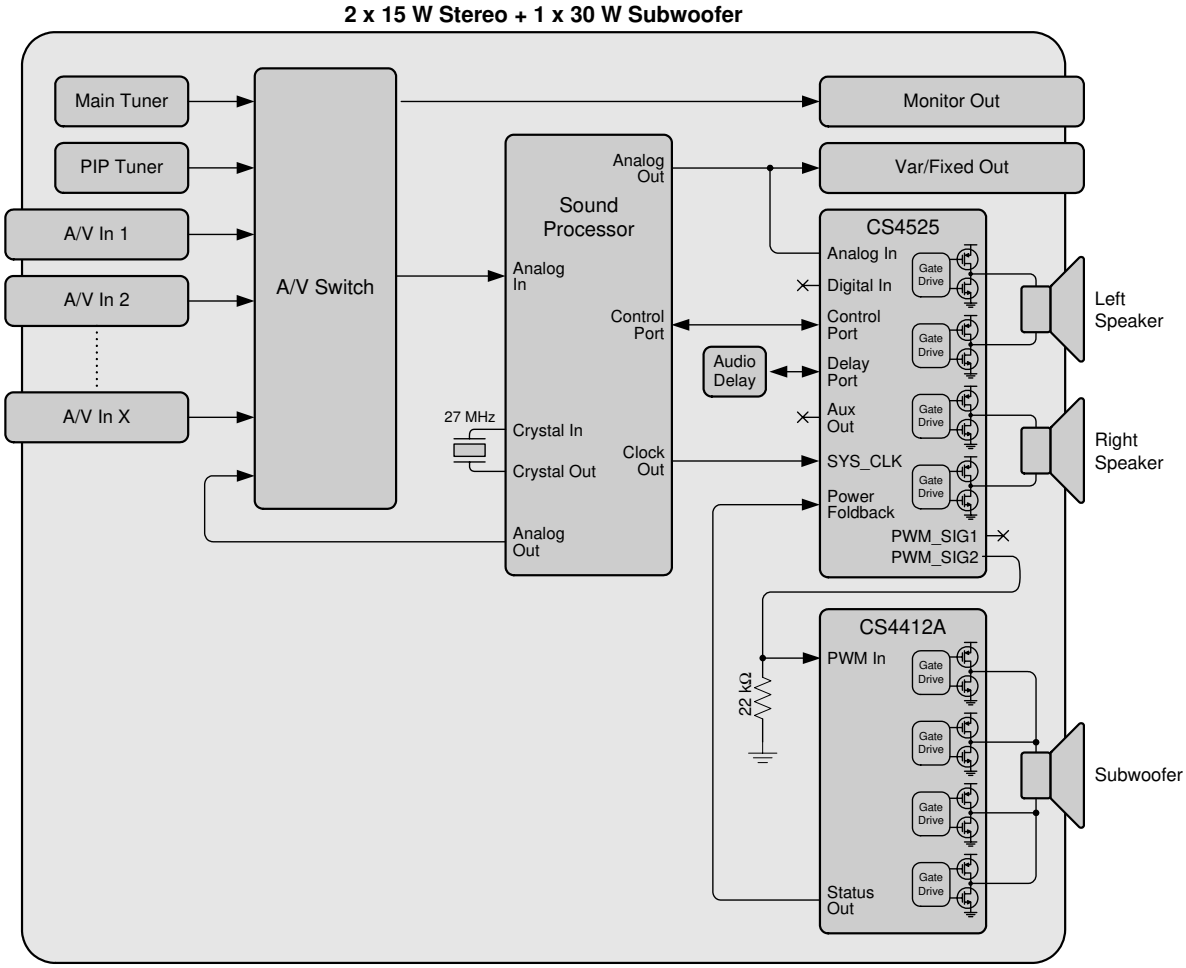


Figure 4. Typical System Configuration 2

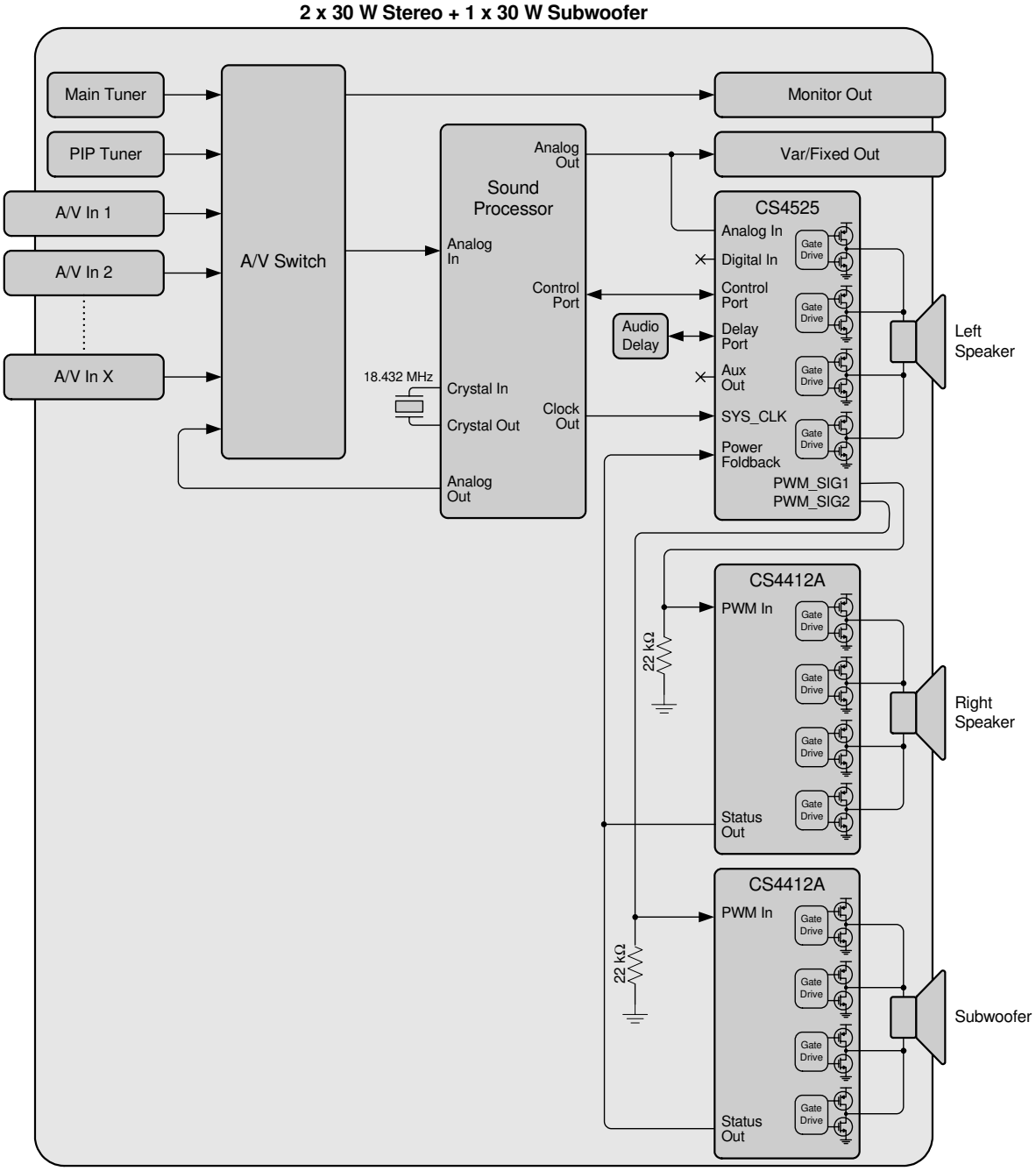


Figure 5. Typical System Configuration 3

2 x 15 W Bi-Amp Stereo with Subwoofer Output

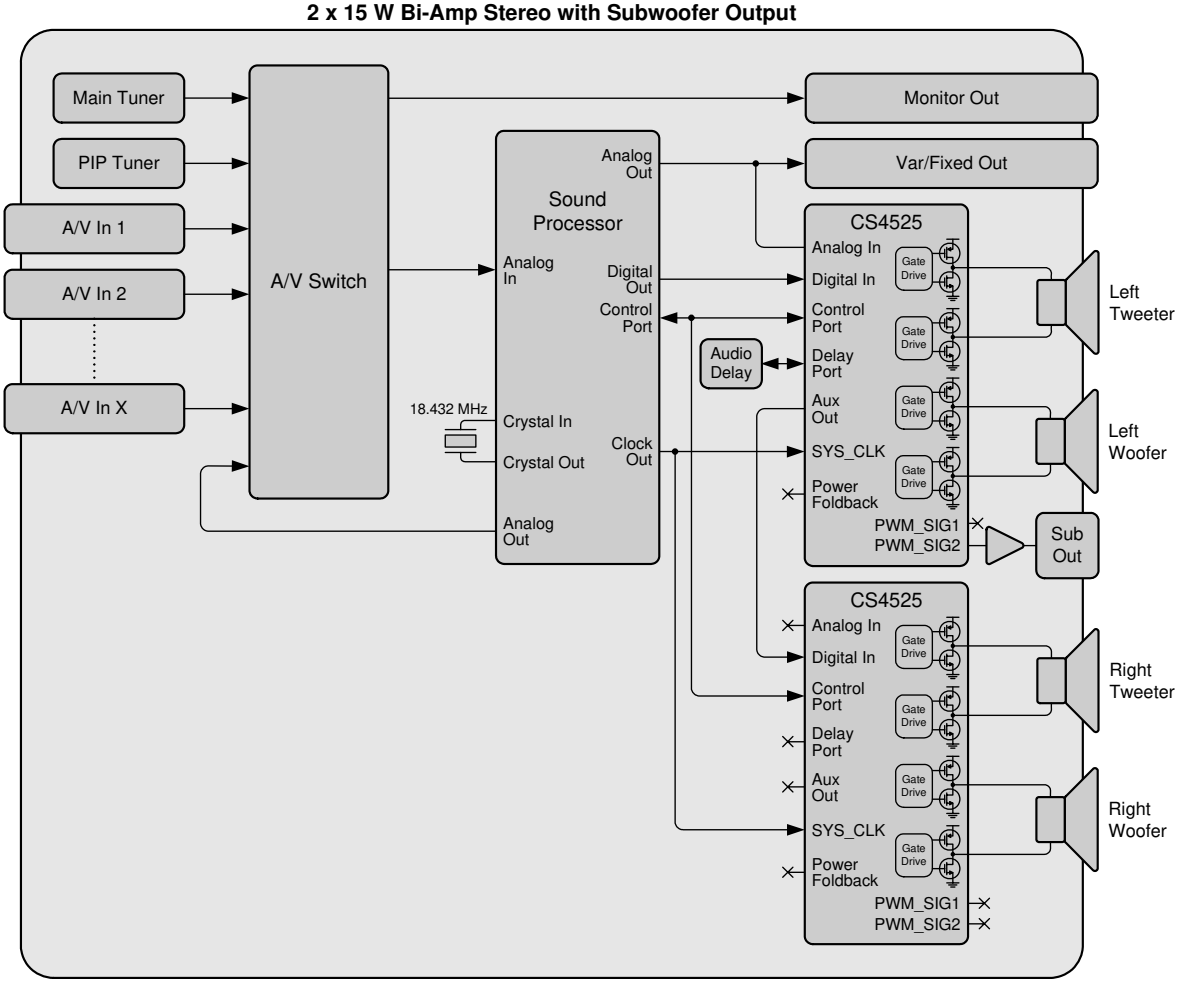


Figure 6. Typical System Configuration 4

5. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

AGND = DGND = PGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supply						
Digital and Analog Core	(Note 1)	VD	2.375	2.5	2.625	V
		VD	3.135	3.3	3.465	V
		VD	4.75	5.0	5.25	V
Amplifier Outputs		VP	8.0	-	18.0	V
Temperature						
Ambient Temperature	Commercial	T_A	-10	-	+70	°C
Junction Temperature		T_J	-10	-	+125	°C

Notes: 1. For VD = 2.5 V, VA_REG and VD_REG must be connected to VD. See section 6.7 on page 63 for details.

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = PGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Power Stage	Outputs Switching and Under Load	VP	-0.3	19.8	V
Power Stage	No Output Switching	VP	-0.3	23.0	V
Digital and Analog Core		VD	-0.3	6.0	V
Inputs					
Input Current	(Note 2)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 3)	V_{INA}	AGND - 0.7	VA_REG + 0.7	V
Digital Input Voltage	(Note 3)	V_{IND}	-0.3	VD + 0.4	V
Temperature					
Ambient Operating Temperature - Power Applied	Commercial	T_A	-20	+85	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

3. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): AGND = DGND = PGND = 0 V; All voltages with respect to ground; T_A = 25°C; VD = 3.3 V; Input Signal: 1 kHz sine wave through the recommended passive input filter shown in Figure 28 on page 61; Capacitor values connected to AFILTA, AFILTB, FILT+, VQ, VD_REG, and VA_REG as shown in Figure 1 on page 13; Sample Frequency = 48 kHz; 10 Hz to 20 kHz Measurement Bandwidth; Power outputs in power-down state (PDnOut1 = 1, PDnOut2 = 1, PDnOut3/4 = 1).

Parameter		Min	Typ	Max	Unit
Dynamic Range (Note 4)	A-weighted	90	95	-	dB
	unweighted	87	92	-	dB
Total Harmonic Distortion + Noise	-1 dB	-	-86	-77	dB
	-20 dB	-	-72	-	dB
	-60 dB	-	-32	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.05	-	dB
Gain Drift		-	±100	-	ppm/°C
Interchannel Isolation		-	90	-	dB
Full-scale Input Voltage	VD = 2.5V (Note 5)	0.786*VD	0.827*VD	0.868*VD	Vpp
	VD = 3.3V	0.590*VD	0.621*VD	0.652*VD	Vpp
	VD = 5.0V	0.398*VD	0.419*VD	0.440*VD	Vpp
Input Impedance	(Note 6)	40	-	-	kΩ

Notes:
4. Referred to the typical full-scale voltage
5. For VD = 2.5 V, VA_REG and VD_REG must be connected to VD. See section 6.7 on page 63 for details.
6. Measured between AINx and AGND.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter		Min	Typ	Max	Unit
Passband (Frequency Response) (Note 7)	to -0.1 dB corner	0	-	0.4948	Fs
Passband Ripple		-0.09	-	0	dB
Stopband	(Note 7)	0.6677	-	-	Fs
Stopband Attenuation		48.4	-	-	dB
Total Group Delay		-	2.7/Fs	-	s
High-Pass Filter Characteristics					
Frequency Response	-3.0 dB	-	3.7	-	Hz
	-0.13 dB	-	24.2	-	Hz
Phase Deviation	20 Hz	-	10	-	Deg
Passband Ripple		-	-	0.17	dB
Filter Settling Time		-	10^5/Fs	-	s

Notes:
7. Filter response is clock dependent and scales with the ADC sampling frequency (Fs). With a 27.000 MHz or 24.576 MHz XTAL/SYS_CLK, Fs is equal to the applied clock divided by 512. With an 18.432 MHz XTAL/SYS_CLK, Fs is equal to the applied clock divided by 384.

PWM POWER OUTPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): AGND = DGND = PGND = 0 V; All voltages with respect to ground; T_A = 25°C; VD = 3.3 V; VP = 18 V; R_L = 8 Ω for full-bridge, R_L = 4 Ω for half-bridge and parallel full-bridge; OutputDly[3:0] = 1111; PhaseShift = 1 for half-bridge, PhaseShift = 0 for full-bridge and parallel full-bridge; Input Signal: full-scale 997 Hz sine wave through serial audio input port, 48 kHz sample rate; Capacitor values connected to AFILTA, AFILTB, FILT+, VQ, VD_REG, and VA_REG as shown in Figure 1 on page 13; PWM Switch Rate = 384 kHz; 10 Hz to 20 kHz Measurement Bandwidth; Performance measurements taken through AES17 filter.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Power Output per Channel						
Stereo Full-Bridge	P_O	THD+N < 10%	-	15	-	W
		THD+N < 1%	-	12	-	W
Half-Bridge		THD+N < 10%	-	7	-	W
		THD+N < 1%	-	5.5	-	W
Parallel Full-Bridge		THD+N < 10%	-	30	-	W
		THD+N < 1%	-	23.5	-	W
Total Harmonic Distortion + Noise						
Stereo Full-Bridge	THD+N	P_O = 1 W	-	0.05	-	%
		P_O = 0 dBFS = 11.3 W	-	0.10	-	%
Half-Bridge		P_O = 1 W	-	0.12	-	%
		P_O = 0 dBFS = 5.0 W	-	0.28	-	%
Parallel Full-Bridge		P_O = 1 W	-	0.1	-	%
		P_O = 0 dBFS = 22.6 W	-	0.3	-	%
Dynamic Range						
Stereo Full-Bridge	DYR	P_O = -60 dBFS, A-Weighted	-	102	-	dB
		P_O = -60 dBFS, Unweighted	-	99	-	dB
Half-Bridge		P_O = -60 dBFS, A-Weighted	-	99	-	dB
		P_O = -60 dBFS, Unweighted	-	96	-	dB
Parallel Full-Bridge		P_O = -60 dBFS, A-Weighted	-	102	-	dB
		P_O = -60 dBFS, Unweighted	-	99	-	dB
MOSFET On Resistance	$R_{DS(ON)}$	I_d = 0.5 A, T_J = 50°C	-	280	-	mΩ
Efficiency	h	P_O = 2 x 15 W, R_L = 8 Ω	-	85	-	%
Minimum Output Pulse Width	PW_{min}	No Load	-	50	-	ns
Rise Time of OUTx	t_r	Resistive Load	-	20	-	ns
Fall Time of OUTx	t_f	Resistive Load	-	20	-	ns
PWM Output Over-Current Error Trigger Point	I_{CE}	T_A = 25°C, OCREF = 16.2 kΩ	-	2.5	-	A
		T_A = 25°C, OCREF = 18 kΩ	-	2.1	-	A
		T_A = 25°C, OCREF = 22 kΩ	-	1.7	-	A
Junction Thermal Warning Trigger Point	T_{TW}		-	105	-	°C
Junction Thermal Error Trigger Point	T_{TE}		-	125	-	°C
VP Under-Voltage Error Falling Trigger Point	V_{UVFALL}	T_A = 25°C	-	4.7	4.9	V
VP Under-Voltage Error Rising Trigger Point	V_{UVRISE}	T_A = 25°C	-	4.95	5.4	V

SERIAL AUDIO INPUT PORT SWITCHING SPECIFICATIONS

AGND = DGND = PGND = 0 V; T_A = 25°C; VD = 3.3 V; Inputs: Logic 0 = DGND; Logic 1 = VD.

Parameters	Symbol	Min	Nominal	Max	Units
Supported Input Sample Rates	F_{SI}	28.5 39.5 39.5 86.4	32 44.1 48 96	35.2 52.8 52.8 105.6	kHz kHz kHz kHz
LRCK Duty Cycle		45	-	55	%
SCLK Frequency (Note 8),(Note 9)	$1/t_p$	F_{SI}*2*N_{bits}	-	$F_{CLK}/3$	Hz
SCLK Duty Cycle		45	-	55	%
LRCK Setup Time Before SCLK Rising Edge	$t_{s(LK-SK)}$	40	-	-	ns
SDIN Setup Time Before SCLK Rising Edge	$t_{s(SD-SK)}$	25	-	-	ns
SDIN Hold Time After SCLK Rising Edge	t_h	10	-	-	ns
$\overline{RST}$ pin Low Pulse Width (Note 10)		1	-	-	ms

Notes:

8. F_{CLK} is the frequency of the crystal connected to the XTI/XTO pins or the input SYS_CLK signal.
9. N_{bits} is the number of bits per sample of the serial digital input.
10. After powering up the CS4525, $\overline{RST}$ should be held low until the power supplies and clocks are stable.

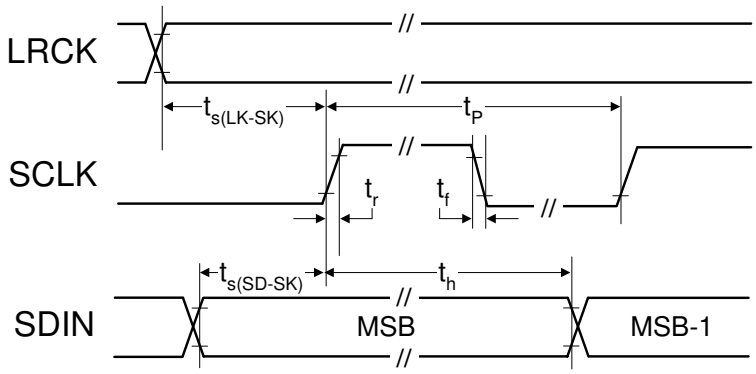


Figure 7. Serial Audio Input Port Timing

AUX SERIAL AUDIO I/O PORT SWITCHING SPECIFICATIONS

AGND = DGND = PGND = 0 V; T_A = 25°C; VD = 3.3 V; AUX_SDOUT & DLY_SDOUT C_L = 15 pF; Inputs: Logic 0 = DGND; Logic 1 = VD; (Note 11).

Parameters		Symbol	Min	Typ	Max	Units
Input Source: Analog Inputs (Internal ADC)						
Output Sample Rate	ClkFreq[1:0] = '00' ClkFreq[1:0] = '01' ClkFreq[1:0] = '10'	F_{SO}	- - -	$F_{CLK}/384$ $F_{CLK}/512$ $F_{CLK}/512$	- - -	Hz Hz Hz
AUX_LRCK Duty Cycle			-	50	-	%
AUX_LRCK Period			-	$1/F_{SO}$	-	s
AUX_SCLK Frequency	ClkFreq[1:0] = '00' ClkFreq[1:0] = '01' ClkFreq[1:0] = '10'	F_{SCLKO}	- - -	$48*F_{SO}$ $64*F_{SO}$ $64*F_{SO}$	- - -	Hz Hz Hz
AUX_SCLK Duty Cycle			-	50	-	%
AUX_SCLK Period			-	$1/F_{SCLKO}$	-	s
Input Source: Serial Audio Input Port						
Output Sample Rate	F_{S-In} = 32kHz, 44.1 kHz, 48 kHz F_{S-In} = 96 kHz	F_{SO}	- -	F_{SI} $F_{SI}/2$	- -	Hz Hz
AUX_LRCK Duty Cycle	(Note 13)		45	-	55	%
AUX_LRCK Period	(Note 12, 13)		$T_{SI} - T_{CLK}$	T_{SI}	$T_{SI} + T_{CLK}$	s
AUX_SCLK Frequency (Note 14)	F_{S-In} = 32kHz, 44.1 kHz, 48 kHz F_{S-In} = 96 kHz		- -	F_{SCLKI} $F_{SCLKI}/2$	- -	Hz Hz
AUX_SCLK Duty Cycle			30	-	70	%
AUX_SCLK Period (Note 13, 14)	F_{S-In} = 32kHz, 44.1 kHz, 48 kHz F_{S-In} = 96 kHz		$T_{SCLKI} - T_{CLK}$ $2*T_{SCLKI} - T_{CLK}$	T_{SCLKI} $2*T_{SCLKI}$	$T_{SCLKI} + T_{CLK}$ $2*T_{SCLKI} + T_{CLK}$	s s
Input Source: Analog Inputs or Serial Audio Input Port						
AUX_LRCK Rising Edge to AUX_SCLK Falling Edge		t_{LTSF}	-	-	20	ns
AUX_SCLK Rising Edge to Data Output Valid		t_{SRDV}	-	-	T_{CLK} + 20	ns
DLY_SDIN Setup Time Before AUX_SCLK Rising Edge		t_{DIS}	25	-	-	ns
DLY_SDIN Hold Time After AUX_SCLK Rising Edge		t_{DIH}	10	-	-	ns

Notes:

11. F_{CLK} is the frequency of the crystal connected to the XTI/XTO pins or the input SYS_CLK signal. $T_{CLK} = 1/F_{CLK}$.
12. F_{SI} is the frequency of the input LRCK signal. $T_{SI} = 1/F_{SI}$
13. May vary during normal operation.
14. F_{SCLKI} is the frequency of the input SCLK signal. $T_{SCLKI} = 1/F_{SCLKI}$.

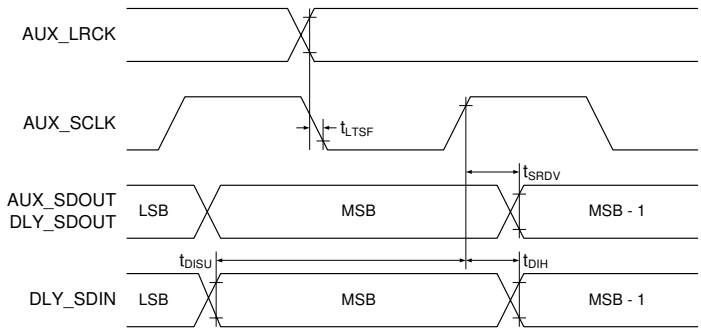


Figure 8. AUX Serial Port Interface Master Mode Timing

XTI SWITCHING SPECIFICATIONS

Parameter		Symbol	Min	Typ	Max	Unit
External Crystal Operating Frequency (Note 15)	ClkFreq[1:0] = '00' ClkFreq[1:0] = '01' ClkFreq[1:0] = '10'	F_{CLK}	18.240 24.330 26.730	18.432 24.576 27.000	18.617 24.822 27.270	MHz MHz MHz
XTI Duty Cycle			45	50	55	%

Notes: 15. See "Clock Frequency (ClkFreq[1:0])" on page 69.

SYS_CLK SWITCHING SPECIFICATIONS

AGND = DGND = PGND = 0 V; T_A = 25°C; VD = 3.3 V; Input: Logic 0 = DGND; Logic 1 = VD, SYS_CLK Output: C_L = 20 pF.

Parameter		Symbol	Min	Typ	Max	Unit
External Clock Operating Frequency (Note 15)	ClkFreq[1:0] = '00' ClkFreq[1:0] = '01' ClkFreq[1:0] = '10'	F_{CLK}	18.240 24.330 26.730	18.432 24.576 27.000	18.617 24.822 27.270	MHz MHz MHz
Rising Edge $\overline{RST}$ to start of SYS_CLK		t_{sclko}	-	$1024*t_{sclki}$	-	
SYS_CLK Period		t_{sclki}	37.04	-	54.25	ns
SYS_CLK Duty Cycle			45	50	55	%
SYS_CLK high time		t_{clkih}	16.67	-	29.84	ns
SYS_CLK low time		t_{clkil}	16.67	-	29.84	ns

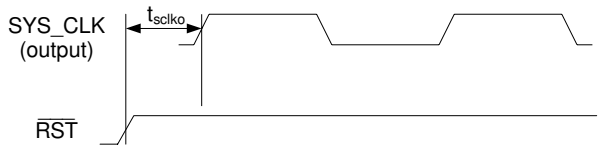


Figure 9. SYS_CLK Timing from Reset

PWM_SIGX SWITCHING SPECIFICATIONS

AGND = DGND = PGND = 0 V; T_A = 25°C; VD = 3.3 V; Load = 10 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time of PWM_SIGx	t_r	-	2.1	-	ns
Fall Time of PWM_SIGx	t_f	-	1.4	-	ns

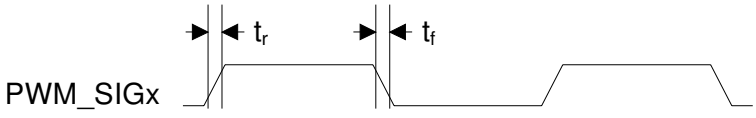


Figure 10. PWM_SIGX Timing

I²C CONTROL PORT SWITCHING SPECIFICATIONS

AGND = DGND = PGND = 0 V; T_A = 25°C; VD = 3.3 V; Inputs: Logic 0 = DGND; Logic 1 = VD; SDA C_L = 30 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 16)	t_{hdd}	10	-	ns
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes: 16. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

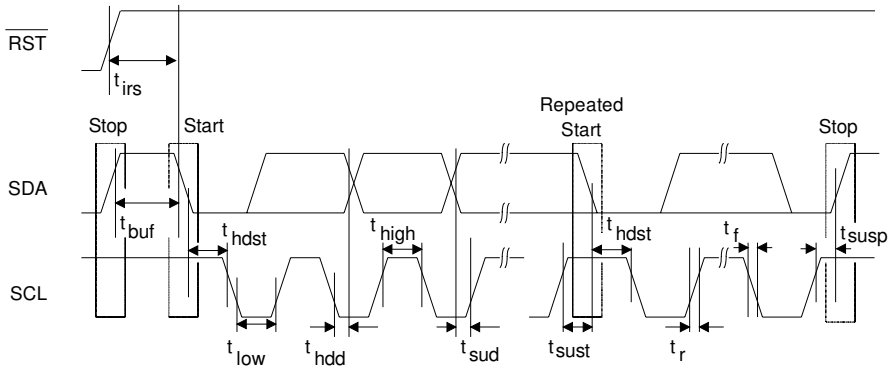


Figure 11. Control Port Timing - I²C

DC ELECTRICAL CHARACTERISTICS

AGND = DGND = PGND = 0 V; All voltages with respect to ground; PWM switch rate = 384 kHz; Unless otherwise specified.

Parameters		Min	Typ	Max	Units
Normal Operation (Note 17)					
Power Supply Current	VD = 3.3 V	-	54	-	mA
Power Dissipation	VD = 3.3 V	-	180	-	mW
Power-Down Mode (Note 18)					
Power Supply Current	VD = 3.3 V	-	2.8	-	mA
VD_REG Characteristics					
Nominal Voltage		2.25	2.5	2.75	V
DC current source		-	-	3	mA
VA_REG Characteristics					
Nominal Voltage		2.25	2.5	2.75	V
DC current source		-	-	1	mA
VQ Characteristics					
Nominal Voltage		-	0.5*VA_REG	-	V
Output Impedance		-	23	-	kΩ
DC current source/sink	(Note 19)	-	-	10	µA
Filt+ Nominal Voltage		-	VA_REG	-	V
Power Supply Rejection Ratio (Note 20)	1 kHz 60 Hz	- -	60 40	- -	dB dB

Notes:

17. Normal operation is defined as $\overline{RST}$ = HI.
18. Power-Down Mode is defined as $\overline{RST}$ = LOW with all input lines held static.
19. The DC current drain represents the allowed current from the VQ pin due to typical leakage through the electrolytic de-coupling capacitors.
20. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will increase the PSRR.

DIGITAL INTERFACE SPECIFICATIONS

AGND = DGND = PGND = 0 V; All voltages with respect to ground; Unless otherwise specified.

Parameters		Symbol	Min	Max	Units
Digital Interface Signal Characteristics (Note 21)					
High-Level Input Voltage		V_{IH}	0.75*VD_REG	-	V
Low-Level Input Voltage		V_{IL}	-	0.20*VD_REG	V
High-Level Output Voltage	I_o=2 mA	V_{OH}	0.90*VD	-	V
Low-Level Output Voltage	I_o=2 mA	V_{OL}	-	0.2	V
Input Leakage Current		I_{in}	-	±10	uA
Input Capacitance			-	8	pF
PWM_SIGx Characteristics					
High-Level PWM_SIGx Output Voltage	I_o=2 mA	V_{OHPS}	0.90*VD_REG	-	V
Low-Level PWM_SIGx Output Voltage	I_o=2 mA	V_{OLPS}	-	0.2	V

Notes:

21. Digital interface signals include all pins sourced from the VD supply as shown in "Digital I/O Pin Characteristics" on page 12.