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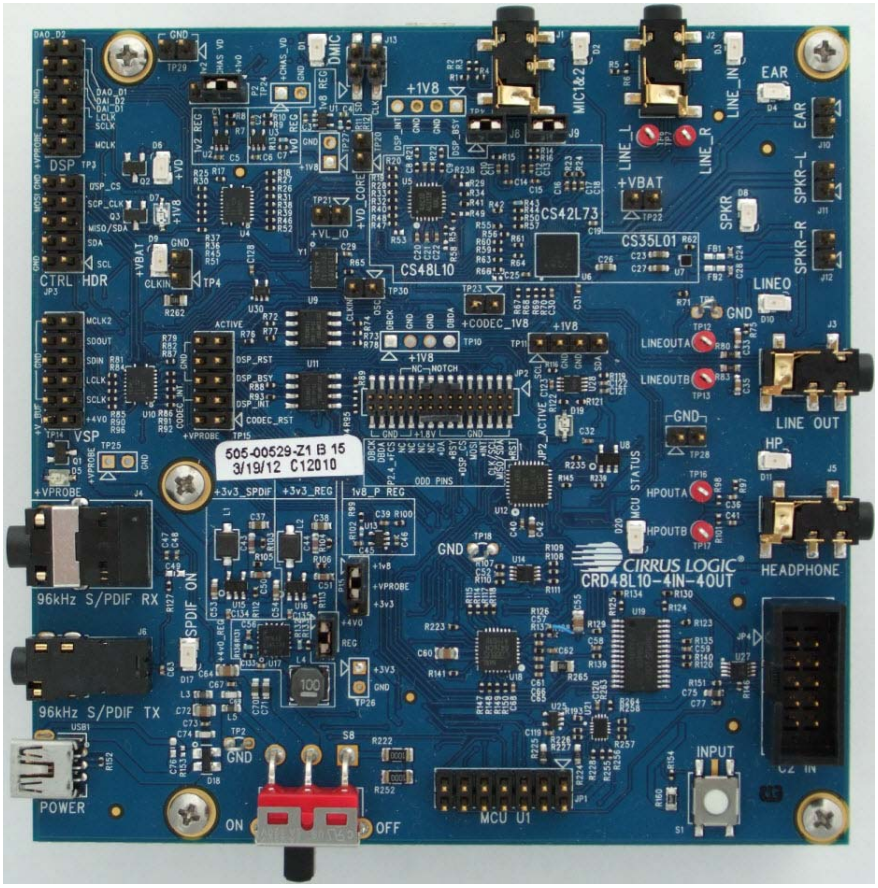
CIRRUS LOGIC®

**CS48L10**
***32-Bit Audio DSP Product***

# CRD48L10-4in4out

## Board Manual





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To find the one nearest you, go to www.cirrus.com.

## Chapter 1
## Introduction to the CRD48L10-4in4out Board



## Chapter 2
## Input/Output Specifications



## Chapter 3
## Standalone Modes



## Chapter 4
## Quick Start for the CRD48L10-4in4out

# Chapter 1
# Introduction to the CRD48L10-4in4out Board

**Table 1-1. CRD48L10 Kit Contents**

| Item | Quantity |
|---|---|
| Cirrus Logic CRD48L10 Board | 1 |
| Cirrus Logic CRD48L10 MCU USER INTERFACE Board | 1 |
| Cirrus Logic CDB-MCU-DEBUG Board | 1 |
| USB cable A-Mini | 2 |
| Stereo audio cables RCA female, 3.5 mm male | 1 |
| 5x2 ribbon cable | 1 |
| 7x2 ribbon cable | 1 |
| 15x2 ribbon cable | 1 |
| TOSLINK female to TOSLINK mini male adapter | 2 |
| Doc card universal DSP | 1 |
| Doc evaluation board disclaimer notice | 1 |

## 1.1 Requirements

This section lists the requirements for the CRD48L10-4in4out evaluation board:

- PC requirements
  - Microsoft® Windows XP™ or Windows 7™ operating system.
  - USB 2.0 support
- Software requirements
  - Cirrus DSP Software Development Kit (available from your local Cirrus Logic representative)
- Support hardware requirements
  - Digital or analog audio source (for example, DVD player, PC with a digital audio card/device)
  - Speakers for audio playback (for example, powered PC speakers, AVR/amp + speakers, stereo speakers) or headphones
- Cabling requirements
  - Digital audio inputs—TOSLINK optical or coaxial cable with 1/8” plug (connect to digital audio card or DVD player); audio stream input/output (ASIO) card.
  - Digital audio output—TOSLINK optical cable
  - Analog Audio Inputs—1/8” stereo plug microphone or line in cable (connect microphone or line in to ADC)
  - Analog Audio Outputs—1/8” stereo plug for lineout and headphones, speaker/speakerphone outputs use 2x1 headers.

## 1.2 CRD48L10-4in4out Main Board Description

Fig. 1-1 shows a detailed block diagram of the CRD48L10-4in4out board.

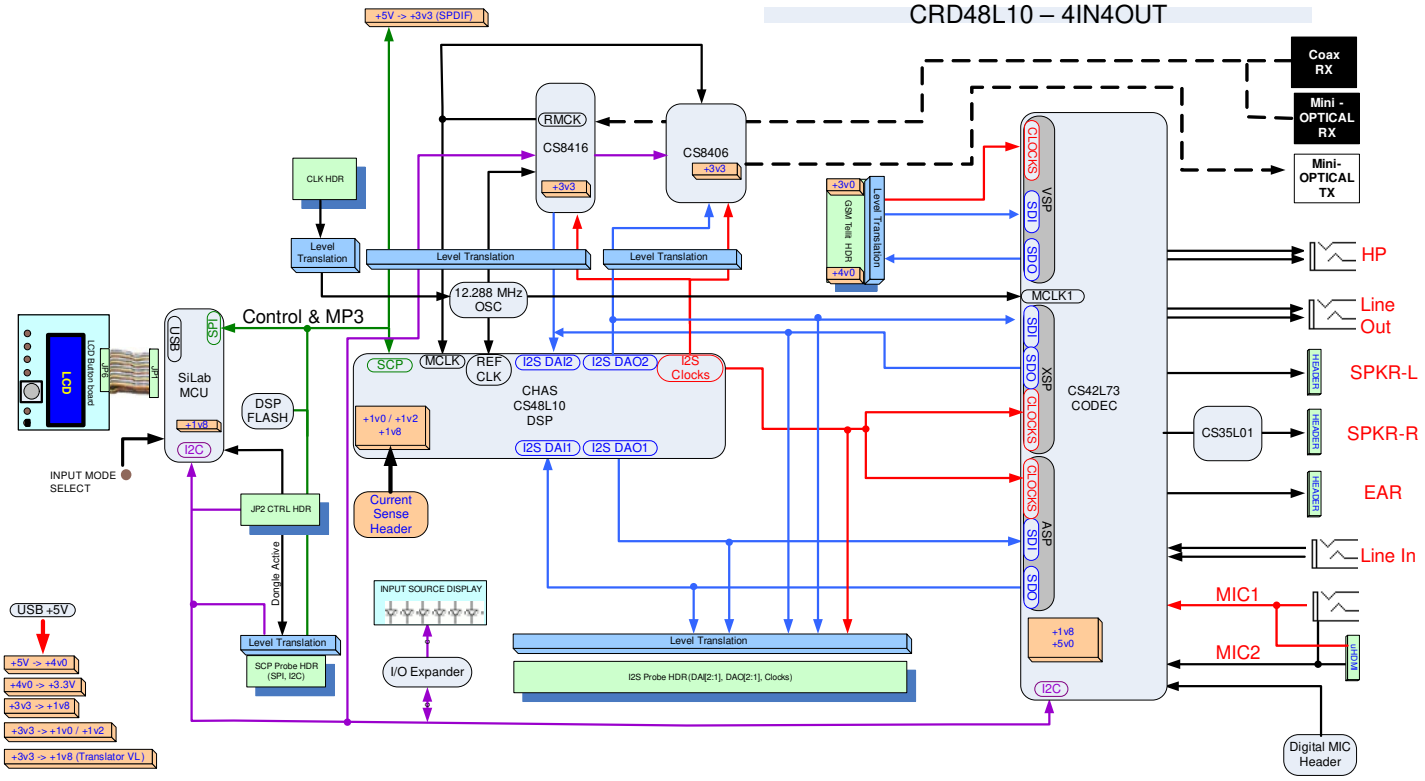


**Figure 1-1. CRD48L10-4in4out Block Diagram**

The main components to be familiar with on the board are:

- CS48L10 DSP
- CS42L73 Ultra Low-power CODEC
- CS35L01 Mono Class-D Amplifier
- CS8416 S/PDIF Rx
- CS8406 S/PDIF Tx
- Silicon Labs™ C8051F930 MCU

The main purpose of this board is to allow a customer to evaluate the Cirrus Logic CS48L10 DSP and other Cirrus Logic analog semiconductors in a complete audio subsystem.

The Silicon Labs MCU handles the SPI, I²C, and GPIO to control the board components. USB control of the DSP is possible by connecting the CDB-MCU-DEBUG dongle to the JP2 header.

## 1.3 Introduction to the CRD48L10 Kit

Fig. 1-2 shows a picture of the CRD48L10-4in4out with labels on the important connections. Fig. 1-3 shows a picture of the CRD48L10 MCU-USER-INTERFACE board. Fig. 1-4 shows a picture of the CDB-MCU-DEBUG board. Fig. 1-5 shows a picture of the supplied ribbon cables. Fig. 1-6 shows a picture of the supplied mini-USB and 1/8” to RCA cables. Fig. 1-7 shows a picture of the TOSLINK to mini TOSLINK adapter.

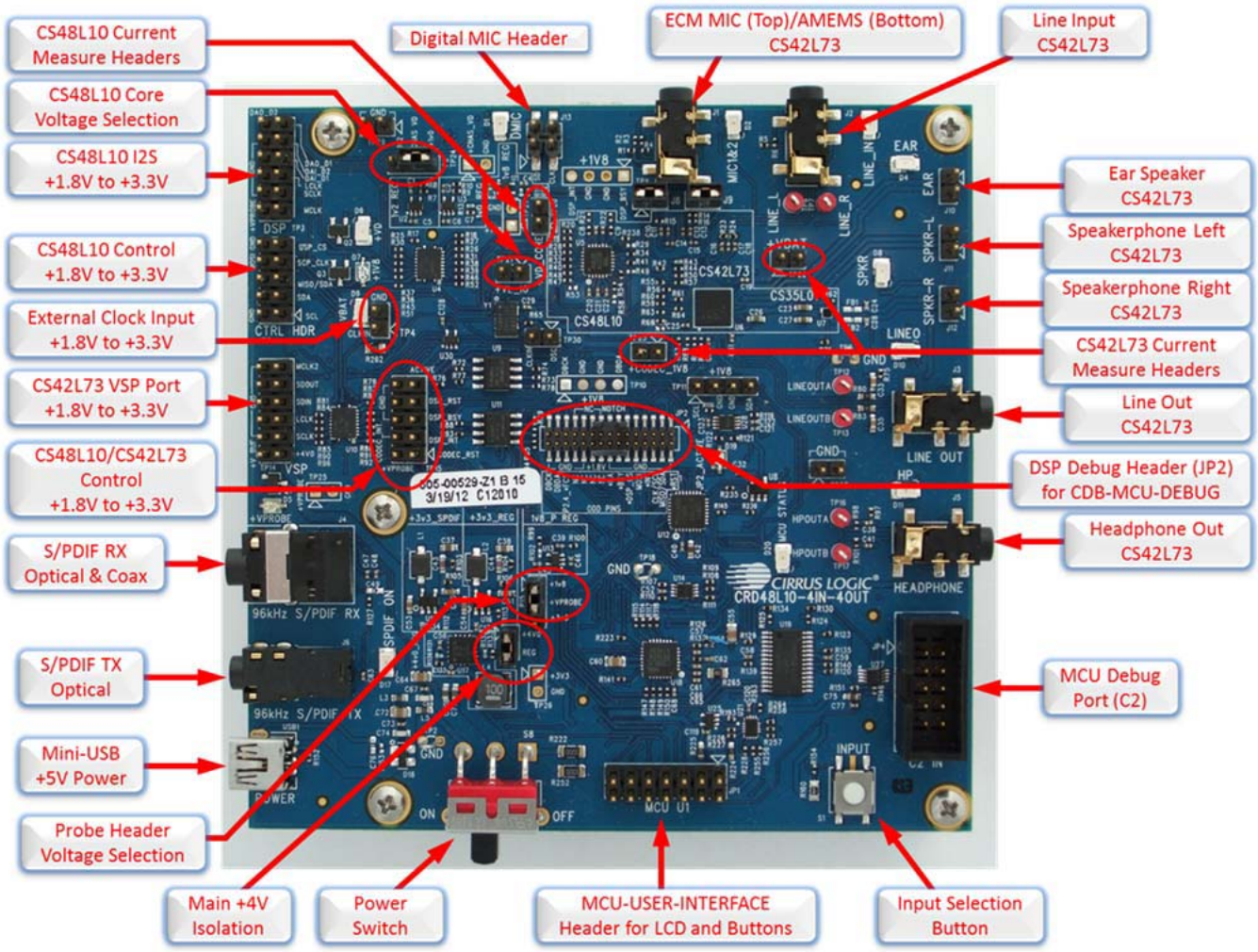


**Figure 1-2. CRD48L10-4in4out**

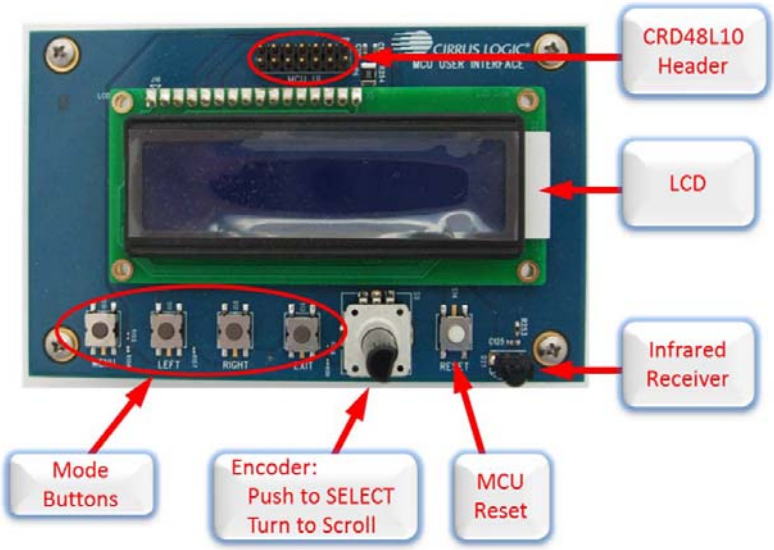


**Figure 1-3. MCU-USER-INTERFACE Board**

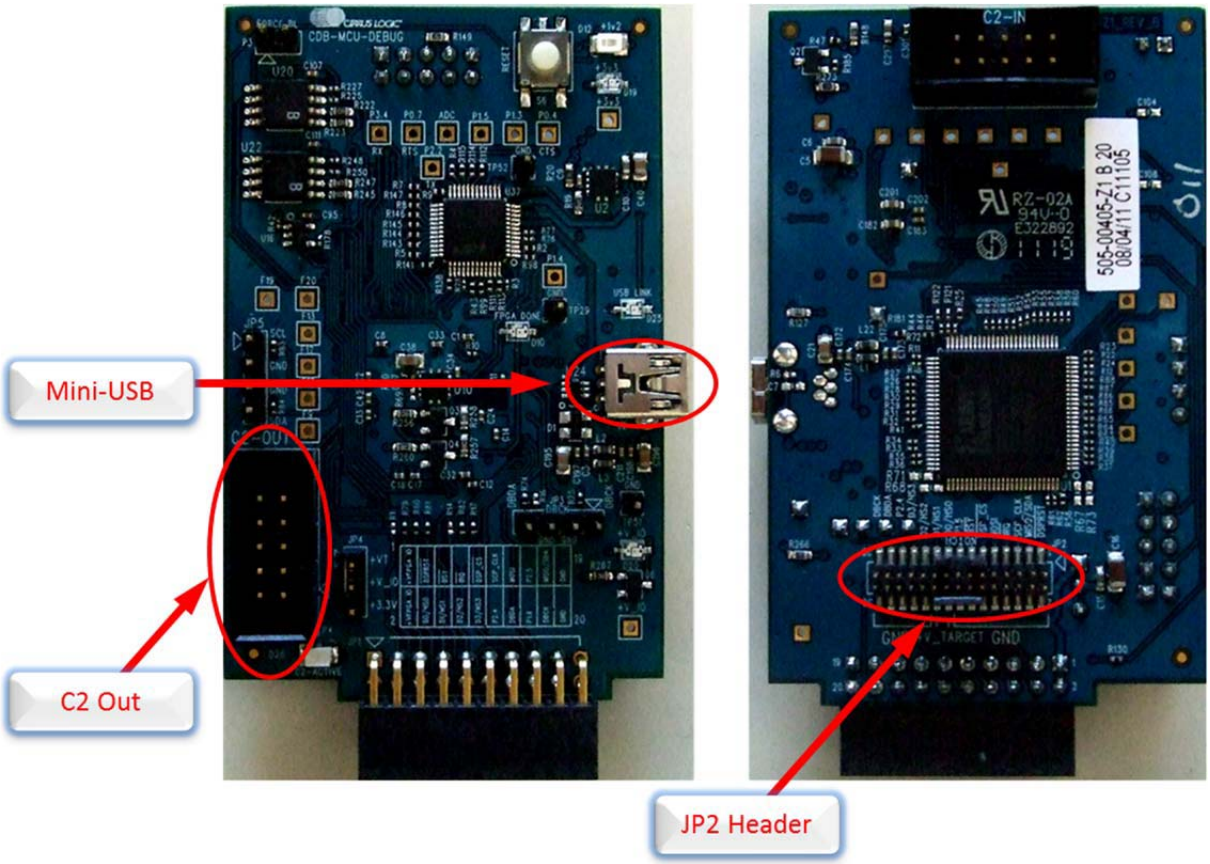


**Figure 1-4. CDB-MCU-DEBUG Board**

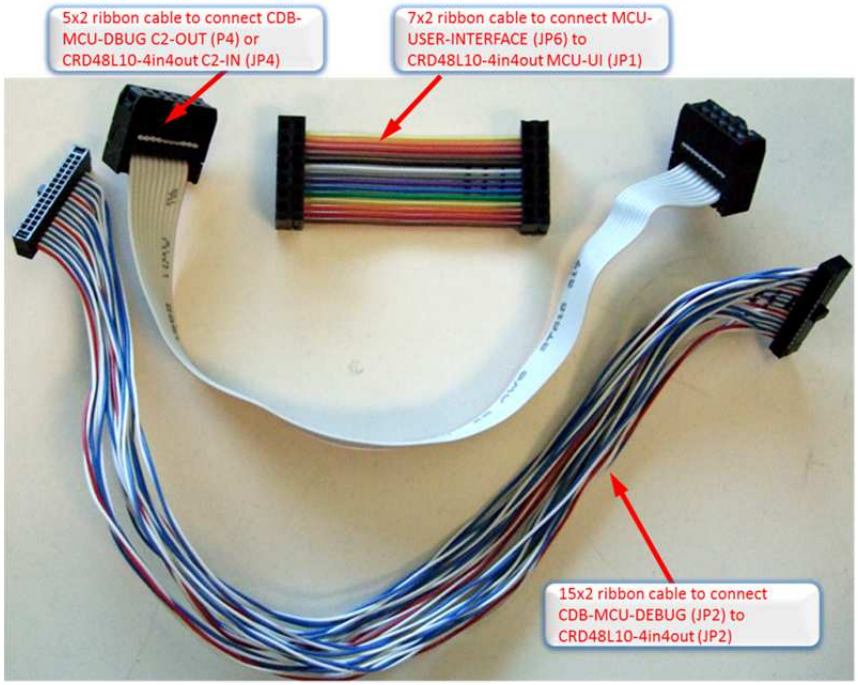


**Figure 1-5. Ribbon Cables**

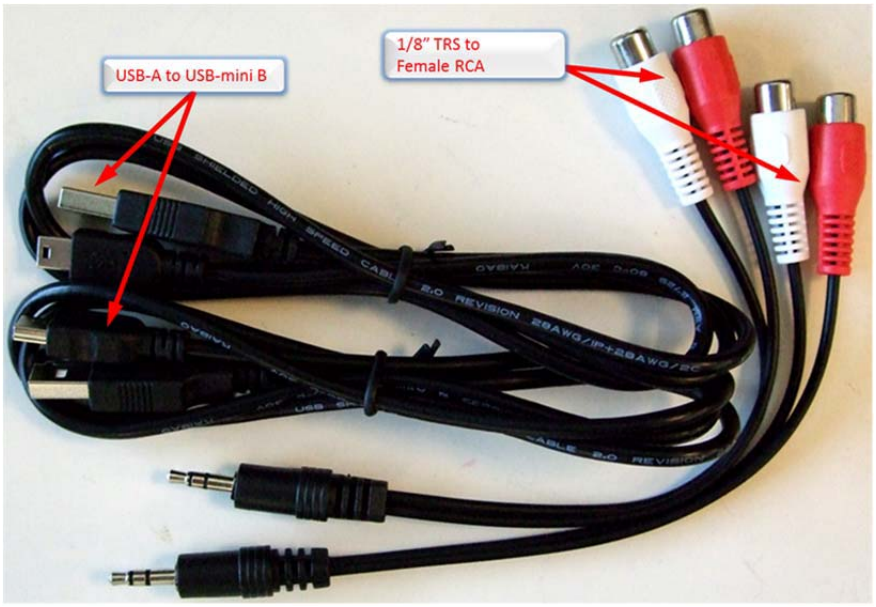


**Figure 1-6. USB and 1/8" to RCA Cables**

**Figure 1-7. TOSLINK to Mini Male Adapter**

# Chapter 2
# Input/Output Specifications

## 2.1 Audio Inputs

### 2.1.1 Analog Line Input

- Connector Type: 1/8 inch (3.5mm) stereo Female
- Absolute Maximum Signal Level: +2.1 V
- Absolute Minimum Signal Level: –0.3 V
- Full Scale Amplitude (PGA VOL = 0 dB): 1.44 Vpp
- Reference Designators: J2 (LINE IN)

### 2.1.2 Analog Microphone Input

- Connector Type: 1/8 inch (3.5mm) stereo Female
- Absolute Maximum Signal Level: +2.1 V
- Absolute Minimum Signal Level: –0.3 V
- Full Scale Amplitude (PGA VOL = 0 dB/MIC PREAMP = +10 dB): 464 mVpp
- Full Scale Amplitude (PGA VOL = 0 dB/MIC PREAMP = +20 dB): 144 mVpp
- Reference Designators: J1 (MIC 1 & 2)

### 2.1.3 Optical Digital Input

- Connector Type: Fiber Optic Mini TOSLINK RX for Digital Audio
- Reference Designators: J4 (OPTICAL)

### 2.1.4 Coaxial Digital Input

- Connector Type: 1/8 inch (3.5mm) stereo Female
- Absolute Maximum Signal Level: +3.6 V
- Absolute Minimum Signal Level: –0.3 V
- Reference Designators: J4 (COAXIAL)

### 2.1.5 Digital Microphone Inputs

- Connector Type: 0.1 inch Male Header
- Absolute Maximum Signal Level: +2.1 V
- Absolute Minimum Signal Level: –0.3 V
- Reference Designators: J13 (DMIC)

### 2.1.6 I²S Digital Inputs

- Connector Type: 0.1 inch Male Header
- Absolute Maximum Signal Level: +6.5 V
- Absolute Minimum Signal Level: –0.5 V
- Reference Designators: TP3 (DSP), TP14 (VSP)

## 2.2 Audio Outputs

### 2.2.1 Analog Line-level Outputs

- Connector Type: 1/8 inch (3.5mm) stereo Female
- Full Scale Output: 2.9 Vpp
- Reference Designators: J3 (LINE OUT)

### 2.2.2 Headphone Output

- Connector Type: 1/8 inch (3.5mm) stereo Female
- Full Scale Output: 1.5 Vpp
- Power: 2 x 17 mW (at THD+N = –60 dB)
- Minimum Load: 16 ohms
- Reference Designator: J5 (HEADPHONE)

**Note:** This output has the same data as J3 (LINE OUT).

### 2.2.3 Ear Speaker Output

- Connector Type: 100-MIL Male Header (2x1)
- Full Scale Differential Output: 2.3 Vpp (Digital Volume = –2.5 dB)
- Power: 0.51 W (at THD+N = –60 dB)
- Minimum Load: 16 ohms
- Reference Designator: J10 (EAR)

### 2.2.4 Speakerphone Left Output

- Connector Type: 100-MIL Male Header (2x1)
- Full Scale Differential Output: 5.8 Vpp (Digital Volume = –5.5 dB)
- Power: 0.53 W (at THD+N = –62 dB)
- Minimum Load: 8 ohms
- Reference Designator: J11 (SPKR-L)

### 2.2.5 Speakerphone Right Output

- Connector Type: 100-MIL Male Header (2x1)
- Full Scale Differential Output: 7.2 Vpp (Digital Volume = –3.5 dB)
- Power: 1.0 W (at THD+N = –74 dB)
- Minimum Load: 4 ohms
- Reference Designator: J12 (SPKR-R)

### 2.2.6 $I^2S$ Digital Output

- Connector Type: 100-MIL Male Header (6x2)
- Maximum Signal Level: +V_PROBE
- Reference Designators: TP3 (DSP), TP14 (VSP)

## 2.3 Digital Control Probe Points

### 2.3.1 DSP Control

- Connector Type: 100-MIL Male Header (5x2)
- Absolute Maximum Input Signal Level: +6.5 V
- Absolute Minimum Input Signal Level: –0.5 V
- Maximum Signal Output Level: +V_PROBE
- Reference Designators: JP3 (CTRL HDR), TP15

### 2.3.2 DSP Debug

- Connector Type: 100-MIL Male Header (4x1)
- Absolute Maximum Input Signal Level: +2.0 V
- Absolute Minimum Input Signal Level: –0.5 V
- Maximum Signal Output Level: +1.8 V
- Reference Designators: TP10

### 2.3.3 DSP Interrupts

- Connector Type: 100-MIL Male Header (4x1)
- Absolute Maximum Input Signal Level: +2.0 V
- Absolute Minimum Input Signal Level: –0.5 V
- Maximum Signal Output Level: +1.8 V
- Reference Designators: TP1

### 2.3.4 Codec Reset

- Connector Type: 100-MIL Male Header (5x2)
- Absolute Maximum Input Signal Level: +6.5 V
- Absolute Minimum Input Signal Level: –0.5 V
- Maximum Signal Output Level: +V_PROBE
- Reference Designators: TP15

### 2.3.5 Codec I²C

- Connector Type: 100-MIL Male Header (4x1)
- Absolute Maximum Input Signal Level: +2.0 V
- Absolute Minimum Input Signal Level: –0.5 V
- Maximum Signal Output Level: +1.8 V
- Reference Designators: TP11

### 2.3.6 Codec Interrupt

- Connector Type: 100-MIL Male Header (5x2)
- Absolute Maximum Input Signal Level: +2.0 V
- Absolute Minimum Input Signal Level: –0.5 V
- Maximum Signal Output Level: +1.8 V
- Reference Designators: TP15

### 2.3.7 Main Clock

- Connector Type: 100-MIL Male Header (2x1)
- Absolute Maximum Input Signal Level: +6.0 V
- Absolute Minimum Input Signal Level: –0.5 V
- Reference Designators: TP4 (CLKIN)

## 2.4 DSP Composer Control Header

- Connector Type: 50-MIL Male Header (15x2)
- Absolute Maximum Input Signal Level: +2.0 V
- Absolute Minimum Input Signal Level: –0.5 V
- Maximum Signal Output Level: +1.8 V
- Reference Designators: JP2

## 2.5 USB Power Input

The USB power input has the following characteristics and is switched by S8:

- Voltage Range: +4.75 VDC to +5.25 VDC
- Minimum Power: +5 V supply (0.5 A)
- Connector Type: USB Mini-B
- Reference Designator: USB1

## 2.6 Input Button (S1)

The button S1 (located near JP4) is used to change the audio input source.

## 2.7 MCU USER INTERFACE Header

- Connector Type: 100-MIL Male Header (7x2)
- Absolute Maximum Input Signal Level: +3.6 V
- Absolute Minimum Input Signal Level: –0.5 V
- Maximum Signal Output Level: +1.8 V
- Reference Designators: JP1

## 2.8 Buttons and Knobs

The buttons S9–S14 (located on MCU-USER-INTERFACE board) are used to control the MCU.

- S9 (Rotary Encoder)—Turn this knob to navigate up/down through menu page. Press down on the knob to select an item
- S10 (Menu)—This button displays the CRD48L10 board configuration options.
- S11 (Left)—This button takes you back one level in the menu system.
- S12 (Right)—This button takes you one level deeper in the menu system.
- S13 (Exit)—This button exits the CRD48L10 board configuration menu.
- S14 (Reset)—This button executes a hard reset of the on-board MCU.

## 2.9 MCU DEBUG C-2 Programming Header

This header is used to program the MCU from a CDB-MCU-DEBUG dongle (P4/C2-OUT connector) OR the Silicon Labs programming dongle.

- Connector Type: Shrouded 100-MIL Male Header (5x2)
- Absolute Maximum Input Signal Level: +3.6 V
- Absolute Minimum Input Signal Level: –0.5 V
- Maximum Signal Output Level: +1.8 V
- Reference Designators: JP4

## 2.10 Current Measurement Points

- Connector Type: 100-MIL Male Header (1x2)
- Reference Designators: TP20–TP23, P16

# Chapter 3
# Standalone Modes

The CRD48L10-4in4out has multiple audio input and output ports. All available data flow paths are shown in the diagram in Fig. 3-1.

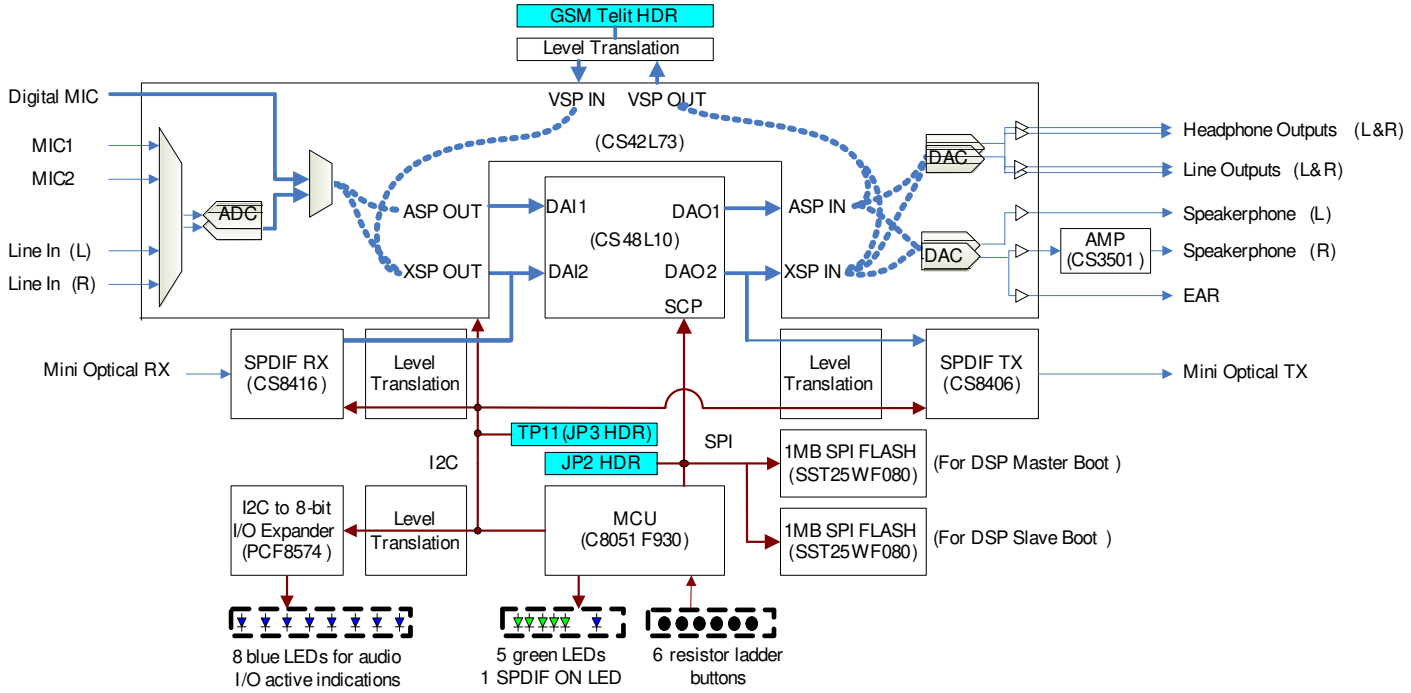


**Figure 3-1. Data Flow Paths**

The data path can be selected using either the mode select button S1 on the CRD48L10-4in4out or with the MCU-USER-INTERFACE board. The data path options available using only S1 are a subset of those available with the MCU-USER-INTERFACE board. The two modes will be described in separate sections below.

It is worth noting that the VSP port of the CS42L73 is always available for external audio through TP14, but not with the default MCU code provided with the CRD48L10-4in4out. An external MCU must configure the CS42L73 to utilize audio data from the VSP.

## 3.1 S1 Button Control (No LCD)

### 3.1.1 Powering Up Board

When powering on the CRD48L10 board, the power LEDs D5–D9 should illuminate indicating that all power rails are good and the output connector LEDs D4, D8, D10, D11, and D20 should illuminate to show that the MCU has configured the codec to drive audio out of the board. No input mode LEDs are illuminated since default input mode is from on-board FLASH. Power up state of the CRD48L10 is shown in Fig. 3-2.

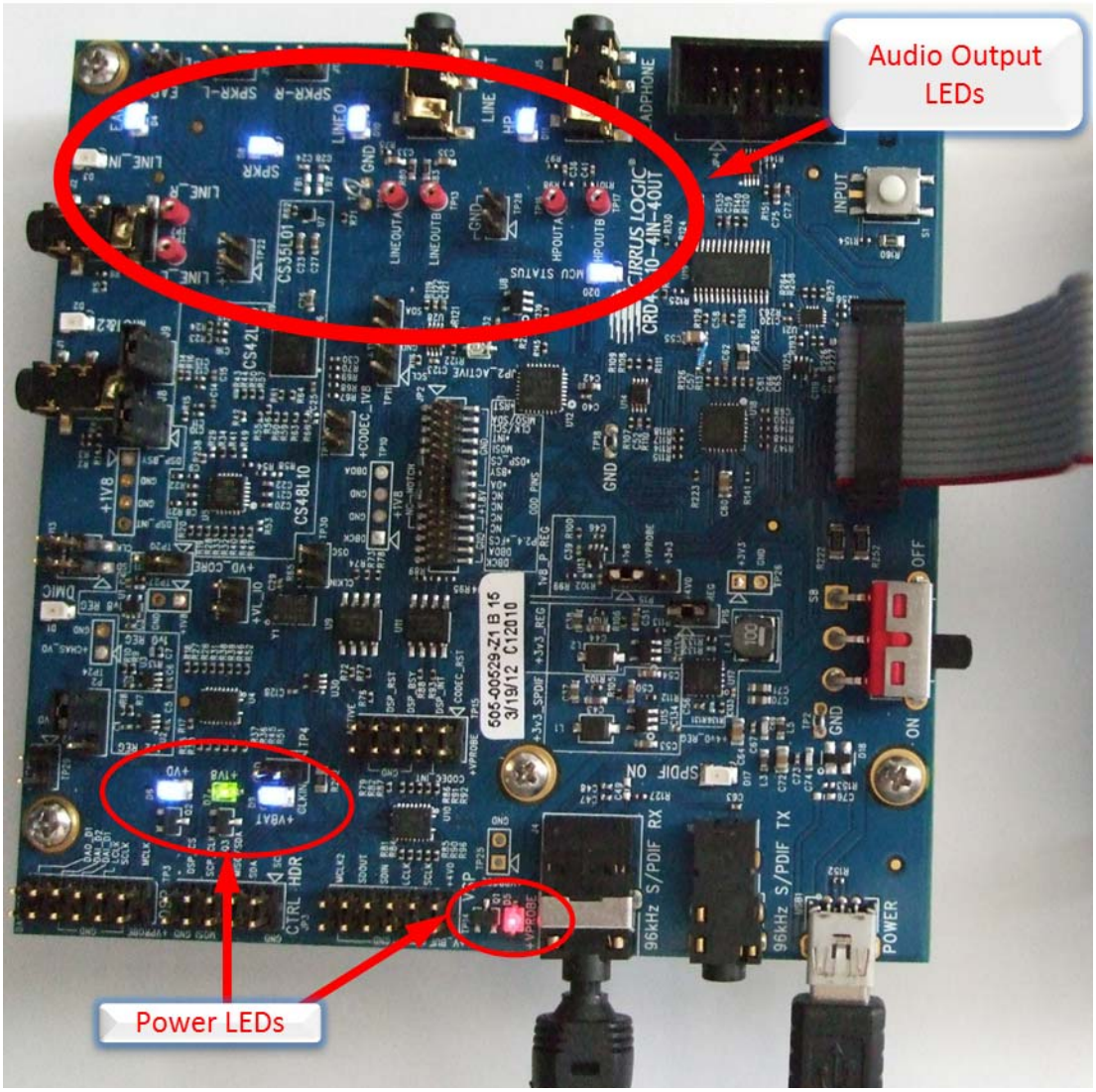


**Figure 3-2. CRD48L10-4in4out S1 Control Only**

### 3.1.2 Selecting Input Audio Source

Input selection is controlled with the S1 button, as shown in Fig 3-3, on the CRD48L10 board. By default, the Input will DSP play back an MP3 from on-board FLASH U9. There is an LED next to each input to indicate which input is active, except when in FLASH playback where no input LED will be illuminated.


**Figure 3-3. S1 Input Selection Button**

The MCU will cycle through the inputs when the button S1 is pressed from FLASH > LINE IN > MIC 1 & 2 > S/PDIF > FLASH. LED locations are shown in Fig. 3-4 to Fig. 3-6.

If the MCU-USER-INTERFACE board is attached, the LCD also displays the active input.

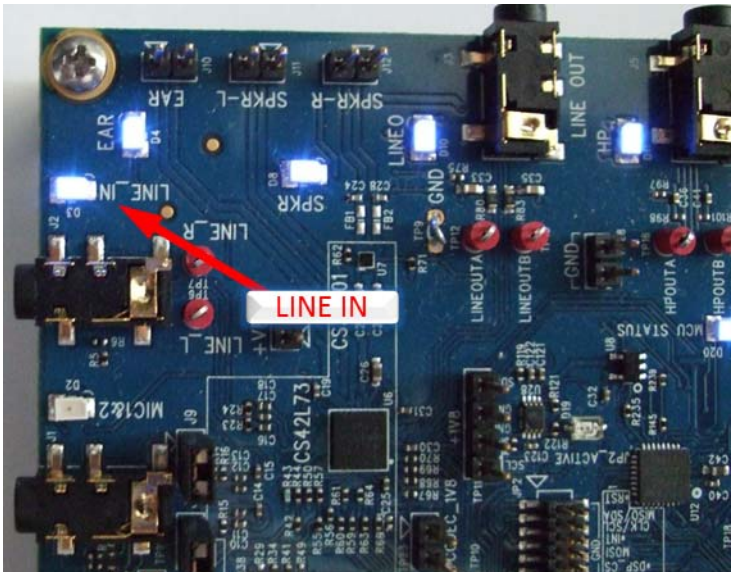


**Figure 3-4. LINE IN Active**

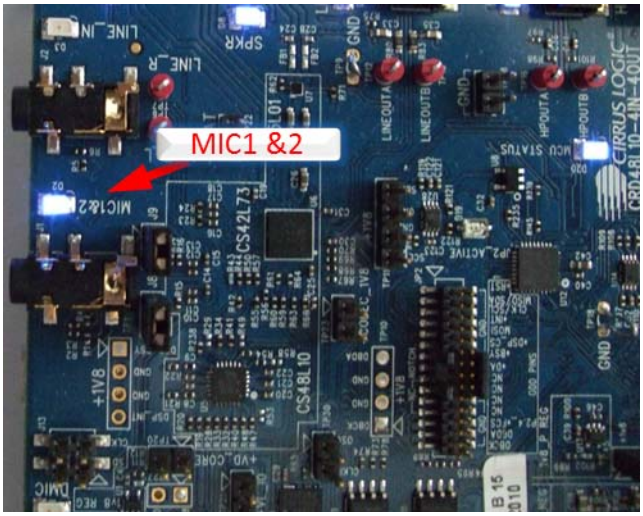


**Figure 3-5. MIC 1 & 2 Active**

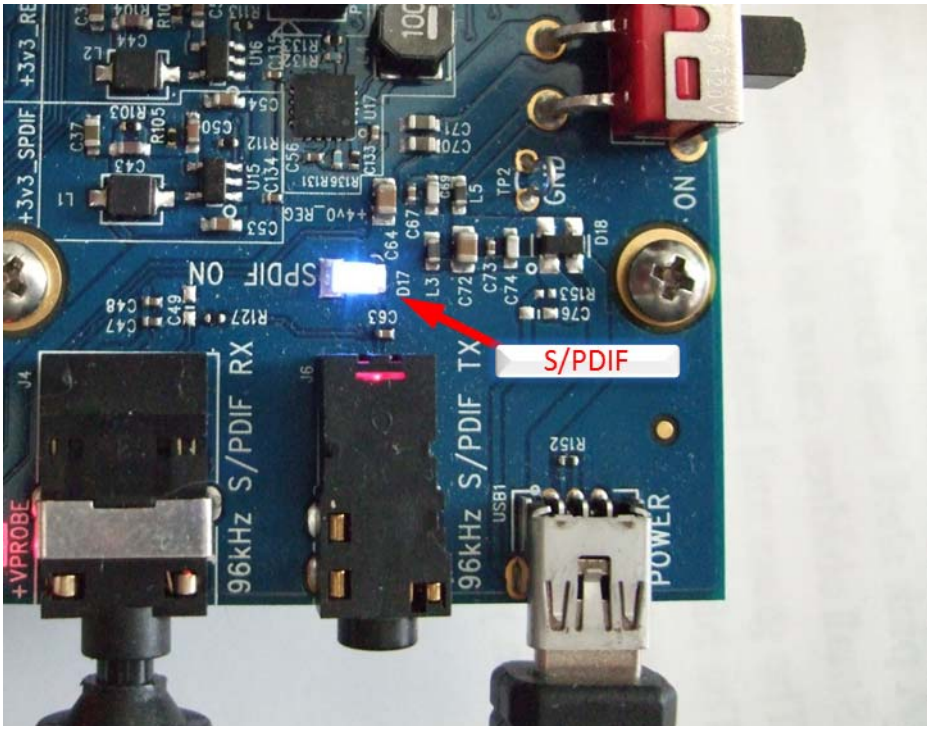


**Figure 3-6. S/PDIF OPTICAL Active**

Each of the input modes is described in the following sections.

The MCU configures the data paths shown feeding the DSP in the following data path diagrams. Inactive paths are shown in gray. The DSP project determines how the audio is processed and which audio goes out each DAO port. The default DSP projects programmed into the CRD48L10 are configured to process the audio paths shown in blue.

### 3.1.3 MP3 Decode from FLASH (U9)

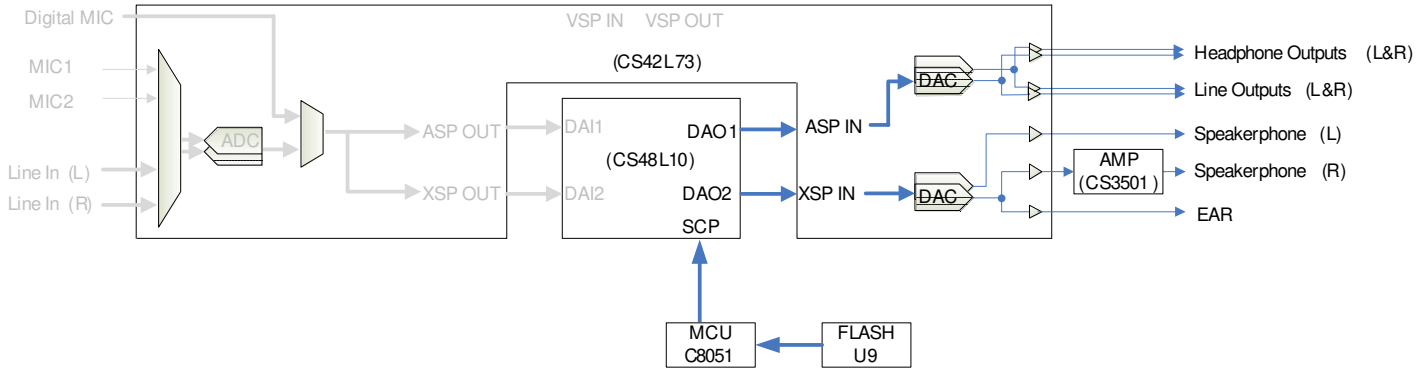


**Figure 3-7. Data Path for FLASH Playback**

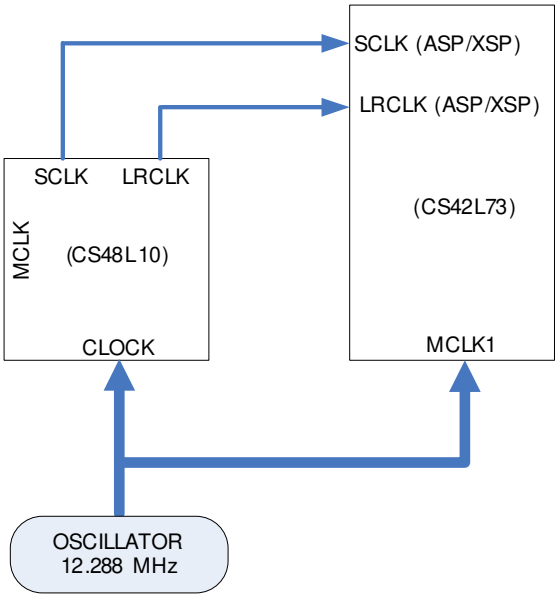


**Figure 3-8. Clocking for FLASH Playback–DSP Master**

This is the default configuration after power up of the CRD48L10-4in4out. Power up and connect headphones to the HEADPHONE jack or a speaker to the LINE OUT jack, and you will hear audio playing in a continuous loop.

## 3.1.4 LINE IN

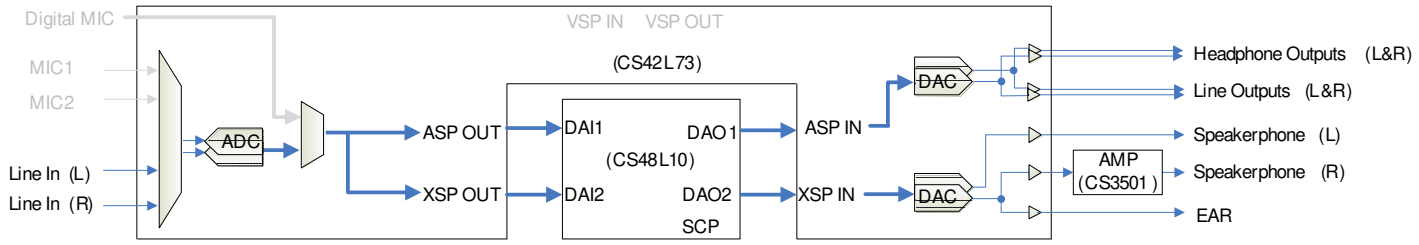


**Figure 3-9. Data Path for LINE IN Audio**

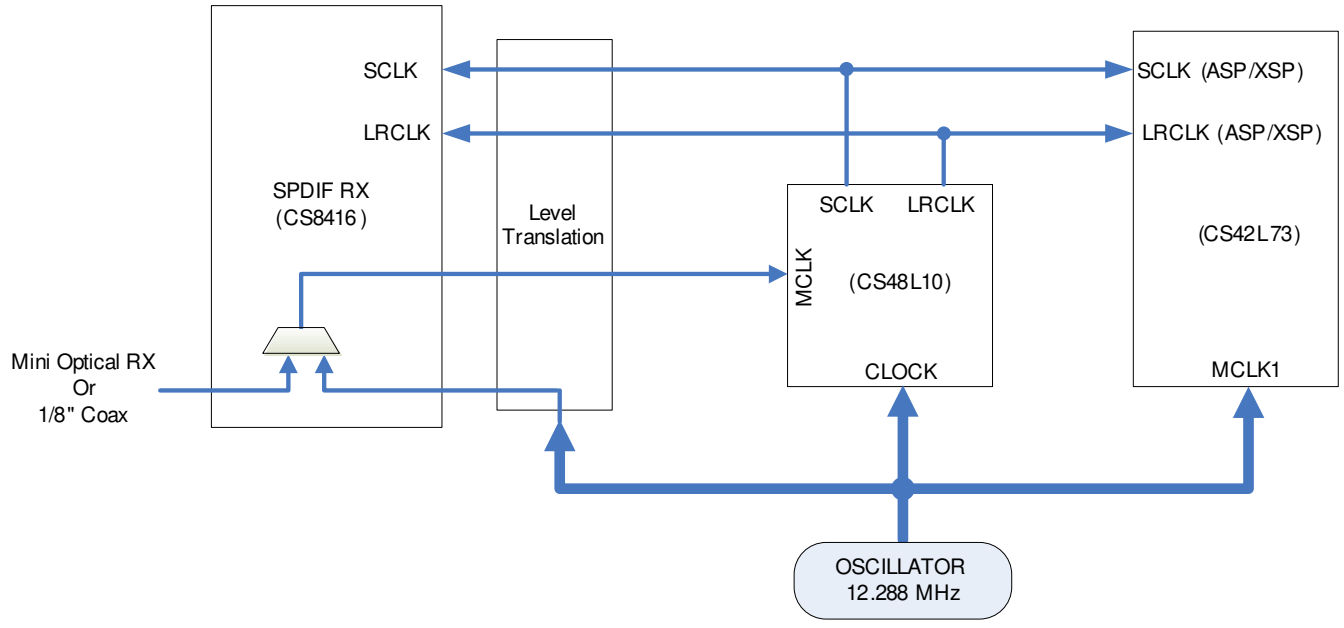


**Figure 3-10. Clocking for LINE IN Audio–DSP MCLK Slave**

The S/PDIF receiver is configured to automatically switch between the on-board oscillator and the clock recovered from an incoming S/PDIF stream.

In the previous diagram, any time a valid S/PDIF stream is presented to the CS8416, the system audio clock will be locked to the Fs of the incoming stream. The S/PDIF cable should be removed when the on-board oscillator (or TP4) is meant to master audio clocks.

### 3.1.5 MIC 1 & 2

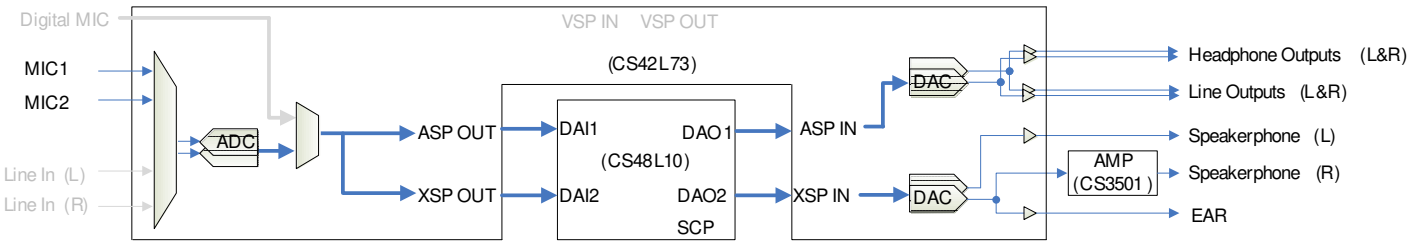


**Figure 3-11. Data Path for MIC 1 & 2 Audio**

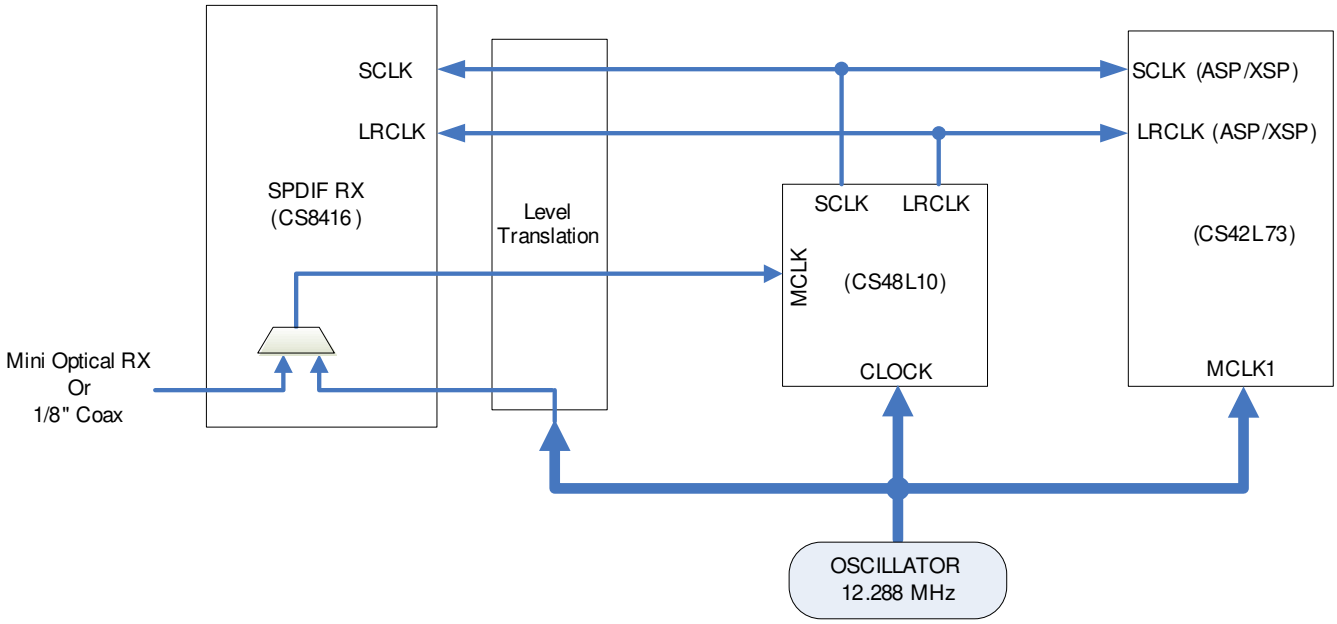


**Figure 3-12. Clocking for MIC 1 & 2 Audio–DSP MCLK Slave**

The S/PDIF receiver is configured to automatically switch between the on-board oscillator and the clock recovered from an incoming S/PDIF stream.

In the previous diagram, any time a valid S/PDIF stream is presented to the CS8416, the system audio clock will be locked to the Fs of the incoming stream. The S/PDIF cable should be removed when the on-board oscillator (or TP4) is meant to master audio clocks.

### 3.1.6 S/PDIF

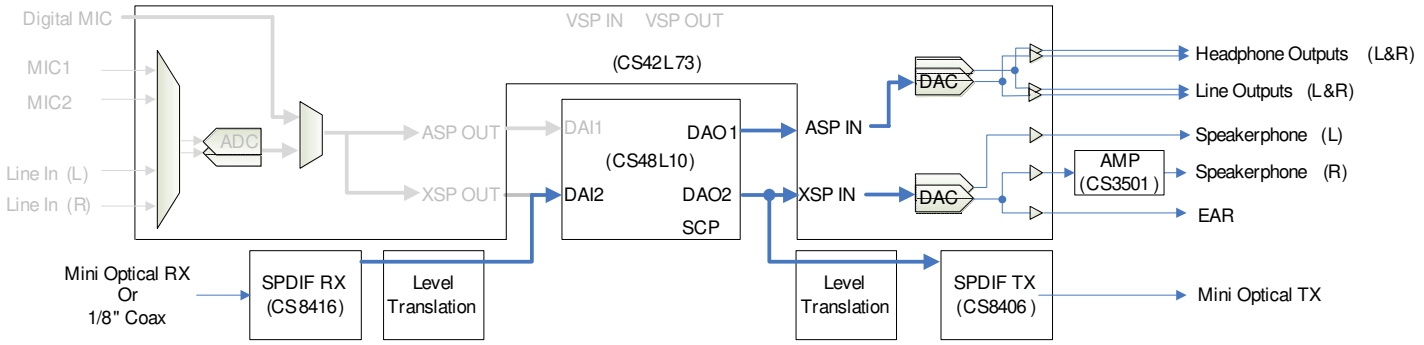


**Figure 3-13. Data Path for S/PDIF Audio**

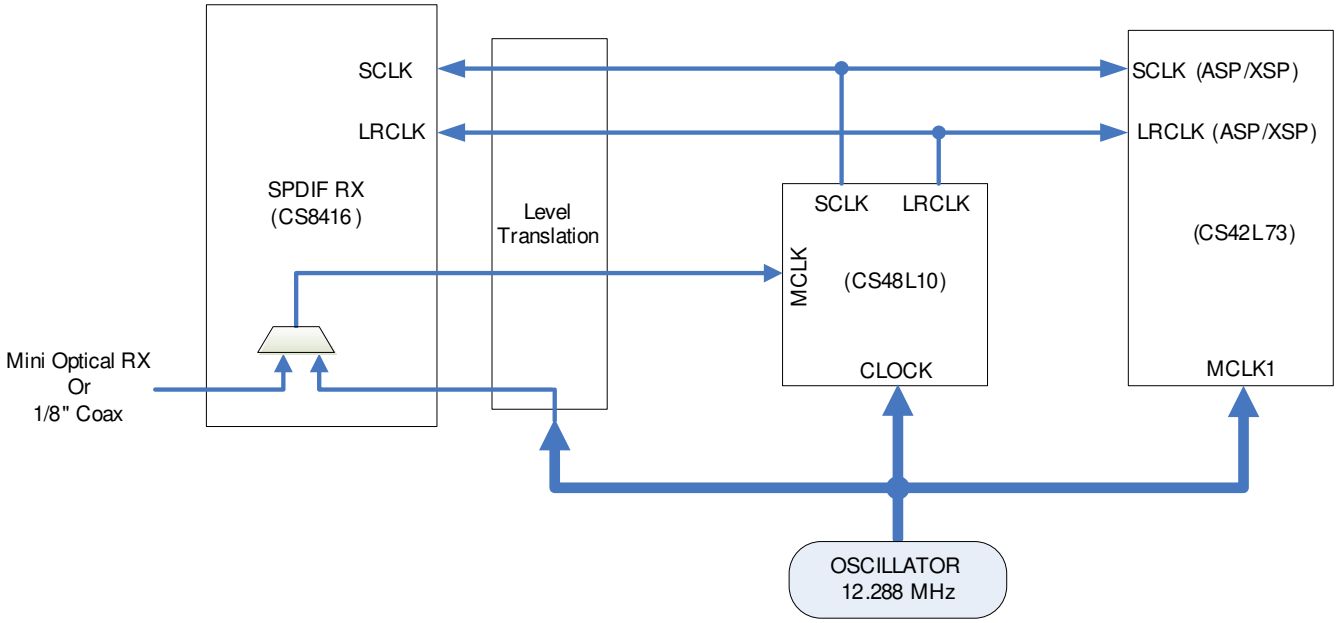


**Figure 3-14. Clocking for S/PDIF Audio–DSP MCLK Slave**

Both the Mini-Optical and 1/8” Coax inputs are connected to the S/PDIF Receiver, but only one can be active at any time (there is only one physical plug). If both the optical and coax were active, the S/PDIF Receiver would be unable to recover clock or data.

## 3.2 MCU UI Controlled

### 3.2.1 Powering Up the Board

When powering on the CRD48L10 board, the power LEDs D5-D9 should illuminate indicating that all power rails are good and the output connector LEDs D4, D8, D10, D11, and D20 should illuminate to show that the MCU has configured the codec to drive audio out of the board. No input mode LEDs are illuminated since default input mode is from on-board FLASH. Power up state of the CRD48L10 is shown in Fig. 3-15.

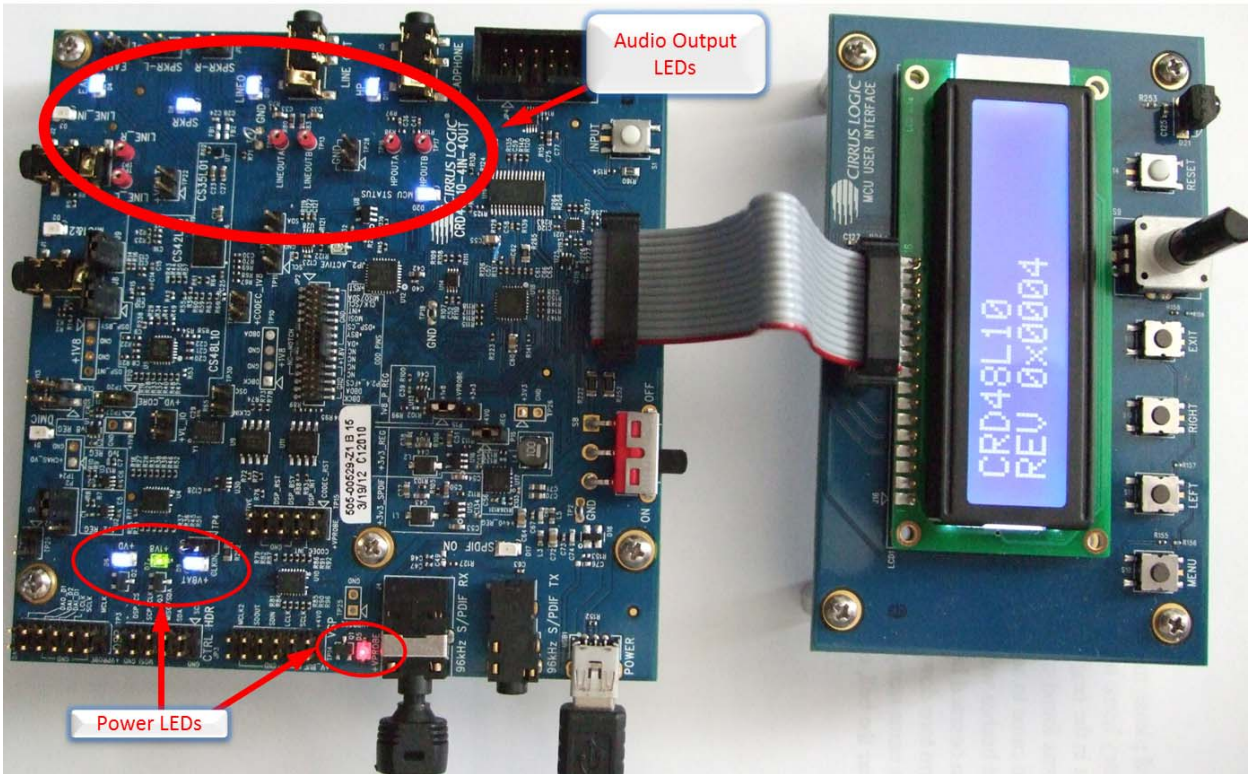


**Figure 3-15. CRD48L10-4in4out MCU UI Control**

1. The LCD will then display the current revision of the on board C8051F930 MCU, as shown below:


2. The MCU will attempt to read a micro_condenser image from the SPI FLASH. If it fails you will get the following error:


3. The MCU will cycle through displays showing the status of the Audio Source, Project:, and Snapshot:


4. Using the buttons and rotary encoder knob on the MCU User Interface board it is possible to configure the CRD48L10 in more ways than is possible just using button S1.
5. Push the “Menu” button to bring up the configuration menu on the LCD. Turn the encoder knob to choose different sub-menus, and press the encoder knob down to select an option.

### 3.2.2 Project Menu

A project is a collection of firmware modules and configurations downloaded to the DSP to process audio in a specific way. For the CRD48L10-4in4out, the Project also defines how the board is configured and data is routed to/from the CS48L10. The Project menu selection on the LCD appears as shown in Fig. 3-16.


**Figure 3-16. Project Menu**

There are four projects available in the default MCU code shipped with the CRD48L10:

- MP3 Decode from FLASH
- LINE IN
- MIC IN
- S/PDIF IN

Each project is described in the following sections.

#### 3.2.2.1 MP3 Decode from FLASH (U9) Project

This project is selected, as shown in Fig. 3-17.


**Figure 3-17. MP3 Decode from FLASH**

This project is the same as described in Section 3.1.3. There is only one snapshot available for this project.

#### 3.2.2.2 LINE IN Project

This project is selected, as shown in Fig. 3-18.


**Figure 3-18. LINE IN Project**

This project is the same as described in Section 3.1.4. There is only one snapshot available for this project.

#### 3.2.2.3 MIC 1 & 2 Project

This project is selected, as shown in Fig. 3-19.


**Figure 3-19. MIC IN Project**

This project is the same as described in Section 3.1.5. There is only one snapshot available for this project.

#### 3.2.2.4 S/PDIF Project

This project is selected, as shown in Fig. 3-20.


**Figure 3-20. S/PDIF IN Project**

The S/PDIF project available through the MCU User Interface is more flexible than that described in Section 3.1.6. This project allows the mixing of the S/PDIF Input and the Line Input according to three snapshots:

- LINE IN
- S/PDIF IN
- LINE + S/PDIF

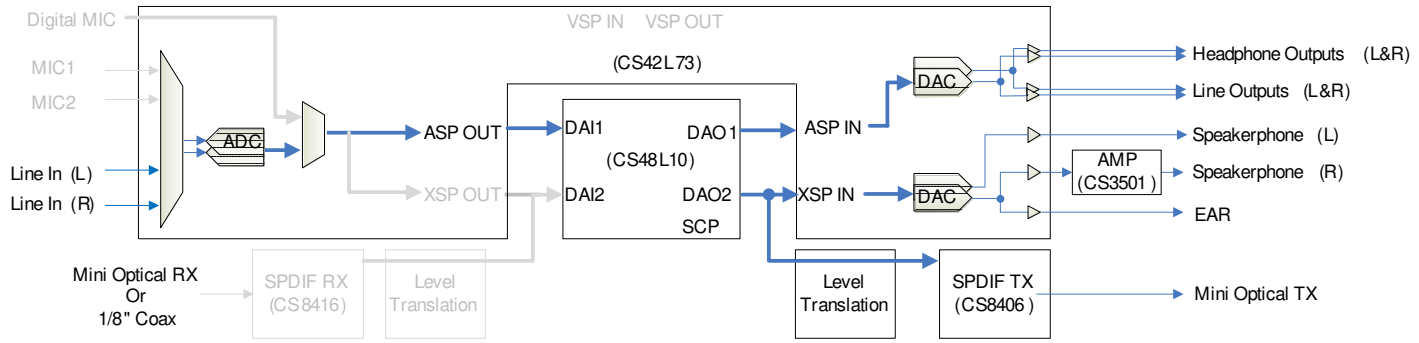


**Figure 3-21. LINE IN Snapshot**

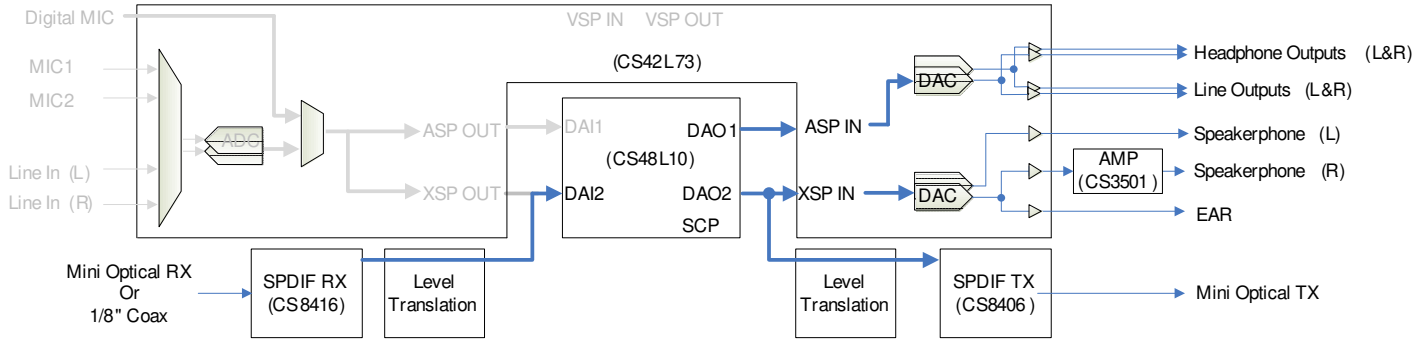


**Figure 3-22. S/PDIF IN (Same as Initial) Snapshot**

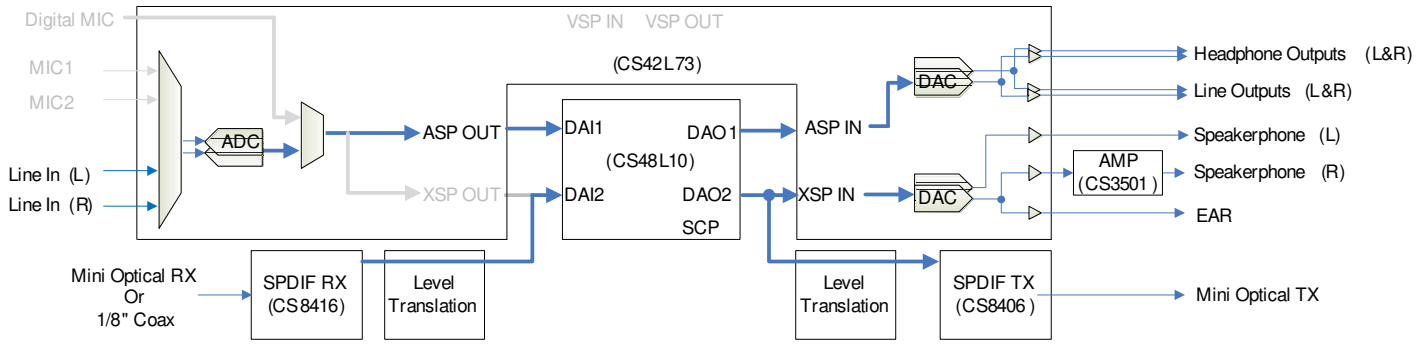


**Figure 3-23. LINE IN + S/PDIF Snapshot**

The clocking topology is the same as used in Section 3.1.6.

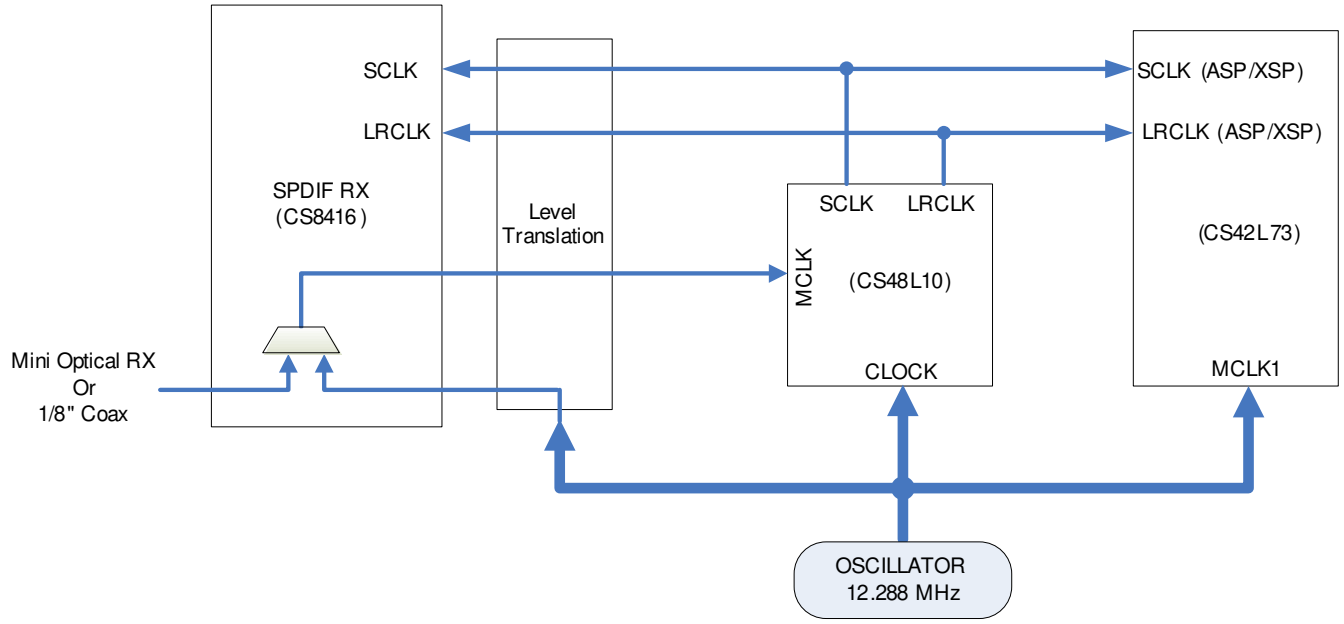


**Figure 3-24. Clocking for All S/PDIF Snapshots–DSP MCLK Slave**

### 3.2.3 Snapshot Menu

A project defines the firmware modules downloaded to the DSP, and the data routing on the board. A snapshot is simply a reconfiguration of the DSP using the same firmware and data routing. The default code released on the CRD48L10-4in4out has snapshots for the S/PDIF project as described in Section 3.2.2.4. The snapshot menu selection on the LCD appears as shown in Fig. 3-25.


**Figure 3-25. Snapshot Menu**

### 3.2.4 AudioIn Source Menu

The CRD48L10-4in4out has an on-board codec for processing analog audio and an S/PDIF transceiver section which allows digital audio in and out. Using the AudioIn Source selection on the LCD menu, the user can configure the CRD48L10 to accept I²S data through the TP3 header. The AudioIn Source menu is shown in Fig. 3-26.


**Figure 3-26. AudioIn Source Menu**

The following are menu choices under AudioIn Source:

- On–board
- External audio via TP3

### 3.2.5 Clock Source Menu

The CRD48L10-4in4out has a 12.288 MHz oscillator which is used to drive the REFCLK input of the CS48L10 and can be used as accurate MCLK source. In some scenarios, it may be useful to use a different clock frequency on the CRD48L10 when attempting to emulate a particular system configuration. This can be accomplished using the “Clock Source” menu of the MCU User Interface board. The snapshot menu selection on the LCD appears as shown in Fig. 3-27.


**Figure 3-27. Clock Source Menu**