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CS2000-CP

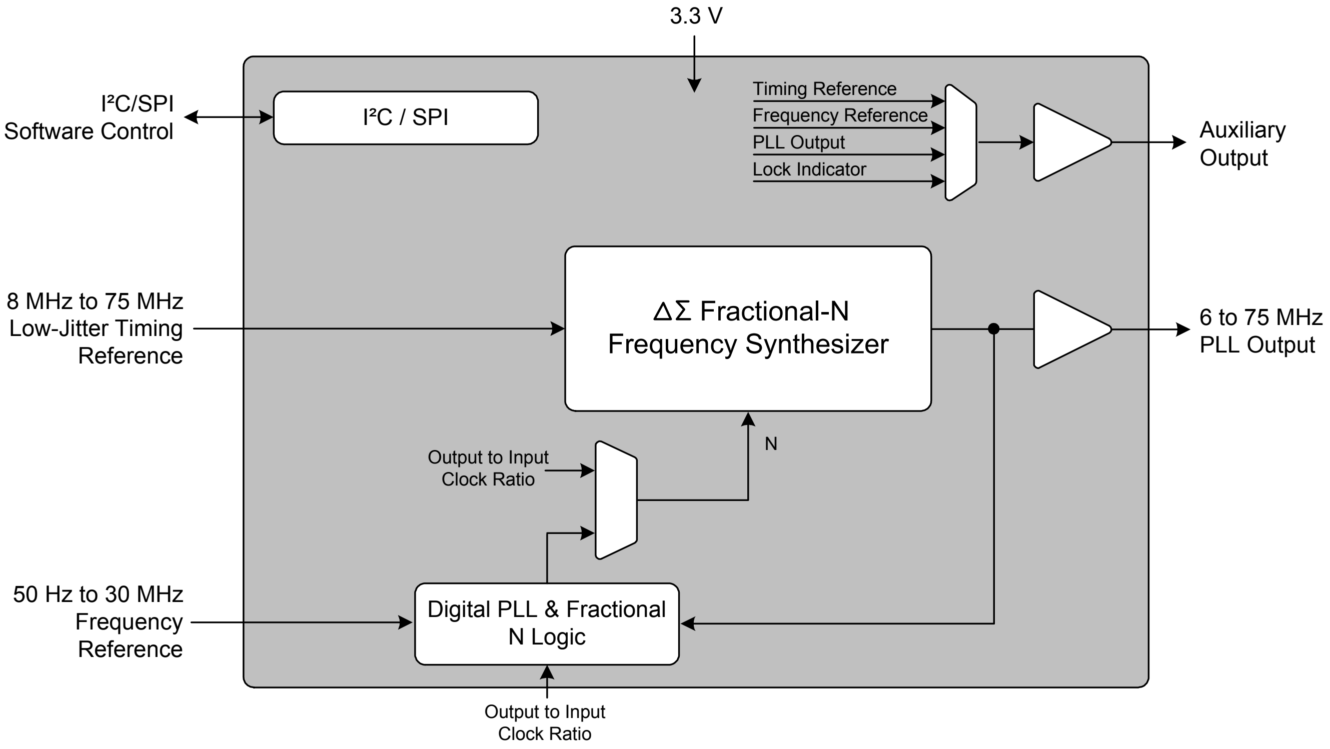
Fractional-N Clock Synthesizer & Clock Multiplier

Features

- Delta-Sigma Fractional-N Frequency Synthesis
  - Generates a Low Jitter 6 - 75 MHz Clock from an 8 - 75 MHz Reference Clock
- Clock Multiplier / Jitter Reduction
  - Generates a Low Jitter 6 - 75 MHz Clock from a Jittery or Intermittent 50 Hz to 30 MHz Clock Source
- Highly Accurate PLL Multiplication Factor
  - Maximum Error Less Than 1 PPM in High-Resolution Mode
- I²C / SPI™ Control Port
- Configurable Auxiliary Output
- Flexible Sourcing of Reference Clock
  - External Oscillator or Clock Source
  - Supports Inexpensive Local Crystal
- Minimal Board Space Required
  - No External Analog Loop-filter Components

The CS2000-CP is an extremely versatile system clocking device that utilizes a programmable phase lock loop. The CS2000-CP is based on a hybrid analog-digital PLL architecture comprised of a unique combination of a Delta-Sigma Fractional-N Frequency Synthesizer and a Digital PLL. This architecture allows for both frequency synthesis/clock generation from a stable reference clock as well as generation of a low-jitter clock relative to an external noisy synchronization clock. The design is also unique in that it can generate low-jitter clocks relative to noisy external synchronization clocks at frequencies as low as 50 Hz. The CS2000-CP supports both I²C and SPI for full software control.

The CS2000-CP is available in a 10-pin MSOP package in Commercial (-10°C to +70°C), Automotive-D (-40°C to +85°C), and Automotive-E (-40°C to +105°C) grades. Customer development kits are also available for device evaluation. Please see "Ordering Information" on page 36 for complete details.



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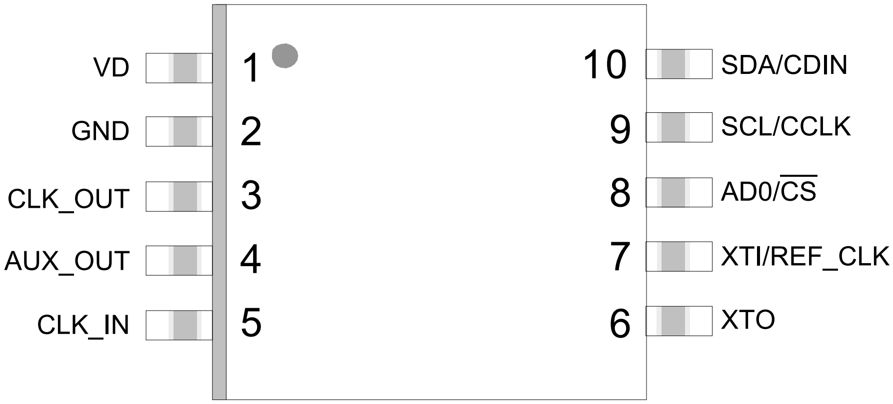
1. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	1	**Digital Power** (*Input*) - Positive power supply for the digital and analog sections.
GND	2	**Ground** (*Input*) - Ground reference.
CLK_OUT	3	**PLL Clock Output** (*Output*) - PLL clock output.
AUX_OUT	4	**Auxiliary Output** (*Output*) - This pin outputs a buffered version of one of the input or output clocks, or a status signal, depending on register configuration.
CLK_IN	5	**Frequency Reference Clock Input** (*Input*) - Clock input for the Digital PLL frequency reference.
XTO XTI/REF_CLK	6 7	**Crystal Connections (XTI/XTO) / Timing Reference Clock Input (REF_CLK)** (*Input/Output*) - XTI/XTO are I/O pins for an external crystal which may be used to generate the low-jitter PLL input clock. REF_CLK is an input for an externally generated low-jitter reference clock.
AD0/$\overline{\text{CS}}$	8	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode. $\overline{\text{CS}}$ is the chip select signal in SPI Mode.
SCL/CCLK	9	**Control Port Clock** *(Input)* - SCL/CCLK is the serial clock for the serial control port in I²C and SPI mode.
SDA/CDIN	10	**Serial Control Data** (*Input/Output*) - SDA is the data I/O line in I²C Mode. CDIN is the input data line for the control port interface in SPI Mode.

2. TYPICAL CONNECTION DIAGRAM

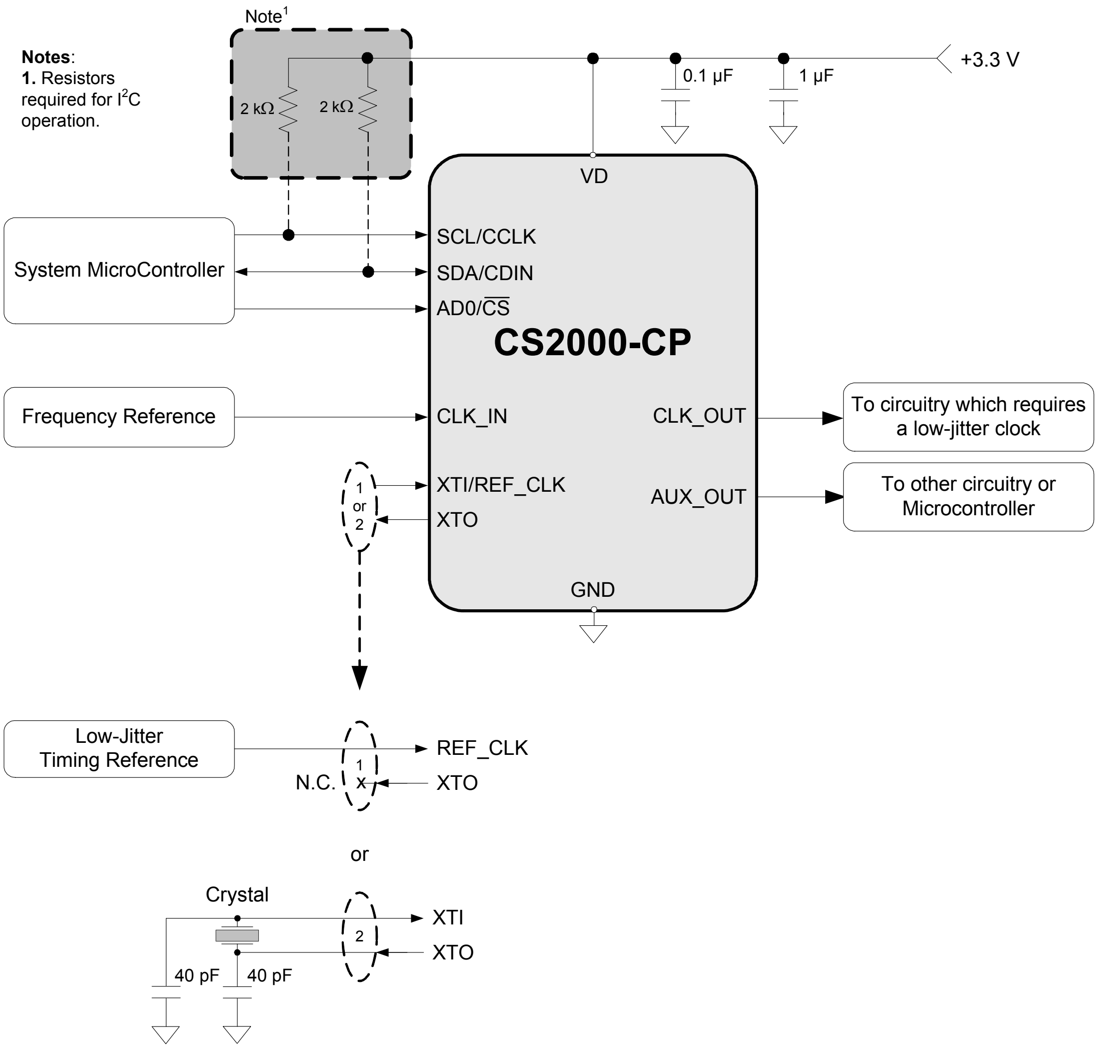


Figure 1. Typical Connection Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = 0 V; all voltages with respect to ground. (Note 1)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply	VD	3.1	3.3	3.5	V
Ambient Operating Temperature (Power Applied)					
Commercial Grade	T_{AC}	-10	-	+70	°C
Automotive-D Grade	T_{AD}	-40	-	+85	°C
Automotive-E Grade	T_{AE}	-40	-	+105	°C

Notes: 1. Device functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; all voltages with respect to ground.

Parameters	Symbol	Min	Max	Units
DC Power Supply	VD	-0.3	6.0	V
Input Current	I_{IN}	-	±10	mA
Digital Input Voltage (Note 2)	V_{IN}	-0.3	VD + 0.4	V
Ambient Operating Temperature (Power Applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

CAUTION: Stresses beyond "Absolute Maximum Ratings" levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 3. on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 2. The maximum over/under voltage is limited by the input current except on the power supply pin.

DC ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise specified): VD = 3.1 V to 3.5 V; T_A = -10°C to +70°C (Commercial Grade); T_A = -40°C to +85°C (Automotive-D Grade); T_A = -40°C to +105°C (Automotive-E Grade)

Parameters	Symbol	Min	Typ	Max	Units
Power Supply Current - Unloaded (Note 3)	I_D	-	12	18	mA
Power Dissipation - Unloaded (Note 3)	P_D	-	40	60	mW
Input Leakage Current	I_{IN}	-	-	±10	µA
Input Capacitance	I_C	-	8	-	pF
High-Level Input Voltage	V_{IH}	70%	-	-	VD
Low-Level Input Voltage	V_{IL}	-	-	30%	VD
High-Level Output Voltage (I_{OH} = -1.2 mA)	V_{OH}	80%	-	-	VD
Low-Level Output Voltage (I_{OH} = 1.2 mA)	V_{OL}	-	-	20%	VD

Notes: 3. To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance and power supply voltage. For example, f_{CLK_OUT} (49.152 MHz) * C_L (15 pF) * VD (3.3 V) = 2.4 mA of additional current due to these loading conditions on CLK_OUT.

AC ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise specified): VD = 3.1 V to 3.5 V; T_A = -10°C to +70°C (Commercial Grade); T_A = -40°C to +85°C (Automotive-D Grade); T_A = -40°C to +105°C (Automotive-E Grade); C_L = 15 pF.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Crystal Frequency Fundamental Mode XTAL	f_{XTAL}	*RefClkDiv[1:0]* = 10 *RefClkDiv[1:0]* = 01 *RefClkDiv[1:0]* = 00	8 16 32	- - -	14 28 50	MHz MHz MHz
Reference Clock Input Frequency	f_{REF_CLK}	*RefClkDiv[1:0]* = 10 *RefClkDiv[1:0]* = 01 *RefClkDiv[1:0]* = 00	8 16 32	- - -	14 28 56	MHz MHz MHz
Reference Clock Input Duty Cycle	D_{REF_CLK}		45	-	55	%
Internal System Clock Frequency	f_{SYS_CLK}		8		14	MHz
Clock Input Frequency	f_{CLK_IN}		50 Hz	-	30	MHz
Clock Input Pulse Width (Note 4)	pw_{CLK_IN}	$f_{CLK\_IN} < f_{SYS\_CLK}/96$ $f_{CLK\_IN} > f_{SYS\_CLK}/96$	2 10	- -	- -	UI ns
Clock Skipping Timeout	t_{CS}	(Notes 5, 6)	20	-	-	ms
Clock Skipping Input Frequency	f_{CLK_SKIP}	(Note 6)	50 Hz	-	80	kHz
PLL Clock Output Frequency	f_{CLK_OUT}	(Note 7)	6	-	75	MHz
PLL Clock Output Duty Cycle	t_{OD}	Measured at VD/2	45	50	55	%
Clock Output Rise Time	t_{OR}	20% to 80% of VD	-	1.7	3.0	ns
Clock Output Fall Time	t_{OF}	80% to 20% of VD	-	1.7	3.0	ns
Period Jitter	t_{JIT}	(Note 8)	-	70	-	ps rms
Base Band Jitter (100 Hz to 40 kHz)		(Notes 8, 9)	-	50	-	ps rms
Wide Band JItter (100 Hz Corner)		(Notes 8, 10)	-	175	-	ps rms
PLL Lock Time - CLK_IN (Note 11)	t_{LC}	$f_{CLK\_IN} < 200$ kHz $f_{CLK\_IN} > 200$ kHz	- -	100 1	200 3	UI ms
PLL Lock Time - REF_CLK	t_{LR}	f_{REF_CLK} = 8 to 75 MHz	-	1	3	ms
Output Frequency Synthesis Resolution (Note 12)	f_{err}	High Resolution High Multiplication	0 0	- -	±0.5 ±112	ppm ppm

Notes: 4. 1 UI (unit interval) corresponds to t_{SYS_CLK} or $1/f_{SYS\_CLK}$.

5. t_{CS} represents the time from the removal of CLK_IN by which CLK_IN must be re-applied to ensure that PLL_OUT continues while the PLL re-acquires lock. This timeout is based on the internal VCO frequency, with the minimum timeout occurring at the maximum VCO frequency. Lower VCO frequencies will result in larger values of t_{CS}.

6. Only valid in clock skipping mode; See "CLK_IN Skipping Mode" on page 15 for more information.

7. f_{CLK_OUT} is ratio-limited when f_{CLK_IN} is below 72 Hz.

8. f_{CLK_OUT} = 24.576 MHz; Sample size = 10,000 points; *AuxOutSrc[1:0]* = 11.

9. In accordance with AES-12id-2006 section 3.4.2. Measurements are Time Interval Error taken with 3rd order 100 Hz to 40 kHz bandpass filter.

10. In accordance with AES-12id-2006 section 3.4.1. Measurements are Time Interval Error taken with 3rd order 100 Hz Highpass filter.

11. 1 UI (unit interval) corresponds to t_{CLK_IN} or $1/f_{CLK\_IN}$.

12. The frequency accuracy of the PLL clock output is directly proportional to the frequency accuracy of the reference clock.

PLL PERFORMANCE PLOTS

Test Conditions (unless otherwise specified): VD = 3.3 V; T_A = 25 °C; C_L = 15 pF; f_{CLK_OUT} = 12.288 MHz; f_{CLK_IN} = 12.288 MHz; Sample size = 10,000 points; Base Band Jitter (100 Hz to 40 kHz); *AuxOutSrc[1:0]* = 11.

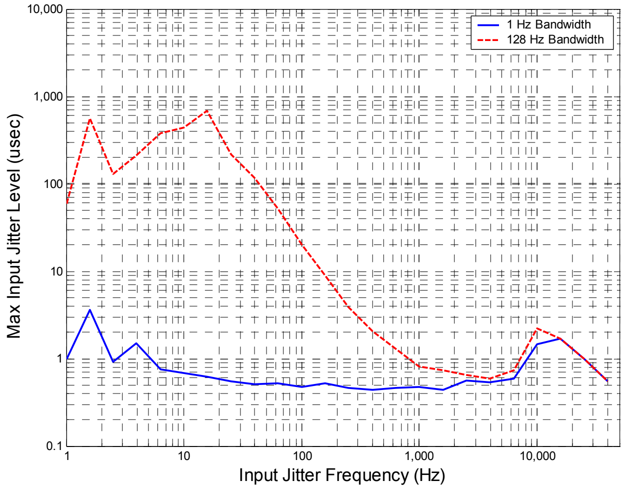


Figure 2. CLK_IN Sinusoidal Jitter Tolerance

Samples size = 2.5M points; Base Band Jitter (100Hz to 40kHz).

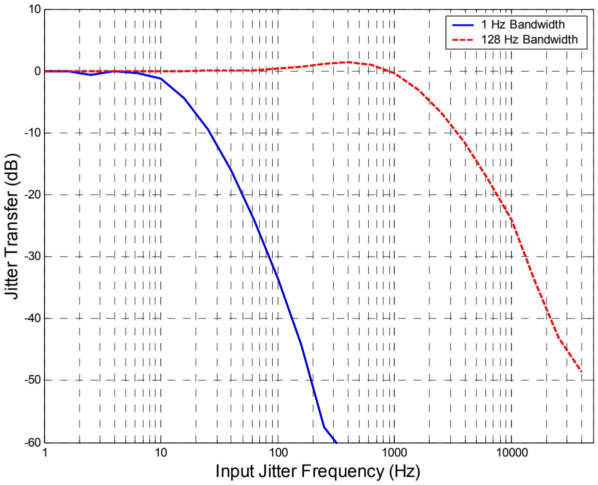


Figure 3. CLK_IN Sinusoidal Jitter Transfer

Samples size = 2.5M points; Base Band Jitter (100Hz to 40kHz).

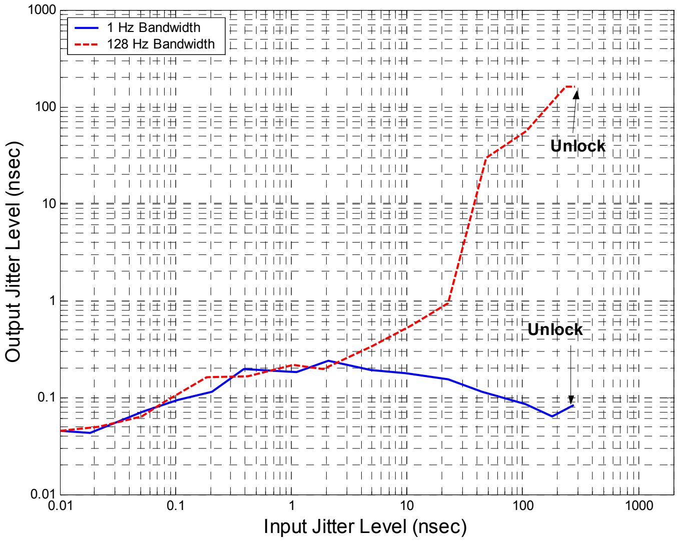


Figure 4. CLK_IN Random Jitter Rejection and Tolerance

CONTROL PORT SWITCHING CHARACTERISTICS- I²C FORMAT

Inputs: Logic 0 = GND; Logic 1 = VD; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free-Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low Time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 13)	t_{hdd}	0	-	µs
SDA Setup Time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_r	-	1	µs
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns
Delay from Supply Voltage Stable to Control Port Ready	t_{dpor}	100	-	µs

Notes: 13. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

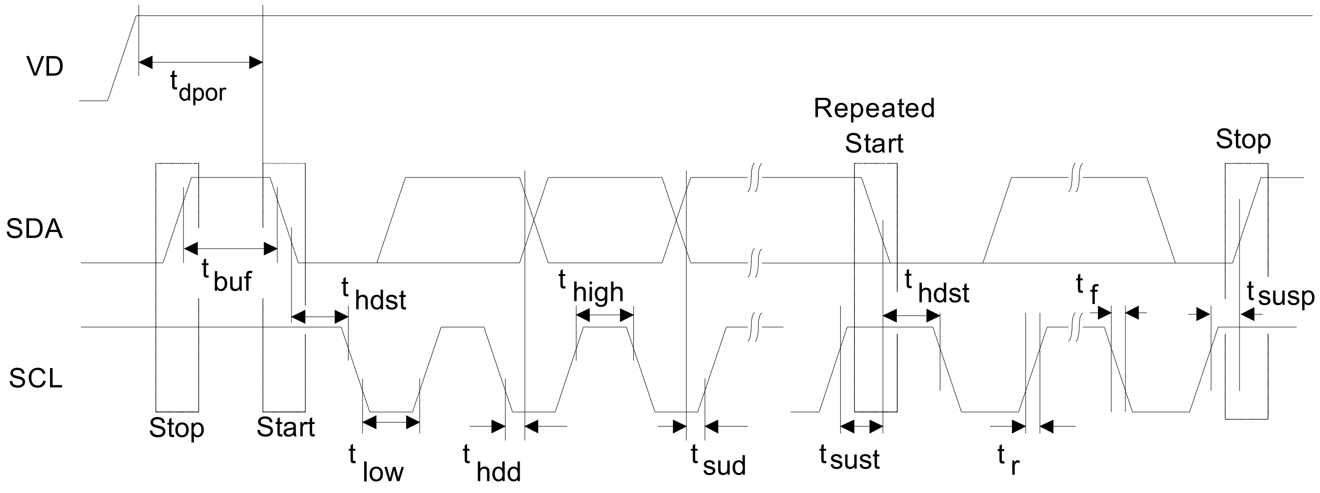


Figure 5. Control Port Timing - I²C Format

CONTROL PORT SWITCHING CHARACTERISTICS - SPI FORMAT

Inputs: Logic 0 = GND; Logic 1 = VD; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f_{cclk}	-	6	MHz
CCLK Edge to $\overline{CS}$ Falling (Note 14)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions	t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 15)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 16)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 16)	t_{f2}	-	100	ns
Delay from Supply Voltage Stable to Control Port Ready	t_{dpor}	100	-	µs

Notes: 14. t_{spi} is only needed before first falling edge of $\overline{CS}$ after power is applied. t_{spi} = 0 at all other times.

15. Data must be held for sufficient time to bridge the transition time of CCLK.

16. For f_{cclk} < 1 MHz.

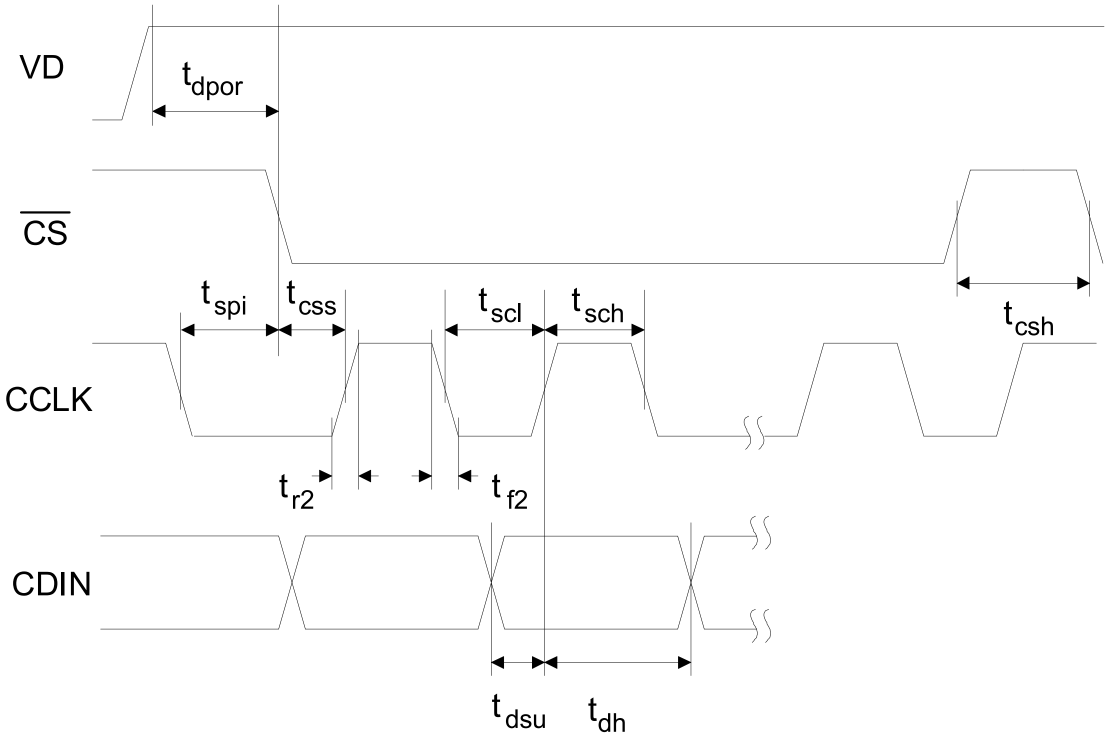


Figure 6. Control Port Timing - SPI Format (Write Only)

4. ARCHITECTURE OVERVIEW

4.1 Delta-Sigma Fractional-N Frequency Synthesizer

The core of the CS2000 is a Delta-Sigma Fractional-N Frequency Synthesizer which has very high-resolution for Input/Output clock ratios, low phase noise, very wide range of output frequencies and the ability to quickly tune to a new frequency. In very simplistic terms, the Fractional-N Frequency Synthesizer multiplies the Timing Reference Clock by the value of N to generate the PLL output clock. The desired output to input clock ratio is the value of N that is applied to the delta-sigma modulator (see Figure 7).

The analog PLL based frequency synthesizer uses a low-jitter timing reference clock as a time and phase reference for the internal voltage controlled oscillator (VCO). The phase comparator compares the fractional-N divided clock with the original timing reference and generates a control signal. The control signal is filtered by the internal loop filter to generate the VCO's control voltage which sets its output frequency. The delta-sigma modulator modulates the loop integer divide ratio to get the desired fractional ratio between the reference clock and the VCO output (thus the one's density of the modulator sets the fractional value). This allows the design to be optimized for very fast lock times for a wide range of output frequencies without the need for external filter components. As with any Fractional-N Frequency Synthesizer the timing reference clock should be stable and jitter-free.

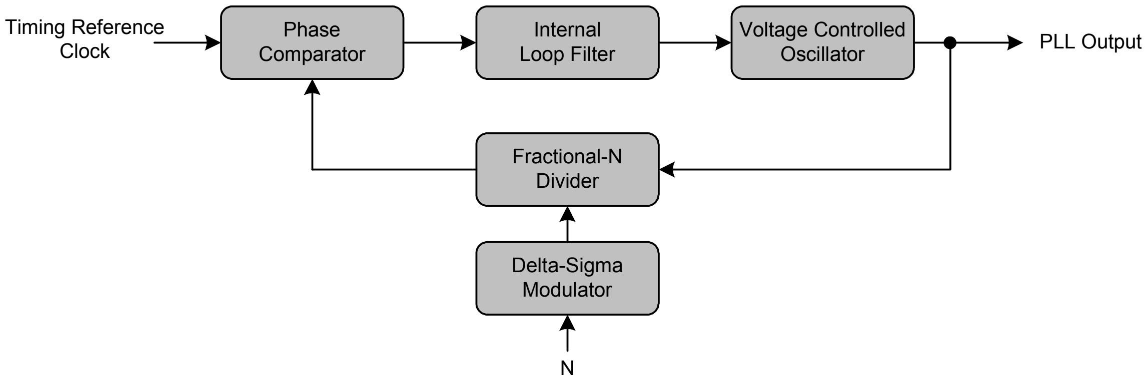


Figure 7. Delta-Sigma Fractional-N Frequency Synthesizer

4.2 Hybrid Analog-Digital Phase Locked Loop

The addition of the Digital PLL and Fractional-N Logic (shown in Figure 8) to the Fractional-N Frequency Synthesizer creates the Hybrid Analog-Digital Phase Locked Loop with many advantages over classical analog PLL techniques. These advantages include the ability to operate over extremely wide frequency ranges without the need to change external loop filter components while maintaining impressive jitter reduction performance. In the Hybrid architecture, the Digital PLL calculates the ratio of the PLL output clock to the frequency reference and compares that to the desired ratio. The digital logic generates a value of N which is then applied to the Fractional-N frequency synthesizer to generate the desired PLL output frequency. Notice that the frequency and phase of the timing reference signal do not affect the output of the PLL since the digital control loop will correct for the PLL output. A major advantage of the Digital PLL is the ease with which the loop filter bandwidth can be altered. The PLL bandwidth is automatically set to a wide-bandwidth mode to quickly achieve lock and then reduced for optimal jitter rejection.

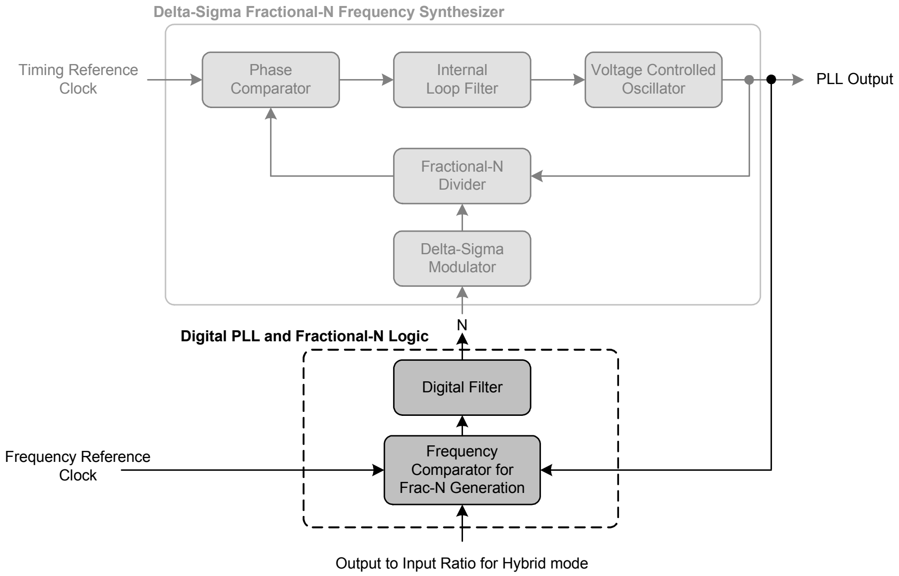


Figure 8. Hybrid Analog-Digital PLL

4.2.1 *Fractional-N Source Selection for the Frequency Synthesizer*

The fractional-N value for the frequency synthesizer can be sourced from either a static ratio or a dynamic ratio generated from the digital PLL (see Figure 9). This allows for the selection between operating in the static ratio based Frequency Synthesizer Mode as a simple frequency synthesizer (for frequency generation from the Timing Reference Clock) and in the dynamic ratio based Hybrid PLL Mode (for jitter reduction and clock multiplication). Selection between these two modes can either be made automatically based on the presence of the Frequency Reference Clock or manually through register controls.

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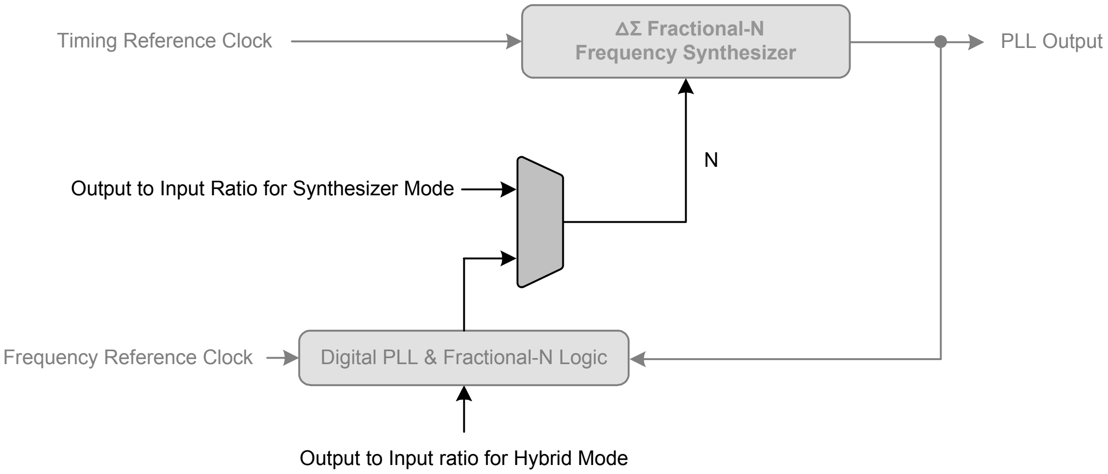

Figure 9. Fractional-N Source Selection Overview

5. APPLICATIONS

5.1 Timing Reference Clock Input

The low jitter timing reference clock (RefClk) can be provided by either an external reference clock or an external crystal in conjunction with the internal oscillator. In order to maintain a stable and low-jitter PLL output the timing reference clock must also be stable and low-jitter; the quality of the timing reference clock directly affects the performance of the PLL and hence the quality of the PLL output.

5.1.1 Internal Timing Reference Clock Divider

The Internal Timing Reference Clock (SysClk) has a smaller maximum frequency than what is allowed on the XTI/REF_CLK pin. The CS2000 supports the wider external frequency range by offering an internal divider for RefClk. The *RefClkDiv[1:0]* bits should be set such that SysClk, the divided RefClk, then falls within the valid range as indicated in "AC Electrical Characteristics" on page 8.

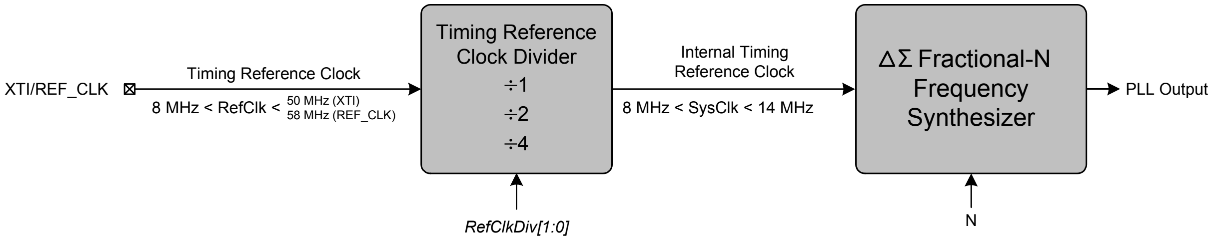

Figure 10. Internal Timing Reference Clock Divider

It should be noted that the maximum allowable input frequency of the XTI/REF_CLK pin is dependent upon its configuration as either a crystal connection or external clock input. See the "AC Electrical Characteristics" on page 8 for more details.

For the lowest possible output jitter, attention should be paid to the absolute frequency of the Timing Reference Clock relative to the PLL Output frequency (CLK_OUT). To minimize output jitter, the Timing Reference Clock frequency should be chosen such that f_{RefClk} is at least +/-15 kHz from f_{CLK_OUT}*N/32 where N is an integer. Figure 11 shows the effect of varying the RefClk frequency around f_{CLK_OUT}*N/32. It should be noted that there will be a jitter null at the zero point when N = 32 (not shown in Figure 11). An example of how to determine the range of RefClk frequencies around 12 MHz to be used in order to achieve the lowest jitter PLL output at a frequency of 12.288 MHz is as follows:

$f_L \leq f_{RefClk} \leq f_H$ where:

$$\begin{aligned} f_L &= f_{\mathrm{CLK\_OUT}} \times \frac{31}{32} + 15kHz \\ &= 12.288MHz \times 0.96875 + 15kHz \\ &= 11.919MHz \end{aligned}$$

and

$$\begin{aligned} f_H &= f_{\mathrm{CLK\_OUT}} \times \frac{32}{32} - 15kHz \\ &= 12.288MHz \times 1 + 15kHz \\ &= 12.273MHz \end{aligned}$$

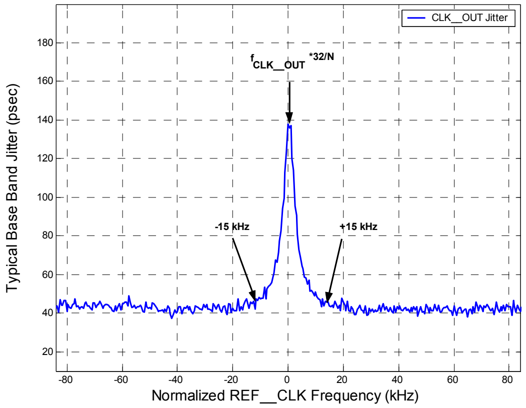

Figure 11. REF_CLK Frequency vs. a Fixed CLK_OUT

Referenced Control	Register Location
RefClkDiv[1:0]	"Reference Clock Input Divider (RefClkDiv[1:0])" on page 32

5.1.2 Crystal Connections (XTI and XTO)

An external crystal may be used to generate RefClk. To accomplish this, a 20 pF fundamental mode parallel resonant crystal must be connected between the XTI and XTO pins as shown in Figure 12. As shown, nothing other than the crystal and its load capacitors should be connected to XTI and XTO. Please refer to the "AC Electrical Characteristics" on page 8 for the allowed crystal frequency range.

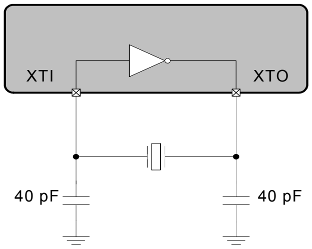

Figure 12. External Component Requirements for Crystal Circuit

5.1.3 External Reference Clock (REF_CLK)

For operation with an externally generated REF_CLK signal, XTI/REF_CLK should be connected to the reference clock source and XTO should be left unconnected or pulled low through a 47 kΩ resistor to GND.

5.2 Frequency Reference Clock Input, CLK_IN

The frequency reference clock input (CLK_IN) is used in Hybrid PLL Mode by the Digital PLL and Fractional-N Logic block to dynamically generate a fractional-N value for the Frequency Synthesizer (see "Hybrid Analog-Digital PLL" on page 13). The Digital PLL first compares the CLK_IN frequency to the PLL output. The Fractional-N logic block then translates the desired ratio based off of CLK_IN to one based off of the internal timing reference clock (SysClk). This allows the low-jitter timing reference clock to be used as the clock which the Frequency Synthesizer multiplies while maintaining synchronicity with the frequency reference clock through the Digital PLL. The allowable frequency range for CLK_IN is found in the "AC Electrical Characteristics" on page 8.

5.2.1 CLK_IN Skipping Mode

CLK_IN skipping mode allows the PLL to maintain lock even when the CLK_IN signal has missing pulses for up to 20 ms (t_{CS}) at a time (see "AC Electrical Characteristics" on page 8 for specifications). CLK_IN skipping mode can only be used when the CLK_IN frequency is below 80 kHz and CLK_IN is reapplied within 20 ms of being removed. The *ClkSkipEn* bit enables this function.

Regardless of the setting of the *ClkSkipEn* bit the PLL output will continue for 2^{23} SysClk cycles (466 ms to 1048 ms) after CLK_IN is removed (see Figure 13). This is true as long as CLK_IN does not glitch or have an effective change in period as the clock source is removed, otherwise the PLL will interpret this as a change in frequency causing clock skipping and the 2^{23} SysClk cycle time-out to be bypassed and the PLL to immediately unlock. If the prior conditions are met while CLK_IN is removed and 2^{23} SysClk cycles pass, the PLL will unlock and the PLL_OUT state will be determined by the *ClkOutUnl* bit; See "PLL Clock Output" on page 23. If CLK_IN is re-applied after such time, the PLL will remain unlocked for the specified time listed in the "AC Electrical Characteristics" on page 8 after which lock will be acquired and the PLL output will resume.

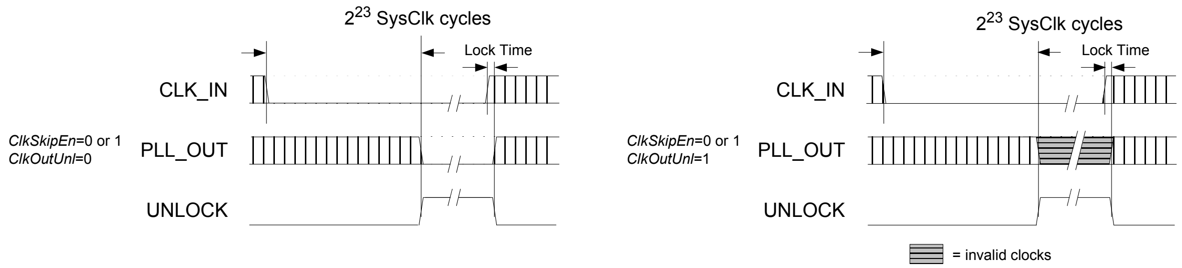

Figure 13. CLK_IN removed for > 2^{23} SysClk cycles

If it is expected that CLK_IN will be removed and then reapplied within 2^{23} SysClk cycles but later than t_{CS}, the *ClkSkipEn* bit should be disabled. If it is not disabled, the device will behave as shown in Figure 14; note that the lower figure shows that the PLL output frequency may change and be incorrect without an indication of an unlock condition.

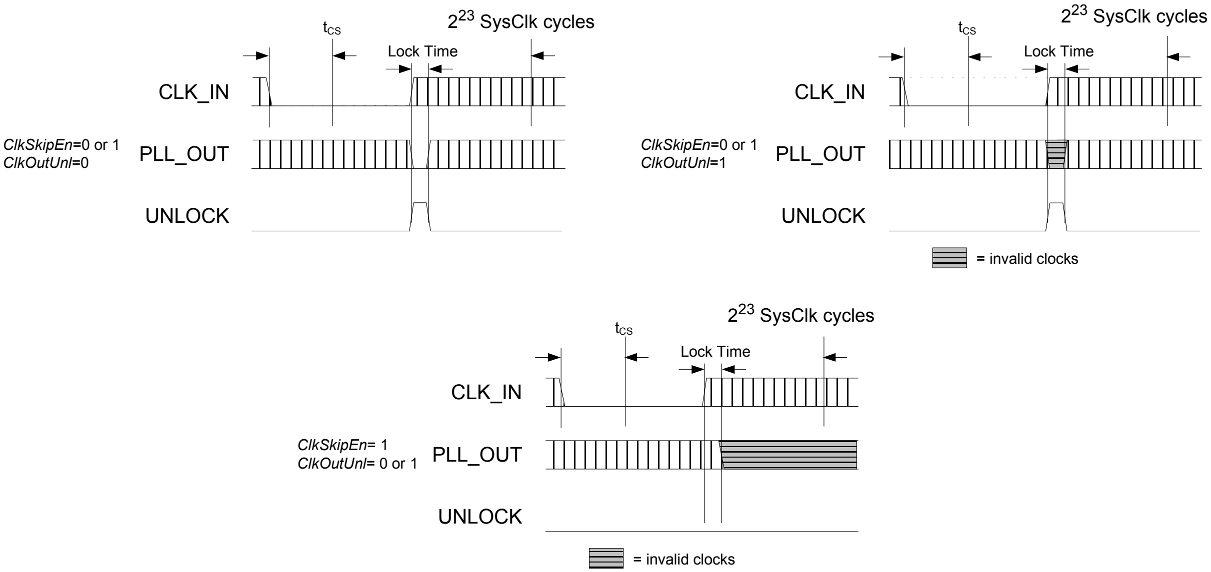

Figure 14. CLK_IN removed for < 2^{23} SysClk cycles but > t_{CS}

If CLK_IN is removed and then re-applied within t_{CS}, the *ClkSkipEn* bit determines whether PLL_OUT continues while the PLL re-acquires lock (see Figure 15). When *ClkSkipEn* is disabled and CLK_IN is removed the PLL output will continue until CLK_IN is re-applied at which point the PLL will go unlocked only for the time it takes to acquire lock; the PLL_OUT state will be determined by the *ClkOutUnl* bit during this time. When *ClkSkipEn* is enabled and CLK_IN is removed the PLL output clock will remain continuous throughout the missing CLK_IN period including the time while the PLL re-acquires lock.

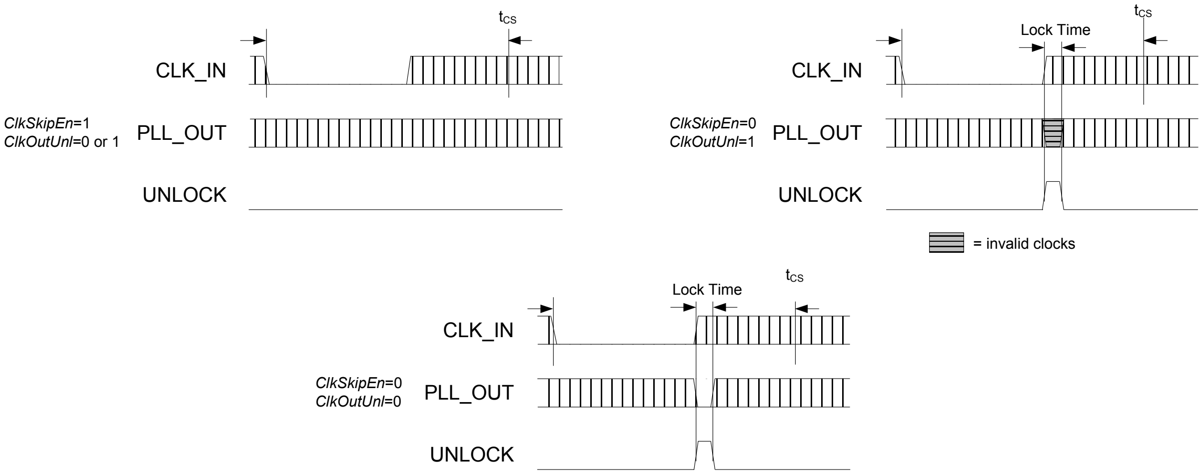

Figure 15. CLK_IN removed for < t_{CS}

Referenced Control	Register Location
ClkSkipEn	"Clock Skip Enable (ClkSkipEn)" on page 31
ClkOutUnl	"Enable PLL Clock Output on Unlock (ClkOutUnl)" on page 32

5.2.2 Adjusting the Minimum Loop Bandwidth for CLK_IN

The CS2000 allows the minimum loop bandwidth of the Digital PLL to be adjusted between 1 Hz and 128 Hz using the *ClkIn_BW[2:0]* bits. The minimum loop bandwidth of the Digital PLL directly affects the jitter transfer function; specifically, jitter frequencies below the loop bandwidth corner are passed from the PLL input directly to the PLL output without attenuation. In some applications it is desirable to have a very low minimum loop bandwidth to reject very low jitter frequencies, commonly referred to as wander. In others it may be preferable to remove only higher frequency jitter, allowing the input wander to pass through the PLL without attenuation.

Typically, applications in which the PLL_OUT signal creates a new clock domain from which all other system clocks and associated data are derived will benefit from the maximum jitter and wander rejection of the lowest PLL bandwidth setting. See Figure 16.

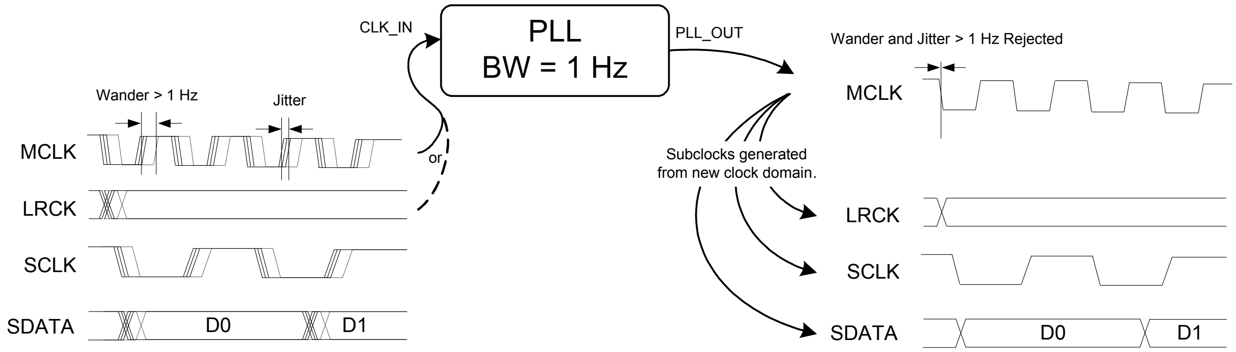

Figure 16. Low bandwidth and new clock domain

Systems in which some clocks and data are derived from the PLL_OUT signal while other clocks and data are derived from the CLK_IN signal will often require phase alignment of all the clocks and data in the system. See Figure 17. If there is substantial wander on the CLK_IN signal in these applications, it may be necessary to increase the minimum loop bandwidth allowing this wander to pass through to the CLK_OUT signal in order to maintain phase alignment. For these applications, it is advised to experiment with the loop bandwidth settings and choose the lowest bandwidth setting that does not produce system timing errors due to wandering between the clocks and data synchronous to the CLK_IN domain and those synchronous to the PLL_OUT domain.

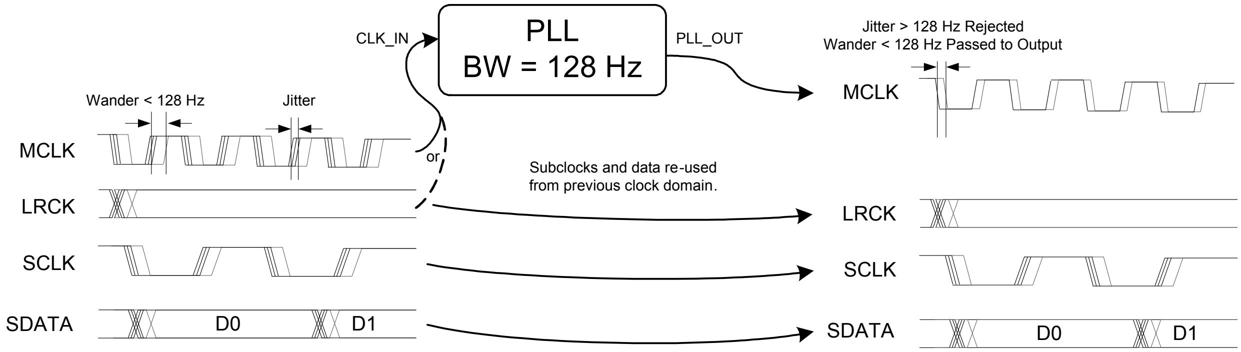

Figure 17. High bandwidth with CLK_IN domain re-use

It should be noted that manual adjustment of the minimum loop bandwidth is not necessary to acquire lock; this adjustment is made automatically by the Digital PLL. While acquiring lock, the digital loop bandwidth is automatically set to a large value. Once lock is achieved, the digital loop bandwidth will settle to the minimum value selected by the *ClkIn_BW[2:0]* bits.

Referenced Control	Register Location
ClkIn_BW[2:0]	“Clock Input Bandwidth (ClkIn_BW[2:0])” on page 33

5.3 Output to Input Frequency Ratio Configuration

5.3.1 User Defined Ratio (R_{UD}), Frequency Synthesizer Mode

The User Defined Ratio, R_{UD}, is a 32-bit un-signed fixed-point number which determines the basis for the desired input to output clock ratio. Up to four different ratios, *Ratio*$_{0\text{-}3}$, can be stored in the CS2000 register space. The ratio pointed to by the *RSel[1:0]* bits is the currently selected ratio for the static ratio based Frequency Synthesizer Mode. The 32-bit R_{UD} is represented in a high-resolution 12.20 format where the 12 MSBs represent the integer binary portion while the remaining 20 LSBs represent the fractional binary portion. The maximum multiplication factor is approximately 4096 with a resolution of 0.954 PPM in this configuration. See "Calculating the User Defined Ratio" on page 34 for more information.

The status of internal dividers, such as the internal timing reference clock divider, are automatically taken into account. Therefore R_{UD} is simply the desired ratio of the output to input clock frequencies.

Referenced Control	Register Location
Ratio$_{0\text{-}3}$	"Ratio 0 - 3 (Address 06h - 15h)" on page 31
Rsel[1:0]	"Ratio Selection (RSel[1:0])" on page 29

5.3.2 User Defined Ratio (R_{UD}), Hybrid PLL Mode

The same four ratio locations, *Ratio*$_{0\text{-}3}$, are used to store the User Defined Ratios for Hybrid PLL Mode. The User Defined Ratio pointed to by the *LockClk[1:0]* bits is the currently selected ratio for the dynamic ratio based Hybrid PLL Mode.

In addition to the High-Resolution format, a High-Multiplication format is also available. In the High-Multiplication Format Mode, the 32-bit R_{UD} is represented in a 20.12 format where the 20 MSBs represent the integer binary portion while the remaining 12 LSBs represent the fractional binary portion. In this configuration, the maximum multiplication factor is approximately 1,048,575 with a resolution of 244 PPM.

The ratio format default is 20.12. The 20.12 ratio format is only available when both the *LFRatioCfg* bit is cleared (20.12) and the *FracNSrc* bit is set (dynamic ratio). In Auto Fractional-N Source Mode (see section 5.3.5.2 on page 21) when CLK_IN is not present the *LFRatioCfg* bit is ignored and the ratio format is 12.20.

It is recommended that the 12.20 High-Resolution format be utilized whenever the desired ratio is less than 4096 since the output frequency accuracy of the PLL is directly proportional to the accuracy of the timing reference clock and the resolution of the R_{UD}.

Referenced Control	Register Location
LockClk[1:0]	"Lock Clock Ratio (LockClk[1:0])" section on page 30
LFRatioCfg	"Low-Frequency Ratio Configuration (LFRatioCfg)" on page 32
FracNSrc	"Fractional-N Source for Frequency Synthesizer (FracNSrc)" section on page 30

5.3.3 Ratio Modifier (R-Mod)

The Ratio Modifier is used to internally multiply/divide the currently addressed R_{UD} (the *Ratio*$_{0-3}$ stored in the register space remain unchanged). The available options for R_{MOD} are summarized in Table 1 on page 20.

The R-Mod value selected by *RModSel[2:0]* is always used in the calculation for the Effective Ratio (R_{EFF}), see "Effective Ratio (REFF)" on page 20. If R-Mod is not desired, *RModSel[2:0]* should be left at its default value of '000', which corresponds to an R-Mod value of 1, thereby effectively disabling the ratio modifier.

RModSel[2:0]	Ratio Modifier
000	1
001	2
010	4
011	8
100	0.5
101	0.25
110	0.125
111	0.0625

Table 1. Ratio Modifier

Referenced Control	Register Location
Ratio$_{0-3}$	"Ratio 0 - 3 (Address 06h - 15h)" on page 31
RModSel[2:0]	"R-Mod Selection (RModSel[2:0])" section on page 29

5.3.4 Effective Ratio (R_{EFF})

The Effective Ratio (R_{EFF}) is an internal calculation comprised of R_{UD} and the appropriate modifiers, as previously described. R_{EFF} is calculated as follows:

$R_{EFF} = R_{UD} \bullet R_{MOD}$

To simplify operation the device handles some of the ratio calculation functions automatically (such as when the internal timing reference clock divider is set). For this reason, the Effective Ratio does not need to be altered to account for internal dividers.

Ratio modifiers which would produce an overflow or truncation of R_{EFF} should not be used; For example if R_{UD} is 1024 an R_{MOD} of 8 would produce an R_{EFF} value of 8192 which exceeds the 4096 limit of the 12.20 format. In all cases, the maximum and minimum allowable values for R_{EFF} are dictated by the frequency limits for both the input and output clocks as shown in the "AC Electrical Characteristics" on page 8.

Selection of the user defined ratio from the four stored ratios is made by using the *RSel[1:0]* bits unless auto clock switching is enabled in which case the *LockClk[1:0]* bits also select the ratio (see *"Manual Fractional-N Source Selection for the Frequency Synthesizer" on page 21*).

Referenced Control	Register Location
RSel[1:0]	"Ratio Selection (RSel[1:0])" on page 29
LockClk[1:0]	"Lock Clock Ratio (LockClk[1:0])" section on page 30

5.3.5 *Fractional-N Source Selection*

To select between the static ratio based Frequency Synthesizer Mode and the dynamic ratio based Hybrid PLL Mode, the source for the fractional-N value for the Frequency Synthesizer must be changed. The Fractional-N value can either be sourced directly from the Effective Ratio (static ratio) or from the output of the Digital PLL (dynamic ratio) (see Figure 18 on page 22). The setting of this function can be made manual or automatically depending on the presence of CLK_IN.

5.3.5.1 *Manual Fractional-N Source Selection for the Frequency Synthesizer*

Manual selection of the fractional-N source for the frequency synthesizer is made by setting the *FracNSrc* bit to select the desired ratio source. The *LockClk[1:0]* bits (even if unused) must be set to the same value as the *RSel[1:0]* bits in order to maintain manual selectability of this function (see Section 5.3.5.2 on page 21).

Referenced Control	Register Location
Rsel[1:0]	“Device Configuration 1 (Address 03h)” on page 29
LockClk[1:0]	“Device Configuration 2 (Address 04h)” section on page 30
FracNSrc	“Device Configuration 2 (Address 04h)” section on page 30

5.3.5.2 *Automatic Fractional-N Source Selection for the Frequency Synthesizer*

Automatic source selection allows for the selection of the frequency synthesizer’s fractional-N value to be made dependent on the presence of the CLK_IN signal. When CLK_IN is present the device will use the dynamic ratio generated from the Digital PLL and CLK_IN for Hybrid PLL Mode. When CLK_IN is not present, the device will use RefClk and the static ratio for Frequency Synthesizer Mode. Before switching to SysClk and re-acquiring lock the CS2000 will wait for 2^{23} SysClk cycles after losing CLK_IN (see “CLK_IN Skipping Mode” on page 15).

The User Defined Ratio pointed to by *RSel[1:0]* should contain the desired CLK_OUT to RefClk ratio to be used when CLK_IN is not present. The User Defined Ratio pointed to by *LockClk[1:0]* should contain the desired CLK_OUT to CLK_IN ratio to be used when CLK_IN is present. Automatic source selection is enabled when the *LockClk[1:0]* bits are set to point to a different User Defined Ratio from the one pointed to by the *RSel[1:0]* bits.

When automatic source selection is enabled, the *FracNSrc* bit (used for manual clock selection) will be ignored.

To disable the automatic source selection feature, set the *LockClk[1:0]* bits and the *RSel[1:0]* bits to the same value. The *FracNSrc* bit must then be used to select the desired clock used for the PLL’s frequency reference.

Referenced Control	Register Location
RSel[1:0]	“Ratio Selection (RSel[1:0])” on page 29
LockClk[1:0]	“Lock Clock Ratio (LockClk[1:0])” section on page 30
FracNSrc	“Fractional-N Source for Frequency Synthesizer (FracNSrc)” section on page 30

5.3.6 Ratio Configuration Summary

The R_{UD} is the user defined ratio for which up to four different values ($Ratio_{0-3}$) can be stored in the register space. The *RSel[1:0]* or *LockClk[1:0]* bits then select the user defined ratio to be used (depending on if static or dynamic ratio mode is to be used). The resolution for the R_{UD} is selectable, for the dynamic ratio mode, by setting *LFRatioCfg*. R-Mod is applied if selected. The user defined ratio, and ratio modifier make up the effective ratio R_{EFF}, the final calculation used to determine the output to input clock ratio. The effective ratio is then corrected for the internal dividers. The frequency synthesizer's fractional-N source selection is made between the static ratio (in frequency synthesizer mode) or the dynamic ratio generated from the digital PLL (in Hybrid PLL mode) by either the *FracNSrc* bit for manual mode or the presence of CLK_IN in automatic mode. The conceptual diagram in Figure 18 summarizes the features involved in the calculation of the ratio values used to generate the fractional-N value which controls the Frequency Synthesizer.

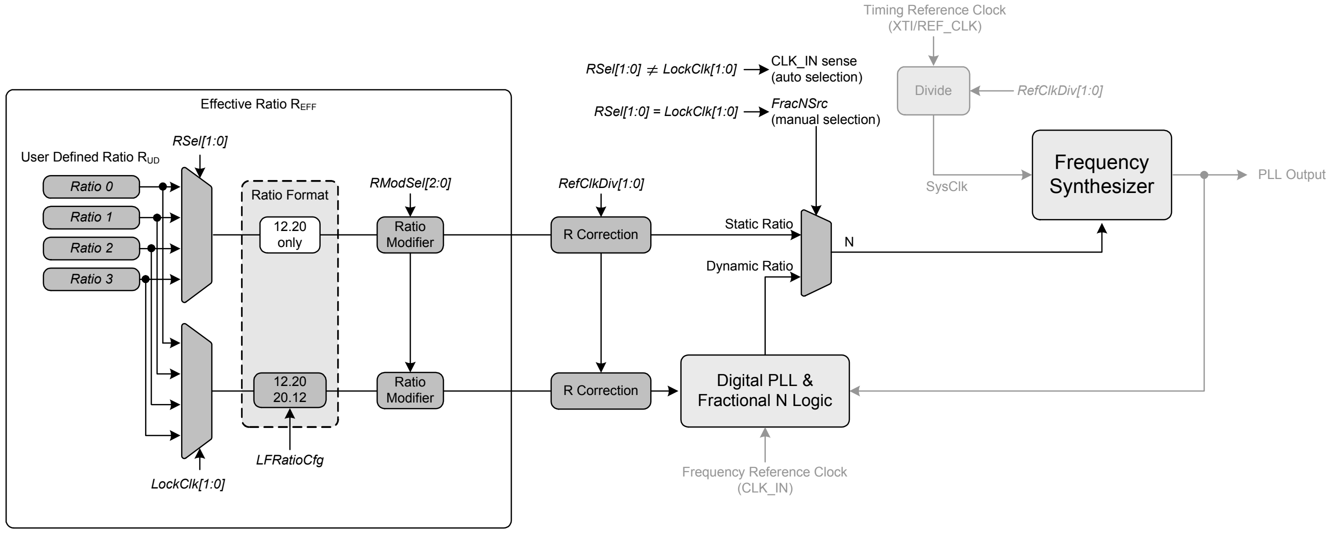

Figure 18. Ratio Feature Summary

Referenced Control	Register Location
$Ratio_{0-3}$	"Ratio 0 - 3 (Address 06h - 15h)" on page 31
RSel[1:0]	"Ratio Selection (RSel[1:0])" on page 29
LockClk[1:0]	"Lock Clock Ratio (LockClk[1:0])" section on page 30
LFRatioCfg	"Low-Frequency Ratio Configuration (LFRatioCfg)" on page 32
RModSel[2:0]	"R-Mod Selection (RModSel[2:0])" section on page 29
RefClkDiv[1:0]	"Reference Clock Input Divider (RefClkDiv[1:0])" on page 32
FracNSrc	"Fractional-N Source for Frequency Synthesizer (FracNSrc)" section on page 30

5.4 PLL Clock Output

The PLL clock output pin (CLK_OUT) provides a buffered version of the output of the frequency synthesizer. The driver can be set to high-impedance with the *ClkOutDis* bit.

The output from the PLL automatically drives a static low condition while the PLL is un-locked (when the clock may be unreliable). This feature can be disabled by setting the *ClkOutUnl* bit, however the state CLK_OUT may then be unreliable during an unlock condition.

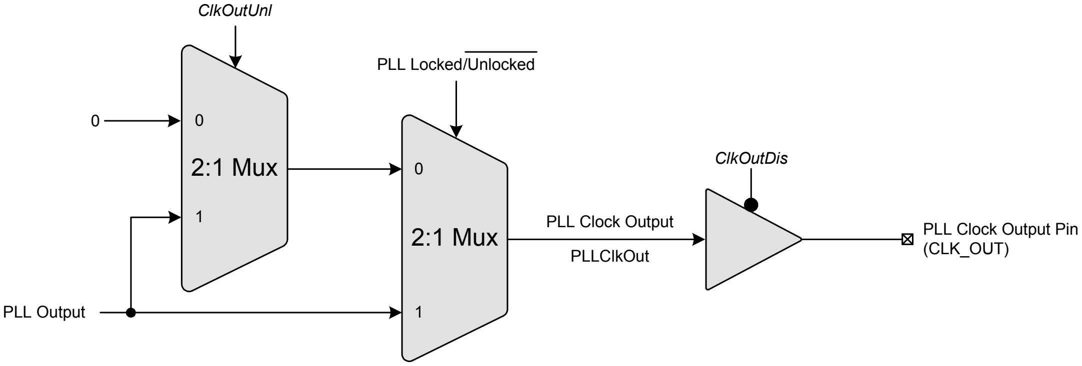

Figure 19. PLL Clock Output Options

Referenced Control	Register Location
ClkOutUnl	"Enable PLL Clock Output on Unlock (ClkOutUnl)" on page 32
ClkOutDis	"PLL Clock Output Disable (ClkOutDis)" on page 29

5.5 Auxiliary Output

The auxiliary output pin (AUX_OUT) can be mapped, as shown in Figure 20, to one of four signals: reference clock (RefClk), input clock (CLK_IN), additional PLL clock output (CLK_OUT), or a PLL lock indicator (Lock). The mux is controlled via the *AuxOutSrc[1:0]* bits. If AUX_OUT is set to Lock, the *AuxLockCfg* bit is then used to control the output driver type and polarity of the LOCK signal (see section 8.7.2 on page 32). In order to indicate an unlock condition, REF_CLK must be present. If AUX_OUT is set to CLK_OUT the phase of the PLL Clock Output signal on AUX_OUT may differ from the CLK_OUT pin. The driver for the pin can be set to high-impedance using the *AuxOutDis* bit.

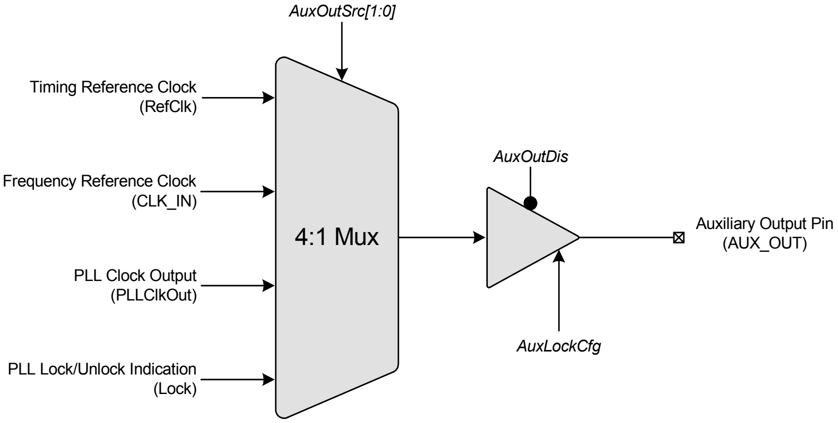

Figure 20. Auxiliary Output Selection

Referenced Control	Register Location
AuxOutSrc[1:0]	"Auxiliary Output Source Selection (AuxOutSrc[1:0])" on page 29
AuxOutDis	"Auxiliary Output Disable (AuxOutDis)" on page 28
AuxLockCfg	"AUX PLL Lock Output Configuration (AuxLockCfg)" section on page 32

5.6 Clock Output Stability Considerations

5.6.1 Output Switching

CS2000 is designed such that re-configuration of the clock routing functions do not result in a partial clock period on any of the active outputs (CLK_OUT and/or AUX_OUT). In particular, enabling or disabling an output, changing the auxiliary output source between REF_CLK and CLK_OUT, changing between Frequency Synthesizer and Hybrid PLL Mode, and the automatic disabling of the output(s) during unlock will not cause a runt or partial clock period.

The following exceptions/limitations exist:

- Enabling/disabling AUX_OUT when *AuxOutSrc[1:0]* = 11 (unlock indicator).
- Switching *AuxOutSrc[1:0]* to or from 01 (PLL clock input) and to or from 11 (unlock indicator) (Transitions between *AuxOutSrc[1:0]* = [00,10] will not produce a glitch).
- Changing the *ClkOutUnl* bit while the PLL is in operation.

When any of these exceptions occur, a partial clock period on the output may result.

5.6.2 PLL Unlock Conditions

Certain changes to the clock inputs and registers can cause the PLL to lose lock which will affect the presence the clock signal on CLK_OUT. The following outlines which conditions cause the PLL to go unlocked:

- Changes made to the registers which affect the Fraction-N value that is used by the Frequency Synthesizer. This includes all the bits shown in Figure 18 on page 22.
- Any discontinuities on the Timing Reference Clock, REF_CLK.
- Discontinuities on the Frequency Reference Clock, CLK_IN, except when the Clock Skipping feature is enabled and the requirements of Clock Skipping are satisfied (see “CLK_IN Skipping Mode” on page 15).
- Gradual changes in CLK_IN frequency greater than ±30% from the starting frequency.
- Step changes in CLK_IN frequency.

5.7 Required Power Up Sequencing

- Apply power to the device. The output pins will remain low until the device is configured with a valid ratio via the control port.
- Write the desired operational configurations. The *EnDevCfg1* and *EnDevCfg2* bits must be set to 1 during the initialization register writes; the order does not matter.
  - The *Freeze* bit may be set prior to this step and cleared afterward to ensure all settings take effect at the same time.

6. SPI / I²C CONTROL PORT

The control port is used to access the registers and allows the device to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to device inputs and outputs. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates with either the SPI or I²C interface, with the CS2000 acting as a slave device. SPI Mode is selected if there is a high-to-low transition on the AD0/$\overline{\text{CS}}$ pin after power-up. I²C Mode is selected by connecting the AD0/$\overline{\text{CS}}$ pin through a resistor to VD or GND, thereby permanently selecting the desired AD0 bit address state. In both modes the *EnDevCfg1* and *EnDevCfg2* bits must be set to 1 for normal operation.

WARNING: All “Reserved” registers must maintain their default state to ensure proper functional operation.

Referenced Control	Register Location
EnDevCfg1	“Enable Device Configuration Registers 1 (EnDevCfg1)” on page 30
EnDevCfg2	“Enable Device Configuration Registers 2 (EnDevCfg2)” section on page 31

6.1 SPI Control

In SPI Mode, $\overline{\text{CS}}$ is the chip select signal; CCLK is the control port bit clock (sourced from a microcontroller), and CDIN is the input data line from the microcontroller. Data is clocked in on the rising edge of CCLK. The device only supports write operations.

Figure 21 shows the operation of the control port in SPI Mode. To write to a register, bring $\overline{\text{CS}}$ low. The first eight bits on CDIN form the chip address and must be 10011110. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP.

There is MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will automatically increment after each byte is read or written, allowing block writes of successive registers.

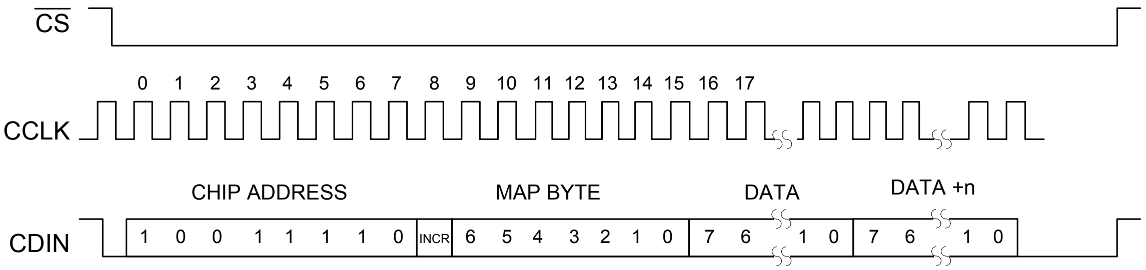

Figure 21. Control Port Timing in SPI Mode

6.2 I²C Control

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the device by the clock, SCL. There is no $\overline{\text{CS}}$ pin. The AD0 pin forms the least-significant bit of the chip address and should be connected to VD or GND as appropriate. The state of the AD0 pin should be maintained throughout operation of the device.

The signal timings for a read and write cycle are shown in Figure 22 and Figure 23. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS2000 after a Start condition consists of the 7-bit chip address field and a R/$\overline{\text{W}}$ bit (high for a read, low for a write). The upper 6 bits of the 7-bit address field are fixed at 100111 followed by the logic state of the AD0 pin. The