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Fractional-N Clock Multiplier with Internal LCO

Features

- Clock Multiplier / Jitter Reduction
  - Generates a Low Jitter 6 - 75 MHz Clock from a Jittery or Intermittent 50 Hz to 30 MHz Clock Source
- Internal LC Oscillator for Timing Reference
- Highly Accurate PLL Multiplication Factor
  - Maximum Error less than 1 PPM in High-Resolution Mode
- I²C / SPI™ Control Port
- Configurable Auxiliary Output
- Minimal Board Space Required
  - No External Analog Loop-filter Components

General Description

The CS2300-CP is an extremely versatile system clocking device that utilizes a programmable phase lock loop. The CS2300-CP is based on a hybrid analog-digital PLL architecture comprised of a unique combination of a Delta-Sigma Fractional-N Frequency Synthesizer and a Digital PLL. This architecture allows for generation of a low-jitter clock relative to an external noisy synchronization clock at frequencies as low as 50 Hz. The CS2300-CP supports both I²C and SPI for full software control.

The CS2300-CP is available in a 10-pin MSOP package in Commercial (-10°C to +70°C) and Automotive-D (-40°C to +85°C) and Automotive-E (-40°C to +105°C) grades. Customer development kits are also available for device evaluation. Please see "Ordering Information" on page 31 for complete details.

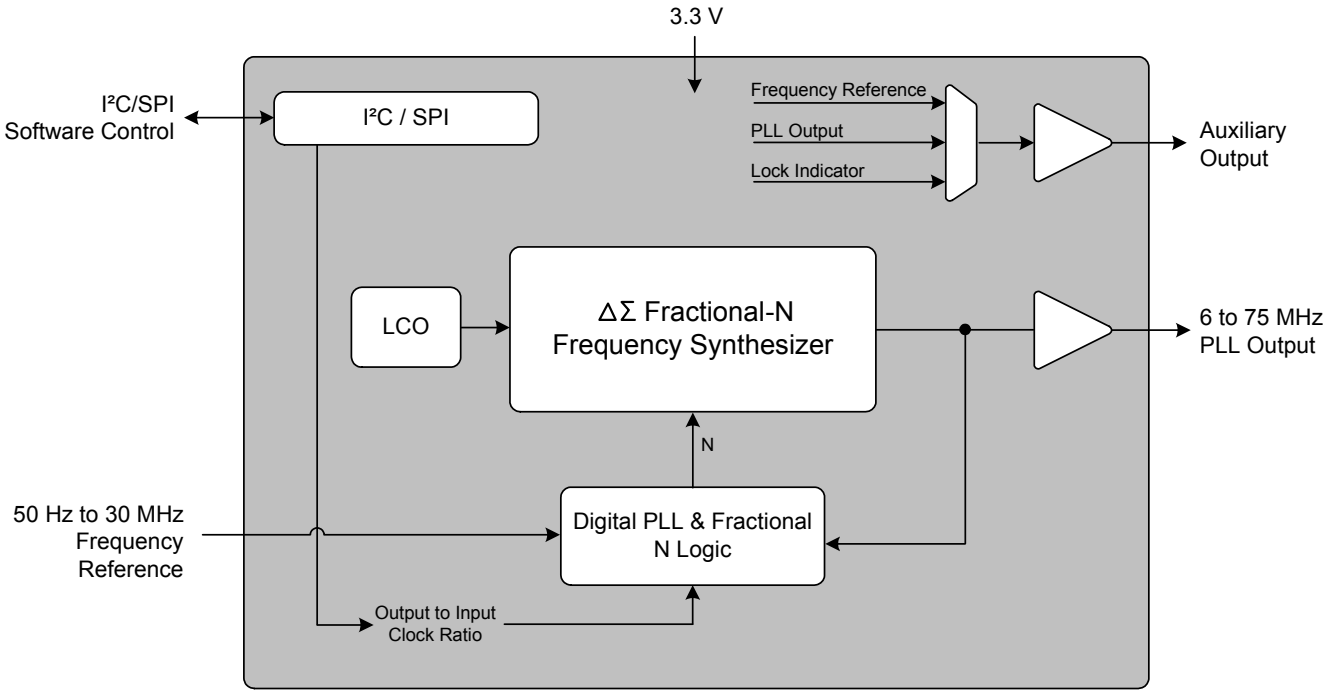
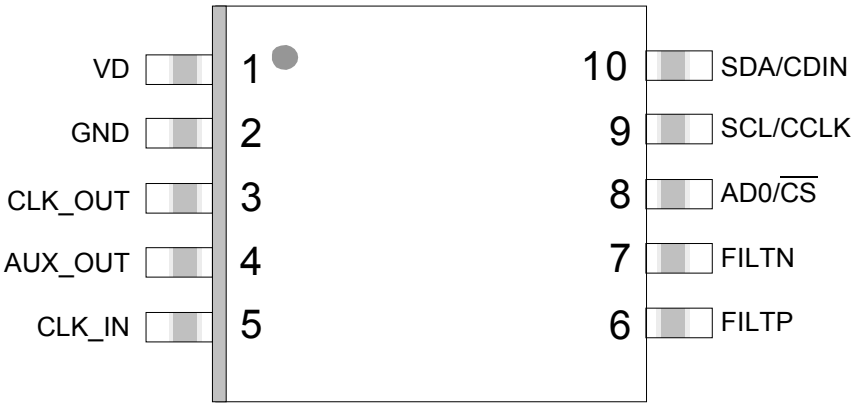


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	1	**Digital Power** (*Input*) - Positive power supply for the digital and analog sections.
GND	2	**Ground** (*Input*) - Ground reference.
CLK_OUT	3	**PLL Clock Output** (*Output*) - PLL clock output.
AUX_OUT	4	**Auxiliary Output** (*Output*) - This pin outputs a buffered version of one of the input or output clocks, or a status signal, depending on register configuration.
CLK_IN	5	**Frequency Reference Clock Input** (*Input*) - Clock input for the Digital PLL frequency reference.
FILTP FILTN	6 7	**LCO Filter Connections** (*Input/Output*) - These pins provide external supply filtering for the internal LC Oscillator.
AD0/$\overline{CS}$	8	**Address Bit 0 (I²C)** / **Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode. $\overline{CS}$ is the chip select signal in SPI Mode.
SCL/CCLK	9	**Control Port Clock** *(Input)* - SCL/CCLK is the serial clock for the serial control port in I²C and SPI mode.
SDA/CDIN	10	**Serial Control Data** (*Input/Output*) - SDA is the data I/O line in I²C Mode. CDIN is the input data line for the control port interface in SPI Mode.

2. TYPICAL CONNECTION DIAGRAM

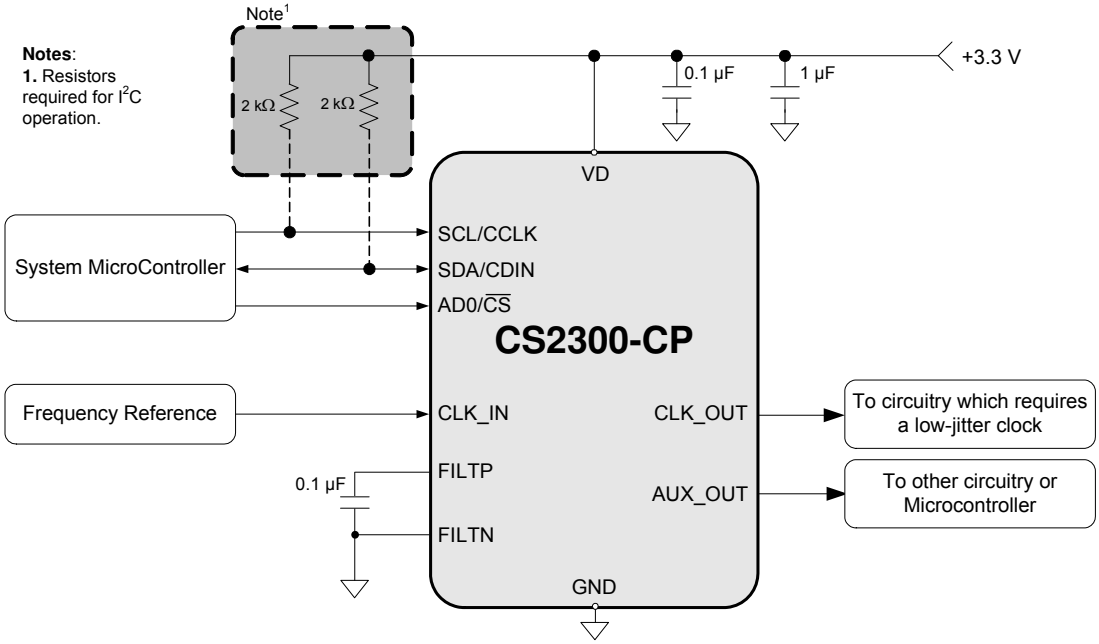


Figure 1. Typical Connection Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = 0 V; all voltages with respect to ground. (Note 1)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply	VD	3.1	3.3	3.5	V
Ambient Operating Temperature (Power Applied)					
Commercial Grade	T_{AC}	-10	-	+70	°C
Automotive Grade	T_{AD}	-40	-	+85	°C

Notes: 1. Device functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; all voltages with respect to ground.

Parameters	Symbol	Min	Max	Units
DC Power Supply	VD	-0.3	6.0	V
Input Current	I_{IN}	-	±10	mA
Digital Input Voltage (Note 2)	V_{IN}	-0.3	VD + 0.4	V
Ambient Operating Temperature (Power Applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Notes: 2. The maximum over/under voltage is limited by the input current except on the power supply pin.

DC ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise specified): VD = 3.1 V to 3.5 V; T_A = -10°C to +70°C (Commercial Grade); T_A = -40°C to +85°C (Automotive-D Grade); T_A = -40°C to +105°C (Automotive-E Grade).

Parameters	Symbol	Min	Typ	Max	Units
Power Supply Current - Unloaded (Note 3)	I_D	-	18	23	mA
Power Dissipation - Unloaded (Note 3)	P_D	-	59	76	mW
Input Leakage Current	I_{IN}	-	-	±10	µA
Input Capacitance	I_C	-	8	-	pF
High-Level Input Voltage	V_{IH}	70%	-	-	VD
Low-Level Input Voltage	V_{IL}	-	-	30%	VD
High-Level Output Voltage (I_{OH} = -1.2 mA)	V_{OH}	80%	-	-	VD
Low-Level Output Voltage (I_{OH} = 1.2 mA)	V_{OL}	-	-	20%	VD

Notes: 3. To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance and power supply voltage.
For example, f_{CLK_OUT} (49.152 MHz) * C_L(15 pF) * VD (3.3 V) = 2.4 mA of additional current due to these loading conditions on CLK_OUT.

AC ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise specified): VD = 3.1 V to 3.5 V; T_A = -10°C to +70°C (Commercial Grade); T_A = -40°C to +85°C (Automotive-D Grade); T_A = -40°C to +105°C (Automotive-E Grade); C_L = 15 pF.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Clock Input Frequency	f_{CLK_IN}		50 Hz	-	30	MHz
Clock Input Pulse Width	pw_{CLK_IN}	f_{CLK_IN} < 175 kHz f_{CLK_IN} > 175 kHz	140 10	- -	- -	ns ns
Clock Skipping Timeout	t_{CS}	(Notes 4, 5)	20	-	-	ms
Clock Skipping Input Frequency	f_{CLK_SKIP}	(Note 5)	50 Hz	-	80	kHz
PLL Clock Output Frequency	f_{CLK_OUT}	(Note 6)	6	-	75	MHz
PLL Clock Output Duty Cycle	t_{OD}	Measured at VD/2	45	50	55	%
Clock Output Rise Time	t_{OR}	20% to 80% of VD	-	1.7	3.0	ns
Clock Output Fall Time	t_{OF}	80% to 20% of VD	-	1.7	3.0	ns
Period Jitter	t_{JIT}	(Note 7)	-	35	-	ps rms
Base Band Jitter (100 Hz to 40 kHz)		(Notes 7, 8)	-	50	-	ps rms
Wide Band JItter (100 Hz Corner)		(Notes 7, 9)	-	150	-	ps rms
PLL Lock Time - CLK_IN (Note 10)	t_{LC}	f_{CLK_IN} < 200 kHz f_{CLK_IN} > 200 kHz	- -	100 1	200 3	UI ms

Notes: 4. t_{CS} represents the time from the removal of CLK_IN by which CLK_IN must be re-applied to ensure that PLL_OUT continues while the PLL re-acquires lock. This timeout is based on the internal VCO frequency, with the minimum timeout occurring at the maximum VCO frequency. Lower VCO frequencies will result in larger values of t_{CS}.

5. Only valid in clock skipping mode; See "CLK_IN Skipping Mode" on page 13 for more information.

6. f_{CLK_OUT} is ratio-limited when f_{CLK_IN} is below 72 Hz.

7. f_{CLK_OUT} = 24.576 MHz; Sample size = 10,000 points; *AuxOutSrc[1:0]* = 11.

8. In accordance with AES-12id-2006 section 3.4.2. Measurements are Time Interval Error taken with 3rd order 100 Hz to 40 kHz bandpass filter.

9. In accordance with AES-12id-2006 section 3.4.1. Measurements are Time Interval Error taken with 3rd order 100 Hz Highpass filter.

10. 1 UI (unit interval) corresponds to t_{CLK_IN} or $1/f_{CLK\_IN}$.

PLL PERFORMANCE PLOTS

Test Conditions (unless otherwise specified): VD = 3.3 V; T_A = 25 °C; C_L = 15 pF; f_{CLK_OUT} = 12.288 MHz; f_{CLK_IN} = 12.288 MHz; Sample size = 10,000 points; Base Band Jitter (100 Hz to 40 kHz); *AuxOutSrc[1:0]* = 11.

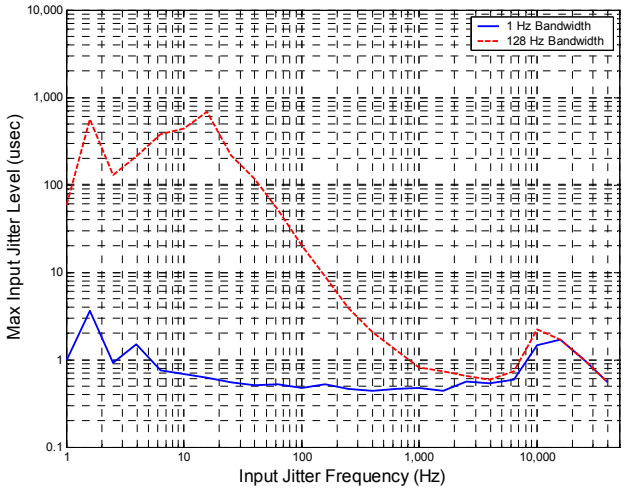


Figure 2. CLK_IN Sinusoidal Jitter Tolerance

Samples size = 2.5M points; Base Band Jitter (100Hz to 40kHz).

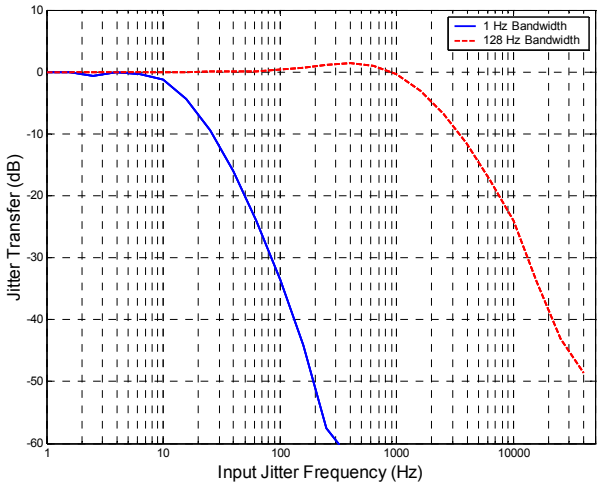


Figure 3. CLK_IN Sinusoidal Jitter Transfer

Samples size = 2.5M points; Base Band Jitter (100Hz to 40kHz).

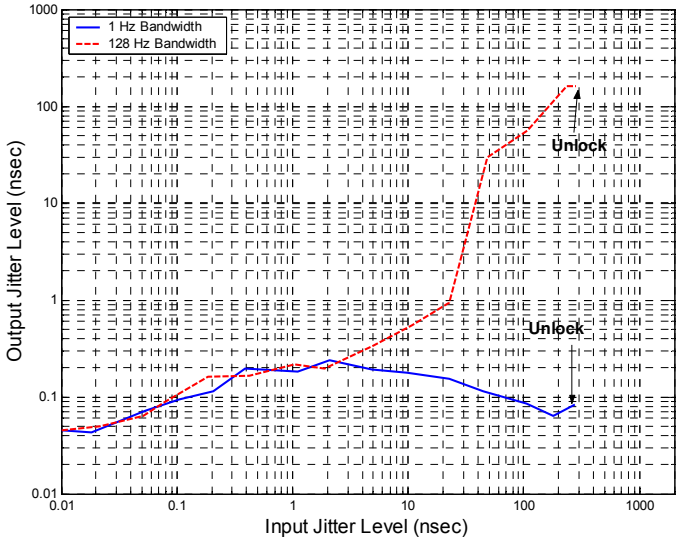


Figure 4. CLK_IN Random Jitter Rejection and Tolerance

CONTROL PORT SWITCHING CHARACTERISTICS- I²C FORMAT

Inputs: Logic 0 = GND; Logic 1 = VD; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free-Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low Time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 11)	t_{hdd}	0	-	µs
SDA Setup Time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_r	-	1	µs
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns
Delay from Supply Voltage Stable to Control Port Ready	t_{dpor}	100	-	µs

Notes: 11. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

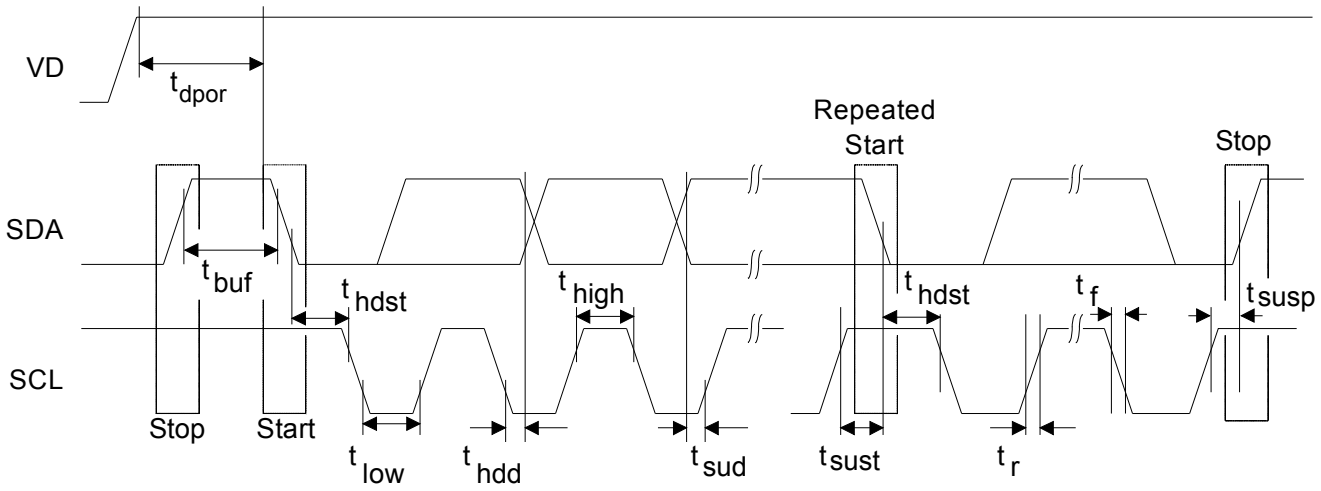


Figure 5. Control Port Timing - I²C Format

CONTROL PORT SWITCHING CHARACTERISTICS - SPI FORMAT

Inputs: Logic 0 = GND; Logic 1 = VD; C_L = 20 pF.

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency		f_{cclk}	-	6	MHz
CCLK Edge to $\overline{CS}$ Falling	(Note 12)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 13)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 14)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 14)	t_{f2}	-	100	ns
Delay from Supply Voltage Stable to Control Port Ready		t_{dpor}	100	-	µs

Notes: 12. t_{spi} is only needed before first falling edge of $\overline{CS}$ after power is applied. t_{spi} = 0 at all other times.

13. Data must be held for sufficient time to bridge the transition time of CCLK.

14. For f_{cclk} < 1 MHz.

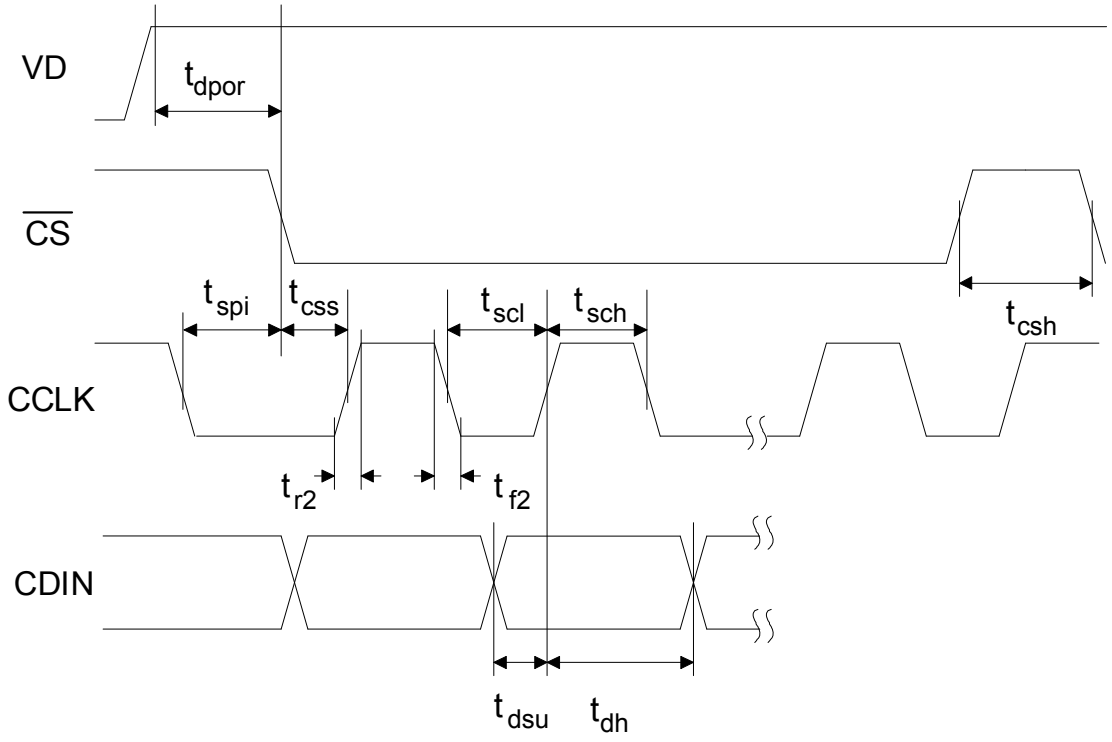


Figure 6. Control Port Timing - SPI Format (Write Only)

4. ARCHITECTURE OVERVIEW

4.1 Delta-Sigma Fractional-N Frequency Synthesizer

The core of the CS2300 is a Delta-Sigma Fractional-N Frequency Synthesizer which has very high-resolution for Input/Output clock ratios, low phase noise, very wide range of output frequencies and the ability to quickly tune to a new frequency. The reference for the synthesizer is an on chip LC Oscillator (LCO) which generates the necessary internal stable clocks. In very simplistic terms, the Fractional-N Frequency Synthesizer multiplies the LC Oscillator by the value of N to generate the PLL output clock. The desired output to input clock ratio is the value of N that is applied to the delta-sigma modulator (see Figure 7).

The analog PLL based frequency synthesizer uses a low-jitter timing reference clock, the LCO, as a time and phase reference for the internal voltage controlled oscillator (VCO). The phase comparator compares the fractional-N divided clock with the original timing reference and generates a control signal. The control signal is filtered by the internal loop filter to generate the VCO's control voltage which sets its output frequency. The delta-sigma modulator modulates the loop integer divide ratio to get the desired fractional ratio between the reference clock and the VCO output (thus the one's density of the modulator sets the fractional value). This allows the design to be optimized for very fast lock times for a wide range of output frequencies without the need for external filter components.

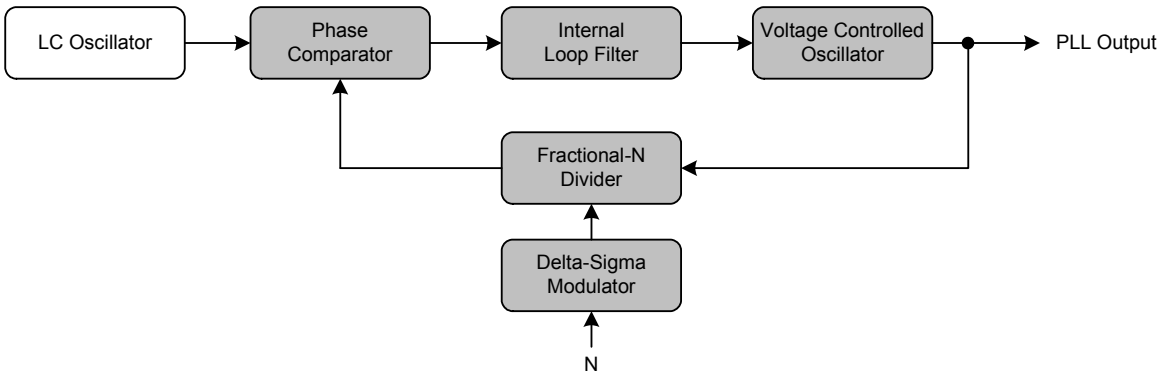


Figure 7. Delta-Sigma Fractional-N Frequency Synthesizer

4.2 Hybrid Analog-Digital Phase Locked Loop

The addition of the Digital PLL and Fractional-N Logic (shown in Figure 8) to the Fractional-N Frequency Synthesizer creates the Hybrid Analog-Digital Phase Locked Loop with many advantages over classical analog PLL techniques. These advantages include the ability to operate over extremely wide frequency ranges without the need to change external loop filter components while maintaining impressive jitter reduction performance. In the Hybrid architecture, the Digital PLL calculates the ratio of the PLL output clock to the frequency reference and compares that to the desired ratio. The digital logic generates a value of N which is then applied to the Fractional-N frequency synthesizer to generate the desired PLL output frequency. Notice that the frequency and phase of the LCO does not affect the output of the PLL since the digital control loop will correct for the PLL output. A major advantage of the Digital PLL is the ease with which the loop filter bandwidth can be altered. The PLL bandwidth is automatically set to a wide-bandwidth mode to quickly achieve lock and then reduced for optimal jitter rejection.

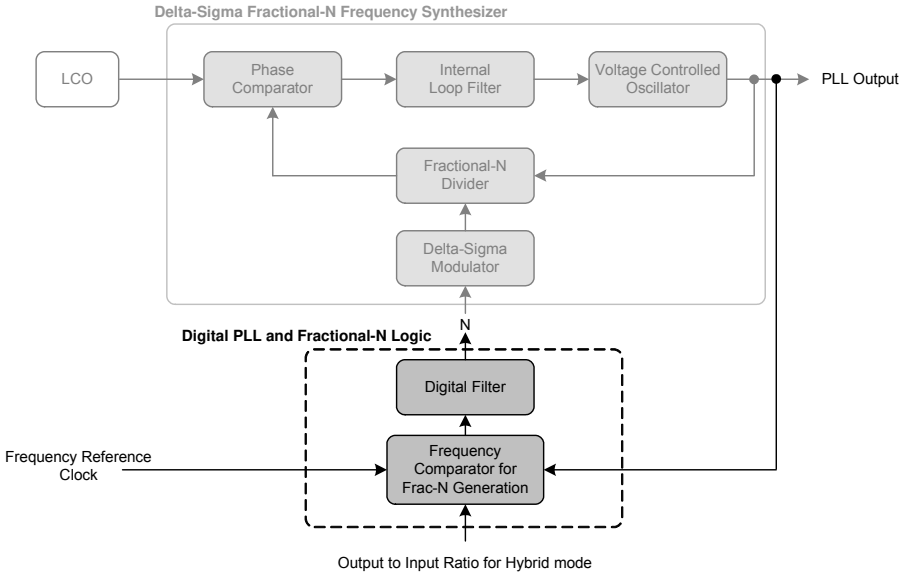


Figure 8. Hybrid Analog-Digital PLL

5. APPLICATIONS

5.1 Timing Reference Clock

The internal LC oscillator is used to generate the internal timing reference clock (see section 4 "Architecture Overview" on page 11 for information on how this internal clock is used by the CS2300). A single 0.1 µF cap must be connected between the FILTP and FILTN pins and the FILTN pin must be connected to ground as shown in Figure 9.

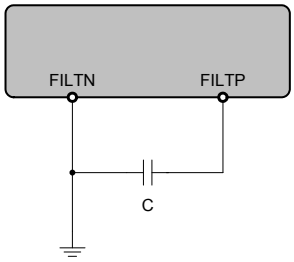


Figure 9. External Component Requirements for LCO

5.2 Frequency Reference Clock Input, CLK_IN

The frequency reference clock input (CLK_IN) is used by the Digital PLL and Fractional-N Logic block to dynamically generate a fractional-N value for the Frequency Synthesizer (see "Hybrid Analog-Digital PLL" on page 12). The Digital PLL first compares the CLK_IN frequency to the PLL output. The Fractional-N logic block then translates the desired ratio based off of CLK_IN to one based off of the internal LCO. This allows the low-jitter internal LCO to be used as the clock which the Frequency Synthesizer multiplies while maintaining synchronicity with the frequency reference clock through the Digital PLL. The allowable frequency range for CLK_IN is found in the "AC Electrical Characteristics" on page 7.

5.2.1 CLK_IN Skipping Mode

CLK_IN skipping mode allows the PLL to maintain lock even when the CLK_IN signal has missing pulses for up to 20 ms (t_{CS}) at a time (see "AC Electrical Characteristics" on page 7 for specifications). CLK_IN skipping mode can only be used when the CLK_IN frequency is below 80 kHz and CLK_IN is reapplied within 20 ms of being removed. The *ClkSkipEn* bit enables this function.

Regardless of the setting of the *ClkSkipEn* bit the PLL output will continue for 2^{23} LCO cycles (518 ms to 634 ms) after CLK_IN is removed (see Figure 10). This is true as long as CLK_IN does not glitch or have an effective change in period as the clock source is removed, otherwise the PLL will interpret this as a change in frequency causing clock skipping and the 2^{23} LCO cycle time-out to be bypassed and the PLL to immediately unlock. If the prior conditions are met while CLK_IN is removed and 2^{23} LCO cycles pass, the PLL will unlock and the PLL_OUT state will be determined by the *ClkOutUnl* bit; See "PLL Clock Output" on page 19. If CLK_IN is re-applied after such time, the PLL will remain unlocked for the specified time listed in the "AC Electrical Characteristics" on page 7 after which lock will be acquired and the PLL

output will resume.

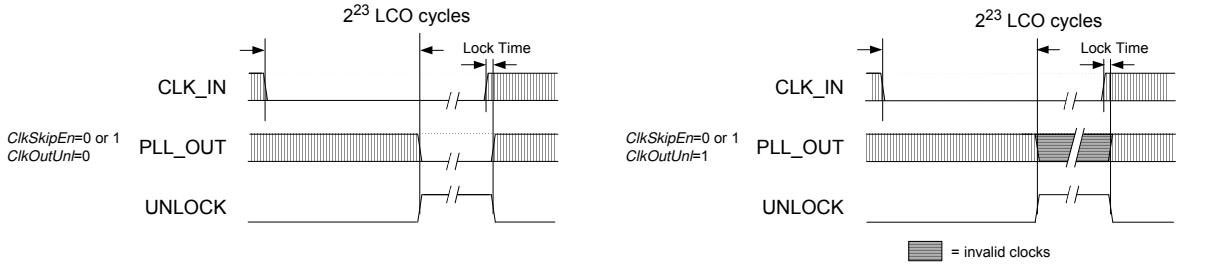


Figure 10. CLK_IN removed for > 2^{23} LCO cycles

If it is expected that CLK_IN will be removed and then reapplied within 2^{23} LCO cycles but later than t_{CS}, the *ClkSkipEn* bit should be disabled. If it is not disabled, the device will behave as shown in Figure 11; note that the lower figure shows that the PLL output frequency may change and be incorrect without an indication of an unlock condition.

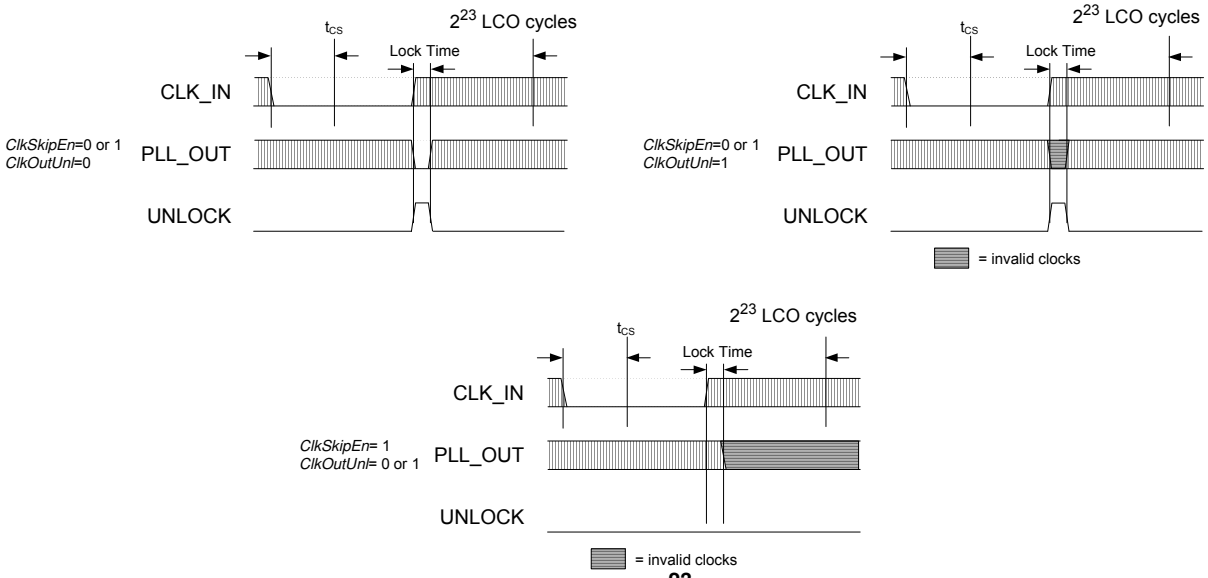


Figure 11. CLK_IN removed for < 2^{23} LCO cycles but > t_{CS}

If CLK_IN is removed and then re-applied within t_{CS}, the *ClkSkipEn* bit determines whether PLL_OUT continues while the PLL re-acquires lock (see Figure 12). When *ClkSkipEn* is disabled and CLK_IN is removed the PLL output will continue until CLK_IN is re-applied at which point the PLL will go unlocked only for the time it takes to acquire lock; the PLL_OUT state will be determined by the *ClkOutUnl* bit during this time. When *ClkSkipEn* is enabled and CLK_IN is removed the PLL output clock will remain continuous throughout the missing CLK_IN period including the time while the PLL re-acquires lock.

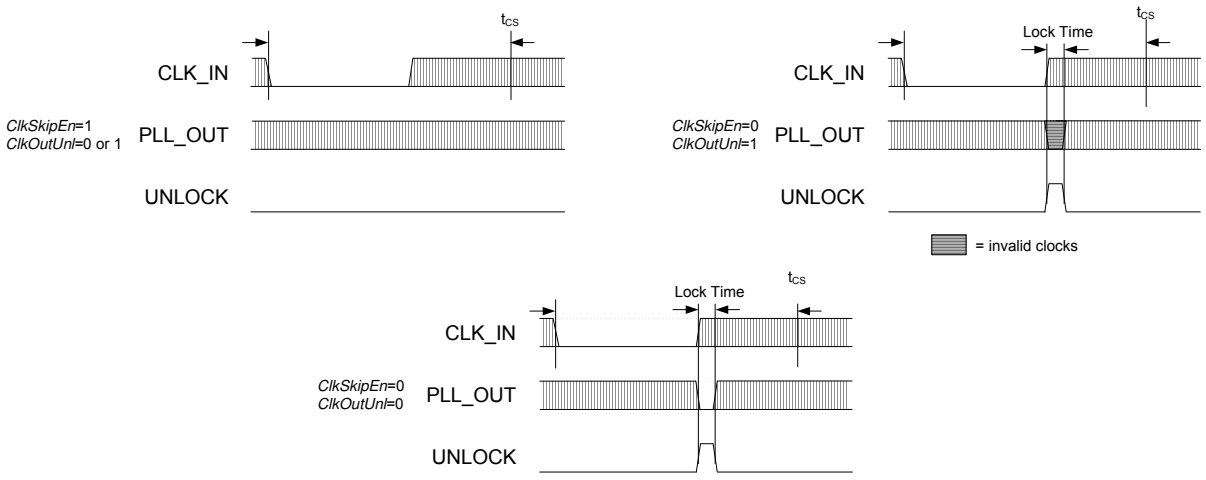


Figure 12. CLK_IN removed for < t_{CS}

Referenced Control	Register Location
ClkSkipEn	"Clock Skip Enable (ClkSkipEn)" on page 27
ClkOutUnl	"Enable PLL Clock Output on Unlock (ClkOutUnl)" on page 28

5.2.2 Adjusting the Minimum Loop Bandwidth for CLK_IN

The CS2300 allows the minimum loop bandwidth of the Digital PLL to be adjusted between 1 Hz and 128 Hz using the *ClkIn_BW[2:0]* bits. The minimum loop bandwidth of the Digital PLL directly affects the jitter transfer function; specifically, jitter frequencies below the loop bandwidth corner are passed from the PLL input directly to the PLL output without attenuation. In some applications it is desirable to have a very low minimum loop bandwidth to reject very low jitter frequencies, commonly referred to as wander. In others it may be preferable to remove only higher frequency jitter, allowing the input wander to pass through the PLL without attenuation.

Typically, applications in which the PLL_OUT signal creates a new clock domain from which all other system clocks and associated data are derived will benefit from the maximum jitter and wander rejection of

the lowest PLL bandwidth setting. See Figure 13.

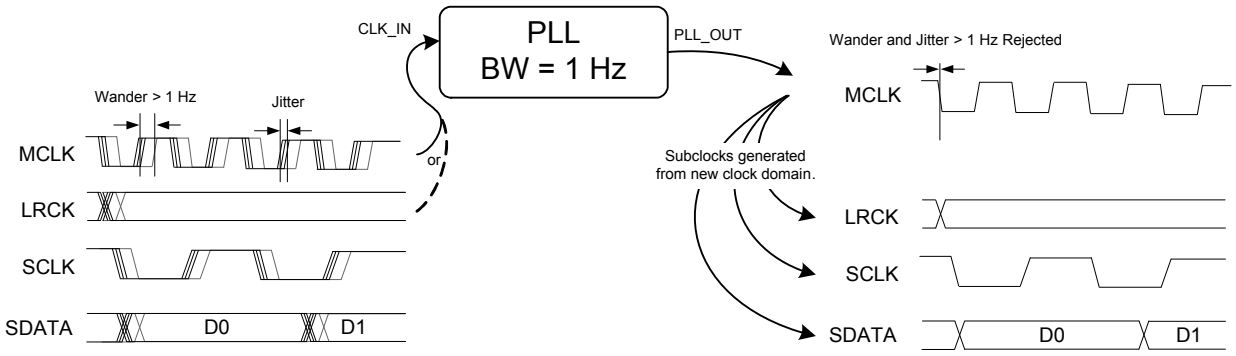


Figure 13. Low bandwidth and new clock domain

Systems in which some clocks and data are derived from the PLL_OUT signal while other clocks and data are derived from the CLK_IN signal will often require phase alignment of all the clocks and data in the system. See Figure 14. If there is substantial wander on the CLK_IN signal in these applications, it may be necessary to increase the minimum loop bandwidth allowing this wander to pass through to the CLK_OUT signal in order to maintain phase alignment. For these applications, it is advised to experiment with the loop bandwidth settings and choose the lowest bandwidth setting that does not produce system timing errors due to wandering between the clocks and data synchronous to the CLK_IN domain and those synchronous to the PLL_OUT domain.

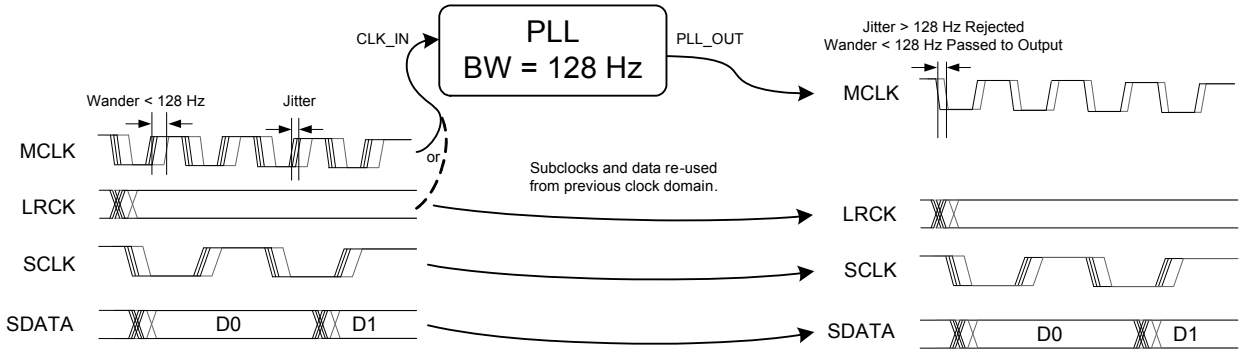


Figure 14. High bandwidth with CLK_IN domain re-use

It should be noted that manual adjustment of the minimum loop bandwidth is not necessary to acquire lock; this adjustment is made automatically by the Digital PLL. While acquiring lock, the digital loop bandwidth is automatically set to a large value. Once lock is achieved, the digital loop bandwidth will settle to the minimum value selected by the *ClkIn_BW[2:0]* bits.

Referenced Control	Register Location
ClkIn_BW[2:0]	"Clock Input Bandwidth (ClkIn_BW[2:0])" on page 28

5.3 Output to Input Frequency Ratio Configuration

5.3.1 User Defined Ratio (R_{UD})

The User Defined Ratio, R_{UD}, is a 32-bit un-signed fixed-point number, stored in the *Ratio* register set, which determines the basis for the desired input to output clock ratio. The 32-bit R_{UD} can be expressed

in either a high resolution (12.20) or high multiplication (20.12) format selectable by the *LFRatioCfg* bit, with 20.12 being the default.

The R_{UD} for high resolution (12.20) format is encoded with 12 MSBs representing the integer binary portion with the remaining 20 LSBs representing the fractional binary portion. The maximum multiplication factor is approximately 4096 with a resolution of 0.954 PPM in this configuration. See "Calculating the User Defined Ratio" on page 29 for more information.

The R_{UD} for high multiplication (20.12) format is encoded with 20 MSBs representing the integer binary portion with the remaining 12 LSBs representing the fractional binary portion. In this configuration, the maximum multiplication factor is approximately 1,048,575 with a resolution of 244 PPM. It is recommended that the 12.20 High-Resolution format be utilized whenever the desired ratio is less than 4096 since the output frequency accuracy of the PLL is directly proportional to the accuracy of the timing reference clock and the resolution of the R_{UD}.

Referenced Control	Register Location
Ratio	"Ratio (Address 06h - 09h)" on page 26
LFRatioCfg	"Low-Frequency Ratio Configuration (LFRatioCfg)" on page 28

5.3.2 Ratio Modifier (R-Mod)

The Ratio Modifier is used to internally multiply/divide the R_{UD} (the *Ratio* stored in the register space remains unchanged). The available options for R_{MOD} are summarized in Table 1 on page 17.

The R-Mod value selected by *RModSel[2:0]* is always used in the calculation for the Effective Ratio (R_{EFF}), see "Effective Ratio (REFF)" on page 17. If R-Mod is not desired, *RModSel[2:0]* should be left at its default value of '000', which corresponds to an R-Mod value of 1, thereby effectively disabling the ratio modifier.

RModSel[2:0]	Ratio Modifier
000	1
001	2
010	4
011	8
100	0.5
101	0.25
110	0.125
111	0.0625

Table 1. Ratio Modifier

Referenced Control	Register Location
Ratio	"Ratio (Address 06h - 09h)" on page 26
RModSel[2:0]	"R-Mod Selection (RModSel[2:0])" section on page 25

5.3.3 Effective Ratio (R_{EFF})

The Effective Ratio (R_{EFF}) is an internal calculation comprised of R_{UD} and the appropriate modifiers, as previously described. R_{EFF} is calculated as follows:

$$R_{EFF} = R_{UD} \bullet R_{MOD}$$

Ratio modifiers which would produce an overflow or truncation of R_{EFF} should not be used; For example if R_{UD} is 1024 an R_{MOD} of 8 would produce an R_{EFF} value of 8192 which exceeds the 4096 limit of the 12.20 format. In all cases, the maximum and minimum allowable values for R_{EFF} are dictated by the frequency limits for both the input and output clocks as shown in the "AC Electrical Characteristics" on page 7.

5.3.4 Ratio Configuration Summary

The R_{UD} is the user defined ratio stored in the register space. The resolution for the R_{UD} is selectable by setting *LFRatioCfg*. R-Mod is applied if selected. The user defined ratio, and ratio modifier make up the effective ratio R_{EFF}, the final calculation used to determine the output to input clock ratio. The conceptual diagram in Figure 15 summarizes the features involved in the calculation of the ratio values used to generate the fractional-N value which controls the Frequency Synthesizer.

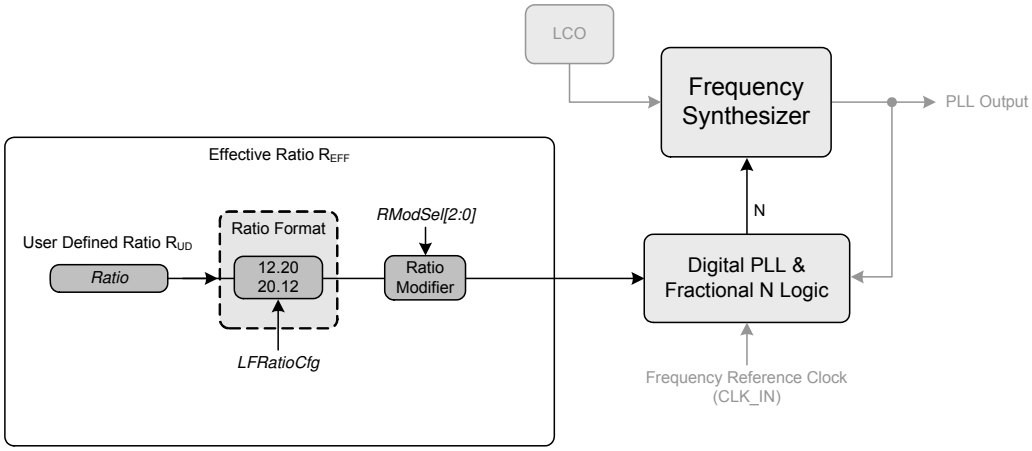


Figure 15. Ratio Feature Summary

Referenced Control	Register Location
Ratio	"Ratio (Address 06h - 09h)" on page 26
LFRatioCfg	"Low-Frequency Ratio Configuration (LFRatioCfg)" on page 28
RModSel[2:0]	"R-Mod Selection (RModSel[2:0])" section on page 25

5.4 PLL Clock Output

The PLL clock output pin (CLK_OUT) provides a buffered version of the output of the frequency synthesizer. The driver can be set to high-impedance with the *ClkOutDis* bit.

The output from the PLL automatically drives a static low condition while the PLL is un-locked (when the clock may be unreliable). This feature can be disabled by setting the *ClkOutUnl* bit, however the state CLK_OUT may then be unreliable during an unlock condition.

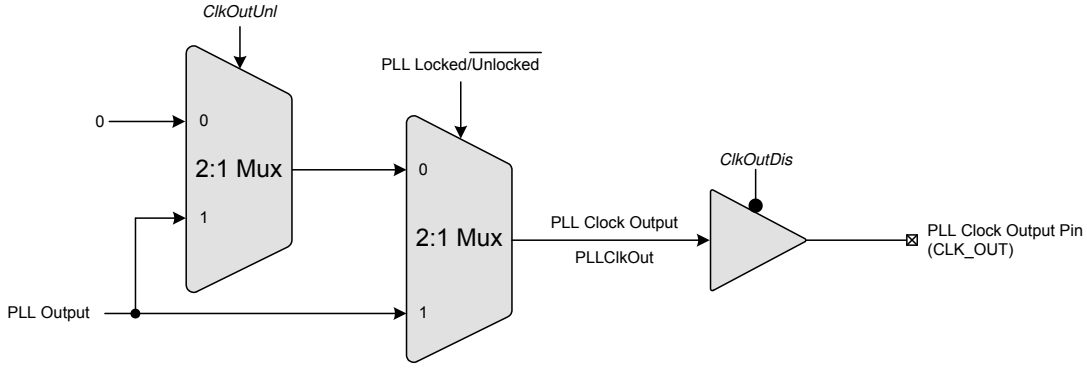


Figure 16. PLL Clock Output Options

Referenced Control	Register Location
ClkOutUnl	"Enable PLL Clock Output on Unlock (ClkOutUnl)" on page 28
ClkOutDis	"PLL Clock Output Disable (ClkOutDis)" on page 25

5.5 Auxiliary Output

The auxiliary output pin (AUX_OUT) can be mapped, as shown in Figure 17, to one of three signals: input clock (CLK_IN), additional PLL clock output (CLK_OUT), or a PLL lock indicator (Lock). The mux is controlled via the *AuxOutSrc[1:0]* bits. If AUX_OUT is set to Lock, the *AuxLockCfg* bit is then used to control the output driver type and polarity of the LOCK signal (see section 8.6.2 on page 27). In order to indicate an unlock condition, REF_CLK must be present. If AUX_OUT is set to CLK_OUT the phase of the PLL Clock Output signal on AUX_OUT may differ from the CLK_OUT pin. The driver for the pin can be set to high-impedance using the *AuxOutDis* bit.

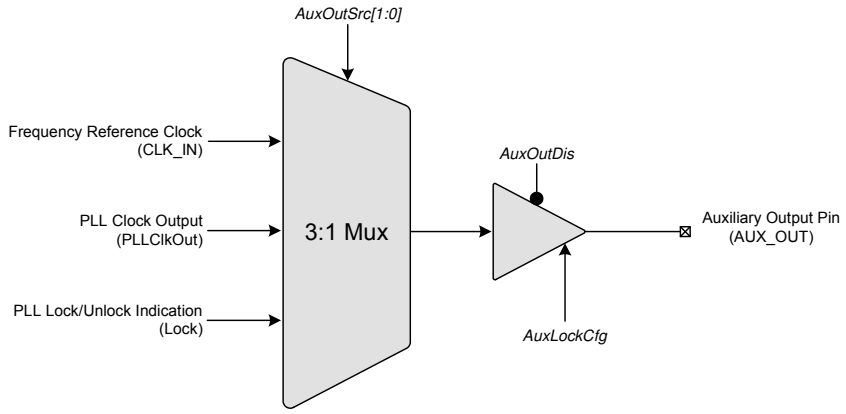


Figure 17. Auxiliary Output Selection

Referenced Control	Register Location
AuxOutSrc[1:0]	"Auxiliary Output Source Selection (AuxOutSrc[1:0])" on page 25
AuxOutDis	"Auxiliary Output Disable (AuxOutDis)" on page 24
AuxLockCfg	"AUX PLL Lock Output Configuration (AuxLockCfg)" section on page 27

5.6 Clock Output Stability Considerations

5.6.1 Output Switching

CS2300 is designed such that re-configuration of the clock routing functions do not result in a partial clock period on any of the active outputs (CLK_OUT and/or AUX_OUT). In particular, enabling or disabling an output, and the automatic disabling of the output(s) during unlock will not cause a runt or partial clock period.

The following exceptions/limitations exist:

- Enabling/disabling AUX_OUT when *AuxOutSrc[1:0]* = 11 (unlock indicator).
- Switching *AuxOutSrc[1:0]* to or from 01 (PLL clock input) and to or from 11 (unlock indicator) (Transitions between *AuxOutSrc[1:0]* = [00,10] will not produce a glitch).
- Changing the *ClkOutUnl* bit while the PLL is in operation.

When any of these exceptions occur, a partial clock period on the output may result.

5.6.2 PLL Unlock Conditions

Certain changes to the clock inputs and registers can cause the PLL to lose lock which will affect the presence the clock signal on CLK_OUT. The following outlines which conditions cause the PLL to go unlocked:

- Changes made to the registers which affect the Fraction-N value that is used by the Frequency Synthesizer. This includes all the bits shown in Figure 15 on page 18.
- Any discontinuities on the Timing Reference Clock, REF_CLK.
- Discontinuities on the Frequency Reference Clock, CLK_IN, except when the Clock Skipping feature is enabled and the requirements of Clock Skipping are satisfied (see "CLK_IN Skipping Mode" on page 13).
- Gradual changes in CLK_IN frequency greater than ±30% from the starting frequency.
- Step changes in CLK_IN frequency.

5.7 Required Power Up Sequencing

- Apply power to the device. The output pins will remain low until the device is configured with a valid ratio via the control port.
- Write the desired operational configurations. The *EnDevCfg1, EnDevCfg2, and EnDevCfg3* bits must be set to 1 during the initialization register writes; the order does not matter.
  - The *Freeze* bit may be set prior to this step and cleared afterward to ensure all settings take effect at the same time.

6. SPI / I²C CONTROL PORT

The control port is used to access the registers and allows the device to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to device inputs and outputs. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates with either the SPI or I²C interface, with the CS2300 acting as a slave device. SPI Mode is selected if there is a high-to-low transition on the AD0/CS pin after power-up. I²C Mode is selected by connecting the AD0/CS pin through a resistor to VD or GND, thereby permanently selecting the desired AD0 bit address state. In both modes the *EnDevCfg1, EnDevCfg2, and EnDevCfg3* bits must be set to 1 for normal operation.

WARNING: All "Reserved" registers must maintain their default state to ensure proper functional operation.

Referenced Control	Register Location
EnDevCfg1	"Enable Device Configuration Registers 1 (EnDevCfg1)" on page 26
EnDevCfg2	"Enable Device Configuration Registers 2 (EnDevCfg2)" section on page 26
EnDevCfg3	"Enable Device Configuration Registers 3 (EnDevCfg3)" section on page 27

6.1 SPI Control

In SPI Mode, CS is the chip select signal; CCLK is the control port bit clock (sourced from a microcontroller), and CDIN is the input data line from the microcontroller. Data is clocked in on the rising edge of CCLK. The device only supports write operations.

Figure 18 shows the operation of the control port in SPI Mode. To write to a register, bring CS low. The first eight bits on CDIN form the chip address and must be 10011110. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP.

There is MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will automatically increment after each byte is read or written, allowing block writes of successive registers.

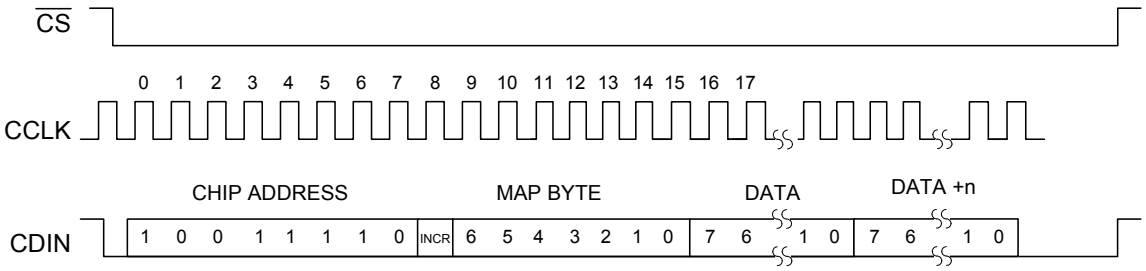


Figure 18. Control Port Timing in SPI Mode

6.2 I²C Control

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the device by the clock, SCL. There is no CS pin. The AD0 pin forms the least-significant bit of the chip address and should be connected to VD or GND as appropriate. The state of the AD0 pin should be maintained throughout operation of the device.

The signal timings for a read and write cycle are shown in Figure 19 and Figure 20. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS2300 after a Start condition consists of the 7-bit chip address field and a R/W bit (high for a read, low for a write). The upper 6 bits of the 7-bit address field are fixed at 100111 followed by the logic state of the AD0 pin. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS2300 after each input byte is read and is input from the microcontroller after each transmitted byte.

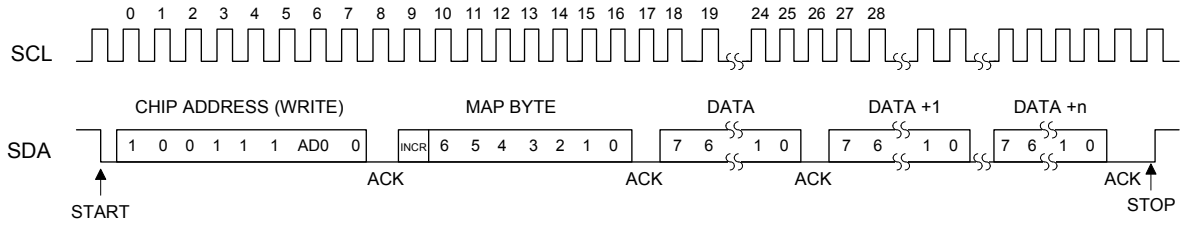


Figure 19. Control Port Timing, I²C Write

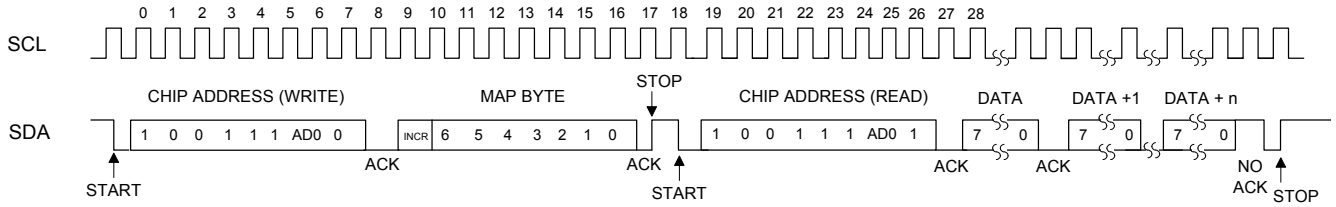


Figure 20. Control Port Timing, I²C Aborted Write + Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 19, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 100111x0 (chip address & write operation).

Receive acknowledge bit.

Send MAP byte, auto increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 100111x1(chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

6.3 Memory Address Pointer

The Memory Address Pointer (MAP) byte comes after the address byte and selects the register to be read or written. Refer to the pseudocode above for implementation details.

6.3.1 Map Auto Increment

The device has MAP auto increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is read or written, allowing block reads or writes of successive registers.

7. REGISTER QUICK REFERENCE

This table shows the register and bit names with their associated default values.
EnDevCfg1, EnDevCfg2, and EnDevCfg3 bits must be set to 1 for normal operation.

WARNING: All “Reserved” registers must maintain their default state to ensure proper functional operation.

Adr	Name	7	6	5	4	3	2	1	0
01h p 24	Device ID	Device4 0	Device3 0	Device2 0	Device1 0	Device0 0	Revision2 x	Revision1 x	Revision0 x
02h p 24	Device Ctrl	Unlock x	Reserved x	Reserved x	Reserved 0	Reserved 0	Reserved 0	AuxOutDis 0	ClkOutDis 0
03h p 25	Device Cfg 1	RModSel2 0	RModSel1 0	RModSel0 0	Reserved 0	Reserved 0	AuxOutSrc1 0	AuxOutSrc0 0	EnDevCfg1 0
05h p 26	Global Cfg	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Freeze 0	Reserved 0	Reserved 0	EnDevCfg2 0
06h - 09h	32-Bit Ratio	MSB MSB-8 LSB+15 LSB+7	.....	.....	.....	.....	.....	.....	MSB-7 MSB-15 LSB+8 LSB
16h p 27	Funct Cfg 1	ClkSkipEn 0	AuxLockCfg 0	Reserved 0	EnDevCfg3 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
17h p 28	Funct Cfg 2	Reserved 0	Reserved 0	Reserved 0	ClkOutUnl 0	LFRatioCfg 0	Reserved 0	Reserved 0	Reserved 0
1Eh p 28	Funct Cfg 3	Reserved 0	ClkIn_BW2 0	ClkIn_BW1 0	ClkIn_BW0 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0

8. REGISTER DESCRIPTIONS

In I²C Mode all registers are read/write unless otherwise stated. In SPI mode all registers are write only. All "Reserved" registers must maintain their default state to ensure proper functional operation. The default state of each bit after a power-up sequence or reset is indicated by the shaded row in the bit decode table and in the "Register Quick Reference" on page 23.

Control port mode is entered when the device recognizes a valid chip address input on its I²C/SPI serial control pins and the *EnDevCfg1, EnDevCfg2, and EnDevCfg3* bits are set to 1.

8.1 Device I.D. and Revision (Address 01h)

7	6	5	4	3	2	1	0
Device4	Device3	Device2	Device1	Device0	Revision2	Revision1	Revision0

8.1.1 Device Identification (Device[4:0]) - Read Only

I.D. code for the CS2300.

Device[4:0]	Device
00000	CS2300.

8.1.2 Device Revision (Revision[2:0]) - Read Only

CS2300 revision level.

REVID[2:0]	Revision Level
100	B2 and B3
110	C1

8.2 Device Control (Address 02h)

7	6	5	4	3	2	1	0
Unlock	Reserved	Reserved	Reserved	Reserved	Reserved	AuxOutDis	ClkOutDis

8.2.1 Unlock Indicator (Unlock) - Read Only

Indicates the lock state of the PLL.

Unlock	PLL Lock State
0	PLL is Locked.
1	PLL is Unlocked.

Note: Bit 7 is sticky until read.

8.2.2 Auxiliary Output Disable (AuxOutDis)

This bit controls the output driver for the AUX_OUT pin.

AuxOutDis	Output Driver State
0	AUX_OUT output driver enabled.
1	AUX_OUT output driver set to high-impedance.
Application:	"Auxiliary Output" on page 19

8.2.3 PLL Clock Output Disable (ClkOutDis)

This bit controls the output driver for the CLK_OUT pin.

ClkOutDis	Output Driver State
0	CLK_OUT output driver enabled.
1	CLK_OUT output driver set to high-impedance.
Application:	"PLL Clock Output" on page 19

8.3 Device Configuration 1 (Address 03h)

7	6	5	4	3	2	1	0
RModSel2	RModSel1	RModSel0	Reserved	Reserved	AuxOutSrc1	AuxOutSrc0	EnDevCfg1

8.3.1 R-Mod Selection (RModSel[2:0])

Selects the R-Mod value, which is used as a factor in determining the PLL's Fractional N.

RModSel[2:0]	R-Mod Selection
000	Left-shift R-value by 0 (x 1).
001	Left-shift R-value by 1 (x 2).
010	Left-shift R-value by 2 (x 4).
011	Left-shift R-value by 3 (x 8).
100	Right-shift R-value by 1 (÷ 2).
101	Right-shift R-value by 2 (÷ 4).
110	Right-shift R-value by 3 (÷ 8).
111	Right-shift R-value by 4 (÷ 16).
Application:	"Ratio Modifier (R-Mod)" on page 17

8.3.2 Auxiliary Output Source Selection (AuxOutSrc[1:0])

Selects the source of the AUX_OUT signal.

AuxOutSrc[1:0]	Auxiliary Output Source
00	Reserved.
01	CLK_IN.
10	CLK_OUT.
11	PLL Lock Status Indicator.
Application:	"Auxiliary Output" on page 19

Note: When set to 11, *AuxLckCfg* sets the polarity and driver type. See "AUX PLL Lock Output Configuration (AuxLockCfg)" on page 27.