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# Phase Control Thyristor

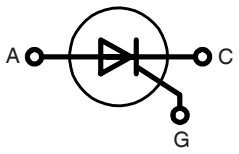
# ISOPLUS220™

## Electrically Isolated Back Surface

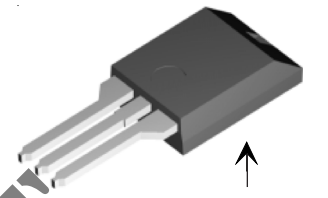
Preliminary Data Sheet

$V_{RRM}$ = 800/1200 V
$I_{T(RMS)}$ = 35 A
$I_{T(AV)M}$ = 23 A

| $V_{RSM}$ $V_{DSM}$ V | $V_{RRM}$ $V_{DRM}$ V | Type |
|---|---|---|
| 800 | 800 | CS 29-08io1C |
| 1200 | 1200 | CS 29-12io1C |




ISOPLUS 220™




| Symbol | Conditions | | Maximum Ratings | |
|---|---|---|---|---|
| $I_{T(RMS)}$ | $T_{VJ} = T_{VJM}$ | | 35 | A |
| $I_{T(AV)M}$ | $T_C$ = 95°C; 180° sine ($I_{T(RMS)}$ current limit) | | 23 | A |
| $I_{TSM}$ | $T_{VJ}$ = 45°C; | t = 10 ms (50 Hz), sine | 200 | A |
| | $V_R$ = 0 V | t = 8.3 ms (60 Hz), sine | 215 | A |
| | $T_{VJ} = T_{VJM}$; | t = 10 ms (50 Hz), sine | 175 | A |
| | $V_R$ = 0 V | t = 8.3 ms (60 Hz), sine | 185 | A |
| $I^2t$ | $T_{VJ}$ = 45°C; | t = 10 ms (50 Hz), sine | 200 | $A^2s$ |
| | $V_R$ = 0 V | t = 8.3 ms (60 Hz), sine | 195 | $A^2s$ |
| | $T_{VJ} = T_{VJM}$; | t = 10 ms (50 Hz), sine | 155 | $A^2s$ |
| | $V_R$ = 0 V | t = 8.3 ms (60 Hz), sine | 145 | $A^2s$ |
| $(di/dt)_{cr}$ | $T_{VJ} = T_{VJM}$; | repetitive, $I_T$ = 40 A | 150 | A/µs |
| | f = 50 Hz; $t_P$ = 200 µs; | | | |
| | $V_D = {}^2/_3 V_{DRM}$; | | | |
| | $I_G$ = 0.2 A; | non repetitive, $I_T = I_{T(AV)M}$ | 500 | A/µs |
| | $di_G/dt$ = 0.2 A/µs | | | |
| $(dv/dt)_{cr}$ | $T_{VJ} = T_{VJM}$; | $V_{DR} = {}^2/_3 V_{DRM}$; | 1000 | V/µs |
| | $R_{GK} = \infty$; method 1 (linear voltage rise) | | | |
| $P_{GM}$ | $T_{VJ} = T_{VJM}$; | $t_P$ = 30 µs | 5 | W |
| | $I_T = I_{T(AV)M}$; | $t_P$ = 300 µs | 2.5 | W |
| $P_{GAV}$ | | | 0.5 | W |
| $V_{RGM}$ | | | 10 | V |
| $T_{VJ}$ | | | -40...+150 | °C |
| $T_{VJM}$ | | | 150 | °C |
| $T_{stg}$ | | | -40...+150 | °C |
| $V_{ISOL}$ | 50/60 Hz RMS; $I_{ISOL} \leq$ 1 mA | 2500 | V~ | |
| $T_L$ | 1.6 mm from case; 10 s | | 260 | °C |
| $F_C$ | Mounting force | | 11...65 / 2.4...11 | N/lb |
| Weight | | | 2 | g |

### Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500 V electrical isolation
- Low cathode-to-tab capacitance (15 pF typical)
- Planar passivated chips
- Epoxy meets UL 94V-0
- High performance glass passivated chip
- Long-term stability of leakage current and blocking voltage

### Applications

- Motor control
- Power converter
- AC power controller
- Light and temperature control
- SCR for inrush current limiting in power supplies or AC drive

### Advantages

- Space and weight savings
- Simple mounting

| Symbol | Conditions | | Characteristic Values | | |
|---|---|---|---|---|---|
| $I_R$, $I_D$ | $T_{VJ} = T_{VJM}$; $V_R = V_{RRM}$; $V_D = V_{DRM}$ | | ≤ | 2 | mA |
| $V_T$ | $I_T$ = 45 A; $T_{VJ}$ = 25°C | | ≤ | 1.5 | V |
| $V_{T0}$ | For power-loss calculations only ($T_{VJ}$ = 125°C) | | | 0.82 | V |
| $r_T$ | | | | 16.5 | mΩ |
| $V_{GT}$ | $V_D$ = 6 V; | $T_{VJ}$ = 25°C | ≤ | 1.0 | V |
| | | $T_{VJ}$ = -40°C | ≤ | 1.2 | V |
| $I_{GT}$ | $V_D$ = 6 V; | $T_{VJ}$ = 25°C | ≤ | 65 | mA |
| | | $T_{VJ}$ = -40°C | ≤ | 80 | mA |
| $V_{GD}$ | $T_{VJ} = T_{VJM}$; $V_D = {}^2/_3\ V_{DRM}$ | | ≤ | 0.2 | V |
| $I_{GD}$ | | | ≤ | 5 | mA |
| $I_L$ | $T_{VJ}$ = 25°C; $t_P$ = 10 µs; $I_G$ = 0.2; $di_G/dt$ = 0.2 A/µs | | ≤ | 150 | mA |
| $I_H$ | $T_{VJ}$ = 25°C; $V_D$ = 6 V; $R_{GK}$ = ∞ | | ≤ | 50 | mA |
| $t_{gd}$ | $T_{VJ}$ = 25°C; $V_D$ = ½ $V_{DRM}$; $I_G$ = 0.2 A; $di_G/dt$ = 0.2 A/µs | | ≤ | 2 | µs |
| $R_{thJC}$ | DC current | | | 1.2 | K/W |
| $R_{thCK}$ | DC current | | typical | 0.6 | K/W |
| a | Max. acceleration, 50 Hz | | | 50 | $m/s^2$ |

See CS 30..io1 data sheet for electrical characteristic curves.

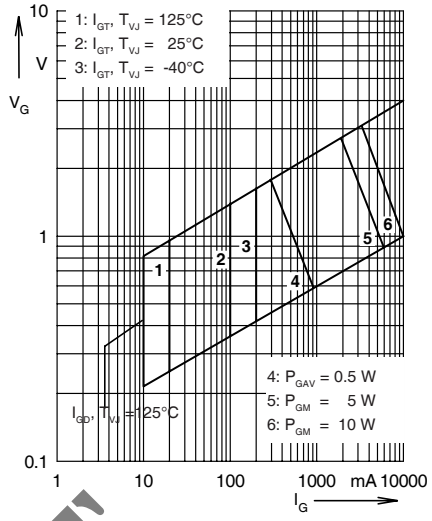



Fig. 1 Gate trigger range

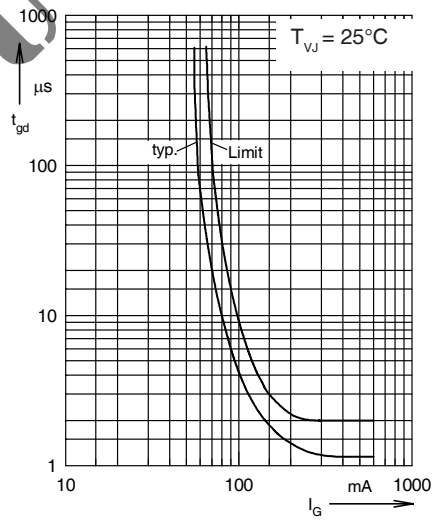
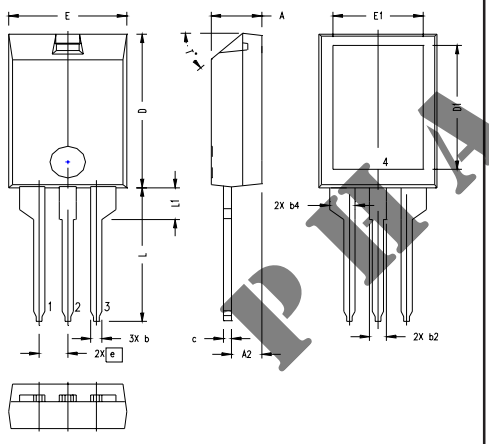



Fig. 2 Gate controlled delay time $t_{gd}$

**ISOPLUS220 Outline**




| SYM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .157 | .197 | 4.00 | 5.00 |
| A2 | .098 | .118 | 2.50 | 3.00 |
| b | .035 | .051 | 0.90 | 1.30 |
| b2 | .049 | .065 | 1.25 | 1.65 |
| b4 | .093 | .100 | 2.35 | 2.55 |
| c | .028 | .039 | 0.70 | 1.00 |
| D | .591 | .630 | 15.00 | 16.00 |
| D1 | .472 | .512 | 12.00 | 13.00 |
| E | .394 | .433 | 10.00 | 11.00 |
| E1 | .295 | .335 | 7.50 | 8.50 |
| e | .100 BASIC | | 2.55 BASIC | |
| L | .512 | .571 | 13.00 | 14.50 |
| L1 | .118 | .138 | 3.00 | 3.50 |
| T° | | | 42.5° | 47.5° |

NOTE:
1. Bottom heatsink (Pin 4) is electrically isolated from Pin 1, 2, or 3.
2. This drawing will meet dimensional requirement of JEDEC SS Product Outline TO-273 except D and D1 dimension.

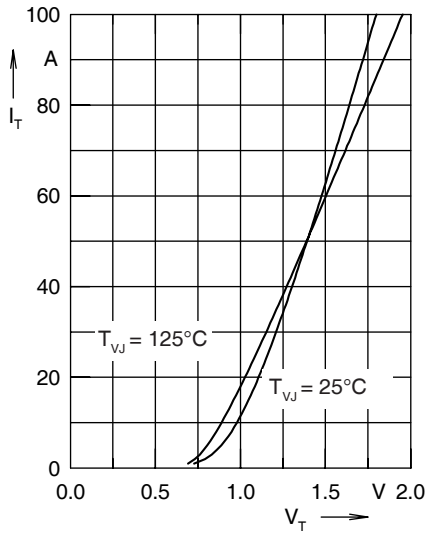



Fig. 3 Forward characteristics

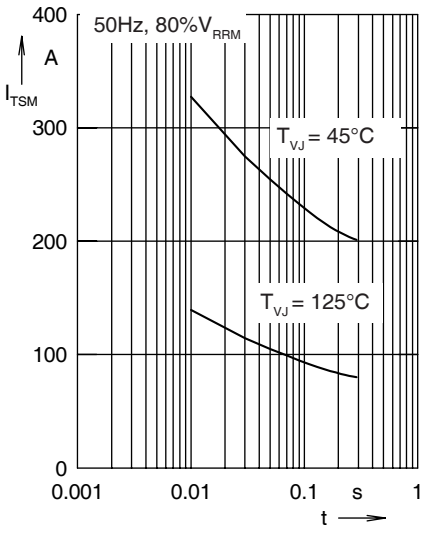



Fig. 4 Surge overload current
$I_{TSM}$: crest value, t: duration

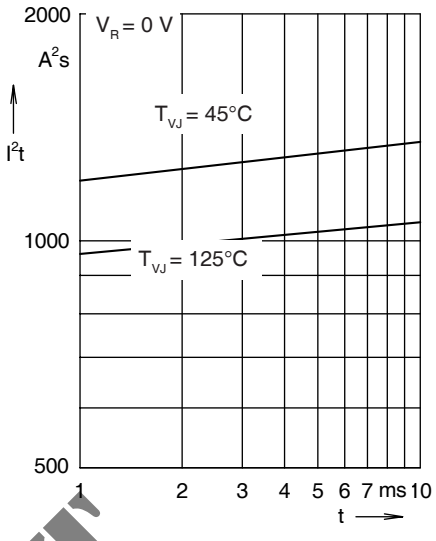



Fig. 5 $I^2t$ versus time (1-10 ms)

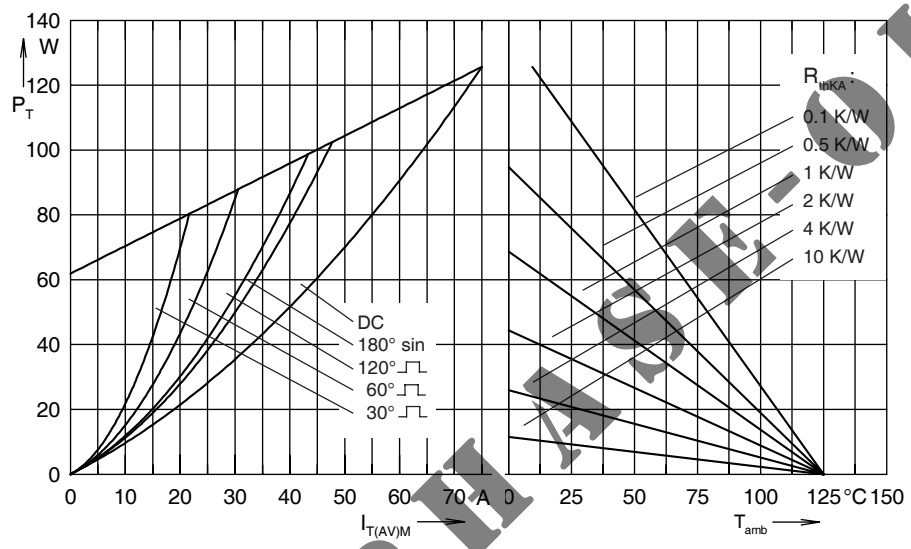



Fig. 6 Power dissipation versus forward current and ambient temperature