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CS3004

Precision Low-voltage Amplifier

Features

- Low Offset:
  - 10 µV Max.
- Low Drift:
  - 0.05 µV/°C Max.
- Low Noise:
  - 17 nV/√Hz
- Open-loop Voltage Gain:
  - 150 dB Typ.
- Rail-to-Rail Inputs
- Rail-to-Rail Output Swing
  - to within 10 mV of supply voltage
- 2.1 mA Supply Current
- Slew rate:
  - 0.25 V/µs

Applications

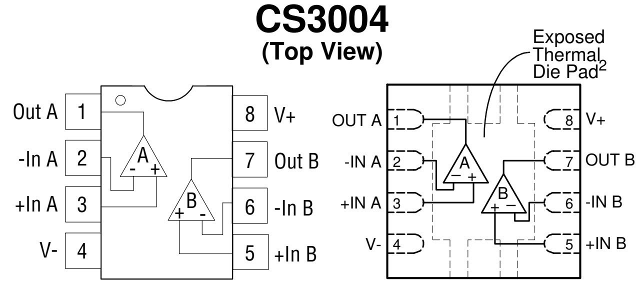
- Thermocouple/Thermopile Amplifiers
- Load Cell and Bridge Transducer Amplifiers
- Precision Instrumentation
- Battery-powered Systems

Description

The CS3004 dual amplifier is designed for precision amplification of low-level signals. These amplifiers achieve excellent offset stability, high open loop gain, and low noise. The devices also exhibit excellent CMRR and PSRR. The common mode input range includes the supply rails. The amplifiers operate with any supply voltage from 2.7 V to 5 V (±1.35 V to ±2.50 V).

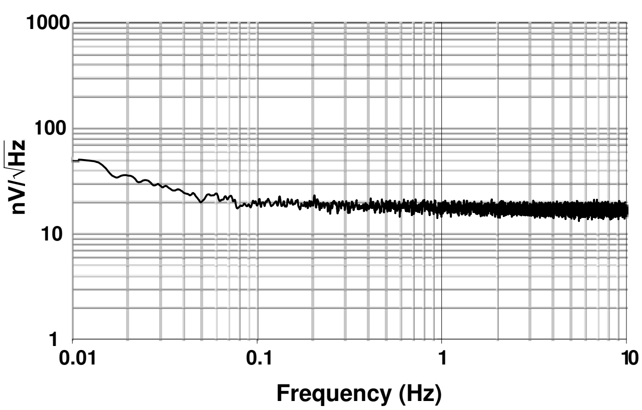
Pin Configurations

CS3004
(Top View)

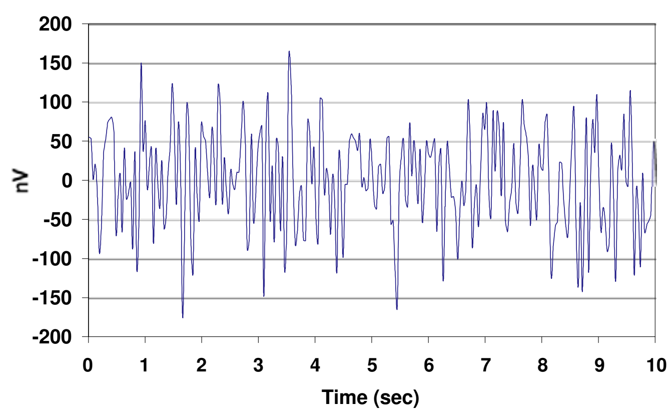


8-Lead SOIC **QFN-8**

1. Must not be connected.
2. Connect thermal die pad to V-.



Noise vs. Frequency (Measured)



0.01 Hz to 10 Hz Noise Performance

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Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **http://www.cirrus.com**

1. CHARACTERISTICS AND SPECIFICATIONS

1.1 5 V Electrical Characteristics

V+ = +5 V, ±5%; V- = 0V; VCM = 2.5 V; Unless otherwise noted, T_A = 25º C (See Note 1).

Parameter			Min	Typ	Max	Unit
Input Offset Voltage	(Note 2)	•	-	±2	±10	µV
Average Input Offset Drift	(Note 2)	•	-	±0.01	±0.05	µV/ºC
Input Bias Current		 •	- -	±170 -	±250 ±1.5	pA nA
Input Offset Current		 •	- -	±340 -	±500 ±3.0	pA nA
Input Noise Voltage Density	R_S = 100 Ω, f_0 = 1 Hz R_S = 100 Ω, f_0 = 1 kHz		- -	17 17	- -	nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$
Input Noise Voltage	0.1 to 10 Hz		-	350	-	nV_{p-p}
Input Noise Current Density	f_0 = 1 Hz		-	100	-	fA/$\sqrt{Hz}$
Input Noise Current	0.1 to 10 Hz		-	1.9		pA_{p-p}
Input Voltage Range	(Note 2)	•	V-	-	V+	V
Common Mode Rejection Ratio (dc)		•	110	120	-	dB
Power Supply Rejection Ratio		•	110	130	-	dB
Large Signal Voltage Gain	(Note 3) R_L = 2 kΩ to V+/2	 •	- 120	150 150	- -	dB dB
Output Voltage Swing	R_L = 2 kΩ to V+/2 (Note 4) R_L = 100 kΩ to V+/2	•	(V+ – 100) (V+ – 10)	- -	(V- + 100) (V- + 10)	mV mV
Slew Rate	R_L = 2 k, 100 pF			0.25	-	V/µs
Overload Recovery Time			-	25	-	µs
Supply Current		•	-	2.0	2.5	mA
Oscillator Frequency			-	150	-	kHz
Input Capacitance	Differential Common Mode		- -	1.5 10	- -	pF pF

Notes: 1. Symbol "•" denotes specification applies over -40 to +125 °C.

2. This parameter is guaranteed by design and/or laboratory characterization.

3. Guaranteed within the output limits of (V+ – 0.2 V) to (V- + 0.2 V).

4. Specifies the worst case drive voltage relative to the supply rail under stated load conditions.

1.2 3 V Electrical Characteristics

V+ = +3 V, ±10%; V- = 0V; VCM = 1.5 V; Unless otherwise noted, T_A = 25º C (See Note 5).

Parameter			Min	Typ	Max	Unit
Input Offset Voltage	(Note 6)	•	-	±2	±10	µV
Average Input Offset Drift	(Note 6)	•	-	±0.01	±0.05	µV/ºC
Input Bias Current		 •	- -	±110 -	±150 ±1.0	pA nA
Input Offset Current		 •	- -	±220 -	±300 ±2.0	pA nA
Input Noise Voltage Density	R_S = 100 Ω, f_0 = 1 Hz R_S = 100 Ω, f_0 = 1 kHz		- -	17 17	- -	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
Input Noise Voltage	0.1 to 10 Hz		-	350	-	nV_{p-p}
Input Noise Current Density	f_0 = 1 Hz		-	100	-	$fA/\sqrt{Hz}$
Input Noise Current	0.1 to 10 Hz		-	1.9		pA_{p-p}
Input Voltage Range	(Note 6)	•	V-	-	V+	V
Common Mode Rejection Ratio (dc)		•	110	120	-	dB
Power Supply Rejection Ratio		•	110	130	-	dB
Large Signal Voltage Gain	 (Note 7) R_L = 2 kΩ to V+/2	 •	- 120	160 150	- -	dB dB
Output Voltage Swing	R_L = 2 kΩ to V+/2 (Note 8) R_L = 100 kΩ to V+/2	•	(V+ – 100) (V+ – 10)	- -	(V- + 100) (V- + 10)	mV mV
Slew Rate	R_L = 2 k, 100 pF			0.25	-	V/µs
Overload Recovery Time			-	25	-	µs
Supply Current		•	-	2.0	2.5	mA
Oscillator Frequency			-	150	-	kHz
Input Capacitance	Differential Common Mode		- -	1.5 10	- -	pF pF

Notes:
5. Symbol "•" denotes specification applies over -40 to +125 ° C.
6. This parameter is guaranteed by design and/or laboratory characterization.
7. Guaranteed within the output limits of (V+ – 0.2 V) to (V- + 0.2 V).
8. Specifies the worst case drive voltage relative to the supply rail under stated load conditions.

1.3 Absolute Maximum Ratings

Parameter		Min	Typ	Max	Unit
Supply Voltage	[(V+) – (V-)]	2.7	-	5.5	V
Input Voltage		(V-) – 0.3	-	(V+) + 0.3	V
Storage Temperature Range		-65	-	+150	ºC

2. TYPICAL PERFORMANCE PLOTS

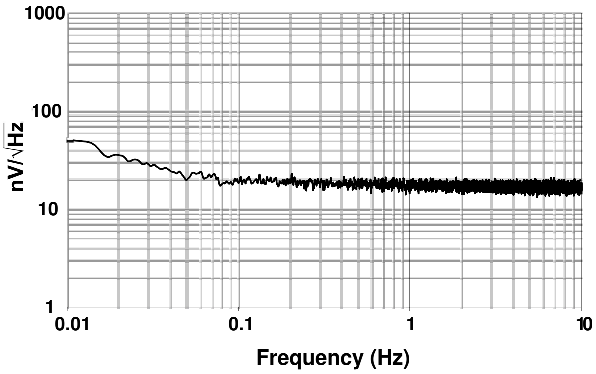


Figure 1. Noise vs Frequency (Measured)

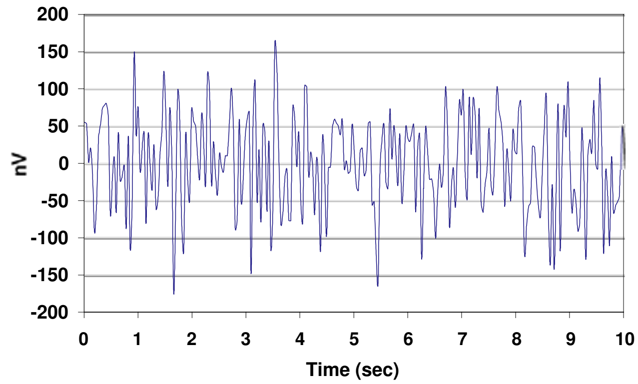


Figure 2. 0.01 Hz to 10 Hz Noise

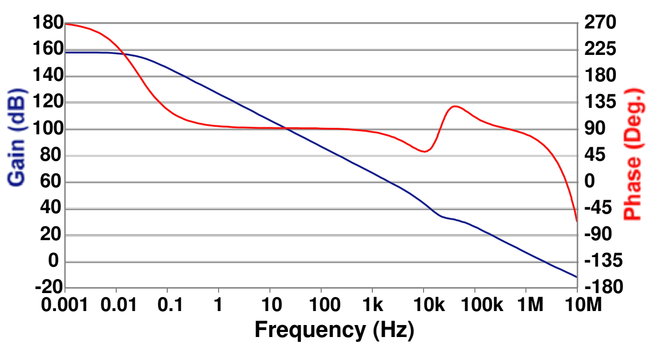


Figure 3. Gain & Phase vs. Frequency (2.7 V)

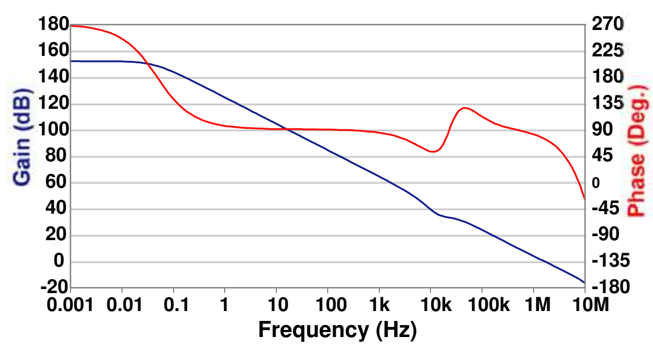


Figure 4. Gain & Phase vs. Frequency (5 V)

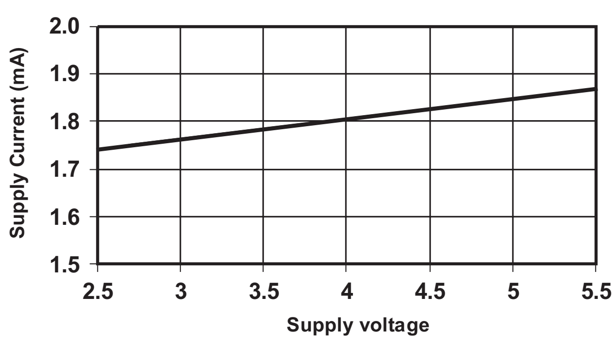


Figure 5. Supply Current vs. Supply Voltage

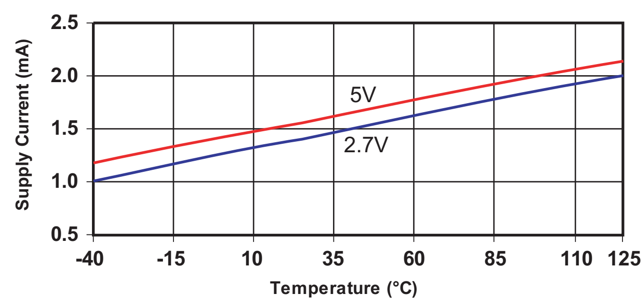


Figure 6. Supply Current vs. Temperature

Typical Performance Plots (Cont.)

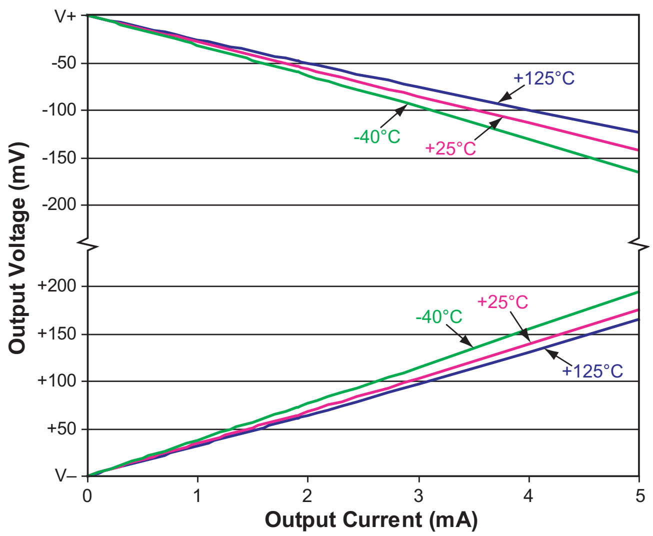


Figure 7. Voltage Swing vs. Output Current (2.7 V)

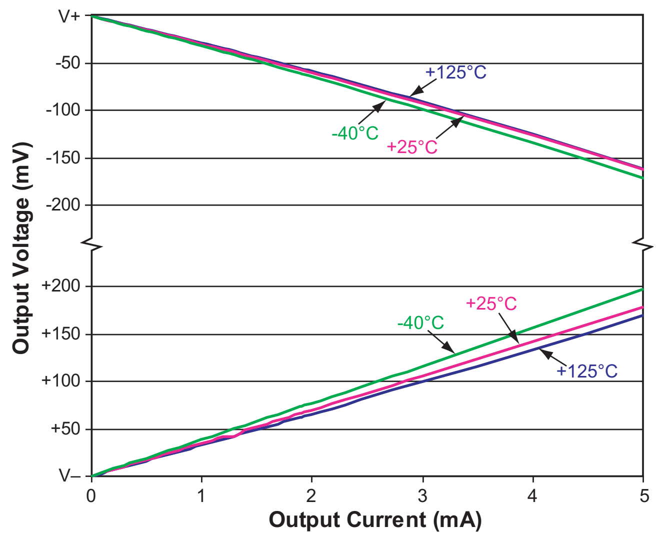
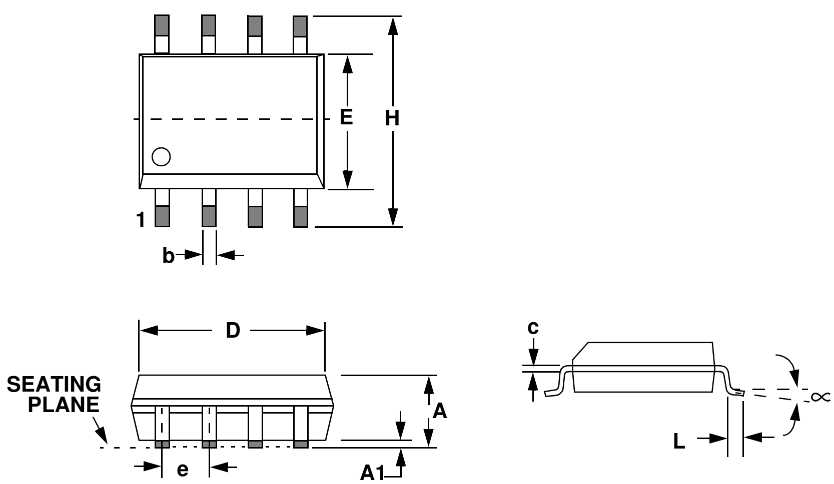


Figure 8. Voltage Swing vs. Output Current (5 V)

3. PACKAGE DRAWINGS

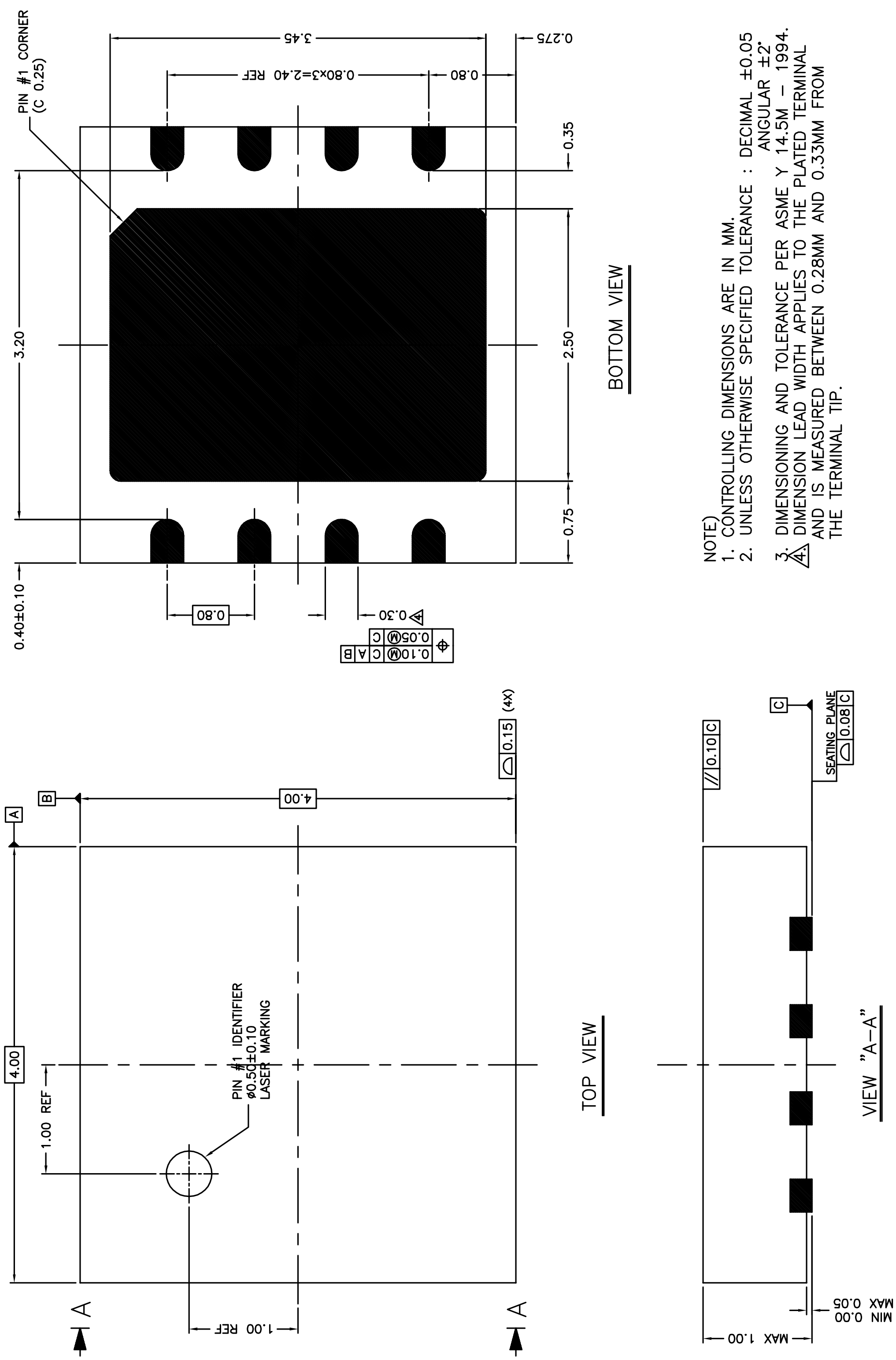
8L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

JEDEC # : MS-012

8L QFN (4 mm X 4 mm) PACKAGE DRAWING



4. ORDERING INFORMATION

Part #	Temperature Range	Package Description
CS3004-FS	-40 °C to +125 °C	8-lead SOIC
CS3004-FSZ	-40 °C to +125 °C	8-lead SOIC, Lead Free
CS3004-FNZ*	-40 °C to +125 °C	8-lead QFN, Lead Free

* Connect thermal die pad to V-.

5. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

<table>
<tr><th>Model Number</th><th>Peak Reflow Temp</th><th>MSL Rating*</th><th>Max Floor Life</th></tr>
<tr><td>CS3004-FS</td><td>240 °C</td><td rowspan="3">2</td><td rowspan="3">365 Days</td></tr>
<tr><td>CS3004-FSZ</td><td rowspan="2">260 °C</td></tr>
<tr><td>CS3004-FNZ</td></tr>
</table>

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

6. REVISION HISTORY

Revision	Date	Changes
PP4	FEB 2007	First public release.
F1	AUG 2007	Updated to “Final” per QPL process.