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CS3318

8-Channel Analog Volume Control

Features

- Complete Analog Volume Control
  - 8 Independently Controllable Channels
  - 3 Configurable Master Volume and Muting Controls
- Wide Adjustable Volume Range
  - -96 dB to +22 dB in ¼ dB Steps
- Low Distortion & Noise
  - -112 dB THD+N
  - 127 dB Dynamic Range
- Noise-Free Level Transitions
  - Zero-Crossing Detection with Programmable Time-Out
- Low Channel-to-Channel Crosstalk
  - 120 dB Inter-Channel Isolation
- Comprehensive Serial Control Port
  - Supports I²C® and SPI™ Communication
  - Independent Control of up to 128 Devices on a Shared 2-Wire I²C or 3-Wire SPI Control Bus
  - Supports Individual and Grouped Control of all CS3318 Devices on the I²C or SPI Control Bus
- Flexible Power Supply Voltages
  - ±8 V to ±9 V Analog Supply
  - +3.3 V Digital Supply

Description

The CS3318 is an 8-channel digitally controlled analog volume control designed specifically for high-end audio systems. It features a comprehensive I²C/SPI serial control port for easy device and volume configuration.

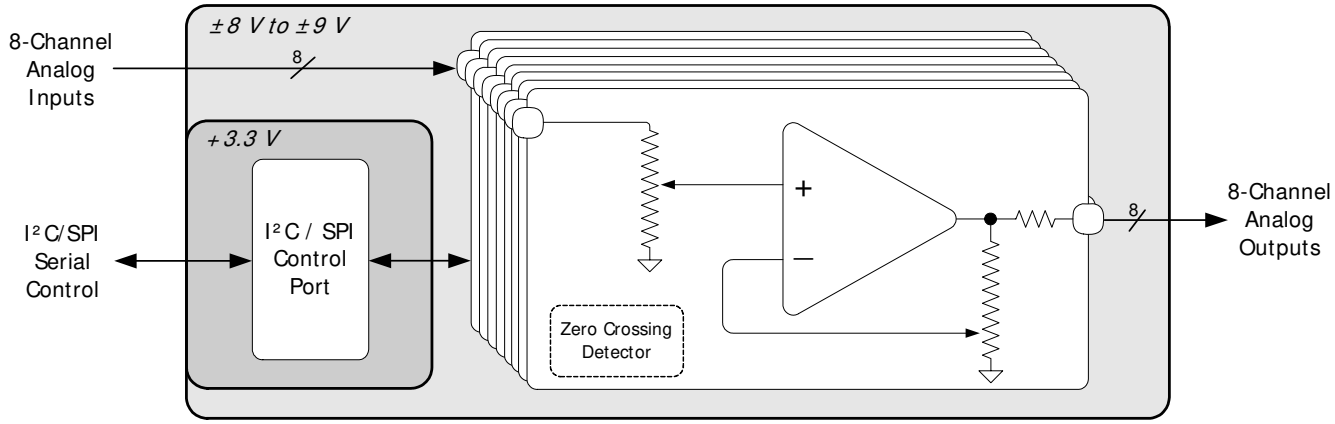
The CS3318 includes arrays of well-matched resistors and complementary low-noise active output stages. A total adjustable range of 118 dB, in ¼ dB steps, is spread evenly over 96 dB of attenuation and 22 dB of gain.

The CS3318 implements configurable zero-crossing detection to provide glitch-free volume-level changes.

The I²C/SPI control interface provides for easy system integration of up to 128 CS3318 devices over a single 2-wire I²C or 3-wire SPI bus, allowing many channels of volume control with minimal system controller I/O requirements. Devices may be controlled on an individual and grouped basis, simplifying simultaneous configuration of a group of channels across multiple devices, while allowing discrete control over all channels on an individual basis.

The device operates from ±8 V to ±9 V analog supplies and has an input/output voltage range of ±6.65 V to ±7.65 V. The digital control interface operates at +3.3 V.

The CS3318 is available in a 48-pin LQFP package in Commercial grade (-10° to 70° C). The CS3318 Customer Demonstration board is also available for device evaluation. Refer to "Ordering Information" on page 44 for complete details.



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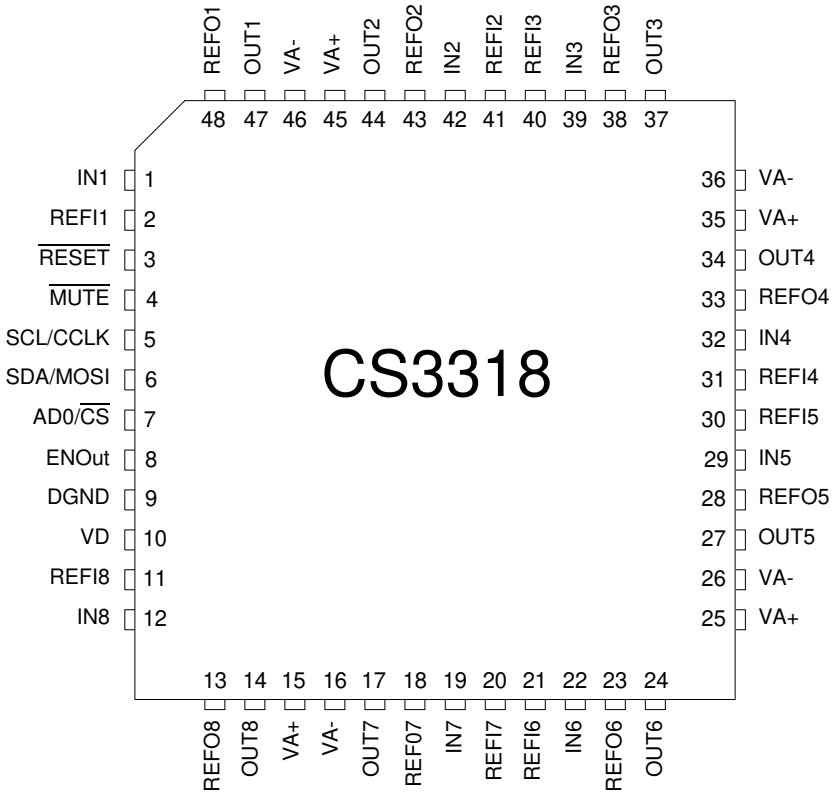


Pin Name	#	Pin Description
IN1	1	
IN2	42	
IN3	39	
IN4	32	**Analog Inputs** (*Input*) **-** The full-scale level is specified in the Analog Characteristics specification table.
IN5	29	
IN6	22	
IN7	19	
IN8	12	

Pin Name	#	Pin Description
OUT1	47	**Analog Outputs** (*Output*) - The full-scale output level is specified in the Analog Characteristics specification table.
OUT2	44	
OUT3	37	
OUT4	34	
OUT5	27	
OUT6	24	
OUT7	17	
OUT8	14	
REFI1	2	**Reference In** (*Input*) - Analog reference pin.
REFI2	41	
REFI3	40	
REFI4	31	
REFI5	30	
REFI6	21	
REFI7	20	
REFI8	11	
REFO1	48	**Reference Out** (*Output*) - Analog reference pin.
REFO2	43	
REFO3	38	
REFO4	33	
REFO5	28	
REFO6	23	
REFO7	18	
REFO8	13	
VA+	15, 25, 35, 45	**Positive Analog Power** *(Input)* **-** Positive power for the internal analog section.
VA-	16, 26, 36, 46	**Negative Analog Power** *(Input)* **-** Negative power for the internal analog section.
$\overline{\text{RESET}}$	3	**Reset** (*Input*) - The device enters a low-power mode when this pin is driven low.
$\overline{\text{MUTE}}$	4	**Mute** (*Input*) - This pin defaults to an active low mute input, and may be configured as an active high mute input.
SCL/CCLK	5	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
SDA/MOSI	6	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O line for the control port interface in I²C Mode. MOSI is the input data line for the control port interface in SPI Mode.
AD0/$\overline{\text{CS}}$	7	**Default Address Bit 0 (I²C) / Control Port Chip Select (SPI)** *(Input)* - AD0 sets the LSB of the default chip address in I²C Mode. $\overline{\text{CS}}$ is the chip-select signal for SPI format.
ENOut	8	**Enable Output** (*Output*) **-** Enable output signal for multi-device serial control chain configuration.
DGND	9	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VD	10	**Digital Power** (*Input*) **-** Positive power for the internal digital section.

2. CHARACTERISTICS AND SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.

SPECIFIED OPERATING CONDITIONS

(DGND = 0 V; All voltages with respect to ground.)

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Positive Analog	VA+	7.6	9.0	9.45	V
	Negative Analog	VA-	-9.45	-9.0	-7.6	V
	Digital	VD	3.1	3.3	3.5	V
Ambient Operating Temperature (Power Applied)		T_A	-10	-	+70	°C

ABSOLUTE MAXIMUM RATINGS

(DGND = 0 V; All voltages with respect to ground. (Note 1)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	10.5	V
	Negative Analog	VA-	-10.5	0.3	V
	Digital	VD	-0.3	3.63	V
Input Current	(Note 2)	I_{in}	-	±10	mA
Analog Input Voltage		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	VD - 0.3	VD + 0.3	V
Ambient Operating Temperature (Power Applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes:

1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

ANALOG CHARACTERISTICS

(Test conditions (unless otherwise specified): R_S = 0; R_L = 20 kΩ; C_L = 20 pF; 10 Hz to 20 kHz Measurement Bandwidth)

Parameter		Symbol	Min	Typ	Max	Unit
DC Characteristics						
Step Size			-	0.25	-	dB
Gain Error	(Vol = +22 dB)		-	±0.5	-	dB
Gain Matching Between Channels	(Vol = +22 dB)		-	±0.1	-	dB
Input Resistance		R_{IN}	8	10	-	kΩ
Input Capacitance		C_{IN}	-	10	-	pF
AC Characteristics						
Total Harmonic Distortion + Noise	(Note 3)	THD+N	-	0.00025	0.00063	%
Dynamic Range			121	127	-	dB
Input/Output Voltage Range	(THD+N < 1 %)	V_{FS}	(VA-) + 1.35	-	(VA+) - 1.35	V
Output Noise	(Note 4)		-	1.8	3.6	µVrms
Interchannel Isolation	(1 kHz)		-	-120	-	dB
Output Buffer						
Offset Voltage	(Note 4)	V_{OS}	-	0.75	5	mV
Output Resistance		R_{OUT}	-	100	-	Ω
AC Load Resistance		R_{LOAD}	2	-	-	kΩ
Load Capacitance			-	-	100	pF
Short Circuit Current			-	20	-	mA
Unity Gain Bandwidth, Small Signal			-	5	-	MHz
Power Supplies						
Supply Current (No Load, V_{in} = 0 V)	Normal Operation	I_{VA+}	-	36	50	mA
		I_{VA-}	-	36	50	mA
		I_{VD}	-	0.6	1.07	mA
	Power-Down, All Supplies (Note 5)	I_{PD}	-	60	-	µA
Power Consumption	Normal Operation		-	650	904	mW
	Power Down (Note 5)		-	540	-	µW
Power Supply Rejection Ratio (250 Hz)		PSRR	-	80	-	dB

3. V_{in} = [($V_{FS\ Max}$ - $V_{FS\ Min}$) - 1.6 V] V_{p-p}, 1 kHz, Volume = 0 dB.
   Note that for (VA+) = -(VA-) = 9 V, V_{in} = 13.7 V_{p-p} = 4.8 V_{RMS}.
4. Measured with input grounded and volume = 0 dB. Will increase as a function of volume settings >0 dB.
5. Power-down is defined as $\overline{\text{RESET}}$ = low, all clock and data lines held static, and no analog input signals applied.

DIGITAL INTERFACE CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	0.7 x VD	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.2 x VD	V
High-Level Output Voltage at I_o=2 mA	V_{OH}	VD - 1.0	-	-	V
Low-Level Output Voltage at I_o=2 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

$\overline{\text{MUTE}}$ SWITCHING CHARACTERISTICS

(Inputs: Logic 0 = DGND, Logic 1 = VD)

Parameters		Symbol	Min	Typ	Max	Units
$\overline{\text{MUTE}}$ Active Pulse Width	(Note 6)	-	2	-	-	ms

6. The $\overline{\text{MUTE}}$ active state (low/high) is set by the MutePolarity bit in the Device Configuration 1 register (see page 33).

CONTROL PORT SWITCHING CHARACTERISTICS - I²C FORMAT

(Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	100	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 7)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rd}	-	1	µs
Fall Time SCL and SDA	t_{fc}, t_{fd}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

7. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

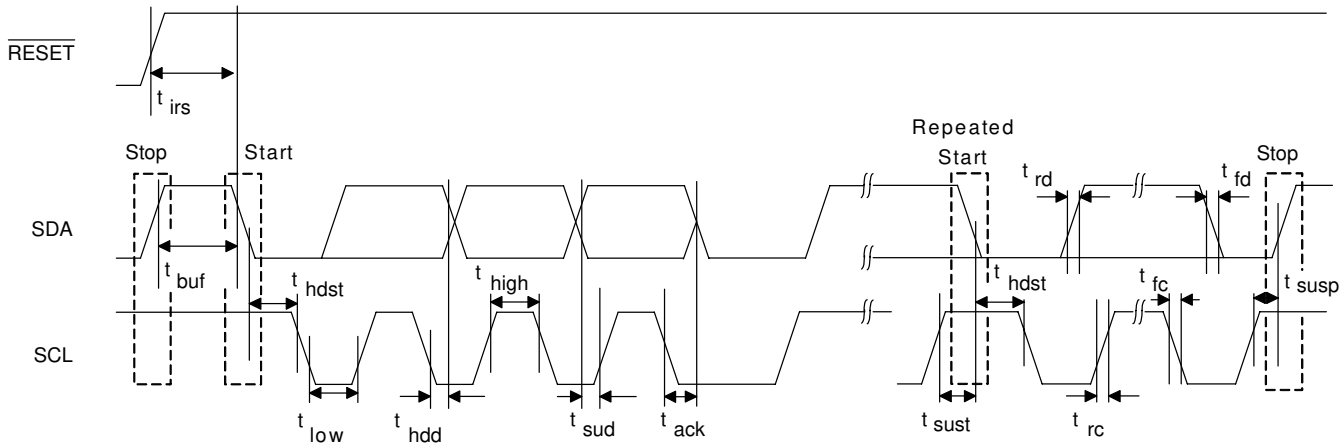


Figure 1. Control Port Timing - I²C Format

CONTROL PORT SWITCHING CHARACTERISTICS - SPI™ FORMAT

(Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{\text{RESET}}$ Rising Edge to $\overline{\text{CS}}$ Falling		t_{srs}	100	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{\text{CS}}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 8)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 9)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 9)	t_{f2}	-	100	ns

8. Data must be held for sufficient time to bridge the transition time of CCLK.
9. For f_{sck} <1 MHz.

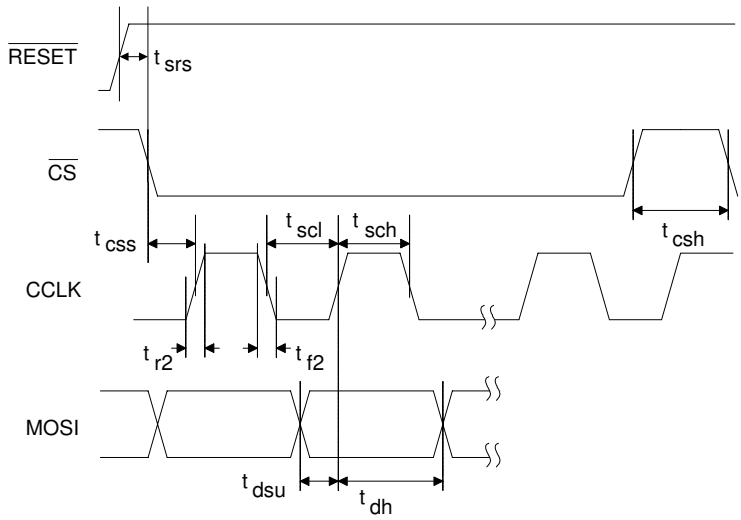


Figure 2. Control Port Timing - SPI Format

3. TYPICAL CONNECTION DIAGRAM

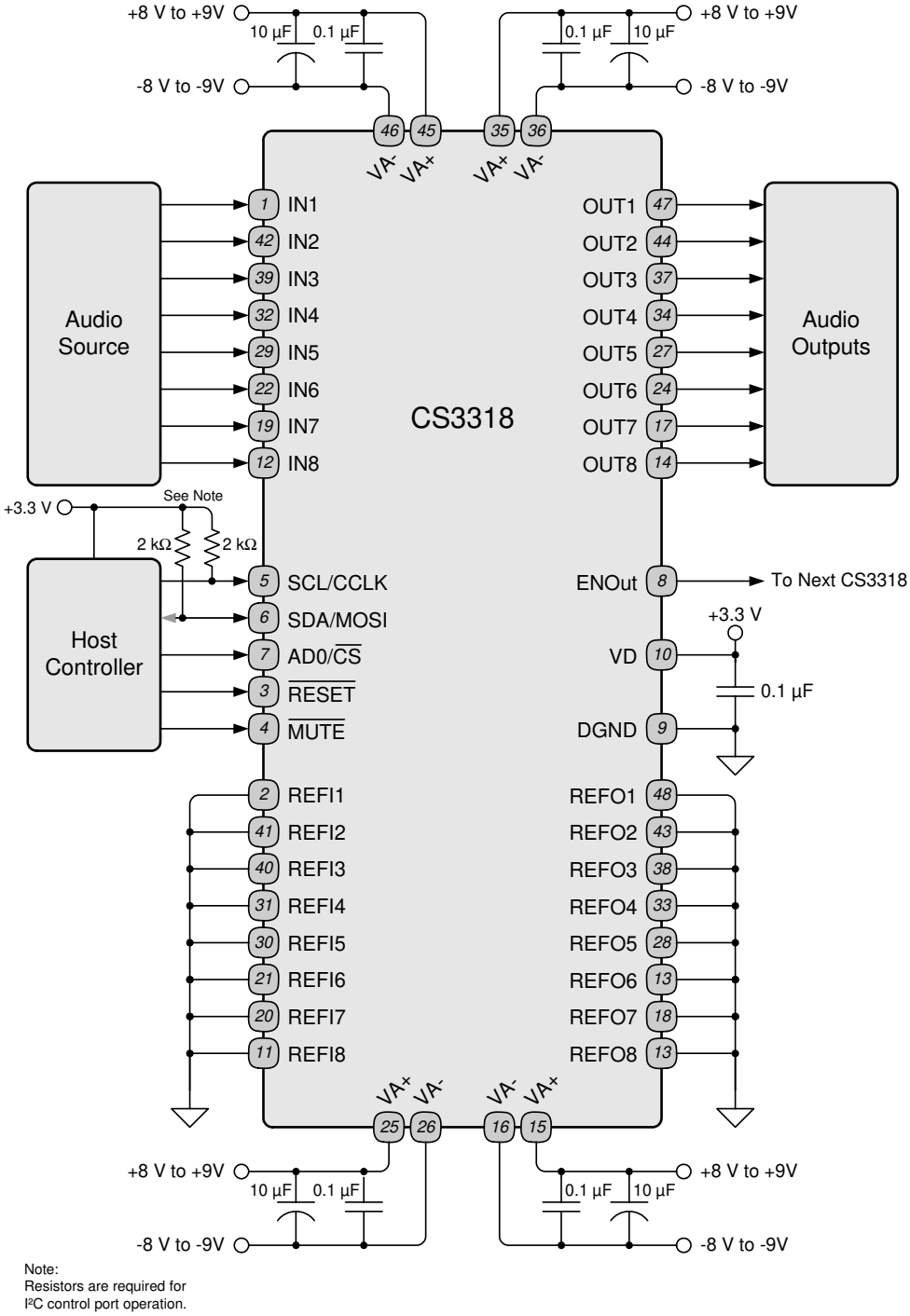
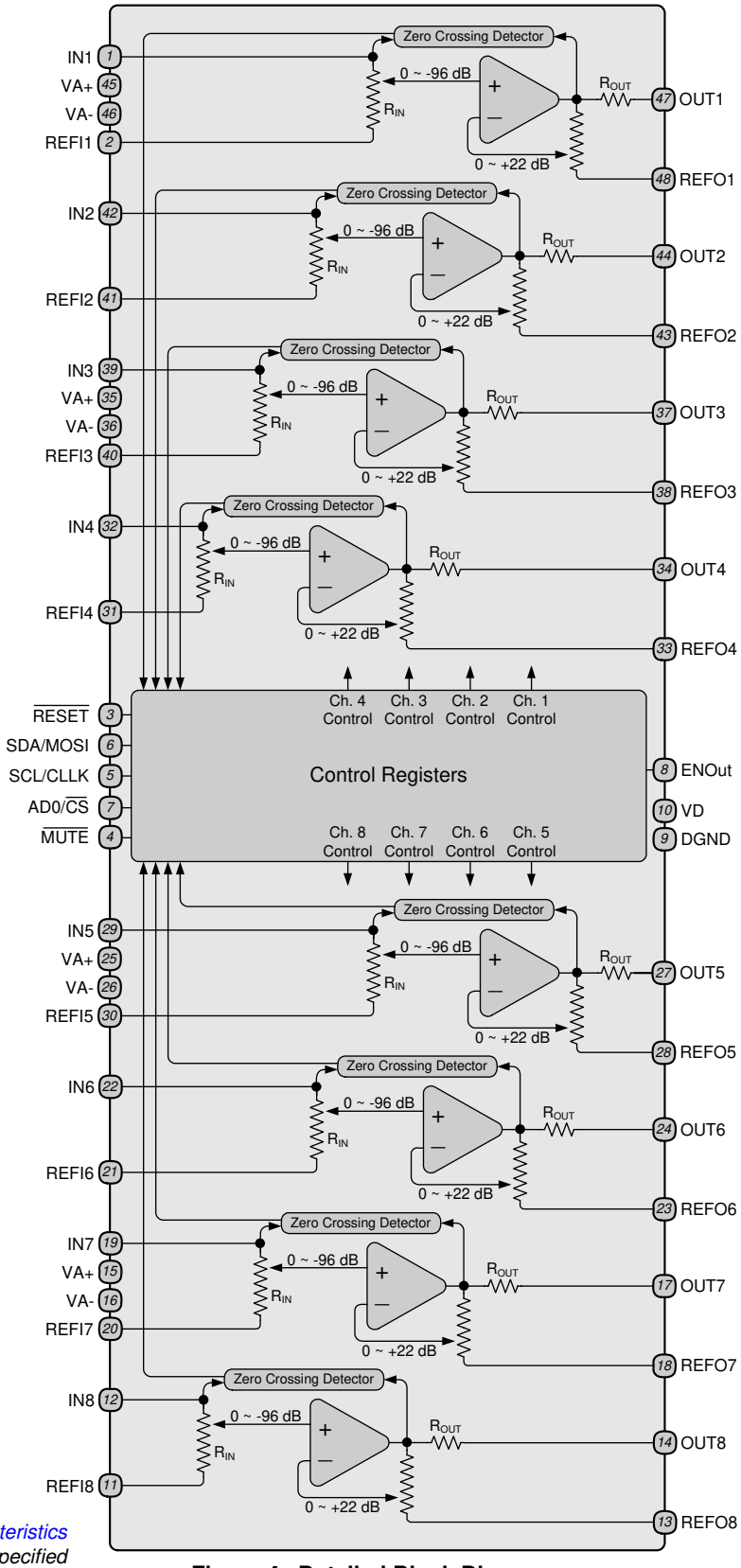


Figure 3. Typical Connection Diagram

4. DETAILED BLOCK DIAGRAM



Refer to the Analog Characteristics table on page 8 for the specified values of R_{IN} and R_{OUT}.

Figure 4. Detailed Block Diagram

5. APPLICATIONS

5.1 General Description

The CS3318 is an 8-channel digitally controlled analog volume control designed for audio systems. It incorporates a total adjustable range of 118 dB in ¼ dB steps, spread evenly over 96 dB of attenuation and 22 dB of gain.

The internal analog architecture includes one op-amp per channel, each with an input resistor network for attenuation and a feedback resistor network for gain. Analog switch arrays are used to select taps in the input and feedback resistor networks, thereby setting the gain or attenuation of each channel. These switch arrays are controlled via the digital control port, bridging the gap between the analog and digital domains. Figure 4 on page 13 provides a detailed diagram of the CS3318's internal architecture.

The CS3318 incorporates highly configurable zero-crossing detection for glitch-free volume level changes. Volume changes may be configured to occur immediately or on a signal zero-crossing. In the event that the signal does not cross zero, the CS3318 provides 8 selectable time-out periods in the range of 5 ms to 50 ms after which the volume level will be changed immediately. When the CS3318 receives more than one volume change command before a zero-crossing or a time-out, the CS3318 is able to implement the previous volume change command immediately or discard it and act only on the most recent command. The "Zero-Crossing Detection" section on page 22 provides a detailed description of the CS3318's zero-crossing detection functionality and controls.

The CS3318 includes a comprehensive I²C/SPI serial control port interface for volume changes and device configuration. This interface provides for easy system integration of up to 128 CS3318 devices over a single 2-wire I²C or 3-wire SPI bus, allowing many channels of volume control with minimal system controller I/O requirements. Devices may be addressed on an individual and grouped basis, simplifying simultaneous configuration of a group of channels across multiple devices, while allowing discrete control over all channels on an individual basis. The "System Serial Control Configuration" section on page 23 provides a detailed description of the serial control port features and functionality.

5.2 System Design

Very few external components are required to support the CS3318. Typical power supply decoupling components are the only external requirements, as shown in Figure 3 on page 12.

5.2.1 Analog Inputs

No external circuitry is required to interface between the audio source and the CS3318's inputs. However, as with any adjustable gain stage, the affects of a DC offset at the input must be considered. Capacitively coupling the analog inputs may be required to prevent "clicks and pops" which occur with gain changes if an appreciable offset is present.

The addition of an input coupling capacitor will form a high-pass filter with the CS3318's input impedance. Given nominal values of input impedance and coupling capacitor, a 10 µF coupling capacitor will result in less than 0.03 dB of attenuation at 20 Hz. If additional low-frequency attenuation can be tolerated, a smaller coupling capacitor may be used.

The CS3318 requires a low source impedance to achieve maximum performance, and a source-impedance of 600 Ω or less is recommended.

The maximum input level is limited by the input signal swing capability of the internal op-amp. Signals approaching the analog supply voltages may be applied to the analog input pins if the internal attenuator limits the output signal to within 1.35 V of the analog supply rails.

5.2.2 Analog Outputs

The analog outputs are capable of driving 2 kΩ loads to within 1.35 V of the analog supply rails and are short-circuit protected to 20 mA.

The minimum output load resistance is 2 kΩ; a load smaller than 2 kΩ may cause increased distortion. As the load resistance decreases, the potential for increased internal heating and the possibility of damage to the device is introduced. Additionally, the load capacitance should be less than 100 pF. Increased load capacitance may cause increased distortion, and the potential for instability in the output amplifiers.

If a low-impedance or high-capacitance load must be driven, an external amplifier should be used to isolate the outputs of the CS3318.

5.2.3 Recommended Layout, Grounding, and Power Supply Decoupling

As with any high-performance device that contains both analog and digital circuitry, careful attention must be provided to power supply and grounding arrangements to optimize performance. Figure 3 on page 12 shows the recommended power arrangements, with VA+, VA-, and VD connected to clean supplies.

Power supply decoupling capacitors should be placed as near to the CS3318 as possible, with the low value ceramic capacitor being the nearest. Care should be taken to ensure that there is minimal resistance in the analog ground leads to the device to prevent any changes in the defined gain/attenuation settings. The use of a unified ground plane is recommended for optimal performance and minimal radiated noise. The CS3318 evaluation board demonstrates the optimum layout and power supply arrangements.

Should the printed circuit board have separate analog and digital regions with independent ground planes, the CS3318 should reside in the analog region of the board.

Extensive use of ground plane fill on the circuit board will yield large reductions in radiated noise effects.

5.3 Power-Up and Power-Down

The CS3318 will remain in a completely powered-down state with the control port inaccessible until the $\overline{\text{RESET}}$ pin is brought high. Once $\overline{\text{RESET}}$ is high, the control port will be accessible, but the internal amplifiers will remain powered-down until the PDN_ALL bit is cleared.

To bring a channel out of power-down, both the PDN_ALL and the channel's PDNx bit must be cleared. By default, all channels' PDNx bits are cleared, and the PDN_ALL bit is set. To minimize audible artifacts during power-up process, the CS3318 automatically holds each channel's volume at mute until its amplifier has completed its power-up sequence. Once the power-up process is complete, each channel's volume will automatically be set to the correct level according to the CS3318's control port settings.

To place a channel in power-down, either the channel's PDNx bit or the PDN_ALL bit must be set. To minimize audible artifacts during the power-down process, the CS3318 automatically places each channel in mute before the amplifier begins its power-down sequence.

The power-up and power-down muting/volume changes are implemented as dictated by the zero-crossing detection settings (see "Zero-Crossing Detection" on page 22). If an immediate power-up or power-down is required, the zero-crossing mode should be set to immediate before changing the power-down state of the device or channel.

Referenced Control	Register Location
PDN_ALL	"Power Down All (Bit 0)" on page 35
PDNx	"Channel Power - Address 0Dh" on page 35

5.3.1 Recommended Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supplies are stable. In this state, the control port is reset to its default settings.
2. Bring $\overline{\text{RESET}}$ high. The device will remain in a low power state with the PDN_ALL bit set by default. The control port will be accessible.
3. The desired register settings can be loaded while the PDN_ALL bit remains set.
4. Clear the PDN_ALL bit to initiate the power-up sequence.

5.3.2 Recommended Power-Down Sequence

1. Set the PDN_ALL bit to mute all channels and power-down all internal amplifiers.
2. If desired, hold $\overline{\text{RESET}}$ low to bring the CS3318's power consumption to an absolute minimum.

5.4 Volume & Muting Control Architecture

The CS3318's volume and muting control architecture provides the ability to control each channel on an individual and master basis.

Individual control allows the volume and mute state of a single channel to be changed independently from all other channels within the device. The CS3318 provides 8 individual volume and muting controls, each permanently assigned to one channel within the device.

Master control allows the volume and mute state of multiple channels to be changed simultaneously with a single register write. The CS3318 provides three master controls, and each may be configured to affect any group of channels within a device.

Refer to the "Volume Controls" section beginning on page 19 and the "Muting Controls" section beginning on page 21 for an in-depth description of the operation of the available controls.

5.4.1 Control Mapping Matrix

Figure 5 shows a conceptual drawing of the CS3318's internal control-to-channel mapping matrix. Notice that the individual channel controls are fixed to their respective channel, and the master controls may be configured to affect any or all channels within the device.

Each master control has a corresponding Master X Mask register which allows the user to select which channels are affected by the control. By default, each master control is configured to affect all channels within the device. Referring to Figure 5 below, each configurable connection shown may be made and broken by setting or clearing its corresponding bit in the control's Master X Mask register.

The contents of the Master X Mask registers determine which channels are affected by both a master control's volume and mute settings. Refer to the "Volume & Muting Control Implementation" section on page 18 for a complete diagram of the CS3318's volume and muting control architecture.

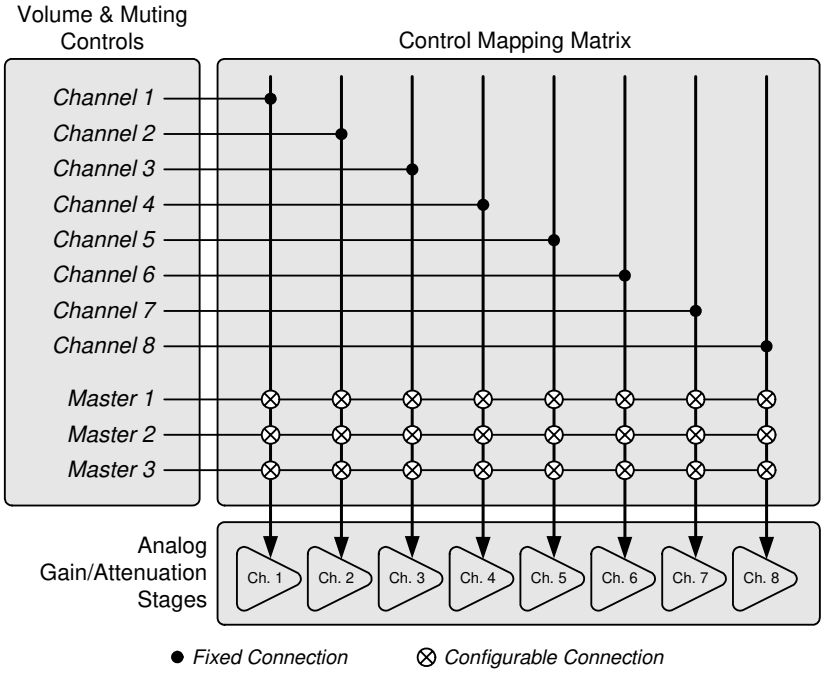


Figure 5. CS3318 Control Mapping Matrix

Combining the multiple group addressing capabilities of the CS3318 (as detailed in section 5.8.2 on page 24) with the internal master control mapping abilities described above allows the configuration and direct addressing of multiple logical groups of channels across multiple CS3318 devices within a system.

Referenced Control	Register Location
Master X Mask	"Master 1 Mask - Address 10h" on page 36 "Master 2 Mask - Address 13h" on page 37 "Master 3 Mask - Address 16h" on page 38

5.4.2 Volume & Muting Control Implementation

Figure 6 below diagrams in detail the volume and muting control architecture of the CS3318 for an arbitrary channel 'N'.

This diagram incorporates all volume and muting control concepts presented in sections 5.4 - 5.6; it is included as a reference and will serve to corroborate the information presented in these sections.

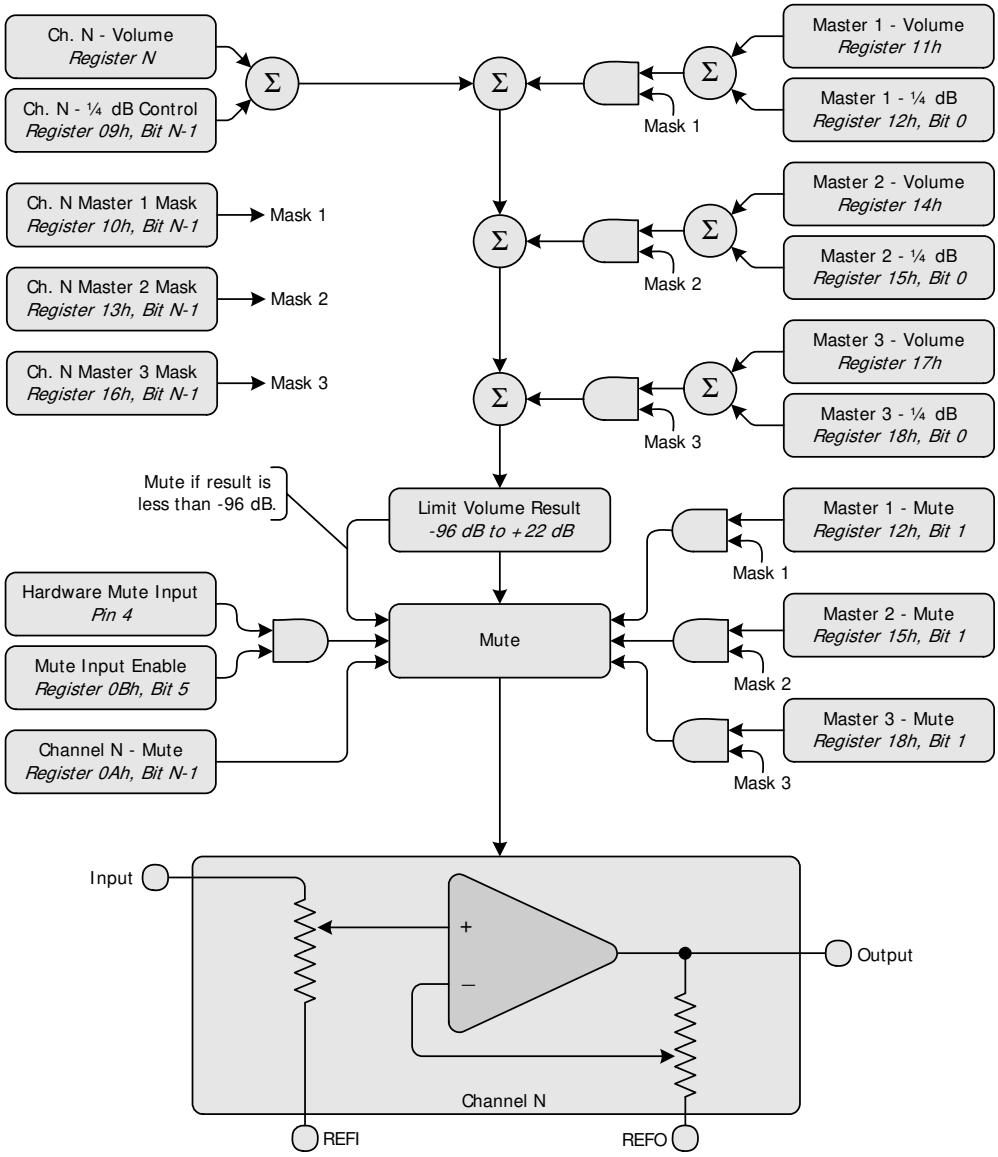


Figure 6. Volume & Muting Control Implementation

5.5 Volume Controls

The CS3318 provides comprehensive volume control functionality, allowing each channel's volume to be changed on an individual or master basis. Refer to the "Volume & Muting Control Architecture" section on page 17 for complete details about the configuration of the CS3318's individual and master controls.

The CS3318 incorporates zero-crossing detection capabilities, and all volume changes are implemented as dictated by the zero-crossing detection settings (see "Zero-Crossing Detection" on page 22).

5.5.1 Individual Channel Volume Controls

The CS3318 provides 8 individual channel volume controls. These controls can be used to independently gain and/or attenuate each of the input/output channels over a range of +22 dB to -96 dB in ¼ dB steps.

Each channel has a corresponding Ch. X Volume register used to gain or attenuate the channel from +22 dB to -96 dB in ½ dB steps. The ¼ dB Control register contains one bit per channel used to add an additional ¼ dB gain to the channel's volume as set by its Ch. X Volume register.

Referenced Control	Register Location
Ch. X Volume	"Ch 1-8 Volume - Addresses 01h - 08h" on page 31
¼ dB Control	"¼ dB Control - Address 09h" on page 32

5.5.2 Master Volume Controls

The CS3318 master volume controls allow the user to simultaneously gain or attenuate a user defined set of channels from +22 dB to -96 dB in ¼ dB increments. A total of 3 master volume controls, Master 1, Master 2, and Master 3, are provided for comprehensive and flexible control.

Each master volume control has a corresponding Master X Volume register which is used to gain or attenuate the control's respective unmasked channels from +22 dB to -96 dB in ½ dB steps. The LSB of the corresponding Master X Control register contains one bit used to add an additional ¼ dB gain to the master volume control's value as set by its Master X Volume register.

As discussed in the "Volume & Muting Control Architecture" section on page 17, each master volume control has a corresponding Master X Mask register which allows the user to select which channels are affected by the control. By default, each master control is configured to affect all channels within the device.

The *effective volume* setting of an individual channel is determined by the following equation:

$$EffVol_{ChN} = Individual_{ChN} + (Master\ 1\ \&\ Mask\ 1_{ChN}) + (Master\ 2\ \&\ Mask\ 2_{ChN}) + (Master\ 3\ \&\ Mask\ 3_{ChN})$$

Equation 1. Effective Volume Setting

In this equation, $EffVol_{ChN}$ represents the actual gain or attenuation level, in dB, of the individual channel "N" as determined by the its constituent volume settings within the CS3318. The effective volume is limited to the range of +22 dB to -96 dB; see "Volume Limits" on page 20.

$Individual_{ChN}$ is the individual channel volume setting in dB as set by the channel's individual volume control register and ¼ dB bit (see "Individual Channel Volume Controls" on page 19).

Master X is the Master X volume setting in dB as set by the master volume control registers and their respective ¼ dB bits.

$Mask\ X_{ChN}$ is the channel N mask bit associated with the Master X volume control setting.

This volume control architecture in combination with the multiple group addressing capabilities of the CS3318 (as detailed in section 5.8.2 on page 24) allows easy volume control of multiple channels across multiple devices in a system while eliminating the system controller overhead typically associated digitally driven analog volume control devices.

Table 1 shows example volume settings using individual and master volume controls.

	Individual$_{ChX}$	Master 1	Mask 1$_{ChX}$	Master 2	Mask 2$_{ChX}$	Master 3	Mask 3$_{ChX}$	Level$_{ChX}$
Channel 1	+3.75 dB	+1.0 dB	0	+5.25 dB	0	-8.5 dB	0	+3.75 dB
Channel 2	+2.5 dB		0		0		1	-6.0 dB
Channel 3	+1.25 dB		0		1		0	+6.5 dB
Channel 4	0 dB		0		1		1	-3.25 dB
Channel 5	-1.25 dB		1		0		0	-0.25 dB
Channel 6	-2.5 dB		1		0		1	-10.0 dB
Channel 7	-3.75 dB		1		1		0	+2.5 dB
Channel 8	-4.0 dB		1		1		1	-6.25 dB

Table 1. Example Volume Settings

Refer to Figure 6 on page 18 for a graphical representation of the volume controls' functionality.

Referenced Control	Register Location
Master X Volume	"Master 1 Volume - Address 11h" on page 36 "Master 2 Volume - Address 14h" on page 37 "Master 3 Volume - Address 17h" on page 38
Master X Control	"Master 1 Control - Address 12h" on page 37 "Master 2 Control - Address 15h" on page 38 "Master 3 Control - Address 18h" on page 39
Master X Mask	"Master 1 Mask - Address 10h" on page 36 "Master 2 Mask - Address 13h" on page 37 "Master 3 Mask - Address 16h" on page 38

5.5.3 Volume Limits

The analog section of the CS3318 is designed to accommodate gain and attenuation over the range of +22 dB to -96 dB. Values outside this range may, however, be written to the CS3318's internal registers. As shown in Figure 6 on page 18, the value of the Individual and Master volume control registers are summed before being limited to the range allowed by the CS3318's analog section. This architecture has the benefit of allowing both individual and master volume control input beyond the analog range of the CS3318.

If the effective volume (See Equation 1 on page 19) of an individual channel is greater than +22 dB, the channel's volume will be set to +22 dB.

If the effective volume of an individual channel is less than -96 dB, the channel will mute, but the MuteChX bit will not be set. When the channel's effective volume returns to -96 dB or above, the mute condition will be released. It should be noted that if the channel's MuteChX bit or any of the channel's unmasked Master X Mute bits are set, the channel will remain muted until the necessary mute conditions are released.

Referenced Control	Register Location
MuteChX	"Mute Control - Address 0Ah" on page 33
Master X Mute	"Master 1 Mute (Bit 1)" on page 37 "Master 2 Mute (Bit 1)" on page 38 "Master 3 Mute (Bit 1)" on page 39

5.6 Muting Controls

The CS3318 provides flexible muting capabilities to complement its comprehensive volume control abilities. Each channel's mute state may be controlled on an individual channel basis, by any of 3 master mute controls, and by the hardware $\overline{\text{MUTE}}$ input pin.

The mute state of any channel within the CS3318 is determined by the logical OR of four conditions, and the channel will mute if any one or more of the conditions are met. These conditions are:

1. The channel's individual mute condition is set.
2. One or more of the channel's unmasked master mute conditions are set.
3. The hardware mute input is enabled and active.
4. The channel's effective volume (See Equation 1 on page 19) is less than -96 dB.

The CS3318 incorporates zero-crossing detection capabilities, and all muting changes are implemented as dictated by the zero-crossing detection settings (see "Zero-Crossing Detection" on page 22).

5.6.1 Individual Channel Mute Controls

The CS3318 provides 8 individual channel mute controls. These controls can be used to individually mute each of the input/output channels independent of all other volume and mute settings.

Individual channel mute control is accomplished by setting or clearing the channel's corresponding MuteChX bit in the Mute Control register.

Referenced Control	Register Location
MuteChX	"Mute Control - Address 0Ah" on page 33

5.6.2 Master Mute Controls

The CS3318 master mute controls allow the user to simultaneously control the mute state of all channels, or a user-defined subset of all channels within a device. A total of 3 master mute controls, M1_Mute, M2_Mute, and M3_Mute, are provided for comprehensive and flexible control.

Master mute control is accomplished by setting or clearing the MX_Mute bit in the corresponding Master Control register. Each master mute control affects only those channels unmasked in its corresponding Master X Mask register.

Referenced Control	Register Location
MX_Mute	"Master 1 Mute (Bit 1)" on page 37 "Master 2 Mute (Bit 1)" on page 38 "Master 3 Mute (Bit 1)" on page 39
Master X Mask	"Master 1 Mask - Address 10h" on page 36 "Master 2 Mask - Address 13h" on page 37 "Master 3 Mask - Address 16h" on page 38

5.6.3 Hardware Mute Control

The CS3318 implements a hardware $\overline{\text{MUTE}}$ input pin to allow the user to control the mute state of all channels with an external level-active signal. By default, the $\overline{\text{MUTE}}$ input is configured for active low operation, and all channels will be held in a mute state whenever this input is low.

For enhanced flexibility, setting the MutePolarity bit will configure the $\overline{\text{MUTE}}$ input pin for active high operation. Additionally, the EnMuteIn bit may be cleared to disable the CS3318's response to the $\overline{\text{MUTE}}$ input signal.

Referenced Control	Register Location
MutePolarity	"MUTE Input Polarity (Bit 4)" on page 33
EnMuteIn	"Enable MUTE Input (Bit 5)" on page 33

5.7 Zero-Crossing Detection

The CS3318 incorporates comprehensive zero-crossing detection features to provide for noise-free level transitions. Three zero-crossing detection modes and 8 selectable time-out periods are available for enhanced flexibility. Zero-crossing detection and time-out is implemented independently for each channel.

5.7.1 Zero-Crossing Modes

The zero-crossing mode for all channels within the CS3318 are configured via the ZCMode[1:0] bits in the Device Config 2 register. By default, zero-crossing mode 1 is selected. The zero-crossing modes are detailed in Table 2.

Mode	Zero-Crossing Function
0	Volume changes take effect immediately.
1	Volume changes take effect on a signal zero-crossing. If a zero-crossing is not detected before the time-out period has elapsed, the volume change will be implemented immediately when the time-out period elapses. If the volume setting is changed again before the original volume change has been implemented, the original change will be discarded, the time-out period will be reset, and the new volume setting will take effect when a zero-crossing is detected or the time-out period elapses.
2	Volume changes take effect on a signal zero-crossing. If a zero-crossing is not detected before the time-out period has elapsed, the volume change will be implemented immediately when the time-out period elapses. If the volume setting is changed again before the original volume change has been implemented, the original volume change will be implemented immediately upon reception of the new volume change command, the time-out period will be reset, and the new volume setting will take effect when a zero-crossing is detected or the time-out period elapses.

Table 2. Zero-Crossing Modes

Referenced Control	Register Location
ZCMode[1:0]	"Zero-Crossing Mode (Bits 1:0)" on page 35

5.7.2 Zero-Crossing Time-Out

When in zero-crossing mode 1 or 2, the zero-crossing time-out period dictates how long the CS3318 will wait for a signal zero-crossing before implementing the requested volume change without a zero-crossing, thereby allowing the possibility of audible artifacts. The CS3318 provides 8 selectable time-out periods ranging from 5 ms to 50 ms; these are shown in Table 3.

Time-Out Setting	Time-Out Period
0	5 ms
1	10 ms
2	15 ms
3	18 ms
4	20 ms
5	30 ms
6	40 ms
7	50 ms

Table 3. Zero-Crossing Time-Out Periods

The zero-crossing time-out period for all channels within the CS3318 is configured via the TimeOut[2:0] bits in the Device Config 2 register. The time-out period is set to 18 ms (setting 3) by default.

Referenced Control	Register Location
TimeOut[2:0]	"Zero-Crossing Time-Out Period (Bits 4:2)" on page 34

5.8 System Serial Control Configuration

The CS3318 includes a comprehensive serial control port which supports both SPI and I²C modes of communication (See the "I²C/SPI Serial Control Formats" section on page 27). The control port uses the shared serial control bus to define each device's slave address. This allows independent control of up to 128 devices on the shared serial control bus without requiring hardware device address configuration pins or any more than one $\overline{CS}$ signal (for SPI mode).

Each device will respond to three different chip addresses; Individual, Group 1, and Group 2. The device's Individual chip address provides read and write access to the CS3318's internal registers. The device's Group 1 and Group 2 addresses provide write-only access to the CS3318's internal registers. If a read operation is requested using either the Group 1 or Group 2 address, the devices will not respond to the request. Upon the release of $\overline{RESET}$, each of these device addresses initializes to the default address. In this state, the device will respond to both register reads and writes when addressed with this default address.

Each of the device's addresses may be changed via a standard serial register write to an internal register of the CS3318. Using this method, each device may be assigned a unique Individual address, and groups of devices may be assigned shared Group 1 and Group 2 addresses for simultaneous control. Use of the master volume and mute controls in combination with the available group addresses provides for easy master and sub-master control within a multiple CS3318 system.

Referenced Control	Register Location
Individual Address	"Individual Chip Address 1Bh" on page 41
Group 1 Address	"Group 1 Chip Address 1Ah" on page 40
Group 2 Address	"Group 2 Chip Address 19h" on page 40

5.8.1 Serial Control within a Single-CS3318 System

In a single CS3318 system, no special attention must be given to the serial control port operation of the CS3318. The standard serial control signals (SDA and SCL for I²C Mode, or MOSI, CCLK, and $\overline{CS}$ for SPI Mode) should be connected to the system controller, and the ENOut signal is not used (see Figures 7 and 8). Upon the release of $\overline{RESET}$, the CS3318 must be addressed with its default chip address.

Although it is not necessary, the default Individual, Group 1, and Group 2 chip addresses may be changed by writing their respective control port registers. Once the contents of these registers has been modified, the device must be addressed with the registers' new contents. When the device is reset, its device addresses will return to their default value.

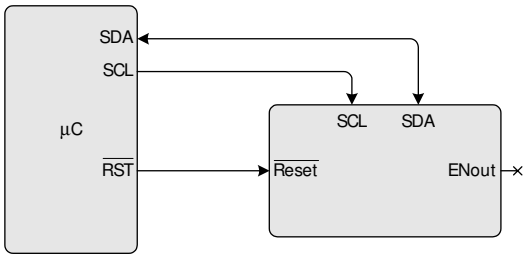


Figure 7. Standard I²C Connections

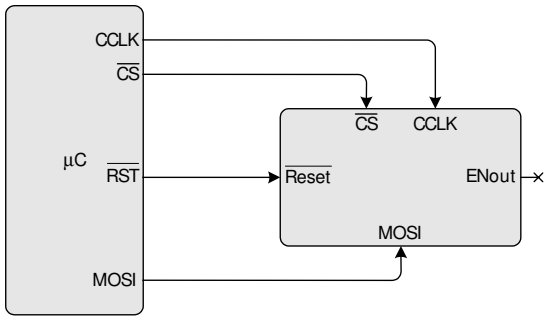


Figure 8. Standard SPI Connections

5.8.2 Serial Control within a Multiple-CS3318 System

The CS3318 allows both independent and simultaneous control of up to 128 devices on a shared I²C or SPI serial control bus. The address of each device is configured by the host controller via the shared serial control bus. All serial communication, including the configuration of each device's address, adheres to a standard I²C or SPI bus protocol.

A device's Individual device address, which provides read and write access to the device's internal registers, should be set to a unique value, different from all other addresses recognized by devices on the serial communication bus. This address facilitates independent control of each CS3318 on the serial control bus.

A device's Group 1 and Group 2 addresses, which provide write-only access to the device's internal registers, may be set to the same value across multiple CS3318's on the shared serial communication bus. Assigning common Group addresses to multiple devices in a system allows system sub-master and system master volume control. For instance, a system containing 8 CS3318's may configure the Group 1 address of the first set of 4 CS3318's to 10h, the Group 1 address of the second set of 4 CS3318's to 20h, and the Group 2 address of all 8 CS3318's to A0h. In this manner, a serial control data write to address 10h would act as a system sub-master control to the first set of 4 devices, a write to 20h would act as a system sub-master control to the second set of 4 devices, and a write to A0h would act as a system master control to all devices.

By default, the CS3318 will not respond to serial communication when addressed with its Group 1 or Group 2 address. The CS3318 will only respond to one or both of these addresses if the corresponding address has been enabled via the control port. To enable a Group address, its corresponding Enable bit, located in the LSB of its respective Group address register, must be set.

The CS3318 implements an ENOut signal to facilitate the device address configuration process. This signal is used to hold all but one un-configured device in a reset state. After the Individual device address of each device has been set, the ENOut signal is used to enable the "next" device in the chain, allowing its Individual device address to be set. See "SPI Mode Serial Control Configuration" section on page 24 and "I²C Mode Control Configuration" on page 26 for more information about system configuration in each communication mode.

5.8.2.1 SPI Mode Serial Control Configuration

Up to 128 CS3318's sharing the same $\overline{CS}$ signal may be connected to a common SPI serial control bus. This shared serial bus is used to assign a unique device address to each device on the bus such that they may be independently addressed. To implement this method of device address configuration, the devices must be connected as shown in Figure 9.

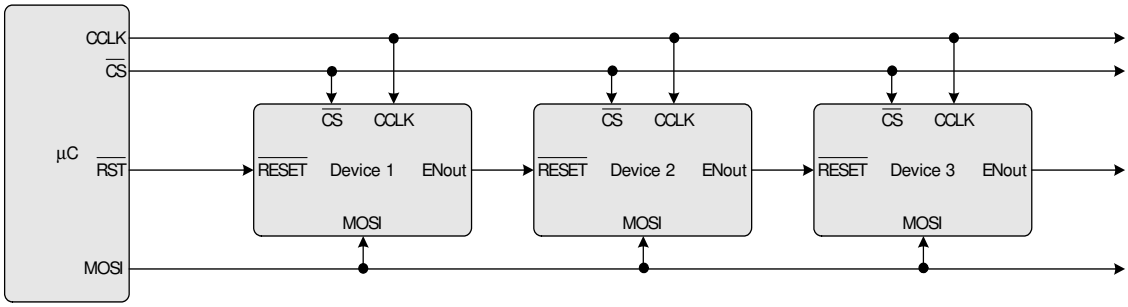


Figure 9. SPI Serial Control Connections

Note that the serial control signals CCLK, CS, and MOSI are connected in parallel to each CS3318. The active low reset output of the system controller is connected to the $\overline{RESET}$ input of the first CS3318 in the chain. The ENOut of the first device is connected to the $\overline{RESET}$ input of the second CS3318 whose ENOut signal is connected to the third CS3318. This pattern of connecting the ENOut of device N to the $\overline{RESET}$

input of device N+1 may be repeated for up to 128 devices per single $\overline{CS}$ signal. If more than 128 devices are required in a system, separate $\overline{CS}$ signals may be used to create additional chains of up to 128 devices per $\overline{CS}$ signal.

As each device is placed into reset ($\overline{RESET}$ is low), its ENOut signal is driven low. The ENOut signal will continue to be driven low until the device is taken out of reset ($\overline{RESET}$ is high) and the Enable bit (see "Enable Next Device (Bit 0)" on page 41) is set, at which time the ENOut signal will be driven high.

To configure a unique Individual device address for each device on the shared serial bus, the first device must be reset (a low to high transition on its $\overline{RESET}$ pin), the Individual device address register must be written (using the CS3318's default device address) with a unique device address, and the Enable bit must be set to take the next device in the serial control chain out of reset. This process may be repeated until all devices in the serial control chain have been assigned a new Individual device address. Figure 10 diagrams this configuration process.

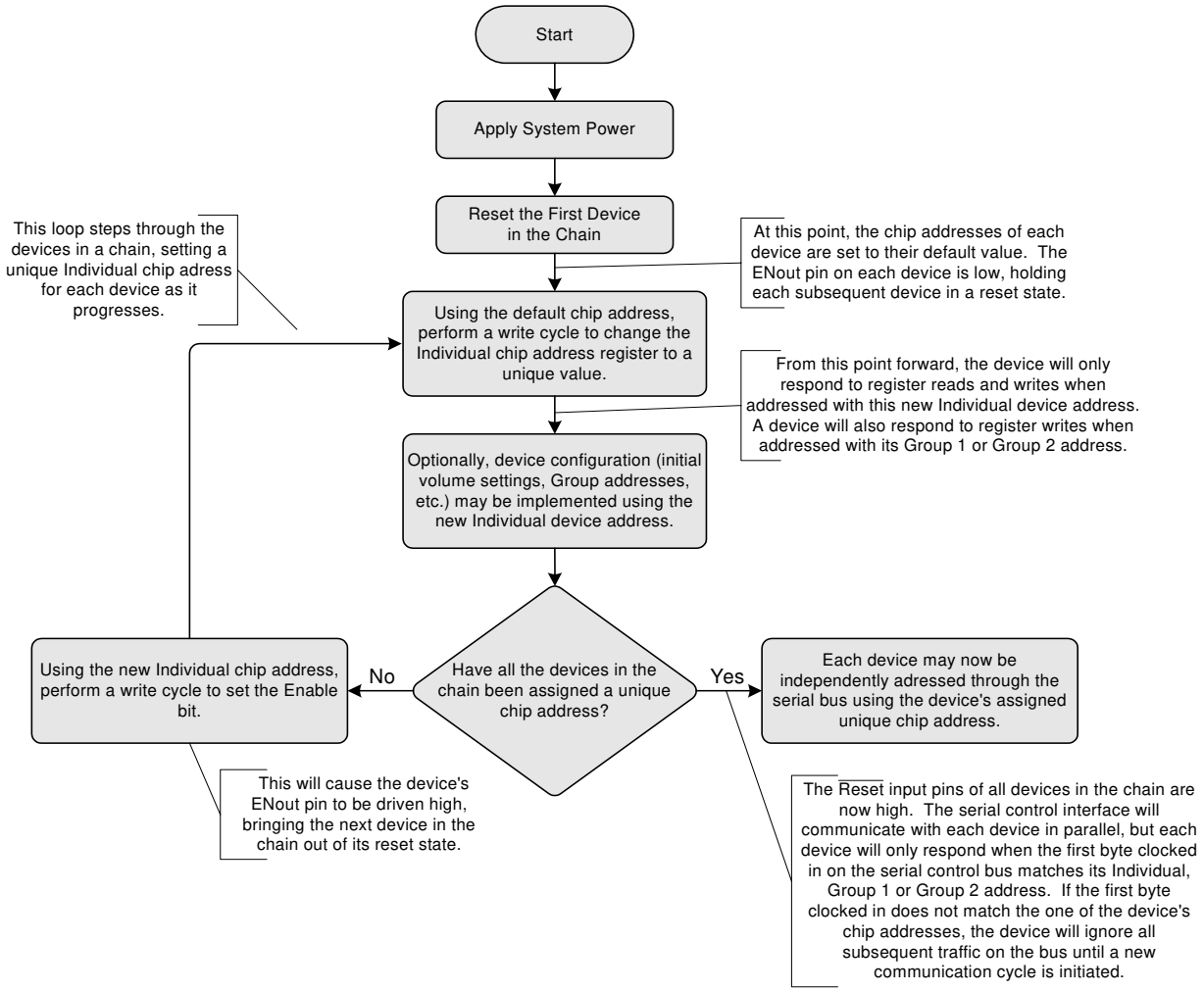


Figure 10. Individual Device Address Configuration Process

Notice that Figure 10 shows the setting of the Individual address and the setting of the Enable bit as two discrete steps. While this demonstrates one approach to device configuration, it should be noted that two steps are not necessary to complete the action of setting the Individual address and enabling the next device. This may be done simultaneously with one register write (containing the new Individual address and the Enable bit set) to the Individual address register.