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2.8 W Mono Class-D Audio Amplifier with Low Idle Current

CS35L00 Features

- ◆ Hybrid Class-D Architecture
 - <1 mA Quiescent Current
 - 1 x 2.8 W into 4 Ω (10% THD+N)
 - 1 x 2.3 W into 4 Ω (1% THD+N)
 - 1 x 1.7 W into 8 Ω (10% THD+N)
 - 1 x 1.4 W into 8 Ω (1% THD+N)
- ◆ Advanced ΔΣ Closed-loop Modulation
 - 98 dB Signal-to-Noise Ratio (A-Weighted)
 - 0.02% THD+N @ 1 W (SD & HD Mode)
- ◆ Integrated Protection and Automatic Recovery for Output Short-circuit and Thermal Overload
- ◆ Thermally Enhanced 10-pin DFN Package with Pin-selectable Gain of +6 dB or +12 dB
- ◆ Pop and Click Suppression

Common Applications

- ◆ Laptops
- ◆ Netbooks
- ◆ Portable Navigation Devices
- ◆ Active Speakers
- ◆ Portable Gaming

General Description

The CS35L00 is a 2.8 W high efficiency Hybrid Class-D audio amplifier with low idle current consumption and a selectable gain.

The CS35L00 features an advanced closed-loop architecture to provide 0.02% THD+N at 1 W and -88 dB PSRR at 217 Hz.

A flexible Hybrid Class-D output stage offers four modes of operation: Standard Class-D (SD) mode offers full audio bandwidth and high audio performance; Hybrid Class-D (HD) mode offers a substantial reduction in idle power consumption with an integrated Class-H controller; Reduced Frequency Class-D (FSD) mode reduces the output switching frequency, producing lower electromagnetic interference (EMI); and Reduced Frequency Hybrid Class-D (FHD) mode produces both the lower idle power consumption of HD mode and the reduced EMI benefits of FSD mode.

Requiring minimal external components and PCB space, the CS35L00 is available in a 3.0 mm x 3.0 mm, 10-pin DFN package in Commercial grade (-10°C to +70°C). Please see [“Ordering Information” on page 33](#) for package options and gain configurations.

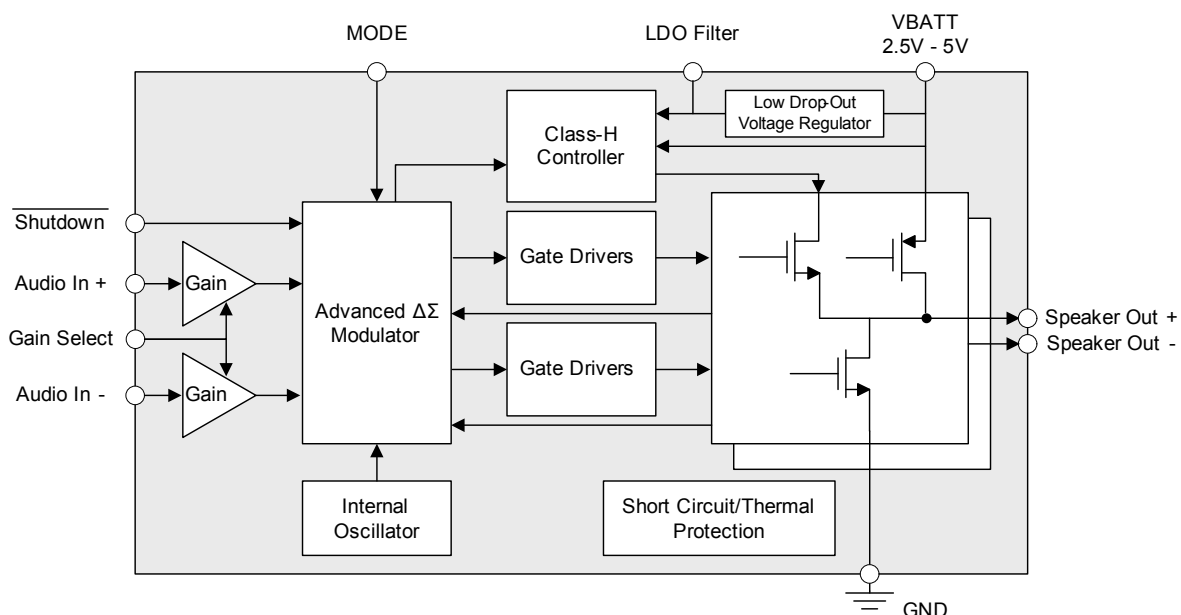


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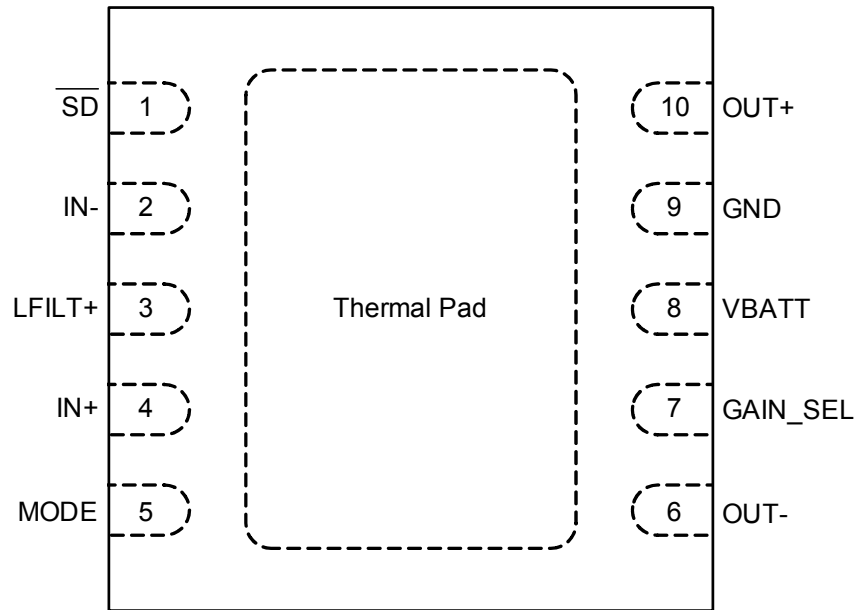
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1. PIN DESCRIPTIONS FOR CS35L00



**Figure 1. Top View of DFN Pin Out
(Looking down through package)**

Pin Name	#	Pin Description
$\overline{\text{SD}}$	1	Shutdown (<i>Input</i>) - Pulling this pin low places the CS35L00 in shutdown.
IN-	2	Negative Analog Input (<i>Input</i>) - Differential negative audio signal input
LFILT+	3	Low Drop Out Regulator Filter (<i>Output</i>) - Bypass capacitor connection point for internal LDO. Connecting this net to VBATT places the device into SD mode.
IN+	4	Positive Analog Input (<i>Input</i>) - Differential positive audio signal input.
MODE	5	Switching Mode (<i>Input</i>) - Controls the output switching modes of the CS35L00.
OUT-	6	Negative PWM Output (<i>Output</i>) - Differential negative PWM output.
GAIN_SEL	7	Gain Select (<i>Input</i>) - Sets the gain of the amplifier. When pulled low, gain is +12 dB. When pulled high, gain is +6 dB.
VBATT	8	Positive Analog Power Supply (<i>Input</i>) - Positive power supply input.
GND	9	Ground (<i>Input</i>) - Power supply ground.
OUT+	10	Positive PWM Output (<i>Output</i>) - Differential Positive PWM output.
Thermal Pad	-	Thermal Pad (<i>Input</i>) - Thermal relief pad for optimized heat dissipation. Connect to GND. See “DFN Thermal Pad” on page 31 for more information.

2. DIGITAL PIN CONFIGURATIONS

See [\(Note 1\)](#) and [\(Note 2\)](#) below the table.

Power Supply	I/O Name	Pin #	Direction	Internal Connections	Configuration
VBATT	\overline{SD}	1	Input	No Internal Pull Up	Hysteresis on CMOS Input
	MODE	5	Input	No Internal Pull Up	Hysteresis on CMOS Input
	GAIN_SEL	7	Input	No Internal Pull Up	Hysteresis on CMOS Input

Note:

1. Refer to specification table [“Digital Interface Specifications & Characteristics”](#) on page 14 for details on the digital I/O characteristics.
2. I/O voltage levels must not exceed the voltage listed in table [“Absolute Maximum Ratings”](#) on page 8.

3. TYPICAL CONNECTION DIAGRAMS

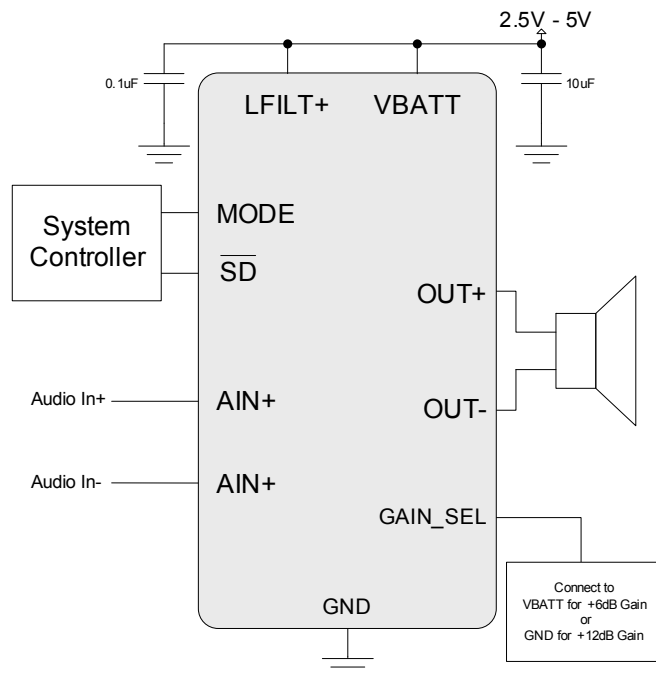


Figure 2. Typical Connection Diagram for SD & FSD Mode

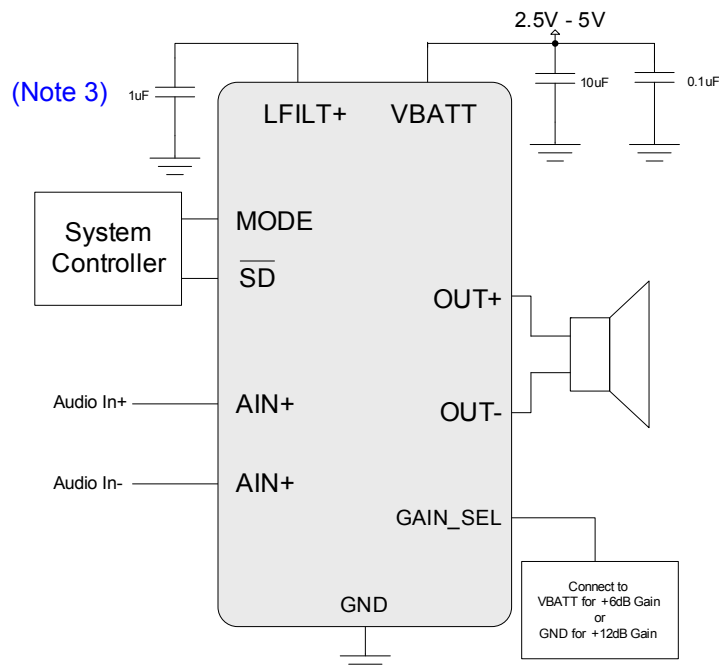


Figure 3. Typical Connection Diagram for HD & FHD Mode

Note:

- The value of the capacitance connected to the LFILT+ net should not exceed 4.7 µF. Presence of a capacitance above 4.7 µF will prevent proper HD and FHD operation.

4. CHARACTERISTICS & SPECIFICATIONS

Test Conditions (unless otherwise specified): GND = 0 V; All voltages with respect to ground; Input signal = 997 Hz differential sine wave; $T_A = 25^\circ\text{C}$; VBATT = 5.0 V; $R_L = 8\ \Omega$; 22 Hz to 20 kHz measurement bandwidth; Measurements taken with AES17 measurement filter and Audio Precision AUX-0025 passive filter.

RECOMMENDED OPERATING CONDITIONS

GND = 0 V; All voltages with respect to ground. Please see (Note 4).

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply					
Supply Voltage	VBATT	2.5	5.0	5.5	V
Temperature					
Ambient Temperature	T_A	-10	-	+70	$^\circ\text{C}$
Junction Temperature	T_J	-10	-	+150	$^\circ\text{C}$

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; All voltages with respect to ground.

Parameters	Symbol	Min	Max	Units
DC Power Supply				
Supply Voltage	VBATT	-0.3	6.0	V
LFILT+ Current (Note 5)	I_{VDREG}	-	10	μA
Inputs				
Input Current	I_{in}	-	± 10	mA
Temperature				
Ambient Operating Temperature (power applied)	T_A	-20	+125	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65	+150	$^\circ\text{C}$

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Notes:

- Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.
- No external loads should be connected to the LFILT+ net. Any connection of a load to this point may result in errant operation or performance degradation in the device.

ELECTRICAL CHARACTERISTICS - ALL OPERATIONAL MODES

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units	
Max. Current from LFILT+ (Note 6)	I_{LFILT+}		-	10	-	μA	
LFILT+ Output Impedance	Z_{LFILT+}		-	0.7	-	Ω	
VBATT Limit for HD/FHD Mode (Note 7)	V_{BLIM}		-	3.0	-	VDC	
Input Level for Entering LDO Operation in HD/FHD Modes (Note 8)	V_{IN-LDO}	GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	$0.015 \cdot V_{BATT}$ $0.029 \cdot V_{BATT}$	-	Vrms Vrms	
Input Level for Entering VBATT Operation in HD/FHD Modes (Note 9)	$V_{IN-VBATT}$	GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	0.10 0.20	-	Vrms Vrms	
LDO Entry Time Delay	t_{LDO}		-	1200	-	ms	
LDO Level for HD/FHD Modes	V_{LDO}		-	1.0	-	V	
Output Offset Voltage	V_{OFFSET}	Inputs AC coupled to GND	-	+/-2	-	mV	
Amplifier Gain	A_V	GAIN_SEL = Low GAIN_SEL = High	-	12 6	-	dB dB	
Shutdown Supply Current	$I_{A(SD)}$	$\overline{SD} = \text{Low}$	-	0.05	-	μA	
MOSFET On Resistance	$R_{DS(ON)}$	$I_{bias} = 0.5 \text{ A}$	-	350	-	$\text{m}\Omega$	
Thermal Error Threshold (Note 10)	T_{TE}		-	150	-	$^{\circ}\text{C}$	
Thermal Error Retry Time (Note 10)	R_{TE}		-	1200	-	ms	
Under Voltage Lockout Threshold (Note 10)	UVLO		-	2.0	-	V	
Operating Efficiency	η	Output Levels at 10% THD+N					
		$8 \Omega + 33 \mu\text{H}$ Load	VBATT = 5 VDC	-	90	-	%
			VBATT = 3.7 VDC	-	89	-	%
		$4 \Omega + 33 \mu\text{H}$ Load	VBATT = 5 VDC	-	84	-	%
			VBATT = 3.7 VDC	-	83	-	%

Note:

6. No external loads should be connected to the LFILT+ net. Any connection of a load to this point may result in errant operation or performance degradation in the device.
7. When VBATT is below this threshold (V_{BLIM}), operation is automatically restricted to SD mode.
8. When operating in HD or FHD mode and the differential input voltage remains below the input level threshold (V_{IN-LDO}) for a period of time (t_{LDO}), the PWM outputs will be powered by the internally generated LDO supply (V_{LDO}).
9. When operating in HD or FHD mode and the differential input voltage is above this input level threshold ($V_{IN-VBATT}$), the PWM outputs will be powered directly from the VBATT supply.
10. Refer to [Section 5.5](#) for more information on Thermal Error functionality.
11. Under Voltage Lockout is the threshold at which a decreasing VBATT supply will disable device operation.

ELECTRICAL CHARACTERISTICS - SD MODE

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	P _O	THD+N = 1% R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R _L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.35/0.95/0.73	-	W
			-	2.25/1.58/1.22	-	W
		THD+N = 10% R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R _L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.67/1.18/0.91	-	W
			-	2.82/2.00/1.53	-	W
Total Harmonic Distortion + Noise	THD+N	P _O = 1.0 W	-	0.02	-	%
Power Supply Rejection Ratio	PSRR	V _{ripple} = 200 mV _{PP} , AINx AC coupled to GND @ 217 Hz @ 1 kHz	-	88	-	dB
			-	82	-	dB
Common-Mode Rejection Ratio	CMRR	V _{ripple} = 1 V _{PP} , f _{ripple} = 217 Hz	-	73	-	dB
Signal to Noise Ratio A-Weighted	SNR _A	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	96	-	dB
			-	97	-	dB
Idle Channel Noise A-Weighted	ICN _A	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	54	-	μVrms
			-	49	-	μVrms
Idle Channel Noise	ICN	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	110	-	μVrms
			-	100	-	μVrms
Frequency Response	FR	20 Hz to 20 kHz	-0.1	0	0.4	dB
Total Group Delay	GD		-	6	-	μs
Output Switching Frequency	f _{sw1}		-	192	-	kHz
Idle Current Draw (Note 12)	I _{IDLE}	AIN+ connected AIN-, No Output Load VBATT = 5.0 VDC	-	1.42	-	mA
		VBATT = 4.2 VDC	-	1.31	-	mA
		VBATT = 3.7 VDC	-	1.24	-	mA
Input Impedance, Single Ended	Z _{IN}	GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	65	-	kΩ
			-	100	-	kΩ
Input Voltage @ 1 % THD+N	V _{ICLIP}	R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	0.85/0.72/0.63	-	Vrms
			-	1.70/1.43/1.25	-	Vrms

ELECTRICAL CHARACTERISTICS - FSD MODE

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	P _O	THD+N = 1% R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R _L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.28/0.90/0.69	-	W
		THD+N = 10% R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R _L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.65/1.17/0.90	-	W
Total Harmonic Distortion + Noise	THD+N	P _O = 1.0 W	-	0.10	-	%
Power Supply Rejection Ratio	PSRR	V _{ripple} = 200 mV _{PP} , AINx AC coupled to GND	-	88	-	dB
		@ 217 Hz @ 1 kHz	-	80	-	dB
Common-Mode Rejection Ratio	CMRR	V _{ripple} = 1 V _{PP} , f _{ripple} = 217 Hz	-	71	-	dB
Signal to Noise Ratio A-Weighted	SNR _A	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13)	-		-	
		GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	80	-	dB
Idle Channel Noise A-Weighted	ICN _A	AIN+ connected to AIN-	-	300	-	μVrms
		GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	290	-	μVrms
Idle Channel Noise	ICN	AIN+ connected to AIN-	-	570	-	μVrms
		GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	550	-	μVrms
Frequency Response	FR	20 Hz to 20 kHz	-4.0	0	0.5	dB
Total Group Delay	GD		-	14	-	μs
Output Switching Frequency	f _{sw2}		-	76	-	kHz
Idle Current Draw (Note 12)	I _{IDLE}	AIN+ connected AIN-, No Output Load	-	1.07	-	mA
		VBATT = 5 VDC	-	1.01	-	mA
		VBATT = 4.2 VDC VBATT = 3.7 VDC	-	0.97	-	mA
Input Impedance, Single Ended	Z _{IN}	GAIN_SEL = Low (12 dB)	-	160	-	kΩ
		GAIN_SEL = High (6 dB)	-	250	-	kΩ
Input Voltage @ 1 % THD+N	V _{ICLIP}	R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	0.83/0.69/0.61	-	Vrms
		GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	1.65/1.38/1.21	-	Vrms

Note:

12. Idle Current Draw (I_{IDLE}) is specified without any output filtering. Refer to [Section 5.3 on page 17](#) for information on output filtering.

ELECTRICAL CHARACTERISTICS - HD MODE

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	P _O	THD+N = 1% R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R _L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.34/0.94/0.73	-	W
			-	2.25/1.58/1.22	-	W
		THD+N = 10% R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R _L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.67/1.18/0.91	-	W
			-	2.83/2.00/1.53	-	W
Total Harmonic Distortion + Noise	THD+N	P _O = 1.0 W	-	0.02	-	%
Power Supply Rejection Ratio	PSRR	V _{ripple} = 200 mV _{PP} , AINx AC coupled to GND @ 217 Hz	-	88	-	dB
		@ 1 kHz	-	86	-	dB
Common-Mode Rejection Ratio	CMRR	V _{ripple} = 1 V _{PP} , f _{ripple} = 217 Hz	-	73	-	dB
Signal to Noise Ratio A-Weighted	SNR _A	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13)				
		GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	97 98	-	dB dB
Idle Channel Noise A-Weighted	ICN _A	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	49 43	-	μVrms μVrms
Idle Channel Noise	ICN	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	86 83	-	μVrms μVrms
Frequency Response	FR	20 Hz to 20 kHz	-0.1	0	0.4	dB
Total Group Delay	GD		-	6	-	μs
Output Switching Frequency	f _{sw1}		-	192	-	kHz
Idle Current Draw (Note 14)	I _{IDLE}	AIN+ connected AIN-, No Output Load VBATT = 5 VDC	-	1.11	-	mA
		VBATT = 4.2 VDC	-	1.06	-	mA
		VBATT = 3.7 VDC	-	1.03	-	mA
Input Impedance, Single Ended	Z _{IN}	GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	65 100	-	kΩ kΩ
Input Voltage @ 1 % THD+N	V _{ICLIP}	R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	0.85/0.71/0.63	-	Vrms Vrms
			-	1.70/1.42/1.25	-	

ELECTRICAL CHARACTERISTICS - FHD MODE

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	P _O	THD+N = 1% R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R _L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.28/0.89/0.68	-	W
		THD+N = 10% R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R _L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	2.17/1.51/1.15	-	W
Total Harmonic Distortion + Noise	THD+N	P _O = 1.0 W	-	0.10	-	%
Power Supply Rejection Ratio	PSRR	V _{ripple} = 200 mV _{PP} , AINx AC coupled to GND @ 217 Hz	-	89	-	dB
		@ 1 kHz	-	85	-	dB
Common-Mode Rejection Ratio	CMRR	V _{ripple} = 1 V _{PP} , f _{ripple} = 217 Hz	-	71	-	dB
Signal to Noise Ratio A-Weighted	SNR _A	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13)	-	93	-	dB
		GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	94	-	dB
Idle Channel Noise A-Weighted	ICN _A	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	71	-	μVrms
			-	63	-	μVrms
Idle Channel Noise	ICN	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	125	-	μVrms
			-	115	-	μVrms
Frequency Response	FR	20 Hz to 20 kHz	-4.0	0	0.5	dB
Total Group Delay	GD		-	14	-	μs
Output Switching Frequency	f _{sw1}	Input level below V _{IN-LDO}	-	192	-	kHz
Output Switching Frequency	f _{sw2}	Input level above V _{IN-VBATT}	-	76	-	kHz
Idle Current Draw (Note 14)	I _{IDLE}	AIN+ connected AIN-, No Output Load VBATT = 5 VDC	-	1.11	-	mA
		VBATT = 4.2 VDC	-	1.06	-	mA
		VBATT = 3.7 VDC	-	1.03	-	mA
Input Impedance, Single Ended	Z _{IN}	GAIN_SEL = Low (12 dB)	-	160	-	kΩ
		GAIN_SEL = High (6 dB)	-	250	-	kΩ
Input Voltage @ 1 % THD+N	V _{ICLIP}	R _L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	0.83/0.69/0.61	-	Vrms
		GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	-	1.65/1.38/1.20	-	Vrms

Note:

13. SNR_A dB is referenced to the output signal amplitude resulting in the specified output power at THD+N <1%. See [“Parameter Definitions” on page 29](#) for more information.
14. Idle Current Draw (I_{IDLE}) is specified without any output filtering. Refer to [Section 5.3 on page 17](#) for information on output filtering. At idle, the output devices will switch at the same rate in HD and FHD mode. FHD only changes the output switching frequency when the input levels are above the “Input Level for Entering VBATT Operation in HD/FHD Modes (V_{IN-VBATT})” given in [“Electrical Characteristics - All Operational Modes” on page 9](#).

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters	Symbol	Min	Max	Units
Input Leakage Current	I_{in}	-	±10	μA
Input Capacitance		-	10	pF
\overline{SD} Pulse Width Requirement		1	-	ms
Logic I/Os (Applicable to GAIN_SEL, MODE, and \overline{SD})				
High-Level Input Voltage	V_{IH}	0.7•VBATT	-	V
Low-Level Input Voltage	V_{IL}	-	0.3•VBATT	V

POWER-UP & POWER-DOWN CHARACTERISTICS

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Start-Up Time (Note 15)	t_{start}	After “Low” to “High” \overline{SD} Pin transition edge	-	18	-	ms
Zero Crossing Power-Up Timeout	$t_{timeout}$	No audio input applied	-	25	-	ms
Power-Down Time	t_{off}	After “High” to “Low” \overline{SD} Pin transition edge	-	1	-	ms

Note:

15. Start-Up Time (t_{start}) refers to the internal start-up time from when \overline{SD} is released to when the device is ready to activate the PWM outputs. The total power-up time from \overline{SD} release to the PWM outputs becoming active will vary based on the input signal, not exceeding the Start-Up Time + Zero Crossing Power-Up Timeout ($t_{start} + t_{timeout}$). For more information refer to [Section 5.4](#).

5. APPLICATIONS

5.1 MODE Descriptions

The CS35L00 device can be operated in one of four operating modes, determined by the MODE pin and the LFILT+ pin. The four modes of operation are Standard Class-D operation (SD), Reduced Frequency Standard Class-D operation (FSD), Hybrid Class-D operation (HD), and Reduced Frequency Hybrid Class-D operation (FHD). Each of these modes can be leveraged to optimize different performance criteria in an array of applications.

		MODE connected to:	
		GND	VBATT
LFILT+ connected to:	VBATT	Reduced Frequency Class-D Mode (FSD)	Standard Class-D Mode (SD)
	Filter Cap to Ground	Reduced Frequency Hybrid Class-D Mode (FHD)	Hybrid Class-D Mode (HD)

Table 1. LFILT+ and MODE Operation Configurations

5.1.1 Standard Class D Modes of Operation

5.1.1.1 SD Mode

Standard Class-D (SD) mode supports full audio bandwidth with very good SNR and THD+N performance. This mode of operation is characterized by a traditional closed loop, analog $\Delta\Sigma$ modulated Class-D amplifier. With an output switching frequency of 192 kHz, this mode ensures flat frequency response across the entire audio frequency range.

5.1.1.2 FSD Mode

The Reduced Frequency Class-D (FSD) mode provides competitive audio performance and a reduction in radiated emissions by decreasing the switching frequency of the output devices to 76 kHz. This reduction in switching frequency reduces the high frequency energy being created by the output switching events. Idle channel noise is slightly higher in this mode of operation than SD mode, with the trade-off being better EMI performance and power consumption.

5.1.2 Hybrid Class D Modes of Operation

Hybrid Class-D and Reduced Frequency Hybrid Class-D modes of operation allows the rail voltage for the output devices to switch between a high voltage net and a low voltage net depending on the audio content being amplified. This is explained in more detail in [Section 5.1.2.1](#) and [Section 5.1.2.2](#). Operation in these modes requires that the voltage present on the VBATT pin be above the level listed as “VBATT Limit for HD/FHD Mode (V_{B_LIM})” in [“Electrical Characteristics - All Operational Modes” on page 9](#). If it is not, HD and FHD modes of operation of the device will automatically be disabled and operation will be limited to the SD mode of operation.

In both HD and FHD mode, the value of the capacitance connected to the LFILT+ pin must not exceed 4.7 μF . If this value is greater than 4.7 μF , it will prevent the rail voltage of the output devices from transitioning properly between VBATT and the internal LDO.

5.1.2.1 HD Mode

Hybrid Class-D mode (HD) provides competitive analog performance with a substantial reduction in idle power dissipation and radiation emissions. In this mode, the output switches at 192 kHz and a secondary supply is derived from VBATT using an internal 1.0 VDC low drop-out linear regulator (LDO). When the output signal is at a low amplitude, the Class-D output stage begins to switch from the lower rail voltage created by the internal LDO. This not only decreases idle power consumption when output capacitors are used, but also reduces electromagnetic emissions by reducing the amplitude of the square waves being created at the output of the CS35L00 when operating at low amplitude or idle power.

5.1.2.2 FHD Mode

The Reduced Frequency Hybrid Class-D (FHD) mode provides the best overall EMI performance and the lowest power consumption with slightly decreased frequency response near the top frequency range of the audio band, for high amplitude signals. In this mode of operation, the output switching frequency is reduced to 76 kHz during high amplitude transients on the output. The threshold at which this transition from 192 kHz to 76 kHz switching rate occurs is given as the Input Level Threshold for FHD Operation in [“Electrical Characteristics - FHD Mode” on page 13](#). Combined with the lower amplitude switching offered by the Hybrid design, this reduction in switching energy dramatically reduces the emissions levels of the output stage and its associated components.

5.2 Reducing the Gain with External Series Resistors

If necessary, it is possible to decrease the gain of the CS35L00 by adding series resistors to the audio input signal as is shown in [Figure 4](#) below.

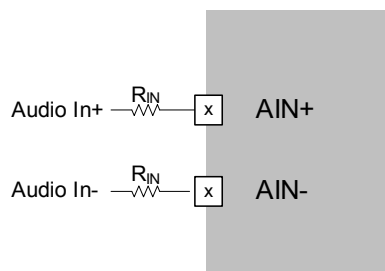


Figure 4. Adjusting Gain via External Series Resistance

If input resistors are added, the new gain of the amplifier can be determined by the following equation:

$$A_{V(\text{adjusted})} = A_V - 20 \times \log\left(\frac{Z_{IN}}{Z_{IN} + Z_{EXT}}\right)$$

Where:

$A_{V(\text{adjusted})}$ = The new, adjusted gain of the system

Z_{IN} = Input impedance of the device being used (See “Electrical Characteristics - SD Mode” on page 10, “Electrical Characteristics - FSD Mode” on page 11, “Electrical Characteristics - HD Mode” on page 12, or “Electrical Characteristics - FHD Mode” on page 13 for this value.)

Z_{EXT} = Value of the resistor added in series with the inputs

A_V = Original gain of the device being used (See “Electrical Characteristics - All Operational Modes” on page 9 for this value.)

5.3 Output Filtering with the CS35L00

The CS35L00 is specifically designed to minimize radiated electromagnetic interference (EMI) signals. All of the devices are capable of meeting all stated data sheet performance numbers with no special filtering required. Additionally, the device has shown to be below the compliance limits of both FCC and CISPR testing with no external filtering required.

Ultimately, compliance with any radiated emissions requirements depends significantly on the entire system under test. In applications where system-level trade-offs, such as compromised component layout or lengthy speaker wires, have increased emissions levels, a passive output filter can be added to the outputs of the device in order to decrease EMI levels.

5.3.1 Reduced Filter Order with the CS35L00

In applications which require an output filter, the unique design of the CS35L00 allows a much smaller, less expensive output filter to be used than what is normally found in Class D amplifiers. In contrast to a second order filter implemented with a series inductive element (traditional inductor or ferrite beads) and a shunt capacitive element, basic filtering for the CS35L00 is accomplished by a single-order capacitive element attached to the OUTx terminals. This is highlighted in Figure 5 below. Of course, if the system requires more aggressive filtering, a ferrite bead can be added in series with the outputs to further attenuate system level noise.

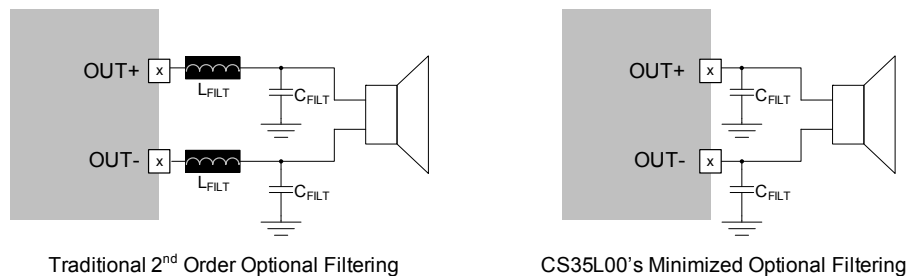


Figure 5. Optional Output Filter Components

5.3.2 Filter Component Selection

Usually, the need for output filtering is determined after the system under test has failed EMI testing. During this testing, problem frequencies are easily identified by the peaks which appear in the spectral plots gathered in the EMI testing.

Selection of the filter components should ensure that shunt elements (i.e. C_{FILT} in Figure 5 on page 17) present a very low impedance at the frequency corresponding to the tallest peak in the spectral plot. If needed, series components such as ferrite beads (i.e. L_{FILT} in Figure 5 on page 17) should be chosen to present a very high impedance at the frequency corresponding to the tallest peak in the spectral plot.

Careful attention should be paid to the current carrying capabilities of any included ferrite beads and the impedance of the ferrite beads in the audio band. A proper trade-off in ferrite bead selection is one that

allows the ferrite bead to sufficiently attenuate the problematic high-frequency emissions without compromising audio performance.

5.3.3 Output Filter Power Dissipation Considerations

In systems without inductive series elements like inductors or ferrite beads, power losses in the output filter are equal to the switching losses that occur in the system due to the cyclical charging and discharging of capacitors connected to the amplifier outputs. In systems that require an inductive series element, conducted losses also occur due to the series impedance added to the output path.

5.3.3.1 Conduction Losses for All Modes of Operation

For all modes of operation (SD, FSD, HD, and FHD), conduction losses are governed by the following equation:

$$P = I^2Z$$

Where:

P = Power dissipated in the series impedance.

I = RMS AC output current

Z = impedance of the series element at the frequency of the AC current

This equation neglects any series impedances presented by the PCB traces or speaker wires in the output path.

5.3.3.2 Switching Losses in SD/FSD Mode

Switching losses in SD/FSD Mode are governed by the equation

$$P = \frac{1}{2}CV^2f$$

Where:

P = Power dissipated in the capacitor (neglecting parasites).

C = Value of filtering capacitor

V = Peak voltage developed across the capacitor

f = Switching frequency of the outputs

These calculations are straightforward, as the peak voltage is simply the voltage level attached to VBATT, the capacitor is the value of capacitor that has been added for filtering (neglecting parasitic board capacitances), and the frequency is 192 kHz for SD and 76 kHz for FSD, respectively.

5.3.3.3 Switching Losses in HD/FHD.

Many factors affect the switching losses when the device is operated in HD/FHD mode. These factors include the frequency of the content being amplified, the voltage level of VBATT, and the amplitude of the output signal will factor into both the voltage presented across the capacitors and the frequency at which the capacitors are charged or discharged.

Static signals (i.e. sine waves at a fixed amplitude) are easier to consider than are dynamic signals (i.e. musical content), as they are governed by the same equation as that listed in [Section 5.3.3.1](#) and [Section 5.3.3.2 on page 18](#). Modifications to that equation are limited to the voltage term (V) and the frequency term (f), depending on whether the static input signal amplitude is causing the output devices to switch at 76 kHz or 192 kHz, and to operate off of the VBATT supply or off of the internally generated LDO.

It is important to note that the HD and FHD modes offer significant improvement over traditional Class D in idle power dissipation when an external output filter is necessary. This is because the voltage term (V) is significantly reduced in HD and FHD mode. As can be seen in the equation, this is notable because reduction in the operating voltage reduces power losses not linearly, but instead *exponentially*- due to the voltage squared term (V^2). It is also notable that when operated at high output levels, FHD modes also offers unique improvement in output filter losses, due to reducing the switching frequency (f) at higher output levels.

5.4 Power-Up and Power-Down

When pulled to a logic low state, the \overline{SD} pin tristates the outputs and shuts down the CS35L00 device, putting it into a low power mode.

5.4.1 Recommended Power-Up Sequence

1. With the \overline{SD} pin pulled low, apply power to the CS35L00 and wait for the power supply to be stable.
2. Set the \overline{SD} pin high to begin normal operation.

5.4.1.1 Zero Crossing on Power-Up Functionality

The CS35L00 implements an input-signal zero-crossing detection function that is enabled during power-up. This function is designed to prevent audible artifacts and eliminate any need to mute the amplifier's input audio signal during the power-up process.

After a minimum start-up time of t_{start} , the CS35L00 will begin to detect input-signal zero-crossings. The amplifier will then enable its switching outputs at the time of the first detected input-signal zero-crossing transition. If no input-signal zero-crossing is detected before $t_{timeout}$, the zero-crossing function will time-out and the outputs will begin switching immediately.

Both t_{start} and $t_{timeout}$ are specified in ["Power-Up & Power-Down Characteristics"](#) on page 14.

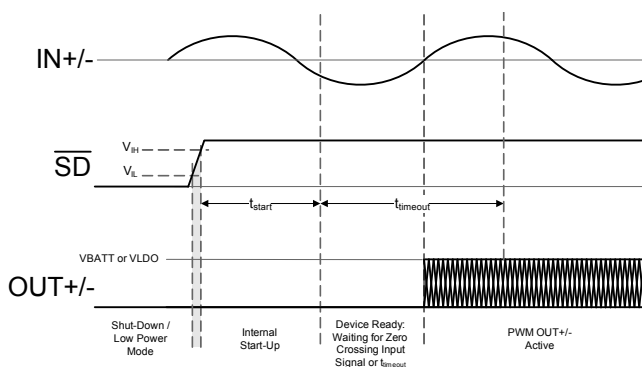


Figure 6. Power-Up Timing with Input Zero-Crossing

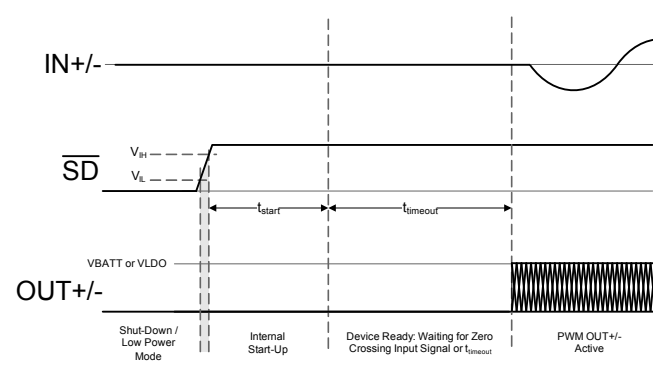


Figure 7. Power Up Timing without Input Zero-Crossing

5.4.2 **Recommended Power-Down Sequence**

1. Mute the audio supplied to the CS35L00.
2. Pull the \overline{SD} pin low in order to reset the device and put it into the low power mode.
3. The power supply to the CS35L00 can now be removed.

5.5 **Over Temperature Protection**

The CS35L00 is internally protected against thermal overload. Built in die temperature sensing circuitry monitors the die temperature and will place the device into shut-down if thermal overload occurs. A thermal overload is characterized by the die temperature reaching the Thermal Error Threshold (T_{TE}) at which time the outputs will tristate and shut down.

If the device has entered into shut-down due to a thermal overload, the die temperature must remain below the Thermal Error Threshold (T_{TE}) for the time specified by the Thermal Error Retry Time (R_{TE}) in order for the device to automatically return to normal operation.

Both T_{TE} and R_{TE} are specified in [“Electrical Characteristics - All Operational Modes” on page 9](#).

6. TYPICAL PERFORMANCE PLOTS

Test Conditions (unless otherwise specified): GND = 0 V; All voltages with respect to ground; $A_V = 6$ dB; Input signal = 997 Hz differential sine wave; $T_A = 25^\circ\text{C}$; VBATT = 5.0 V; $R_L = 8 \Omega$; 10 Hz to 20 kHz measurement bandwidth; Measurements taken with AES17 measurement filter and Audio Precision AUX-0025 passive filter.

6.1 SD Mode Typical Performance Plots

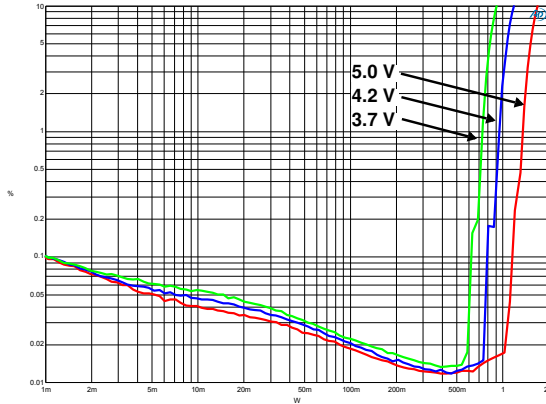


Figure 8. THD+N vs. Output Power - SD Mode
 $R_L = 8 \Omega$

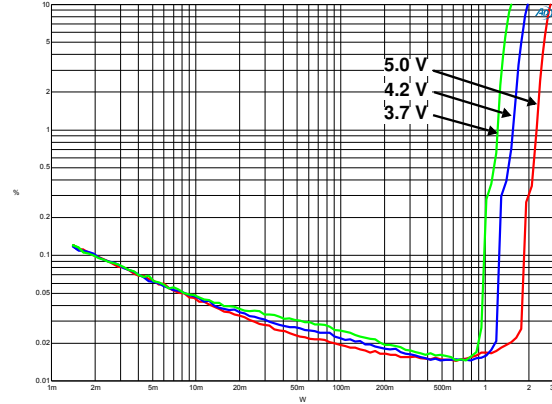


Figure 9. THD+N vs. Output Power - SD Mode
 $R_L = 4 \Omega$

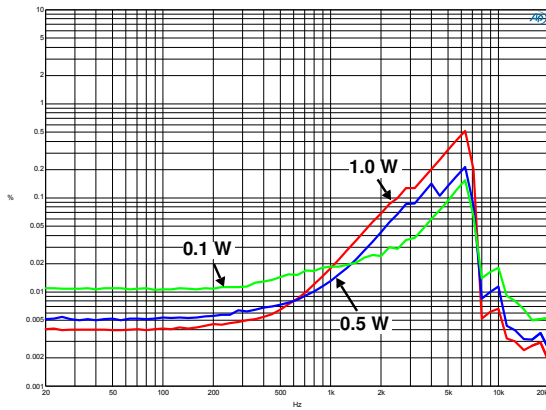


Figure 10. THD+N vs. Frequency - SD Mode
VBATT = 5.0 V

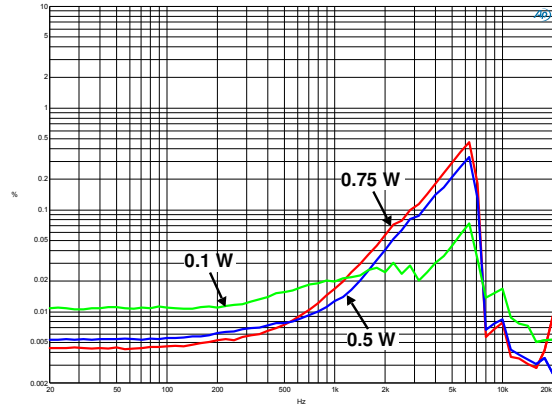


Figure 11. THD+N vs. Frequency - SD Mode
VBATT = 4.2 V

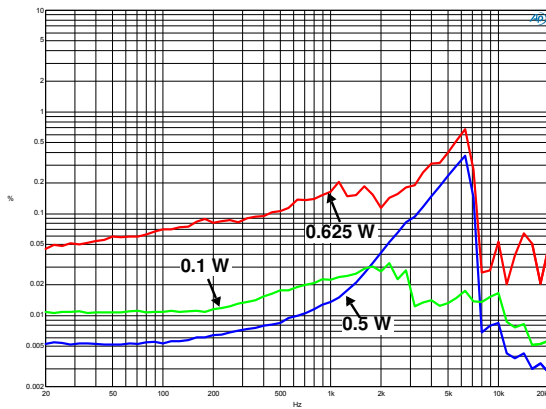


Figure 12. THD+N vs. Frequency - SD Mode
VBATT = 3.7 V

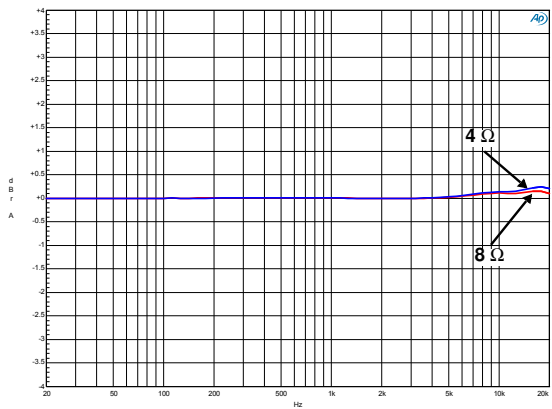


Figure 13. Frequency Response - SD Mode

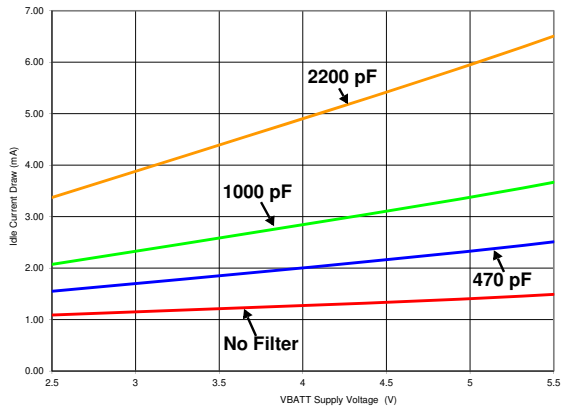


Figure 14. Idle Current Draw vs. VBATT - SD Mode
 $R_L = 8 \Omega + 33 \mu H$ (Note 16)

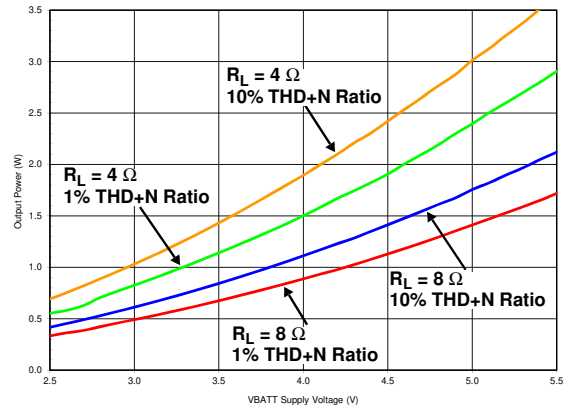


Figure 15. Output Power vs. VBATT - SD Mode

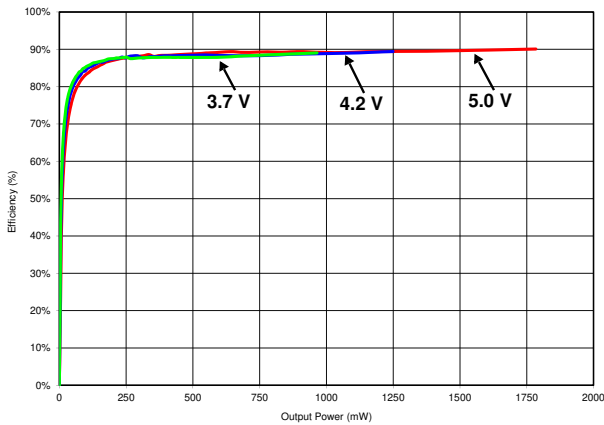


Figure 16. Efficiency vs. Output Power - SD Mode
 $R_L = 8 \Omega + 33 \mu H$

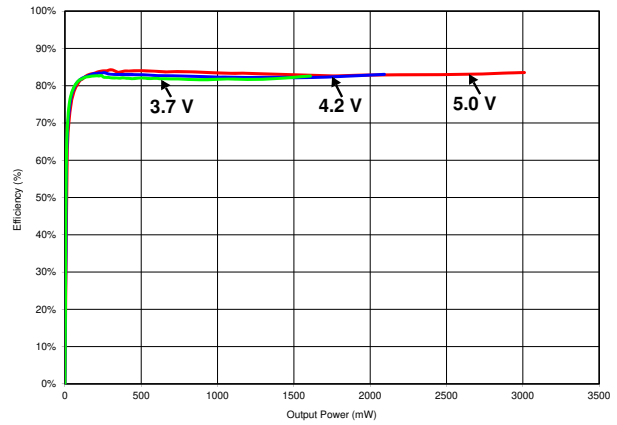


Figure 17. Efficiency vs. Output Power - SD Mode
 $R_L = 4 \Omega + 33 \mu H$

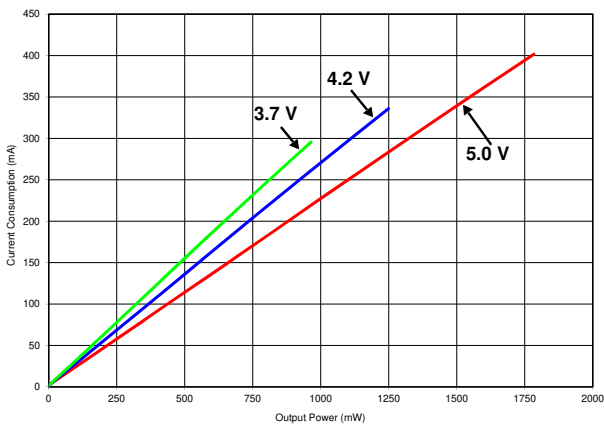


Figure 18. Supply Current vs. Output Power - SD Mode
 $R_L = 8 \Omega + 33 \mu H$

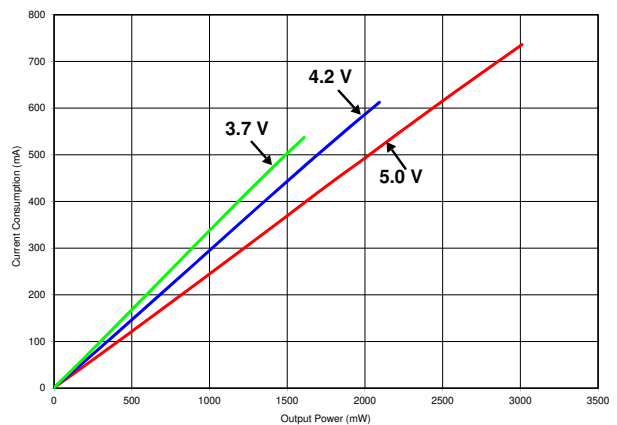


Figure 19. Supply Current vs. Output Power - SD Mode
 $R_L = 4 \Omega + 33 \mu H$

Note:

16. "Idle Current Draw vs. VBATT - SD Mode" capacitor values refer to C_{FILT} when configured as the "CS35L00's Minimized Optional Output Filter", shown in Figure 5 on page 17.

6.2 FSD Mode Typical Performance Plots

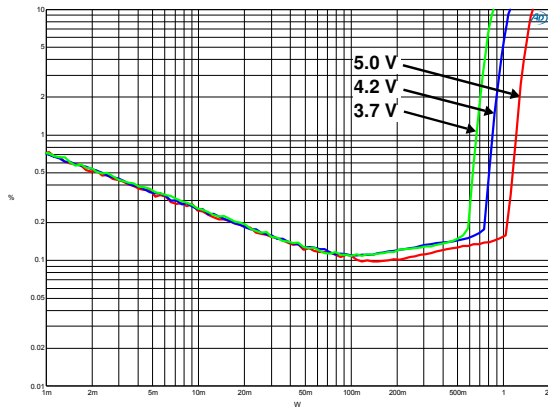


Figure 20. THD+N vs. Output Power - FSD Mode
 $R_L = 8 \Omega$

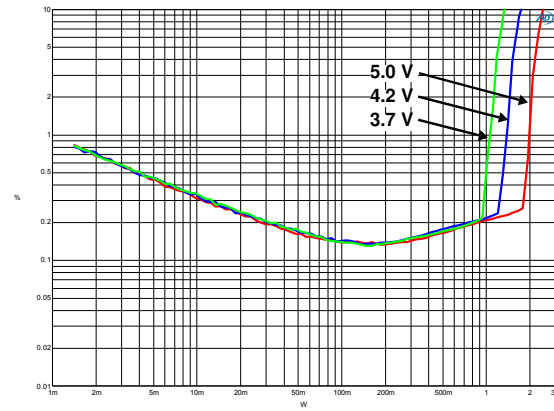


Figure 21. THD+N vs. Output Power - FSD Mode
 $R_L = 4 \Omega$

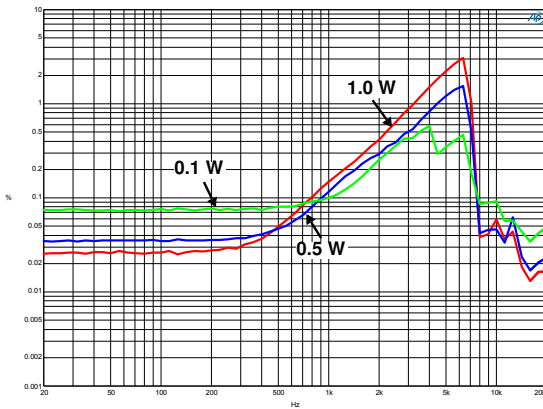


Figure 22. THD+N vs. Frequency - FSD Mode
 $V_{BATT} = 5.0 V$

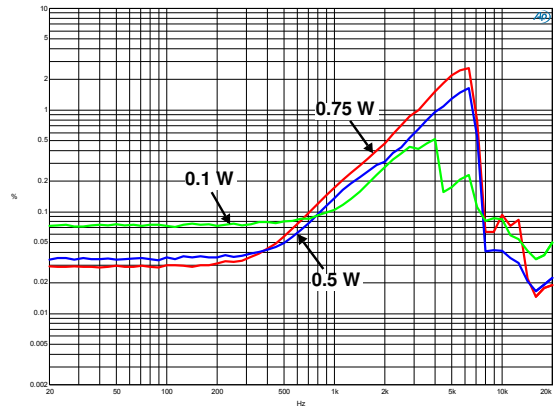


Figure 23. THD+N vs. Frequency - FSD Mode
 $V_{BATT} = 4.2 V$

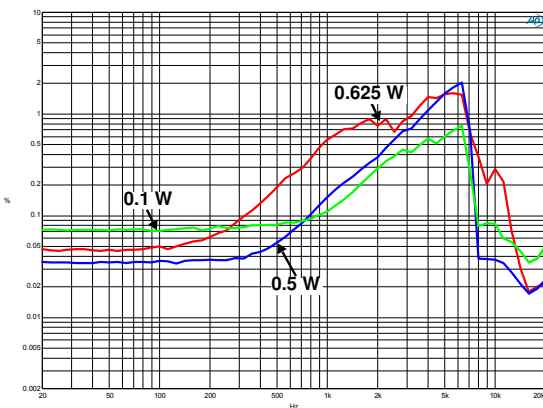


Figure 24. THD+N vs. Frequency - FSD Mode
 $V_{BATT} = 3.7 V$

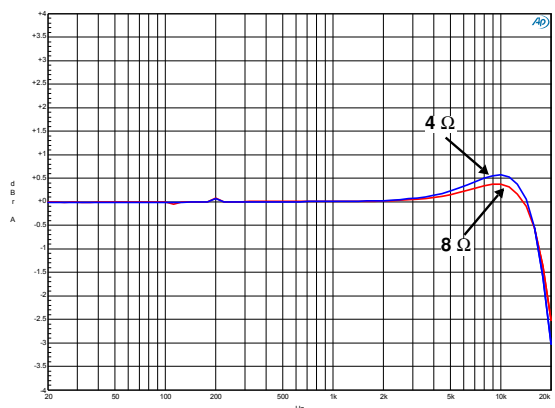


Figure 25. Frequency Response - FSD Mode

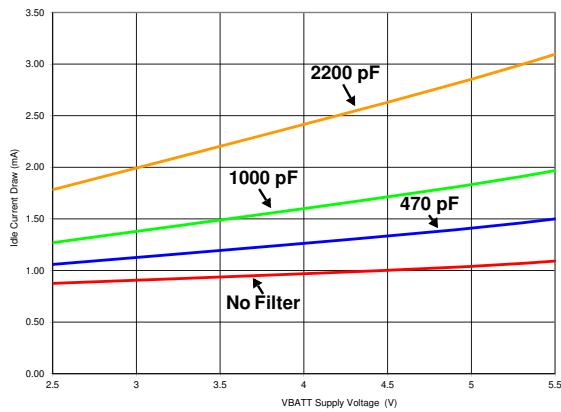


Figure 26. Idle Current Draw vs. VBATT - FSD Mode
 $R_L = 8 \Omega + 33 \mu H$ (Note 17)

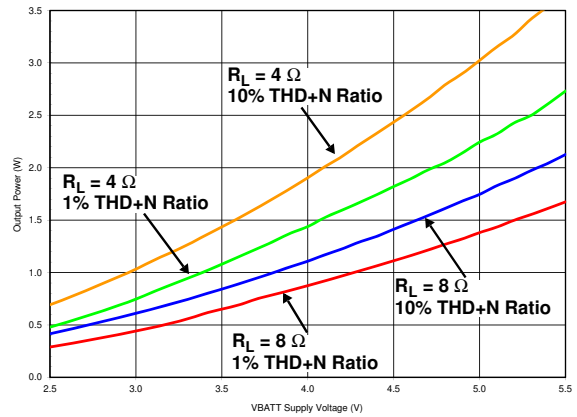


Figure 27. Output Power vs. VBATT - FSD Mode

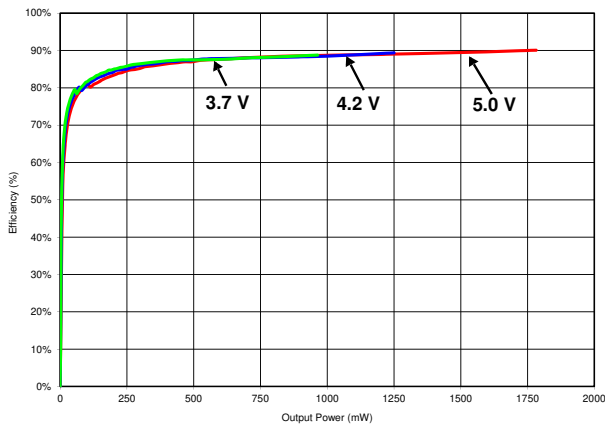


Figure 28. Efficiency vs. Output Power - FSD Mode
 $R_L = 8 \Omega + 33 \mu H$

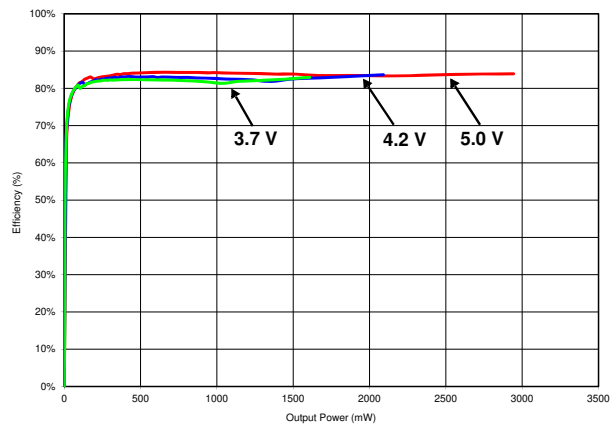


Figure 29. Efficiency vs. Output Power - FSD Mode
 $R_L = 4 \Omega + 33 \mu H$

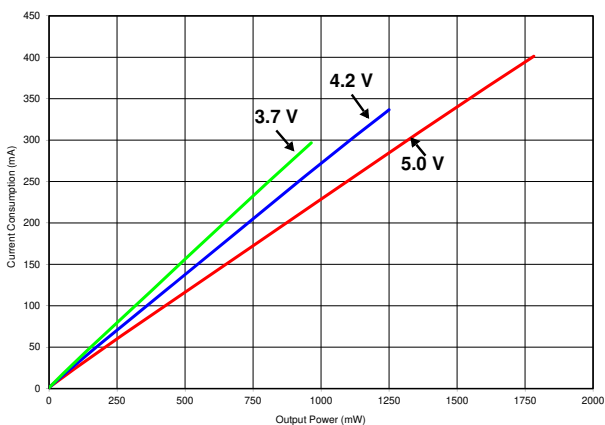


Figure 30. Supply Current vs. Output Power - FSD Mode
 $R_L = 8 \Omega + 33 \mu H$

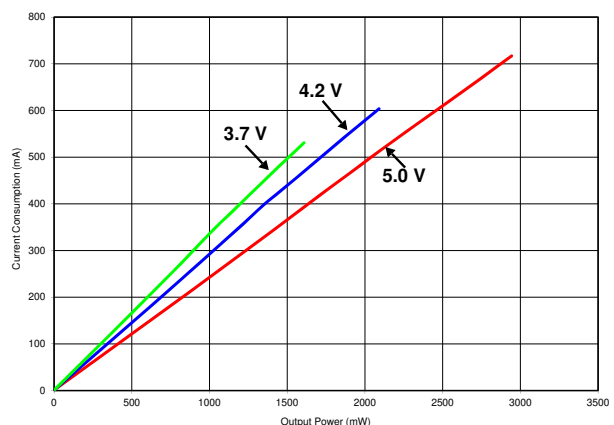


Figure 31. Supply Current vs. Output Power - FSD Mode
 $R_L = 4 \Omega + 33 \mu H$

Note:

- “Idle Current Draw vs. VBATT - FSD Mode” capacitor values refer to C_{FILT} when configured as the “CS35L00’s Minimized Optional Output Filter”, shown in [Figure 5 on page 17](#).

6.3 HD Mode Typical Performance Plots

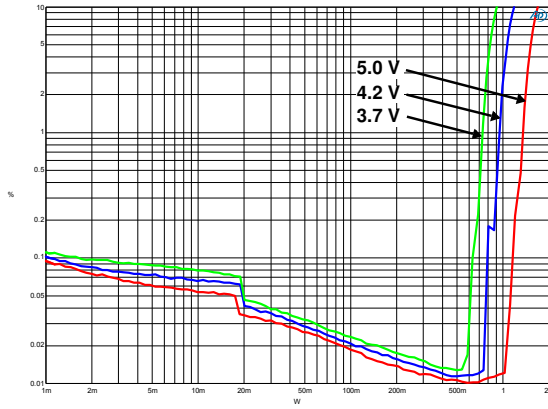


Figure 32. THD+N vs. Output Power - HD Mode
 $R_L = 8 \Omega$

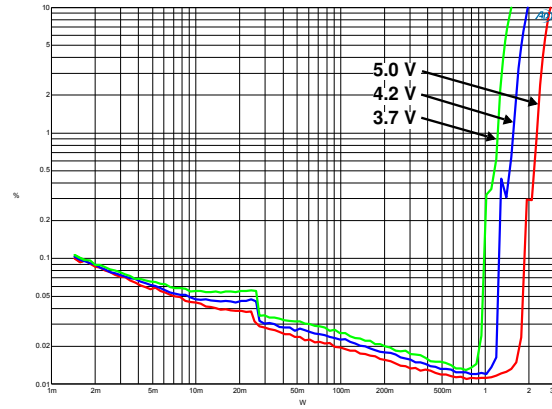


Figure 33. THD+N vs. Output Power - HD Mode
 $R_L = 4 \Omega$

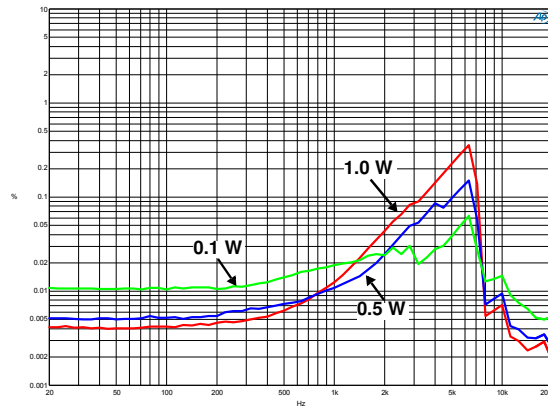


Figure 34. THD+N vs. Frequency - HD Mode
 $V_{BATT} = 5.0 V$

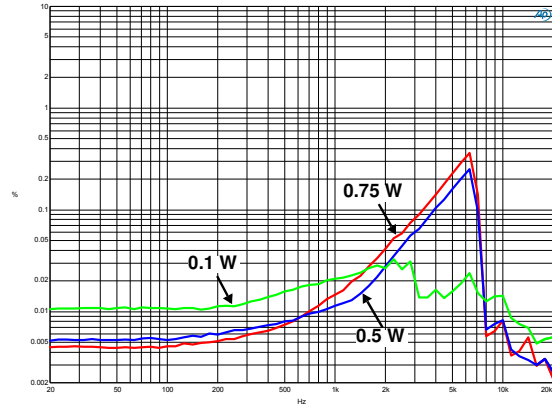


Figure 35. THD+N vs. Frequency - HD Mode
 $V_{BATT} = 4.2 V$

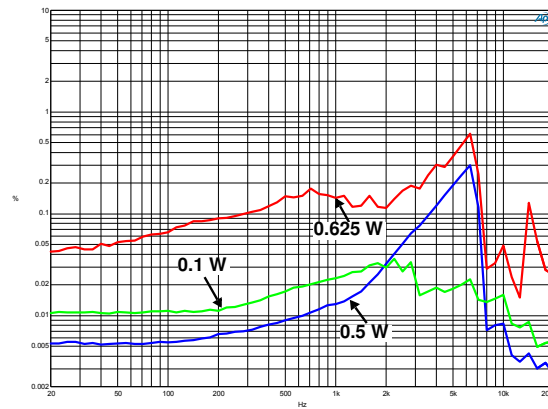


Figure 36. THD+N vs. Frequency - HD Mode
 $V_{BATT} = 3.7 V$

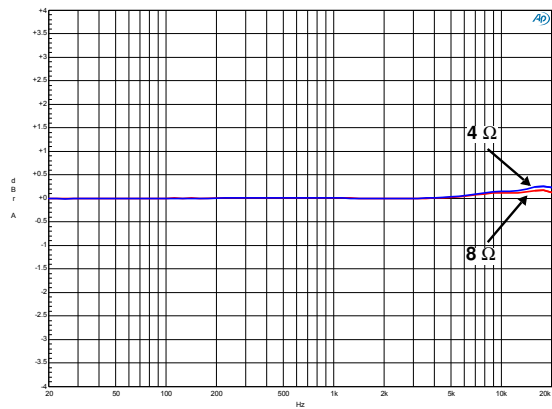


Figure 37. Frequency Response- HD Mode