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Boosted Class D Amplifier with Speaker-Protection Monitoring and Flash LED Drivers

Mono Class D Speaker Amplifier

- Two-level Class G operation:
  - Boosted: 5 V nominal
  - Bypassed: battery voltage is supplied directly
- 2.5-mA quiescent current, monitors powered down
- 1.7 W into 8 Ω (@ 10% THD+N)
- 102-dB signal-to-noise ratio (SNR, A-weighted)
- Idle channel noise 25 μVrms (A-weighted)
- 90% efficiency

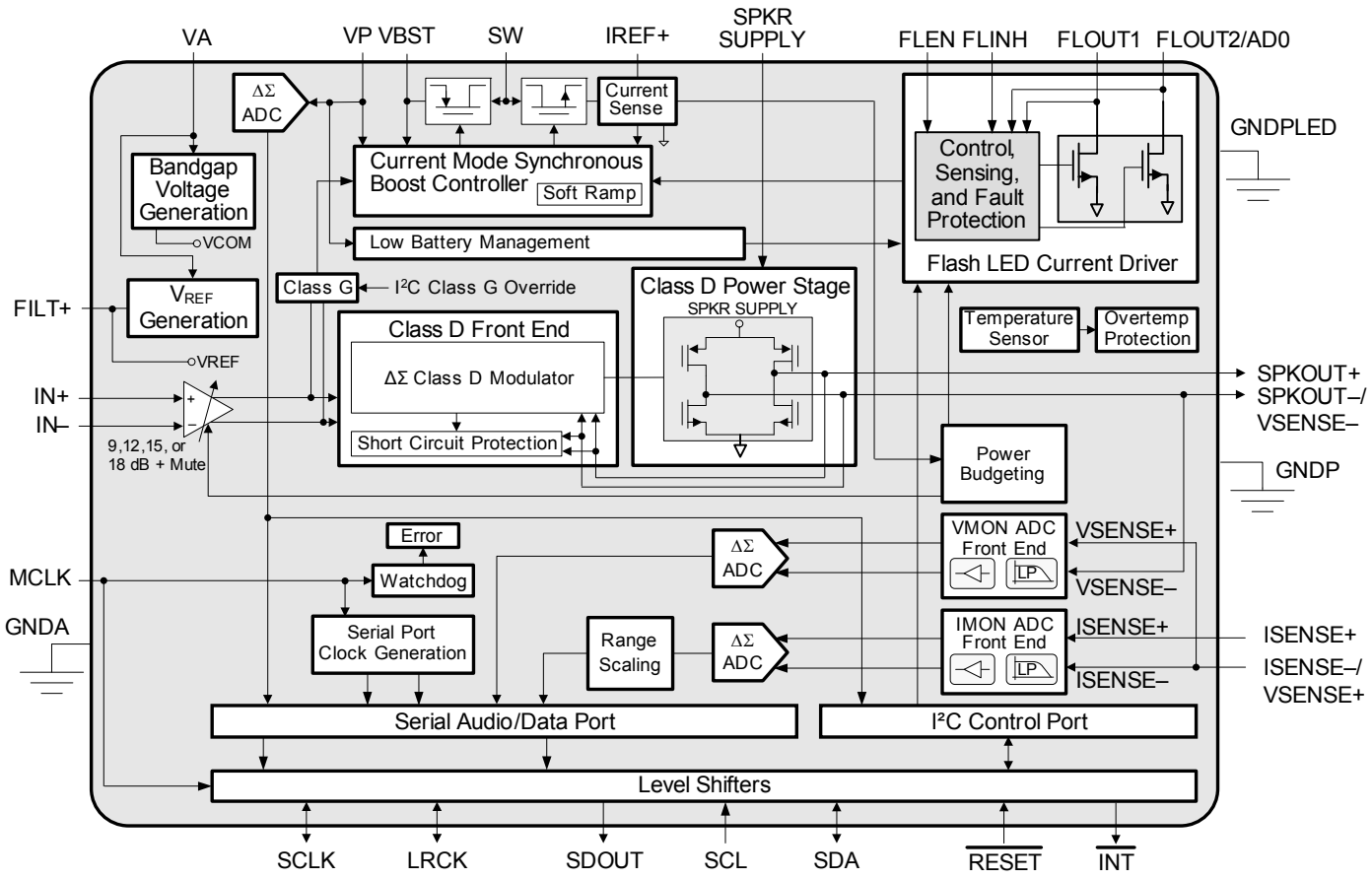
Audio Input and Gain

- One differential analog input
- Speaker gain:
  - 9, 12, 15, and 18 dB and mute
  - Pop suppression, zero-crossing detect transitions

Flash LED Drivers

- Integrated dual LED drivers using the following:
  - Boost supply output voltage
  - Dual matched current regulators, 750 mA max each
- Programmable setting for Flash Mode current: 50–750 mA, in 50-mA steps
- Programmable setting for Flash-Inhibit Mode current: 50–350 mA, in 50-mA steps
- Programmable setting for Movie Mode current: 150, 120, 100, 80, 60, 40, 20 mA
- Programmable flash timer setting: 50–500 ms, in 25-ms steps
- Dedicated pin for flash trigger (FLEN)
- Dedicated pin for flash inhibit (FLINH)
- Thermally managed through boost-voltage regulation

(**Features** continue on page 2)



Monitors and Protection

- Protection:
  - Latched overtemperature shutdown
  - Latched amplifier output short circuit shutdown
  - LED short or open detection and LED driver shutdown
  - Flash inhibit LED current reduction
  - Low battery flash LED current reduction
  - VP undervoltage lockout (UVLO) shutdown
  - Programmable boost inductor current limiting
  - Audio and LED shutdown upon stopped MCLK, with autorecovery
  - Interrupt driven error reporting
- Speaker current and voltage monitoring:
  - 16-bit resolution
  - 60-dB dynamic range (unweighted) for voltage
  - 56-dB dynamic range (unweighted) for current
  - Bused over I²S bus
- Battery voltage monitoring:
  - 7-bit resolution
  - Bused over I²S and I²C bus
- System reset

I²C Control Settings and Registers

- Low-power standby
- LED and audio power budgeting programmable settings
- Boost inductor current limit programmable setting
- Speaker programmable settings:
  - Pop suppression through zero-crossing transitions
  - Gain and mute
- Battery voltage monitor register, 8 bits
- LED driver programmable settings:
  - Flash current register
  - Flash inhibit current register
  - Movie Mode current register
  - Flash timer register
- Error status bit, including the following:
  - Stopped MCLK error
  - Low battery detection with programmable thresholds
  - VP UVLO error
  - Overtemperature warning
  - Overtemperature error
  - Boost converter overvoltage error
  - Boost inductor current-limiting error
  - Amplifier short-circuit error
  - Shorted or open LED error

I²S Reporting

- Monitoring:
  - Speaker voltage monitor
  - Speaker current monitor
  - Battery voltage monitor
- Error reporting:
  - VP UVLO shutdown error
  - Overtemperature warning
  - Overtemperature error
  - Boost converter overvoltage error
  - Boost inductor current limiting error
  - Amplifier short-circuit error
  - Speaker voltage monitor overflow error
  - Speaker current monitor overflow error
  - Battery voltage monitor overflow error
- Status reporting:
  - Power-down done
  - LED flash event
  - LED Movie Mode event
  - Flash timer on

Package

- 30-ball WLCSP

Applications

- Smart phones
- Tablets

General Description

The CS35L32 is a low-quiescent power-integrated audio IC, with a mono full-bridge Class D speaker amplifier operating with a self-boosted Class G supply. Audio input is received differentially. Pop-and-click reduction is achieved with zero-crossing transitions at turn-on, turn-off and upon gain changes. Communication with the host processor is done using an I²C interface. In addition, an I²S bus is used to send monitor and status data.

When two CS35L32 devices are available on the same board, each is identified by its I²C chip address. Upon power-up or upon deasserting $\overline{\text{RESET}}$, each CS35L32 reads the AD0 pin logic level and configures its I²C device address.

The speaker amplifier, using closed-loop $\Delta\Sigma$ modulation, achieves low levels of distortion. Class D amplifier efficiency allows operation at higher speaker power levels without generating excessive heat and without wasting power. Automatic Class G operation using a boosted supply to the speaker allows for even higher powers and higher crest factor. With a boosted speaker supply, operation at a fixed 5 V is achieved independently of line supplied battery voltage. The user can disable Class G operation.

The battery voltage, speaker voltage, and speaker current signals are monitored, digitized using ΔΣ converters, and serialized over an I²S bus. The speaker monitoring signals are part of a speaker-protection algorithm that is managed externally to the CS35L32. Outgoing data is sent over I²S with the CS35L32 in Slave or Master Mode. Battery voltage monitor data is accessible through I²C.

An integrated dual LED driver operates up to two LEDs in Flash Mode or Movie Mode. A flash event is triggered by an external signal. A flash-inhibit event is triggered by an external signal, and causes a reduction in flash current. A timer is provided for flash and flash inhibit events. Movie Mode operation has no timer and starts and ends via an I²C command. Flash and Movie Mode current levels, as well as the flash timer are I²C programmable.

Total power consumption when powering LEDs in Flash Mode or Movie Mode, and powering audio simultaneously, is managed by the user's choices in programming the current limit and in power budgeting. The primary goal is to manage audio and LED loads so the boost converter is not current limited and so the CS35L32 does not shut down due to overheating.

A latched shutdown of the audio amplifier occurs in the event of an output short pin to ground, pin to supply, or pin to pin. A latched shutdown of the CS35L32 also occurs on overtemperature. An LED driver shutdown occurs in the event of a shorted or open LED. The CS35L32 shuts down in the event of a battery (VP) undervoltage and autorecovers when the battery voltage recovers. The CS35L32 shuts down in the event of a stopped MCLK and autorecovers when MCLK recovers.

The CS35L32 responds to detection of a low battery in the presence of a flash event by reducing flash current and autorecovers when the battery voltage recovers.

The CS35L32 is reset by asserting $\overline{\text{RESET}}$. CS35L32 power up and power down are managed through the $\overline{\text{RESET}}$ pin.

The CS35L32 is available in a 30-ball WLCSP package in the temperature range –10 to +70°C.

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1 Pin Descriptions

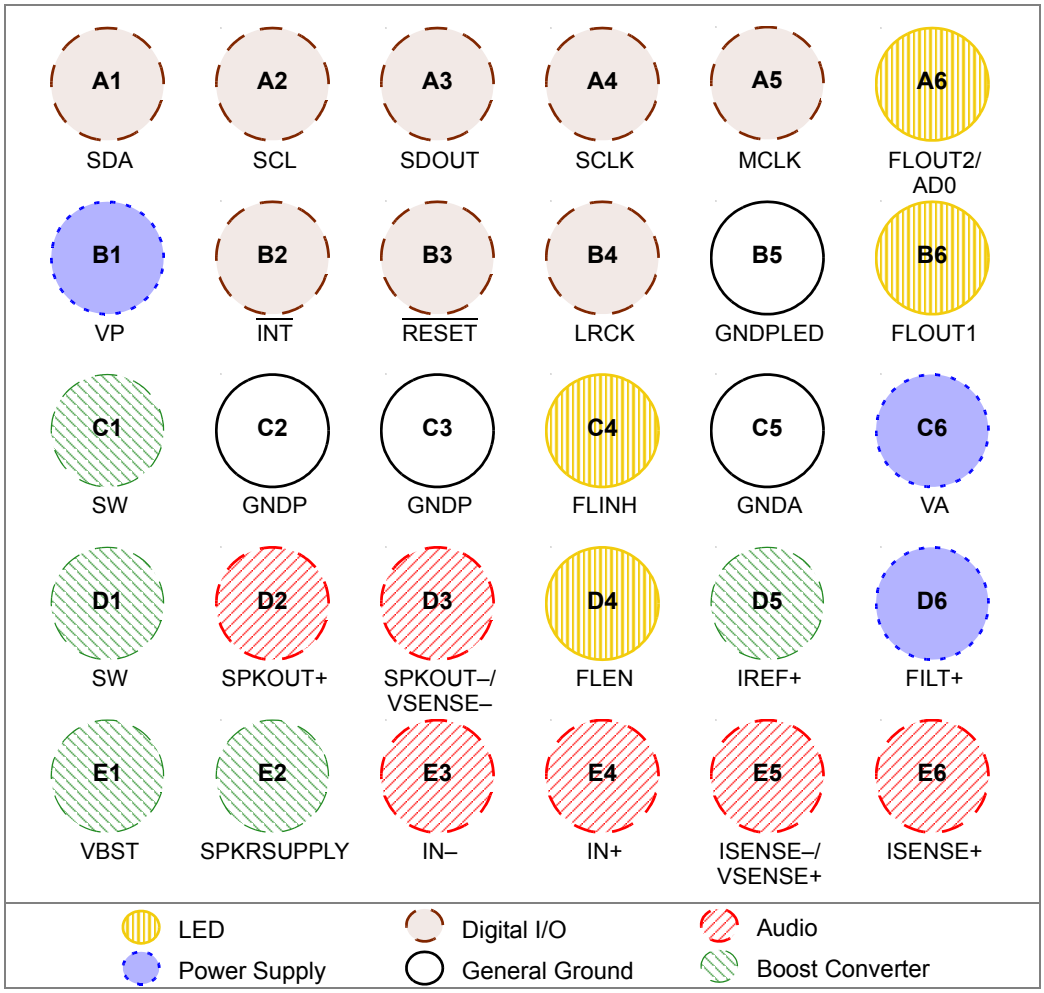


Figure 1-1. Top-Down (Through-Package) View—30-Ball WLCSP Package

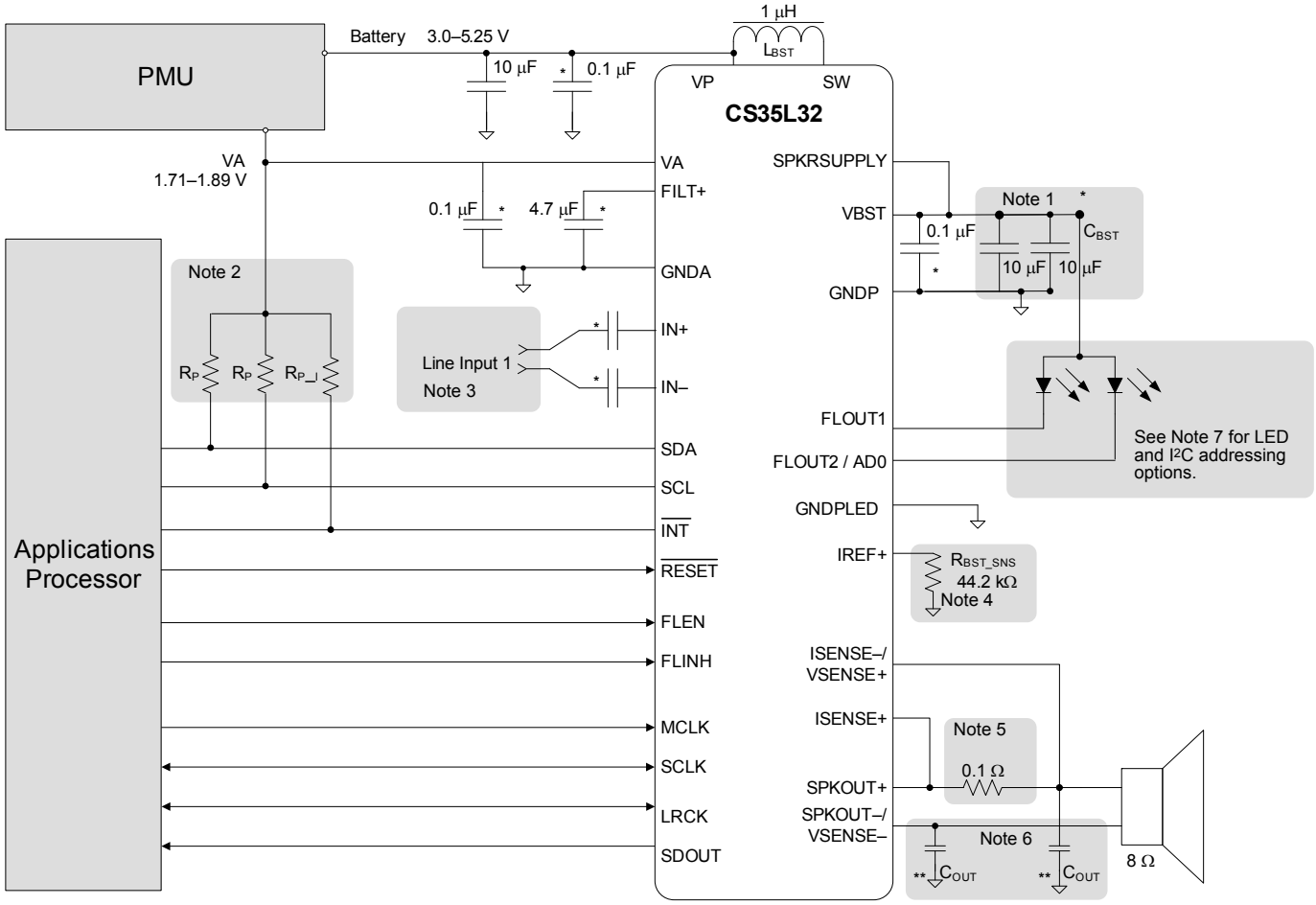
Table 1-1. Pin Descriptions

Ball Name	Ball Number	Power Supply	I/O	Ball Description	Internal Connection	Driver	Receiver	State at Reset
				Digital I/O				
SDA	A1	VA	I/O	**I²C Serial Data Input.** Serial data for the I²C serial port	—	CMOS open-drain output	Hysteresis on CMOS input	Hi-Z
SCL	A2	VA	I	**I²C Clock Input.** Serial clock for the I²C serial port	—	—	Hysteresis on CMOS input	Hi-Z
MCLK	A5	VA	I	**Master Clock Source.** Clock source for A/D converters and audio/data serial port (ADSP). $MCLK_{INT}$, derived from MCLK, is used for other blocks (see Section 4.13 and Section 7.7).	Weak pull-down (~1 MΩ)	—	Hysteresis on CMOS input	Pulled down
SCLK	A4	VA	I/O	**Serial Clock.** Serial shift clock for the serial audio interface	Weak pull-down (~1 MΩ)	CMOS output	Hysteresis on CMOS input	Pulled down
LRCK	B4	VA	I/O	**Left Right Clock.** Determines which channel, left or right, is currently active on the serial audio/data lines	Weak pull-down (~1 MΩ)	CMOS output	Hysteresis on CMOS input	Pulled down
SDOUT	A3	VA	O	**Serial Audio/Data Output.** I²S serial data output used to monitor voltage and current of SPKOUT signal and VP levels	Weak pull-down (~1 MΩ)	CMOS output	—	Pulled down
$\overline{INT}$	B2	VA	O	**Interrupt.** Programmable, open-drain, active-low programmable interrupt output	—	CMOS open-drain output	—	Hi-Z

Table 1-1. Pin Descriptions *(Cont.)*

Ball Name	Ball Number	Power Supply	I/O	Ball Description	Internal Connection	Driver	Receiver	State at Reset
$\overline{\text{RESET}}$	B3	VA	I	**Reset.** When asserted, the device enters a low-power mode, outputs are set to Hi-Z, and I²C register values are set to defaults. Outputs are Hi-Z except those with weak pull-ups or pull-downs as mentioned.	—	—	Hysteresis on CMOS input	Low
				LED				
FLEN	D4	VA	I	**Flash Enable.** Input signal commanding a flash event into both LEDs. It is asserted high.	Weak pull-down (~1 MΩ)	—	Hysteresis on CMOS input	Pulled down
FLINH	C4	VA	I	**Flash Inhibit.** Input signal determining whether the LEDs are in Flash Mode (logic low) or Flash-Inhibit Mode (logic high, LED current reduced).	Weak pull-down (~1 MΩ)	—	Hysteresis on CMOS input	Pulled down
FLOUT1	B6	SPKR SUPPLY	O	**LED Driver 1.** Output driving LED 1 by sinking current from the LED cathode	Weak pull-up (~1 MΩ)	—	—	SPKR SUPPLY
FLOUT2/AD0	A6	SPKR SUPPLY	I/O	**LED Driver 2/Address Zero.** Output driving LED 2 by sinking current from the LED cathode. AD0 programs the chip address when $\overline{\text{RESET}}$ is deasserted. If no LED is used, tying the pin to ground clears the chip address LSB. Otherwise, the LSB is set.	Weak pull-up (~1 MΩ)	—	—	SPKR SUPPLY
				Boost Converter				
VBST	E1	—	O	**Boost Converter Output.** Output of boosted supply. This pin cannot be used to drive any external loads other than the on chip Class D Amplifier and Flash LEDs.	—	—	—	—
SPKRSUPPLY	E2	—	I	**Speaker Supply.** Full-bridge Class D speaker amplifier power supply.	—			—
SW	C1, D1	VBST	I	**Boost Converter Switch Node.** Connects the inductor to the rectifying switch.	—	—	—	—
IREF+	D5	VA	I	**Current Reference Resistor.** Connection for an external resistor to be used for generating the CS35L32's internal main current reference. See Fig. 2-1 for required resistor value.	—	—	—	—
				Audio				
IN+	E4	SPKR SUPPLY	I	**Input 1 Differential Positive Line.** Positive analog input	—	—	—	—
IN–	E3	SPKR SUPPLY	I	**Input 1 Differential Negative Line.** Negative analog input	—	—	—	—
SPKOUT+ SPKOUT–/VSENSE–	D2 D3	SPKR SUPPLY	O	**Speaker Differential Audio Output.** Internal Class D speaker amplifier output. SPKOUT– serves as voltage monitor negative sense pin (VSENSE–).	—	—	—	Hi-Z
ISENSE+ ISENSE–/VSENSE+	E6 E5	SPKR SUPPLY	I	**Current Sense Inputs.** Sense voltage across an external resistor in series with SPKOUT+. ISENSE– serves as voltage monitor positive sense pin (VSENSE+).	—	—	—	—
				Power Supply				
FILT+	D6	VA	O	**Positive Voltage Reference.** Positive reference for internal circuits	—	—	—	—
VA	C6	—	I	**Analog Input Power.** Power supply for internal analog section	—	—	—	—
VP	B1	—	I	**Boost Converter Input Power.** Power supply or battery voltage powering boost converter	—	—	—	—
				General Ground				
GNDA	C5	—		**Analog Ground.** Ground reference for the internal analog section of the IC	—	—	—	—
GNDP	C2, C3	—		**Power Ground.** Ground reference for boost converter and Class D amplifier's output stage	—	—	—	—
GNDPLED	B5	—		**LED Power Ground.** Ground reference for LED current return. Should be tied to ground plane.	—	—	—	—

2 Typical Connection Diagram



Notes:

- All external passive component values are nominal values.
  Key for capacitor types required:
  * Use low ESR, X7R/X5R capacitors.
  ** Use low ESR, X7R capacitors.
  If no type symbol is shown next to a capacitor, any type may be used.
- As required, add protection circuitry to ensure compliance with the absolute maximum ratings in Table 3-2.

1. C_{BST} is a ceramic capacitor and derates at DC voltages higher than 0 V. In this application, the capacitor should not derate to a value lower than 4 µF across the specified boost output voltage in Table 3-4. Capacitor tolerance and the temperature coefficient should also be taken into account to guarantee the 4-µF value.
2. Minimum pull-up resistor values are selected in accordance with the Table 3-8 V_{OL} specification. Maximum pull-up resistances are selected based on load capacitance and relevant switching specs (Table 3-13).
3. Select each capacitor to be 0.22 µF for an 18-Hz passband @ 12-dB amplifier gain, for a 3-dB roll-off. The equation for calculating the capacitance for a given passband is $C = 1/(\pi * f * R_{INDIF})$, where C is in F, R_{INDIF} is the differential input resistance in Ω, and f is in Hz (see the differential input resistance specification in Table 3-3). Signals IN+ and IN– are subject to the recommended ranges in Table 3-1.
4. R_{BST_SNS} is inherently tied to the accuracy of the BST_IPK current limit. A resistor with a 0.1% tolerance is required for this component to meet the specified IMAX(B) max and min values in Table 3-4.
5. The required tolerance on the 0.1-Ω ISENSE resistor is 1%. The required temperature coefficient is ±200 ppm/°C.
6. C_{OUT} capacitors are optional EMI suppressors used with CS35L32 edge-rate control, depending on application requirements. Because switching losses increase linearly with increases to these capacitances, it is recommended that C_{OUT} values not exceed 2 nF. The recommended value is 470 pF.
7. LED and I²C addressing options:

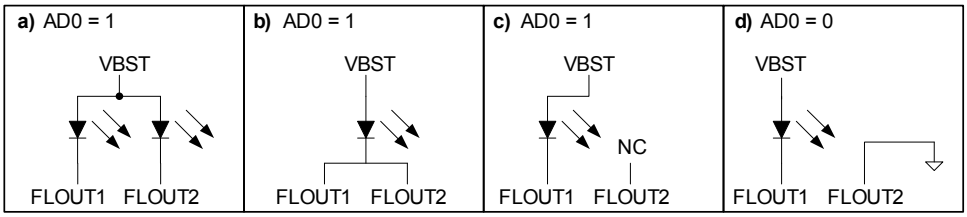


Figure 2-1. Typical Connection Diagram

3 Characteristics and Specifications

Table 3-1. Recommended Operating Conditions

GNDA = GNDP = 0 V, all voltages with respect to ground. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

Parameters		Symbol	Minimum	Maximum	Units
DC power supply	Analog (and digital I/O and core)	VA	1.71	1.89	V
	Battery	VP	3.0	5.25	V
External voltage applied to analog inputs powered by VA (IREF+, FILT+) [1]		V_{INAS}	–0.3	VA + 0.3	V
External voltage applied to analog inputs powered by SPKRSUPPLY (IN+, IN–, ISENSE+, ISENSE–,VSENSE+, VSENSE–)		V_{INSS}	–0.3	SPKRSUPPLY + 0.3	V
External voltage applied to digital inputs		V_{INDI}	–0.3	VA + 0.3	V
Ambient temperature		TA	–10	+70	°C

1. The maximum overvoltage/undervoltage is limited by the input current.

Table 3-2. Absolute Maximum Ratings

GNDA = GNDP = 0 V; all voltages with respect to ground. Operation at or beyond these limits may permanently damage the device.

Parameters		Symbol	Minimum	Maximum	Units
DC power supply	Analog	VA	–0.3	2.22	V
	Battery	VP	–0.3	6.0	V
Input current [1]		I_{IN}	—	±10	mA
Ambient operating temperature (local to device, power applied)		T_A	–40	+115	°C
Junction operating temperature (power applied)		T_J	–40	+150	°C
Storage temperature		T_{STG}	–65	+150	°C

1. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins do not cause SCR latch up.

Table 3-3. DC Characteristics

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = 5.0 V, GNDA = GNDP = 0 V, TA = +25°C.

Parameters	Symbol	Test Conditions	Min	Typical	Max	Units
Differential Input resistance (IN+ to IN–)	R_{INDIF}	Amp gain = 9 dB	—	63	—	kΩ
		Amp gain = 12 dB	—	51	—	kΩ
		Amp gain = 15 dB	—	40	—	kΩ
		Amp gain = 18 dB	—	31	—	kΩ
FILT+ voltage	—	—	—	VA	—	—
Overtemperature shutdown threshold	T_{OP}	—	—	150	—	°C
Overtemperature warning threshold	T_{WRN}	—	—	135	—	°C
Overtemperature warning threshold deviation	—	—	—	±10	—	°C
Low battery threshold	—	LOWBAT_TH = 00	—	3.10	—	V
		LOWBAT_TH = 01	—	3.20	—	V
		LOWBAT_TH = 10	—	3.30	—	V
		LOWBAT_TH = 11	—	3.40	—	V
Low-battery recovery threshold	—	LOWBAT_RECOV = 001	—	3.20	—	V
		LOWBAT_RECOV = 010	—	3.30	—	V
		LOWBAT_RECOV = 011	—	3.40	—	V
		LOWBAT_RECOV = 100	—	3.50	—	V
		LOWBAT_RECOV = 101–11x	—	3.60	—	V
VP undervoltage lockout threshold (VP falling)	UVLO	—	—	2	—	V
VP undervoltage lockout hysteresis	—	—	—	100	—	mV

Table 3-4. Boost Converter Characteristics

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = 5.0 V, amp gain = 12 dB, GNDA = GNDP = 0 V, TA = +25°C, $MCLK_{INT}$ = 6 MHz. $MCLK_{INT}$ is explained in Section 4.13.1 and Section 7.7.

Parameters	Symbol	Test Conditions	Min	Typical	Max	Units
Boost output voltage	VBST	Boosting Bypass	VP*1.15 —	— VP	5.4 —	V V
Boost output voltage tolerance	ΔVBST	No load: I_{LOAD} =0 mA	–5	—	+5	%
Load regulation	$\Delta V_{(Load)}$	3.0 V < VP < 4.2 V; I_{LOAD}= 0.25A to1.5 A	—	60	—	mV/A
Line regulation	$\Delta V_{(Line)}$	3.0 V<VP<4.2 V; I_{LOAD} = 0 A, 500 mA	—	40	—	mV/V
Boost FET peak-current limit (See Section 7.10.)	$I_{MAX(B)}$	BST_IPK = 0000 0000 BST_IPK = 0010 0000 BST_IPK = 0100 0000 BST_IPK = 0110 0000 BST_IPK = 1000 0000	— — — — —	2.89 3.30 3.72 4.14 4.56	— — — — —	A A A A A
Output switching frequency [1]	$f_{SW(B)}$	—	—	$MCLK_{INT}$/3	—	MHz
Boost FET ON resistance	$R_{DS(ON)B}$	$I_{OUT(B)}$ = 1 A	—	80	—	mΩ
Boost FET ON resistance temp coefficient	—	$I_{OUT(B)}$ = 1 A	—	0.2	—	%/°C
Rectifying FET ON resistance	$R_{DS(ON)R}$	$I_{OUT(B)}$ = 1 A	—	150	—	mΩ
Rectifying FET ON resistance temp coefficient		$I_{OUT(B)}$ = 1 A	—	0.2	—	%/°C
Overvoltage detection threshold	V_{OVTH}	Boost enabled	—	5.5	5.7	V
Threshold Class G On, IN+ to IN–	$V_{IN1THON}$	VBST = VP = 3.6 V	—	0.60	—	V
Threshold Class G Off, IN+ to IN–	$V_{IN1THOF}$	VP = 3.6 V, VBST = 5 V	—	0.33	—	V
Minimum Class G boost ON hold-off time	—	VP = 3.6 V, VBST = 5 V	—	800[2]	—	ms
Operating efficiency [3]	η_B	VBST = 5 V, $I_{OUT(B)}$ = 500 mA VBST = 5 V, $I_{OUT(B)}$ = 1.5 A	— —	90 85	— —	% %

1. MCLKDIV2 (see p. 37) should be configured so $MCLK_{INT}$ is 6 or 6.1440 MHz (see Table 4-14) for boost-converter operation at 2 or 2.05 MHz.
2. Minimum Class G boost ON hold-off time is determined from when the low audio detection is latched until when the boost is turned off. The latching mechanism occurs in 800-ms intervals. If the audio level is detected as low between two sequential latches, the hold-off time is extended by the difference between when the detection occurs and the subsequent latch pulse. This may extend the hold-off time up to 1.6 s in extreme cases.
3. Efficiency specified here assumes the boost converter drives an external resistive load via the VBST pin, instead of the onboard Class D amplifier.

Table 3-5. LED Drive Characteristics

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = 5.0 V, GNDA = GNDP = GNDPLED = 0 V, TA = +25°C.

Parameters		Min	Typical	Max	Units
Flash Mode current settings, per LED [1] (Step size = 50 mA)	LED_FLCUR = 1111 … LED_FLCUR = 0001	— … —	750 … 50	— … —	mA … mA
Flash Inhibit Mode current settings, per LED [1] (Step size = 50 mA)	LED_FLINHCUR = 0111 … LED_FLINHCUR = 0001	— … —	350 … 50	— … —	mA … mA
Movie Mode current settings, per LED [1]	LED_MVCUR = 111 LED_MVCUR = 110 LED_MVCUR = 101 LED_MVCUR = 100 LED_MVCUR = 011 LED_MVCUR = 010 LED_MVCUR = 001	— — — — — — —	150 120 100 80 60 40 20	— — — — — — —	mA mA mA mA mA mA mA
LED current accuracy		–10	—	+10	%
LED current matching		—	10	—	%
Flash timer (t_{flash})	$MCLK_{INT}$ = 6 MHz [2]; TIMER = 1 0010–1 1111 TIMER = 0 0001 TIMER = 0 0000 $MCLK_{INT}$ = 6.144 MHz; TIMER = 1 0010–1 1111 TIMER = 0 0001 TIMER = 0 0000	— — — — — —	500 75 50 488.3 73.2 48.8	— — — — — —	ms ms ms ms ms ms
LED flash timer accuracy		0	—	+1	ms
LED flash inhibit time (FLINH high to LED current 3% settling)		—	40	—	µs

1. Flash or Movie Mode current is delivered from the boost converter's output, which provides a voltage higher than the LED voltage. Depending on the LED voltage requirement and on VP supply voltage, the boost converter is internally controlled to boost or be in bypass (rectifying FET fully on).
2. The flash time setting is generated from $MCLK_{INT}$. MCLKDIV2 (see p. 37) should be configured so $MCLK_{INT}$ is 6 or 6.1440 MHz. See Table 4-14.

Table 3-6. Speaker Amplifier Output Characteristics

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = 5.0 V, 1-kHz input, amp gain = 12 dB, GNDA = GNDP = 0 V, T_A = +25°C, measurement bandwidth is 20 Hz to 20 kHz, Fs = 48 kHz, $MCLK_{INT}$ = 6 MHz. $MCLK_{INT}$ is explained in Section 4.13.1 and Section 7.7.

Parameters	Symbol	Test Conditions	Min	Typical	Max	Units
Continuous average power delivered to load [1]	Po	8-Ω load, THD 10% 8-Ω load, THD 1%	— —	1.75 1.45	— —	W W
THD+N	THD+N	8-Ω load, 1.0 W	—	0.02	—	%
Input voltage @ 1% THD+N	V_{ICLIP}	8-Ω load	—	0.84	—	Vrms
Signal to noise ratio	SNR	Referenced to output voltage @1% THD+N, A-weighted	—	102	—	dB
Idle channel noise	ICN	VBST = VP, A-weighted	—	25	—	µVrms
Common-mode rejection ratio	CMRR	V_{ripple} = 1 V_{PP}, f_{ripple} = 217 Hz	—	55	—	dB
Frequency response	FR	20 Hz to 20 kHz, No input DC blocking caps	–0.1	0	0.1	dB
Efficiency [2]	η_A	8-Ω load 33 µH, 1.7 W	—	91	—	%
Class D amplifier gain	—	AMP_GAIN = 000 (mute) AMP_GAIN = 001 AMP_GAIN = 010 AMP_GAIN = 011 AMP_GAIN = 100	— — — — —	–80 9 12 15 18	— — — — —	dB dB dB dB dB
N-FET ON resistance	$R_{DS\ ON,N}$	I_{FET} = 0.5 A	—	185	—	mΩ
P-FET ON resistance	$R_{DS\ ON,P}$	I_{FET} = 0.5 A	—	205	—	mΩ
Output DC offset voltage	V_{OFFSET}	Inputs AC coupled to ground	—	±5	—	mV
Time from shutdown to audio out	t_{SD}	$\overline{RESET}$ deasserted, zero-crossing disabled	—	15	—	ms

1. Power delivered to the speaker from the 0.1-Ω load side terminal (refer to Fig. 2-1).
2. Efficiency collected using a 5-V external supply, as shown in the drawing. For this test, the VBST pin should not be connected to the SPKRSUPPLY pin.

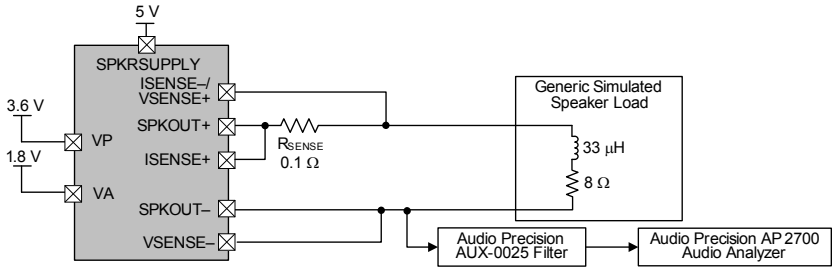
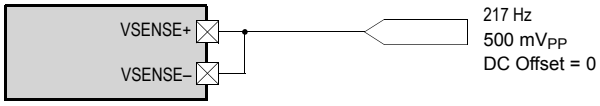


Table 3-7. Signal Monitoring Characteristics

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = 5.0 V, amp gain = 12 dB, 0.1-Ω sense resistor, GNDA = GNDP = 0 V, T_A = +25°C. Measurement bandwidth is 20 Hz to 20 kHz, Fs = 48 kHz, Input Signal = 1 kHz, $MCLK_{INT}$ = 6 MHz, $MCLK_{INT}$ is explained in Section 4.13.1 and Section 7.7.

Parameters		Min	Typical	Max	Units
General ADC characteristics	Power-up time: $t_{PUP(ADC)}$	—	8.5	[1]	ms
VSENSE± monitoring characteristics (VMON)	Data width	—	16	—	Bits
	Dynamic range (unweighted), VSENSE± = ±5.0 V (10 V_{PP})	—	60	—	dB [2]
	Total harmonic distortion + noise, –3.8 dBFS [3]	—	–60	—	dB [2]
	Full-scale signal input voltage	6.59•VA	6.94•VA	7.29•VA	V_{PP}
	Common-mode rejection ratio (217 Hz @ 500 mV_{PP}) [4]	—	60	—	dB [2]
	Group delay [5]	—	7.6/Fs	—	s
ISENSE± monitoring characteristics (IMON)	Data width	—	16	—	Bits
	Dynamic range (unweighted), ISENSE± = ±0.625 A (1.25 A_{PP})	—	56	—	dB [2]
	Total harmonic distortion, –29.5 dBFS [6]	—	–45	—	dB [2]
	Full-scale signal input voltage	1.56•VA	1.64•VA	1.72•VA	V_{PP}
	VMON-to-IMON isolation [7]	—	56	—	dB [2]
	Group delay [8]	—	7.6/Fs	—	s
VP monitoring characteristics	Data width	—	8	—	Bits
	Voltage resolution (See the equation in Section 4.8.4.)	—	35.3	—	mV
	(FF code) signal input voltage (VP)	2.89•VA	3.05•VA	3.20•VA	V
	VPMON = 1011 0011	—	2.8	—	V
	VPMON = 1011 0100	—	2.835	—	V
	…	…	…	…	…
	VPMON = 1111 1111	—	5.482	—	V
	VPMON = 0000 0000	—	5.518	—	V

1. Typical value is specified with PDN_AMP and PDN_xMON bits initially set. Maximum power-up time is affected by the actual $MCLK_{INT}$ frequency.
2. Parameters given in dB are referred to the applicable typical full-scale voltages. Applies to all THD+N and resolution values in the table
3. VSENSE± THD is measured with the Class D amplifier as the audio source connected to an 8-Ω + 33µH speaker load, supplied by a 6.3-V_{PP}, 1-kHz sine wave, operating under the typical performance test conditions to produce a large, unclipped audio signal. This setup produces a –3.8-dBFS VMON output. Larger Class D amplifier amplitudes begin to exhibit clipping behavior, increasing distortion of the signal supplied to VSENSE±
4. CMRR test setup for VSENSE±:



5. VMON group delay is measured from the time a signal is presented on the VSENSE± and pins until the MSB of the digitized signal exits the serial port. Fs is the LRCK rate.
6. For reference, injecting a 125-mVpp fully differential sine wave into the ISENSE± pins (equivalent to a ±0.625 A current with a 0.1-Ω ISENSE resistor) produces an IMON output of –29.5 dBFS (since typical full-scale is 1.64*VA, in V_{PP}). ISENSE± monitoring THD is measured using the Class D amplifier as the audio source, which is connected to an 8-Ω + 33-µH speaker load, supplied by a 7.0-V_{PP}, 1-kHz sine wave, operating under the typical performance test conditions to produce a large, unclipped audio signal. This setup produces a –29.5-dBFS amplitude IMON output. Larger Class D amplifier amplitudes begin to exhibit clipping behavior, increasing the distortion of the signal supplied to ISENSE±.
7. VMON-to-IMON isolation is the error in the current sense due to VMON, expressed relative to full-scale sense current in decibels.
8. IMON group delay is measured from when a signal is presented on the ISENSE± pins until the MSB of the digitized signal exits the serial port. Fs is the LRCK rate.

Table 3-8. Digital Interface Specifications and Characteristics

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = 5.0 V, GNDA = GNDP = 0 V, T_A = +25°C.

Parameters		Symbol	Test Conditions	Min	Max	Units
Input leakage current (per pin) [1,2]	FLOUT2/AD0	I_{IN}	—	—	±7.5	µA
	FLEN, FLINH, LRCK		—	—	±4.5	µA
	MCLK, SCLK, SDOUT		—	—	±4.5	µA
	SCL, SDA, $\overline{INT}$, $\overline{RESET}$		—	—	±0.1	µA
Input capacitance		I_{IN}	—	—	10	pF
VA logic I/Os	High-level output voltage	V_{OH}	I_{OH} = –67/–100 µA [3]	VA–0.2	—	V
	Low-level output voltage	V_{OL}	All outputs, I_{OL} = 67/100 µA [3]	—	0.20	V
			$\overline{INT}$, SDA, I_{OL} = 3 mA	—	0.4	V
	High-level input voltage	V_{IH}	—	0.70•VA	—	V
	Low-level input voltage	V_{IL}	—	—	0.30•VA	V

1. Specification includes current through internal pull up/down resistors, where applicable (as defined in Section 1).
2. Leakage current is measured with VA = 1.80 V, VP = 3.60 V, VBST = 3.60 V, and $\overline{RESET}$ asserted. Each pin is tested while driven high and low.
3. For the ADSP output SDOUT and potential outputs SCLK and LRCK (if M/S = 1), if ADSP_DRIVE = 0 see Section 7.13, I_{OH} and I_{OL} are –100 and +100 µA. If ADSP_DRIVE = 1, I_{OH} and I_{OL} are –67 and +67 µA. For other, non-ADSP_DRIVE-affected outputs, I_{OH} and $I_{OL}$are –100 and +100 µA.

Table 3-9. PSRR Characteristics

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = VP, amp gain = 12 dB, GNDA = GNDP = 0 V, T_A = +25°C.

Parameters	Conditions	Noise Injected Into	Noise Measured On	Noise Amplitude (mV)	Noise Frequency (Hz)	Min	Typical	Max	Units
Speaker amplifier PSRR	VBST = VP	VA	SPKOUT±	100	217	—	75	—	dB
					1k	—	75	—	dB
					20k	—	70	—	dB
		VP	SPKOUT±	100	217	—	70	—	dB
					1k	—	70	—	dB
					20k	—	55	—	dB
VPMON PSRR	VBST = VP	VA	SDOUT	100	217	—	36	—	dB
					1k	—	36	—	dB
					20k	—	33	—	dB
VSENSE± PSRR [1]	VBST = VP	VA	SDOUT	100	217	—	60	—	dB
					1k	—	60	—	dB
					20k	—	50	—	dB
ISENSE± PSRR	VBST = VP	VA	SDOUT	100	217	—	60	—	dB
					1k	—	60	—	dB
					20k	—	60	—	dB

1. The speaker voltage monitor has a lower PSRR because its input path has an attenuation of 16.6 dB. The PSRR specification is referred to the input signal and, as such, includes the loss of 16.6 dB.

Table 3-10. Power Consumption

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = VP, GNDA = GNDP = 0 V, T_A = +25°C.

Use Configuration		Typical Current		
		i_{VP}	i_{VA}	Units
Powered up (PDN_BST = 00)	$\overline{\text{RESET}}$ asserted, MCLK, SCLK, LRCK inactive	1	1	µA
	IN+ IN– shorted to ground, LEDs off, monitors powered down[1] No C_{OUT}	3270	390	µA
	IN+ IN– shorted to ground, LEDs off, monitors powered down [1] C_{OUT} = 470 pF (See Fig. 2-1)	4275	390	µA
	IN+ IN– shorted to ground, LEDs off, monitors powered up [1] No C_{OUT}	3360	1435	µA
	IN+ IN– shorted to ground, LEDs off, monitors powered up [1] C_{OUT} = 470 pF See Fig. 2-1)	4360	1435	µA
Boost Mode bypass (PDN_BST = 01) .	$\overline{\text{RESET}}$ asserted, MCLK, SCLK, LRCK inactive	1	1	µA
	IN+ IN– shorted to ground, LEDs off, monitors powered down [1] No C_{OUT}	1983	390	µA
	IN+ IN– shorted to ground, LEDs off, monitors powered down [1] C_{OUT} = 470 pF (See Fig. 2-1)	3093	390	µA
	IN+ IN– shorted to ground, LEDs off, monitors powered up [1] No C_{OUT}	2074	1435	µA
	IN+ IN– shorted to ground, LEDs off, monitors powered up [1] C_{OUT} = 470 pF See Fig. 2-1)	3185	1435	µA

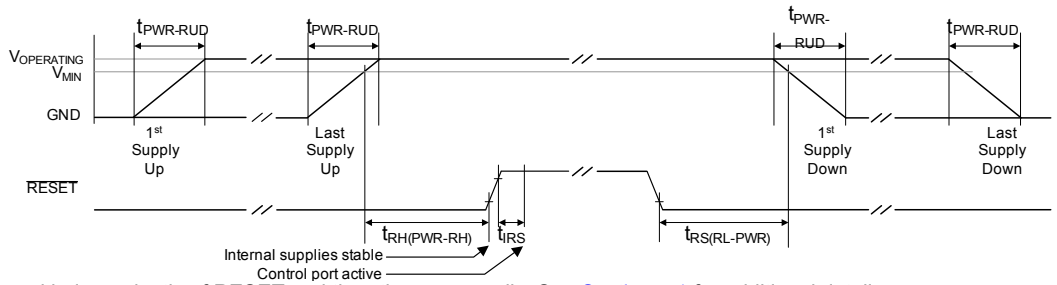
1. Refer to Section 7.6 for configuring monitor power down

Table 3-11. Switching Specifications: Power, Reset, Master Clocks

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = 5.0 V, T_A = +25°C, GNDA = GNDP = 0 V. Fig. 2-1 shows typical connections; GNDA = GNDP = 0 V. Section 9 describes some parameters in detail; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters		Symbol [1]	Min	Max	Units
Power supplies [2]	Power supply ramp up/down	$t_{PWR-RUD}$	—	100	ms
Reset [2]	$\overline{\text{RESET}}$ low (logic 0) pulse width	t_{RLPW}	1	—	ms
	$\overline{\text{RESET}}$ hold time after power supplies ramp up	$t_{RH(PWR-RH)}$	1	—	ms
	$\overline{\text{RESET}}$ setup time before power supplies ramp down	$t_{RS(RL-PWR)}$	1	—	ms
	$\overline{\text{RESET}}$ rising edge to control-port active	t_{IRS}	[3]	—	ns
Master clocks	MCLK frequency [4]	f_{MCLK}	—	12.3	MHz
	MCLK duty cycle	D_{MCLK}	45	55	%

1. Power and reset sequencing



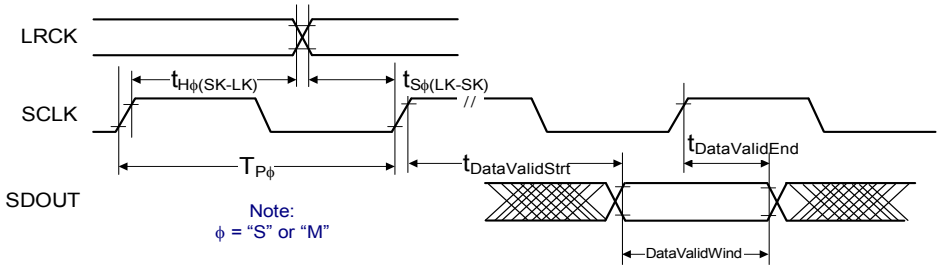
2. VP supply may be applied or removed independently of RESET and the other power rails. See Section 4.1 for additional details.
3. The $\overline{\text{RESET}}$ rising-edge-to-control-port-active timing, t_{irs}, is specified in Table 3-13.
4. Maximum frequency for highest supported nominal rate is indicated. The supported nominal serial port sample rates are found in Section 4.11.2.

Table 3-12. Switching Specifications: ADSP in I²S Mode

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = 5.0 V, T_A = +25°C, Inputs: Logic 0 = GNDA = GNDP = 0 V, Logic 1 = VA; C_{LOAD} = 30 pF. Section 9 describes some parameters in detail; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters		Symbol [1]	Min	Max	Units
Slave Mode	Input sample rate (LRCK) [2]	Fs	—	49	kHz
	LRCK duty cycle	—	45	55	%
	SCLK frequency	$1/t_{PS}$	—	64•Fs	Hz
	SCLK duty cycle	—	45	55	%
	LRCK setup time before SCLK rising edge	$t_{SS(LK–SK)}$	40	—	ns
	LRCK hold time after SCLK rising edge	$t_{HS(SK–LK)}$	20	—	ns
	SDOUT time from SCLK to data valid start [3]	$t_{DataValidStrt}$	—	300	ns
	SDOUT time from SCLK to data valid end [3]	$t_{DataValidEnd}$	155	—	ns
Master Mode	OUTPUT sample rate (LRCK) [4]	Fs	—	[4]	kHz
	LRCK duty cycle	—	45	55	%
	SCLK frequency	$1/t_{PM}$	—	64•Fs	Hz
	SCLK duty cycle RATIO = 0 RATIO = 1 [5]	— —	45 33	55 67	% %
	LRCK setup time before SCLK rising edge	$t_{SM(LK–SK)}$	35	—	ns
	LRCK hold time after SCLK rising edge	$t_{HM(SK–LK)}$	20	—	ns
	SDOUT time from SCLK to data valid start [3]	$t_{DataValidStrt}$	—	300	ns
	SDOUT time from SCLK to data valid end [3]	$t_{DataValidEnd}$	155	—	ns

1. ADSP timing in I²S Mode



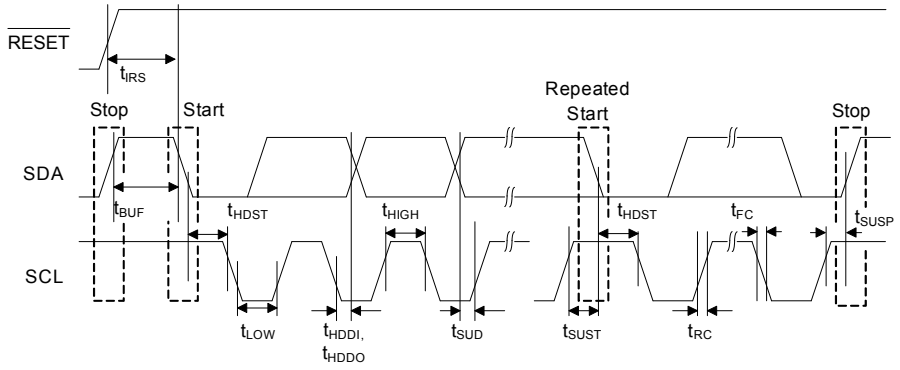
2. Clock rates should be stable when the CS35L32 is powered up.
3. Minimum data valid window, as shown in signal diagram, is (SCLKperiod – 300 + 155) ns. For SCLK = 64*Fs =64*48 = 3072 kHz, this is 180 ns.
4. In Master Mode, the output sample rate follows MCLK rate divided down per Table 4-14 and Section 7.7. Any deviation in internal MCLK from the nominal supported rates is directly imparted to the output sample rate by the same factor (e.g., +100-ppm offset in the frequency of MCLK becomes a +100-ppm offset in LRCK).
5. If RATIO = 1, the MCLK(INT)-to-LRCK ratio is 125. The device periodically extends SCLK high time to compensate for a fractional MCLK/SCLK ratio

Table 3-13. Switching Specifications: I²C Control Port

Test conditions, except where noted otherwise: VA = 1.8 V, VP = 3.6 V, VBST = 5.0 V, T_A = +25°C, Inputs: Logic 0 = GNDA = GNDP = 0 V, Logic 1 = VA; SDA load capacitance equal to maximum value of C_B specified below; minimum SDA pull-up resistance, $R_{P(min)}$.[1] Section 9 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS35L32 with the specified load capacitance; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameter	Symbol [2]	Min	Max	Units
$\overline{\text{RESET}}$ rising edge to start	t_{IRS}	500	—	ns
SCL clock frequency	f_{SCL}	—	400	kHz
Start condition hold time (before first clock pulse)	t_{HDST}	0.6	—	µs
Clock low time	t_{LOW}	1.3	—	µs
Clock high time	t_{HIGH}	0.6	—	µs
Setup time for repeated start condition	t_{SUST}	0.6	—	µs
SDA input hold time from SCL falling [3]	t_{HDDI}	0	0.9	µs
SDA output hold time from SCL falling	t_{HDDO}	0.2	0.9	µs
SDA setup time to SCL rising	t_{SUD}	100	—	ns
Rise time of SCL and SDA	t_{RC}	—	300	ns
Fall time of SCL and SDA	t_{FC}	—	300	ns
Setup time for stop condition	t_{SUSP}	0.6	—	µs
Bus free time between transmissions	t_{BUF}	1.3	—	µs
SDA bus capacitance	C_B	—	400	pF

1. The minimum R_P and R_{P_I} values (resistors shown in Fig. 2-1) are determined using the maximum level of VA, the minimum sink current strength of their respective output, and the maximum low-level output voltage V_{OL}(specified in Table 3-8). The maximum R_P and R_{P_I} values may be determined by how fast their associated signals must transition (e.g., the lower the value of R_P, the faster the I²C bus is able to operate for a given bus load capacitance). See the I²C switching specifications in Table 3-13 and the I²C bus specification referenced in Section 13.
2. I²C control-port timing.



3. Data must be held long enough to bridge the transition time, t_F, of SCL.

4 Functional Description

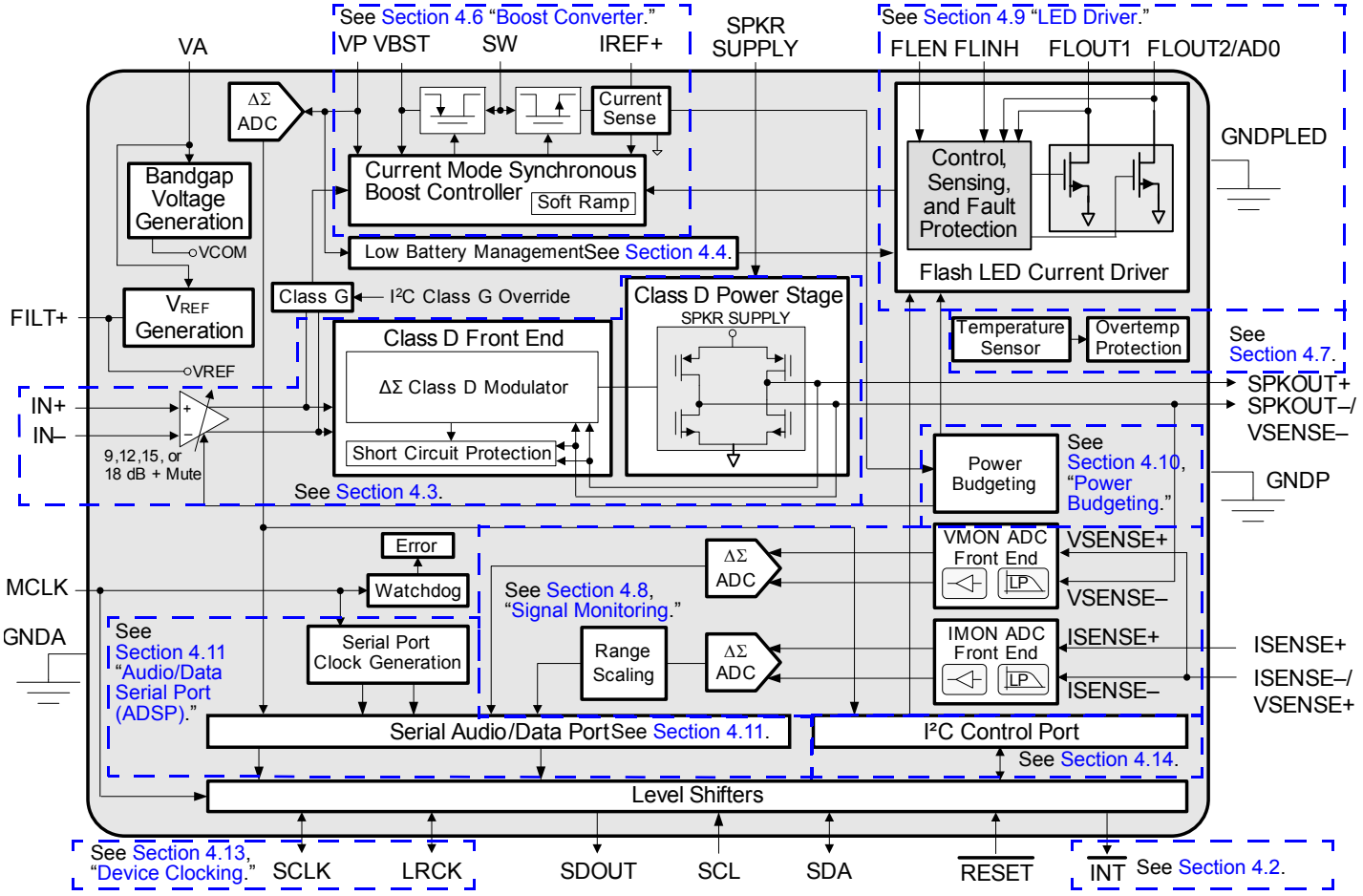


Figure 4-1. CS35L32 Block Diagram

4.1 Power Supplies

The VA and VP supplies are required for proper operation of the CS35L32. Before either supply is powered down, $\overline{\text{RESET}}$ must be asserted. $\overline{\text{RESET}}$ must be held in the asserted state until all supplies are up and within the recommended range. Timing requirement for $\overline{\text{RESET}}$ during supply power up and power down is described in Table 3-11. The VBST supply is generated internally (as described in Section 7.12) and connected to the high-power output stage of the Class D amplifier through two balls: VBST and SPKRSUPPLY. By so doing, the speaker amplifier benefits from the proximity of the external decoupling capacitor that is connected to the boosted supply.

4.2 Interrupts

Events that require special attention, such as when a threshold is exceeded or an error occurs, are reported through the assertion of the interrupt output pin, $\overline{\text{INT}}$. These events are captured within the interrupt status registers. Events can be individually masked by setting corresponding bits in the interrupt mask registers. Table 4-1 lists interrupt status and mask registers. The configuration of mask bits determines which events cause the immediate assertion of $\overline{\text{INT}}$:

- When an unmasked interrupt status event is detected, the status bit is set and $\overline{\text{INT}}$ is asserted.
- When a masked interrupt status event is detected, the interrupt status bit is set, but $\overline{\text{INT}}$ is not affected.

Once $\overline{\text{INT}}$ is asserted, it remains asserted until all unmasked status bits that are set have been read. Interrupt status bits are sticky and read-to-clear: Once set, they remain set until the register is read and the associated interrupt condition is not present. If a condition is still present and the status bit is read, although $\overline{\text{INT}}$ is deasserted, the status bit remains set.

To clear any status bits set due to the initiation of a path or block, all interrupt status bits should be read after reset and before normal operation begins. Otherwise, unmasking these previously set status bits causes INT to assert.

Table 4-1. Interrupt Status Registers and Corresponding Mask Registers

Status Registers	Mask Registers
Interrupt Status 1 (Audio) (Section 7.19) Interrupt Status 2 (Monitors) (Section 7.20) Interrupt Status 3 (LEDs and Boost Converter) (Section 7.21)	Interrupt Mask 1 (Section 7.16) Interrupt Mask 2 (Section 7.17) Interrupt Mask 3 (Section 7.18)

4.3 Speaker Amplifier

The CS35L32 features a high-efficiency mono Class D audio amplifier, shown in Fig. 4-2, with an advanced closed-loop architecture that achieves low levels of output distortion. Automatic Class G operation, using a boosted supply to the amplifier, allows louder speaker performance with high crest factor.

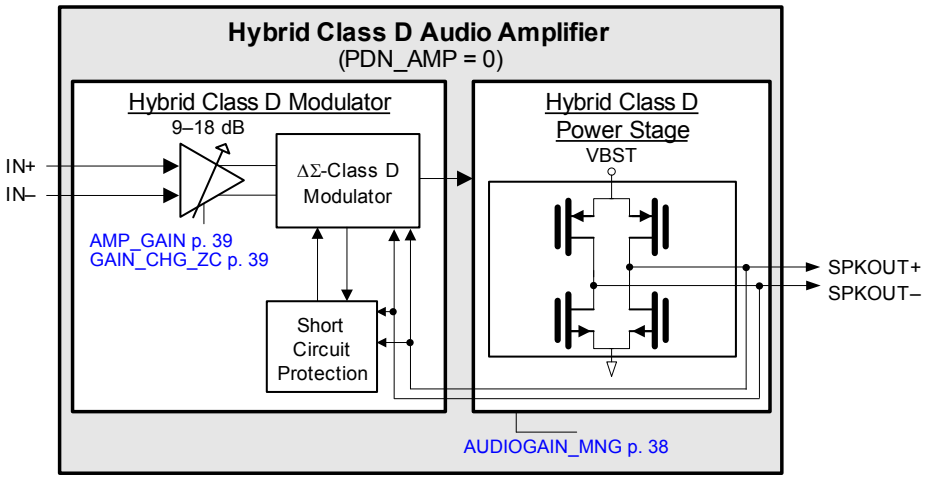


Figure 4-2. Speaker Amplifier Block Diagram

4.3.1 Class G Operation with LEDs Off

The boost converter output is the supply to the speaker amplifier. Audio operation can be programmed to have one of the following supply modes (See Section 7.12 for programming details.):

- Class G where the boost converter is in Bypass Mode for audio input signals below a threshold $V_{IN1THON}$ and in 5-V Boost Mode for audio signal inputs above a threshold $V_{IN1THOFF}$. These thresholds are specified in Table 3-4 for the given conditions. The corresponding equations are shown below.
- Class G disabled, boost converter is in Bypass Mode, and VBST = VP. In this mode, thresholds are ignored.
- Class G disabled, boost converter is in Boost Mode, and VBST = 5 V. In this mode, thresholds are ignored.

The Class G equations for the audio input signal thresholds are as follows:

$$V_{IN1THOF} = \left(\frac{4}{15}K\right) \times \left(\frac{VBST}{Gain}\right)$$

and

$$V_{IN1THON} = \left(\frac{2}{3}K\right) \times \left(\frac{VBST}{Gain}\right)$$

VBST is the boost converter output voltage (whether in Bypass or Boost Mode), and gain is audio gain expressed as a unitless real ratio (nonlogarithmic). K = 1 if MCLK is 6 or 12 MHz; K = 1.024 if MCLK is 6.144 or 12.288 MHz. $MCLK_{INT}$ should be configured as described in Section 4.13.1 and Section 7.7.

4.3.2 Class G Operation with LEDs On

If LEDs are active, the speaker amplifier supply in one of the following supply modes, as specified by VBOOST_MNG (see Section 4.10.3 and Section 7.12 for details):

- Class G operation defaults to the higher supply setting: that requested by the LEDs or that requested by Class G. The latter takes into account both thresholds $V_{IN1THOF}$ and $V_{IN1THON}$, as described in Section 4.3.1.
- Class G disabled and the speaker amplifier supply is set as requested by the LEDs. Thresholds are ignored.
- Class G disabled where the boost converter is in Bypass Mode (VBST = VP). Thresholds are ignored.
- Class G disabled where the boost converter is in Boost Mode and VBST = 5 V. Thresholds are ignored.

4.3.3 Error Conditions

Table 4-2 provides links to error status and mask bits for the Class D audio amplifier errors.

Table 4-2. Class D Audio Amplifier Error Status and Mask Bits

Error	Cross-Reference to Description
Amplifier short/Amplifier short mask	AMP_SHORT p. 41, M_AMP_SHORT p. 40, also see Section 4.3.3
Amplifier short release	AMP_SHORT_RLS p. 39
Overtemperature error/Overtemperature error mask	OTE p. 41, M_OTE p. 40, also see Section 4.3.3
Overtemperature error release	OTE_RLS p. 40

The CS35L32 monitors the OUT± terminals in real time to determine whether the output voltage signal correlates to the PWM data stream driving the gate drivers internal to the device. If it is not, the CS35L32 interprets the discrepancy as a short on the outputs, which may have been caused by a short to ground, across the speaker, or to the VBST rail.

If this error occurs, the AMP_SHORT status bit is set, and, if M_AMP_SHORT = 0, $\overline{INT}$ is asserted. As a result, the device enters Speaker-Safe Mode, which is described in Section 4.3.4.

The CS35L32 also enters Speaker-Safe Mode if its temperature exceeds the overtemperature shutdown threshold specified in Table 3-3. The OTE status bit is set; if M_OTE = 0, $\overline{INT}$ is asserted.

The amplifier shuts down automatically due to battery (VP) undervoltage, as described in Section 4.5. The amplifier restarts automatically upon voltage recovery, with default gain.

The audio amplifier outputs are clamped to ground if MCLK stops, as described in Section 4.13.3.

4.3.4 Speaker-Safe Mode

Speaker-Safe Mode is entered according to the AMP_SHORT and OTE interrupt status bits as follows:

- In the event of an AMP_SHORT, the CS35L32 mutes the amplifier output to Hi-Z to protect the speaker while the boost converter is allowed to operate normally.
- In the event of an OTE, the CS35L32 mutes the amplifier output to Hi-Z to protect the speaker and sets the boost converter in Bypass Mode (VBST = VP). Normal behavior resumes when the error condition ceases and OTE_RLS is sequenced as described in Section 4.7.1.
- If Speaker-Safe Mode is entered as a result of an AMP_SHORT error, normal behavior resumes when the short condition ceases and the AMP_SHORT_RLS bit is sequenced as described in Section 7.15.

4.4 Low-Battery Management

Under heavy current loading, such as a high current LED flash event, the battery voltage drops. LOWBAT_TH (see p. 37) allows the user to select a voltage threshold, below which flash current is reduced from the LED_FLCUR setting (see p. 43) to the LED_FLINHCUR setting (see p. 44). Upon voltage recovery above LOWBAT_RECOV (see p. 37), the flash current setting reverts to normal. The user should select a recovery threshold higher than the low-battery threshold.

Low-Battery Mode is entered only if a battery voltage falls below the programmed LOWBAT_TH during a flash event. This condition is reported by the setting LOWBAT (see p. 42), which can be masked with M_LOWBAT (see p. 41).

$\overline{INT}$ is deasserted after the interrupt registers are cleared by being read, provided the condition no longer exists.

4.5 Undervoltage Lockout (UVLO)

If the VP level falls below the lockout threshold specified in Table 3-3, UVLO protection shuts down all analog circuitry of the CS35L32. Autorecovery occurs as VP rises above the lockout threshold by a voltage equal to the specified hysteresis. During a UVLO condition, control port, UVLO detection, serial clock, watchdog, and thermal detection circuitry stay active.

Note: During an UVLO condition, the I²S port is automatically powered down, preventing the UVLO condition from being fed back via the ADSP SDOUT pin.

4.6 Boost Converter

The CS35L32's boost converter, shown in Fig. 4-3, delivers power to the supply of the audio speaker amplifier as well as to the LEDs. Its output voltage is determined by VBOOST_MNG (see p. 38). Section 4.10 further shows how VBOOST_MNG relates to audio and LED operation. The boost converter features a current-limiting circuit that detects and clamps peak inductor current if such a peak is equal to the user-programmable limit (BST_IPK, see p. 38). BOOST_CURLIM interrupt flag is set when the current limit has been detected.

$MCLK_{INT}$ sets the frequency of the converter to 2 MHz. $MCLK_{INT}$ is derived from MCLK by setting MCLKDIV2 (see p. 37). If $MCLK_{INT}$ stops switching, the converter is placed in Bypass Mode until clocking is restored.

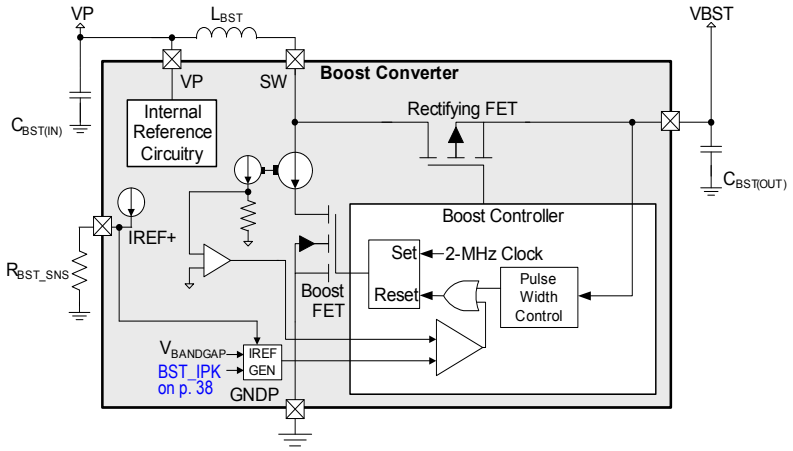


Figure 4-3. Boost Controller Block Diagram

4.7 Die Temperature Monitoring

Onboard die temperature monitoring prevents, shown in Fig. 4-4, the CS35L32 from reaching a temperature that would compromise reliability or functionality. The CS35L32 incorporates a two-threshold thermal-monitoring system. When die temperature exceeds the lower threshold, an overtemperature warning (OTW) event occurs; if it exceeds the second threshold, an overtemperature error (OTE) condition occurs. These conditions are described in Section 4.7.1.

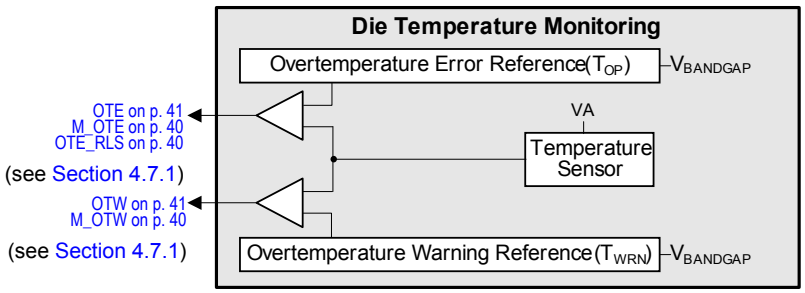


Figure 4-4. Die Temperature Monitoring

Note: The CS35L32 does not support independent powering down of die-temperature monitoring circuitry (other than powering it down via PDN_ALL, see p. 36).

4.7.1 Error Conditions

Table 4-3 lists overtemperature error status and mask bits.

Table 4-3. Die Temperature Monitoring Configuration

Error	Cross-Reference to Register Field Description
Overtemperature error/Overtemperature error mask	OTE p. 41/M_OTE p. 40
Overtemperature warning/Overtemperature warning mask	OTW p. 41/M_OTW p. 40
Overtemperature error release	OTE_RLS p. 40

The overtemperature error and warning error conditions are described in detail in the following:

- Overtemperature warning (OTW). An OTW event occurs when the die temperature exceeds the overtemperature threshold (listed in Table 3-3). When this occurs, an OTW (see p. 41) event is registered in the interrupt status (Section 7.19); if M_OTW = 0, $\overline{INT}$ is asserted.

  To exit the condition, the temperature must drop below the threshold and interrupt status 1 register must be read.
- Overtemperature error (OTE). An OTE event occurs when the die temperature exceeds the internally preset error threshold (see Table 3-3). When this occurs, an OTE (see p. 41) event is registered in the interrupt status and, if M_OTE = 0, $\overline{INT}$ is asserted. The CS35L32 shuts down, the Class D amplifier enters Speaker Safe Mode, as described in Section 4.3.4, and the LED drivers shut down.

  To exit, the temperature must drop below the overtemperature shutdown threshold and OTE_RLS must be sequenced as described in Section 7.15. After OTE release, the amplifier and LED drivers recover to preshutdown settings. The LED drivers must be retriggered with FLEN and/or FLINH inputs for a lighting event to occur.

4.8 Signal Monitoring

Signal-monitoring ADCs, shown in Fig. 4-5, give upstream system processors access to important signals entering and exiting the device. The three monitoring signals are as follows:

- VPMON: Monitors the voltage on the VP pin, which is most commonly the battery for the system.
- VMON: Monitors the output voltage of the Class D amplifier.
- IMON: Monitors the current that flows into the load being driven by the Class D amplifier.

An integrated ADC digitizes these analog signals, at which point, the audio/data serial port (ADSP) can send them to the system processor.

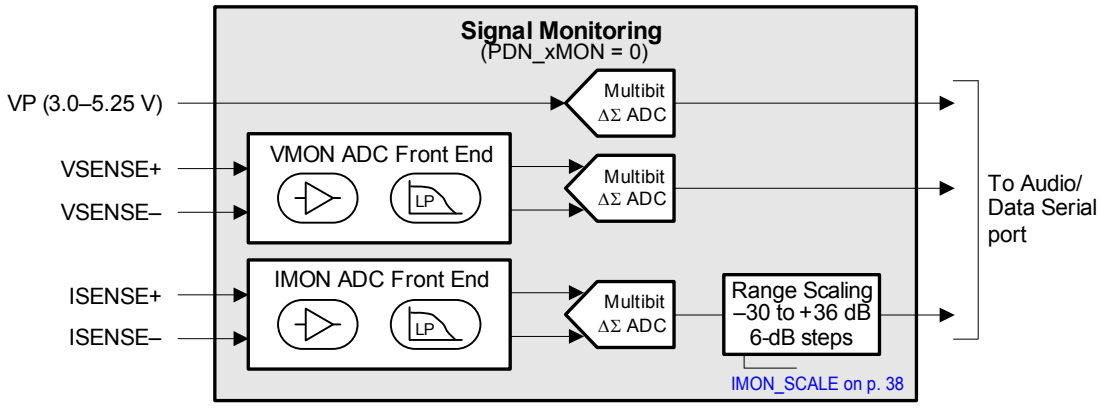


Figure 4-5. Signal Monitoring Block Diagram (PDN_xMON = 0)

4.8.1 Power-Up and Power-Down Bits (PDN_xMON)

The three ADCs can be powered down independently via their respective PDN_xMON bit in the control port, see Section 7.6. To power down an ADC and its associated support circuitry, its PDN_xMON bit must be set; clearing PDN_xMON powers up the corresponding circuitry.

Note: For proper operation, MCLK must be at the correct frequency (MCLK_ERR = 0; see p. 41) and the device must be powered (PDN_ALL = 0; see p. 36).

4.8.2 Monitoring Voltage across the Load—VMON

As shown in Fig. 4-5, monitoring on VMON is accomplished via the VSENSE± pins. Table 3-7 gives operating and performance specifications for this ADC path. The following equation determines the VMON voltage (in Volts):

$$VMON = \left(\frac{D_{OUT}}{2^{15}-1}\right) \times \left(\frac{6.25 \times VA}{1.8}\right)$$

D_{OUT} is the 16-bit digital output monitoring word in signed decimal format (–32,768 to +32,767) and VA is the voltage on the VA pin. Relative to VSENSE+, negative D_{OUT} values equate to a negative load voltage and positive D_{OUT} values equate to a positive load voltage. When VA is 1.8 V, the full-scale signal is 6.25 V.

If VMON is a 12-bit word, its equivalent 16-bit representation for the computational purposes of this section positions the 12 bits in the 12 MSBs and the 4 LSBs are cleared in the computation.

4.8.3 Monitoring Current through the Load—IMON

As shown in Fig. 4-5, monitoring of output current is accomplished via the ISENSE± pins, which are provided to measure a voltage drop across a sense resistor in the output path, as described in Section 3. A precision resistor (≤1%) is chosen for high accuracy when calculating the current from the voltage measured across the resistor. Likewise, to avoid thermal drift, the resistor is chosen to have a low thermal coefficient of 100 ppm/°C. Table 3-7 gives operating and performance specifications for this ADC path.

The following equation determines the IMON current (in Amps) when using a 0.1-Ω sense resistor:

$$IMON = \left(\frac{D_{OUT}}{2^{15}-1}\right) \times \left(\frac{0.82 \times VA}{0.1\Omega}\right)$$

D_{OUT} is the 16-bit digital output monitoring word in signed decimal format (–32,768 to +32,767) and VA is the voltage on the VA pin. Relative to ISENSE+, negative D_{OUT} values equate to a negative current and positive D_{OUT} values equate to a positive current. The default IMON_SCALE, as described in Section 4.8.3.1, is used for the example equation. If the IMON_SCALE value is increased by 1 bit, the 2^{15} power in the IMON equation increases to 2^{15+1}. If the IMON_SCALE value is decreased by 1 bit, the 2^{15} power in the IMON equation decreases to 2^{15-1}.

If IMON is a 12-bit word, its equivalent 16-bit representation for the computational purposes of this section positions the 12 bits in the 12 MSBs, and the 4 LSBs are cleared in the computation.

4.8.3.1 IMON Signal Scaling (IMON_SCALE)

Because the voltage is measured across a resistor of very small value and because output current can vary significantly depending on the program material, a gain-scaling block (shown in Fig. 4-5) is included to improve the reported sample resolution for low-level signals. This control, configured through IMON_SCALE (see p. 38), allows the system processor to determine the range of bits to be received from the available 26-bit word on the IMON ADC's data bus. The default IMON_SCALE configuration (22 down to 7) configures the ADC data MSB (bit 22) to be the 16-bit IMON data packet MSB. ADC bits 23–25 allow the signal to be divided down.

If IMON is a 12-bit word, its equivalent 16-bit representation for the computational purposes of this section positions the 12 bits in the 12 MSBs. The 4 LSBs are cleared in the computation.

4.8.3.2 IMON Sense Resistor

A 0.1-Ω sense resistor is used to generate a differential voltage that is captured by the IMON circuitry to monitor the load current. If PWM output filtering components, such as ferrite beads, are placed in series with the output load, the sense resistor must be placed between the SPKOUT+ pin and the external series filter component, minimizing any performance effects produced by the output filter. If the sense resistor is placed after the series-filtering component, the signal being measured across the sense resistor will have been altered from its expected form.

4.8.4 Monitoring Voltage on the VP Pin—VPMON

Monitoring of the voltage present on the VP pin is integrated internally to the CS35L32. The operating specifications for this ADC path are given in Table 3-7. To determine the voltage present on VP, the following equation must be used:

$$VP = \left(\frac{(D_{OUT} + 128)}{255} \times 5 + \frac{1}{1.8}\right) \times VA$$

D_{OUT} is the digital output word (see VPMON, p. 38) in signed decimal format (–128 to +127), and VA is the voltage on the VA pin. If VA = 1.8 V, VPMON can report values from 2.8 V (D_{OUT} = –77 decimal) to 5.52 V (D_{OUT} = 0 decimal).

4.8.5 Data Transmission out of the CS35L32

The ADSP, described in Section 4.11, can transmit all signals monitored in the CS35L32 to the system processor. The data is presented on these outputs simultaneously.

4.8.6 Error Conditions

The CS35L32 monitors each monitoring ADC for overflow conditions. Table 4-4 lists signal monitoring error conditions and provides links to their associated register field descriptions.

Table 4-4. Signal Monitoring Error Status Conditions

Error	Cross-Reference to Description
xMON overflow. Indicates the overrange status in the VMON, IMON, or VPMON ADC signal paths.	VMON_OVFL p. 42 IMON_OVFL p. 42 VPMON_OVFL p. 42

If an overflow occurs, the appropriate xMON_OVFL bit is set, and, if the respective mask bit is cleared, an interrupt occurs. Exiting the error occurs when the signal is no longer overflowing. No release bit needs to be toggled.

- Overflow for VPMON and VMON signals. Due to the analog prescaling applied to the analog input signals, which are sampled to make the VPMON and VMON signals, overflow conditions are unlikely on these ADCs. This is because the operating specifications for maximum and minimum voltage constrain the voltage on these pins to a level far below that required to make the ADC overflow.

  For VPMON, because a spurious overflow error can occur when the block is taken out of power down, it is advised to read the error status registers after PDN_xMON has been cleared to clear the spurious error status bit.
- Overflow for the IMON signal. As Section 4.8.3.1 describes, the IMON_SCALE (see p. 38) control allows the greatest possible sample resolution over a wide range of output currents and sense resistors. If IMON_SCALE is set too low for either the output current being monitored or the sense resistor being used, overflow of this ADC can occur. When this error occurs, increasing the IMON_SCALE value can prevent the sampled signal from overflowing.

4.9 LED Driver

The CS35L32 includes a high-current flash LED driver (see Fig. 4-6), featuring two channels, FLOUT1 and FLOUT2, and a boost converter and current regulator designed to power LEDs with up to 0.75 A per channel. Both channels can be combined to drive an LED with 1.5 A by tying FLOUT1 and FLOUT2 together.

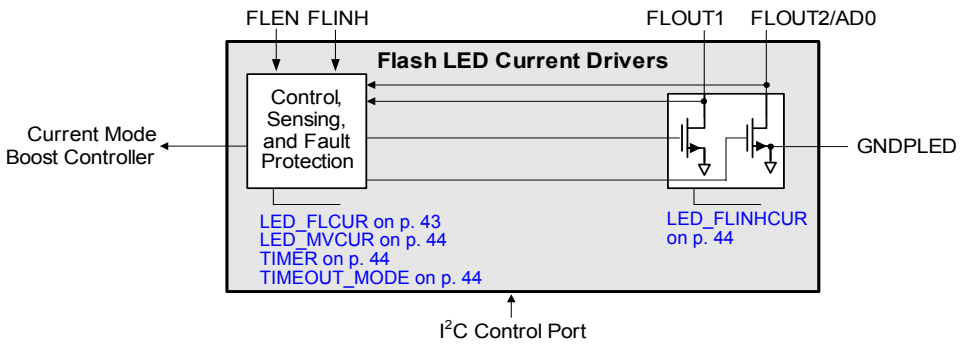


Figure 4-6. LED Driver Block Diagram

The CS35L32 is driven to flash when FLEN is asserted high. The I²C interface allows a host to program Flash and Movie Mode currents, as well as a flash timer. The corresponding registers for these settings are LED_FLCUR (see p. 43), LED_MVCUR (see p. 44), and TIMER (see p. 44). The flash event terminates at the end of a period determined by the flash timer and optionally when FLEN is deasserted; this option is configured through TIMEOUT_MODE (see p. 44).

Flash current is reduced if FLINH is asserted. Currents in both channels are reduced to the LED_FLINHCUR setting (see p. 44). If FLINH is deasserted, the current reverts to the LED_FLCUR setting, subject to the flash timer state.

Movie Mode operation has no timer and starts and ends according to the LED_MVCUR setting. Fig. 4-7 shows how Flash and Flash Inhibit Mode currents are started and terminated.

To power the LED load, the LED driver and current regulator automatically boost the voltage if battery operation is insufficient to produce the required LED currents. The controller bases whether to boost or operate in bypass, based on maintaining a minimum voltage across the current regulator. The boost voltage varies by up to 5 V nominal, as described in Section 4.10 and Section 7.12, depending on user selection.

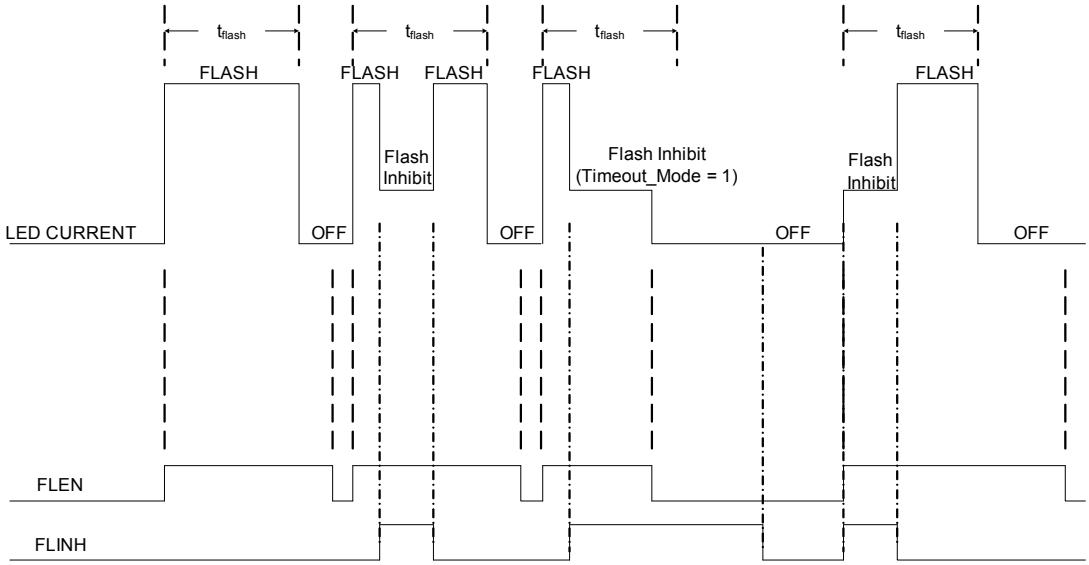


Figure 4-7. LED Flash Timing Diagram

4.9.1 LED Driver Protection

The LED controller shuts down if the CS35L32's temperature exceeds the overtemperature shutdown threshold specified in Table 3-3. The OTE status bit is set and, and if M_OTE = 0, $\overline{INT}$ is asserted. Recovery starts after the user clears OTE_RLS (see p. 40), after which, the LED drivers must be retriggered with a FLEN signal for a flash event to occur, or with the LEDx_MVEN enable bit (see Section 7.24) for a Movie Mode event to occur.

An automatic LED driver shutdown occurs in the event of a shorted or open LED. LED open and short conditions are detected only when a Flash or Movie Mode event is initiated. For a Flash Mode event to occur after clearing the error status bit, the LED drivers must be retriggered with a FLEN signal. For a Movie Mode event to occur after clearing the error status bit, the LEDx_MVEN bit must be set.

4.9.2 LED Driver Interrupt

An interrupt is generated when any of the following conditions or faults occur: LEDx short or open is present when a Flash event is initiated, current limit, boost output overvoltage, or UVLO of VP. The condition is registered in interrupt status register 3, Section 7.21. Its mask is in Section 7.18. If the error conditions are no longer present, $\overline{INT}$ is reset and deasserted after the interrupt register is read.

Note: The device does not generate an LED open circuit interrupt if the boost converter is running in bypass mode (PDN_BST= 01).

4.9.3 LED Lighting Status Register

The LED lighting status register (see Section 7.22) reports the state of LEDs and their controls. Status is reported for LED1 and LED2 flash events, indicating whether each LED is driven with current set by the flash setting. Likewise, status is reported for LED1 and LED2 Movie Mode events, indicating whether each LED is driven with current set by the Movie Mode setting. LED2 disable status is reported if FLOUT2 is used without an LED and is tied to ground, as shown in Fig. 2-1. The logic status of the signal input at FLEN and FLINH is reported. Flash timer events are reported.

4.10 Power Budgeting

Power budgeting is configured through ILED_MNG, AUDIOGAIN_MNG, and VBOOST_MNG (see p. 38), which set the boost converter's output mode and the load management mode, as described in Section 4.10.1–Section 4.10.3. Load management consists of reducing audio or LED load, or both, as long as one of the following conditions exists:

- The boost converter output voltage has dropped, provided that the boost converter is configured for a fixed 5-V Mode through VBOOST_MNG and the load current has settled to its target value.
- The boost converter is in current limit.
- An overtemperature warning (135°C) has occurred.

Power budgeting is configurable to be active automatically without user intervention, semiautomatically, or nonautomatically, where the user controls audio and LED load management.

Fig. 4-8 shows power budgeting.

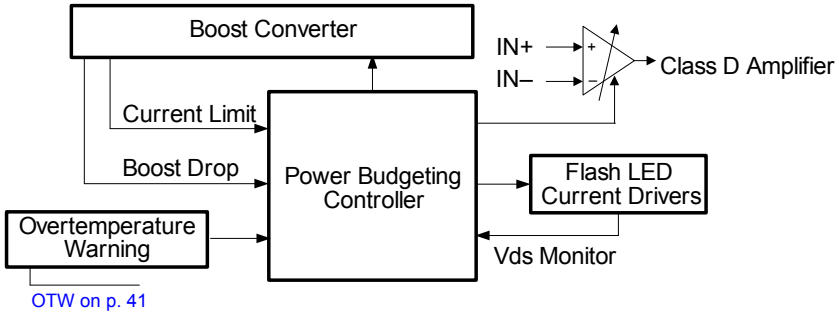


Figure 4-8. Power Budgeting Block Diagram

4.10.1 Audio-Only Operation

If only audio is operating, there are no power-budgeting concerns. As a default, the boost converter's output voltage is fixed in Bypass Mode (VBST = VP). The user can set VBOOST_MNG (see p. 38) to any of the nondefault modes for a different boost behavior. Refer to Section 4.3.1.

4.10.2 LED-Only Operation

If only LEDs are operating, the user can select one of the following courses of action:

- By clearing ILED_MNG (see p. 38), LED current is managed automatically. If the CS35L32 enters load management mode due to a condition listed in Section 4.10, the current is iteratively reduced until the condition no longer exists.
- By setting ILED_MNG, the user maintains full control over LED current.

As a default, the boost converter's output voltage is fixed in Bypass Mode (VBST = VP). The user can set VBOOST_MNG to any of the nondefault modes for a different boost behavior. In particular, if VBOOST_MNG = 00 or 01 and load power consists of LEDs only, the CS35L32 adapts for low power dissipation by automatically reducing the LED driver voltage (Vds) at pins FLOUT1 and FLOUT2 and by reducing the boost converter's output voltage. Such operation increases boost converter efficiency, lowers temperature rise in the CS35L32, and increases battery run time. If VBOOST_MNG is set to 10 or 11, the CS35L32 does not adapt for low-power dissipation because the boost voltage is fixed.

4.10.3 Audio and LED Operation

When audio and LEDs are operating simultaneously, the user can select one of the following courses of action:

- By clearing AUDIOGAIN_MNG, if the CS35L32 enters load management mode due to the conditions listed in Section 4.10, audio gain is reduced once by 3 dB (no reduction for 9-dB gain). If the condition persists, the CS35L32 examines ILED_MNG and responds according to Section 4.10.2. Audio automatically recovers to the original volume after an LED event.
- By setting AUDIOGAIN_MNG, the user maintains full control over audio gain.

As a default, the boost converter's output voltage is fixed in Bypass Mode (VBST = VP). The user can set VBOOST_MNG to any of the nondefault modes for a different boost behavior. In particular, if VBOOST_MNG = 01 in the presence of LED and audio load power, the CS35L32 adapts for low-power dissipation by automatically reducing the LED driver voltage at pins FLOUT1 and FLOUT2 and by reducing the boost converter's output voltage. If VBOOST_MNG = 00 in the presence of LED and audio-load power, the boost converter's output voltage is determined by the higher of the two supply requirements for LED or audio Class G. In such a case, the CS35L32 cannot adapt for low power dissipation if audio Class G requires a 5-V supply, because of the higher audio signal. Refer to Section 4.3.2.

4.11 Audio/Data Serial Port (ADSP)

The ADSP transmits audio and data to and from the systems processor in traditional I²S Mode. Controls are provided to advise the device of the rate of the clocks being applied to its inputs when in Slave Mode. Likewise, the same controls are used to indicate the clock rates to be generated when operating as a clock master.

The serial port I/O interface consists of three signals, described in detail in Table 1-1:

- SCLK: Serial data shift clock
- LRCK: Provides the left/right clock, which identifies the start of each serialized data word and toggles at sample rate
- SDOUT: Serial data output

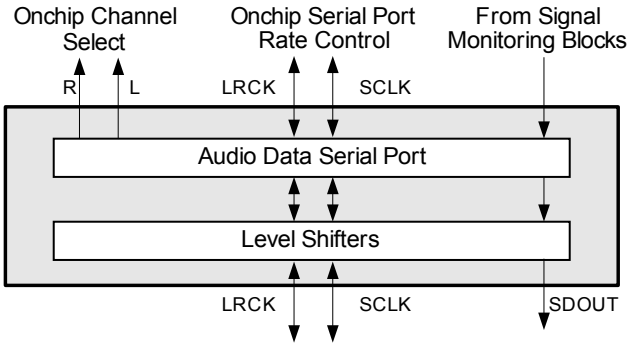


Figure 4-9. Audio/Data Serial Port (ADSP)

Table 4-5 provides links to register fields used to configure components shown in Fig. 4-9.

Table 4-5. ADSP Configuration

Register Field	Cross-Reference to Description
PDN_AMP	Section 7.5
SDOUT_3ST	Section 7.6
MCLKDIS, MCLKDIV2, RATIO	Section 7.7
M/S	Section 7.13
M_ADSPCLK_ERR	Section 7.16
ADSPCLK_ERR	Section 7.19

4.11.1 Power Up, Power Down, and Tristate

The serial port has separate power-down and tristate controls for its output data path (SDOUT_3ST, see p. 37). ADSP master/slave operation is governed only by the M/S setting (see p. 39), irrespective of the SDOUT_3ST setting. Table 4-6 describes ADSP operational mode and pin-output driver-state configuration.

Table 4-6. ADSP Operational Mode and Pin Configurations

M/S	SDOUT_3ST	ADSP Operational Mode	SDOUT Pin Driver	LRCK Pin Driver	SCLK Pin Driver
0	0	I²S Slave Mode	Output	Input	Input
0	1	I²S Slave Mode	Hi-Z	Input	Input
1	0	I²S Master Mode	Output	Output	Output
1	1	I²S Master Mode	Hi-Z	Output	Output

4.11.1.1 Tristating the ADSP SDOUT Path (SDOUT_3ST)

If the SDOUT functionality of the ADSP is not required, power losses caused by the charging and discharging of parasitic capacitances on this pin can be eliminated by setting SDOUT_3ST, so that the SDOUT line is tristated. When reactivating SDOUT, the associated circuits come alive and a full LRCK cycle elapses before SDOUT data is valid.

4.11.2 Master and Slave Timing

The serial port operates as either the master of timing or the slave to another device's timing. When the serial port is master, SCLK and LRCK are outputs; when it is a slave, they are inputs. Master/Slave Mode is configured by the M/S bit.

In I²S Master Mode, the SCLK and LRCK clock outputs are derived from $MCLK_{INT}$. SCLK is generated to have approximately 64 cycles per LRCK cycle.

In Slave Mode, because there is no sample-rate conversion from the serial port to the device core, the serial port audio sample rate (f_{LRCK}) must equal the core sample rate (Fs). To ensure that the CS35L32 maintains synchronization with the serial port sample rate, the RATIO divider (see p. 37) is programmed to indicate the sample rate to $MCLK_{INT}$ relationship.

Table 4-7 shows the corresponding RATIO ($f_{MCLK(INT)}/f_{LRCK}$) for each $MCLK_{INT}$ at the supported LRCK rate. In Master Mode, in a dual-CS35L32 configuration (see Section 4.12.3) with $MCLK_{INT}$ = 6 MHz, a ratio of 125 is not supported.

ADSPCLK_ERR (see p. 41) indicates when the ADSP attempts to resynchronize due to the absence of an LRCK edge at the expected time due to excessive jitter, misprogramming, or clock absence. Note that, given that the clock-checking circuit checks for LRCK edges appearing in the expected location relative to internal timing, if the LRCK frequency is an integer multiple of the expected rate (e.g., the LRCK rate is 96 kHz [2 x 48 kHz] vs. the expected 48 kHz), ADSPCLK_ERR does not detect this error condition. Also note that, since the clock-checking circuit monitors edges, if LRCK is removed and no further clock edges are produced, ADSPCLK_ERR triggers only once while the LRCK is removed.

Table 4-7 lists supported serial-port audio sample rates, their relationship to the $MCLK_{INT}$ rate, and the programming required to generate a given LRCK rate in Master Mode and ensure the serial port maintains synchronization in Slave Mode.

Table 4-7. ADSP Rates

$MCLK_{INT}$ Rate (MHz)	LRCK Rate (kHz)	$f_{MCLK(INT)}/f_{LRCK}$ (Rate Ratio)	RATIO
6.0000	48.000	125	1
6.1440	48.000	128	0

If all amplifier functionality is not being used, but CS35L32 clock mastering is desired, set up the clocks using the clocking control register controls, then set SDOUT_3ST. In this scenario, since the amplifier is inaccessible, it should be powered down to save power (PDN_AMP = 1).

4.11.3 ADSP in I²S Mode

The ADSP operates in traditional I²S format, with a minor modification. On the transmit side, the data structure is modified to transmit nonconventional data (e.g., the monitored signals) in a compatible format. Receive Mode is not supported.

4.11.3.1 Data Bit Depths

The data word length of the I²S interface format is ambiguous. Fortunately, the I²S format is also left justified, with a MSB-to-LSB bit ordering, which negates the need for a word-length control register. The following text describes how different bit depths are handled with the I²S format.