Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CIRRUS LOGIC®

CS4202

Audio Codec '97 with Headphone Amplifier

Features

- AC '97 2.2 Compliant
- Exceeds the Microsoft® PC 2001 Audio Performance Requirements
- Integrated High-Performance Headphone Amplifier
- On-chip PLL for use with External Clock Sources
- Integrated High-Performance Microphone Pre-Amplifier
- Automatic Jack Sense through GPIO
- BIOS-Driver Interface for Audio Feature Configuration through Software
- S/PDIF Digital Audio Output
- I^2S Serial Digital Outputs Enable Cost Effective Six Channel Applications
- Independent Simultaneous S/PDIF and Six Channel Audio Playback
- 20-bit Stereo Digital-to-Analog Converters
- 18-bit Stereo Analog-to-Digital Converters
- Sample Rate Converters
- Three Analog Line-level Stereo Inputs
- High Quality Pseudo-Differential CD Input
- Two Analog Line-level Mono Inputs
- Dual Microphone Inputs
- Stereo and Mono Line-level Outputs
- Extensive Power Management Support

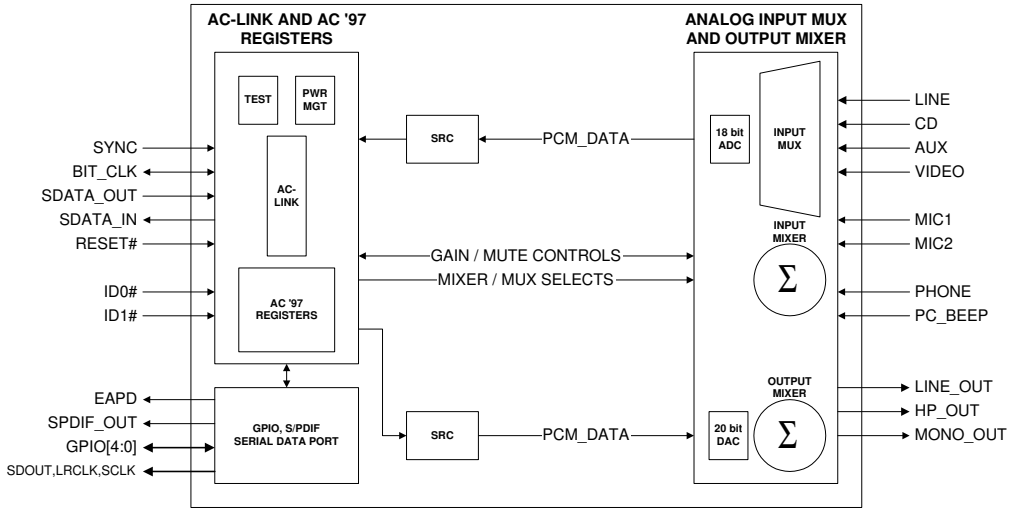
Description

The CS4202 is an AC '97 2.2 compliant stereo audio codec designed for PC multimedia systems. It uses industry leading delta-sigma and mixed signal technology. This advanced technology and these features are designed to help enable the design of PC 99 and PC 2001 compliant high-quality audio systems for desktop, portable, and entertainment PCs.

Coupling the CS4202 with a PCI audio accelerator or core logic supporting the AC '97 interface implements a cost effective, superior quality audio solution. The CS4202 surpasses PC 99, PC 2001, and AC '97 2.2 audio quality standards.

ORDERING INFO

CS4202-JQZ, Lead Free 48-pin TQFP 9x9x1.4 mm



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

TABLE OF CONTENTS

Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com/corporate/contacts/sales.cfm

LIST OF FIGURES

LIST OF TABLES

1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS

(Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V ±5%, DVdd = 3.3 V ±5%; 1 kHz Input Sine wave; Sample Frequency, Fs = 48 kHz; Z_{AL}=100 kΩ/ 1000 pF load for Mono and Line Outputs; C_{DL} = 18 pF load (Note 1); Measurement bandwidth is 20 Hz - 20 kHz, 18-bit linear coding for ADC functions, 20-bit linear coding for DAC functions; Mixer registers set for unity gain.

Parameter (Note 2)	Symbol	Path (Note 3)	CS4202-JQZ			Unit
			Min	Typ	Max	
Full Scale Input Voltage						
Line Inputs		A-D	0.91	1.00	-	V_{RMS}
Mic Inputs (10dB = 0, 20dB = 0)		A-D	0.91	1.00	-	V_{RMS}
Mic Inputs (10dB = 1, 20dB = 0)		A-D	0.283	0.315	-	V_{RMS}
Mic Inputs (10dB = 0, 20dB = 1)		A-D	0.091	0.10	-	V_{RMS}
Mic Inputs (10dB = 1, 20dB = 1)		A-D	0.0283	0.0315	-	V_{RMS}
Full Scale Output Voltage						
Line and Mono Outputs		D-A	0.91	1.0	1.13	V_{RMS}
Headphone Output		D-A	-	1.4	-	V_{RMS}
Frequency Response (Note 4)	FR					
Analog Ac = ± 0.25 dB		A-A	20	-	20,000	Hz
DAC Ac = ± 0.25 dB		D-A	20	-	20,000	Hz
ADC Ac = ± 0.25 dB		A-D	20	-	20,000	Hz
Dynamic Range	DR					
Stereo Analog Inputs to LINE_OUT		A-A	90	95	-	dB FS A
Mono Analog Input to LINE_OUT		A-A	85	90	-	dB FS A
DAC Dynamic Range		D-A	85	90	-	dB FS A
ADC Dynamic Range		A-D	85	90	-	dB FS A
DAC SNR	SNR					
(-20 dB FS input w/ CCIR-RMS filter on output)		D-A	-	70	-	dB
Total Harmonic Distortion + Noise	THD+N					
(-3 dB FS input signal):						
Line Output		A-A	-	-90	-80	dB FS
Headphone Output		A-A	-	-75	-70	dB FS
DAC		D-A	-	-87	-80	dB FS
ADC (all inputs)		A-D	-	-84	-80	dB FS
Power Supply Rejection Ratio						
(1 kHz, 0.5 V_{RMS} w/ 5 V DC offset) (Note 4)			40	60	-	dB
Interchannel Isolation			70	87	-	dB
Spurious Tone (Note 4)			-	-100	-	dB FS
Input Impedance (Note 4)			10	-	-	kΩ

Notes:
1. Z_{AL} refers to the analog output pin loading and C_{DL} refers to the digital output pin loading.
2. Parameter definitions are given in Section 13, *Parameter and Term Definitions*.
3. Path refers to the signal path used to generate this data. These paths are defined in Section 13, *Parameter and Term Definitions*.
4. This specification is guaranteed by silicon characterization; it is not production tested.

ANALOG CHARACTERISTICS (Continued)

Parameter (Note 2)	Symbol	Path (Note 3)	CS4202-JQZ Min	CS4202-JQZ Typ	CS4202-JQZ Max	Unit
External Load Impedance						
Line Output, Mono Output			10	-	-	kΩ
Headphone Output			32	-	-	Ω
Output Impedance						
Line Output, Mono Output			-	730	-	Ω
Headphone Output (Note 4)			-	0.8	-	Ω
Input Capacitance (Note 4)			-	5	-	pF
Vrefout			2.3	2.4	2.5	V

MIXER CHARACTERISTICS

Parameter	Min	Typ	Max	Unit
Mixer Gain Range Span				
PC Beep	-	45.0	-	dB
Line In, Aux, CD, Video, Mic1, Mic2, Phone	-	46.5	-	dB
Mono Out, Line Out, Headphone Out	-	46.5	-	dB
ADC Gain	-	22.5	-	dB
Step Size				
All volume controls except PC Beep	-	1.5	-	dB
PC Beep	-	3.0	-	dB

ABSOLUTE MAXIMUM RATINGS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter		Min	Typ	Max	Unit
Power Supplies	+3.3 V Digital	-0.3	-	5.5	V
	+5 V Digital	-0.3	-	5.5	V
	Analog	-0.3	-	5.5	V
Total Power Dissipation	(Supplies, Inputs, Outputs)	-	-	1.25	W
Input Current per Pin	(Except Supply Pins)	-10	-	10	mA
Output Current per Pin	(Except Supply Pins)	-15	-	15	mA
Analog Input voltage		-0.3	-	AVdd+ 0.3	V
Digital Input voltage		-0.3	-	DVdd + 0.3	V
Ambient Temperature	(Power Applied)	0	-	70	°C
Storage Temperature		-65	-	150	°C

RECOMMENDED OPERATING CONDITIONS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	+3.3 V Digital	DVdd1, DVdd2	3.135	3.3	3.465	V
	+5 V Digital	DVdd1, DVdd2	4.75	5	5.25	V
	Analog	AVdd1, AVdd2	4.75	5	5.25	V
Operating Ambient Temperature			0	-	70	°C

DIGITAL CHARACTERISTICS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
DVdd = 3.3V					
Low level input voltage	V_{il}	-	-	0.80	V
High level input voltage	V_{ih}	2.15	-	-	V
High level output voltage	V_{oh}	3.00	3.25	-	V
Low level output voltage	V_{ol}	-	0.03	0.35	V
Input Leakage Current (AC-link inputs)		-10	-	10	µA
Output Leakage Current (Tri-stated AC-link outputs)		-10	-	10	µA
Output buffer drive current BIT_CLK, SDATA_IN SPDIF_OUT EAPD/SCLK, GPIO0/LRCLK, GPIO1/SDOUT, GPIO2, GPIO3, GPIO4/SDO2 (Note 4)		 - - -	 72 24 4	 - - -	 mA mA mA
DVdd = 5.0 V					
Low level input voltage	V_{il}	-	-	0.80	V
High level input voltage	V_{ih}	3.25	-	-	V
High level output voltage	V_{oh}	4.50	4.95	-	V
Low level output voltage	V_{ol}	-	0.03	0.35	V
Input Leakage Current (AC-link inputs)		-10	-	10	µA
Output Leakage Current (Tri-stated AC-link outputs)		-10	-	10	µA
Output buffer drive current BIT_CLK, SDATA_IN SPDIF_OUT EAPD/SCLK, GPIO0/LRCLK, GPIO1/SDOUT, GPIO2, GPIO3, GPIO4/SDO2 (Note 4)		 - - -	 72 24 4	 - - -	 mA mA mA

AC '97 SERIAL PORT TIMING

Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V, DVdd = 3.3 V; C_L = 55 pF load.

Parameter	Symbol	Min	Typ	Max	Unit
RESET Timing					
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK start-up delay (XTL mode)	$T_{rst2clk}$	-	4.0	-	µs
(OSC mode)		-	4.0	-	µs
(PLL mode)		-	2.5	-	ms
1st SYNC active to CODEC READY 'set'	$T_{sync2crd}$	-	62.5	-	µs
Vdd stable to RESET# inactive	$T_{vdd2rst\#}$	100	-	-	µs
Clocks					
BIT_CLK frequency	F_{clk}	-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter (depends on XTL_IN source)		-	-	750	ps
BIT_CLK high pulse width	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width	T_{clk_low}	36	40.7	45	ns
SYNC frequency	F_{sync}	-	48	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs
Data Setup and Hold					
Output propagation delay from rising edge of BIT_CLK	T_{co}	8	10	12	ns
Input setup time from falling edge of BIT_CLK	T_{isetup}	10	-	-	ns
Input hold time from falling edge of BIT_CLK	T_{ihold}	0	-	-	ns
Input signal rise time	T_{irise}	2	-	6	ns
Input signal fall time	T_{ifall}	2	-	6	ns
Output signal rise time (Note 4)	T_{orise}	2	4	6	ns
Output signal fall time (Note 4)	T_{ofall}	2	4	6	ns
Misc. Timing Parameters					
End of Slot 2 to BIT_CLK, SDATA_IN low (PR4)	T_{s2_pdown}	-	0.285	1.0	µs
SYNC pulse width (PR4) Warm Reset	T_{sync_pr4}	1.0	-	-	µs
SYNC inactive (PR4) to BIT_CLK start-up delay	$T_{sync2clk}$	162.8	285	-	ns
Setup to trailing edge of RESET# (ATE test mode) (Note 4)	$T_{setup2rst}$	15	-	-	ns
Rising edge of RESET# to Hi-Z delay (Note 4)	T_{off}	-	-	25	ns

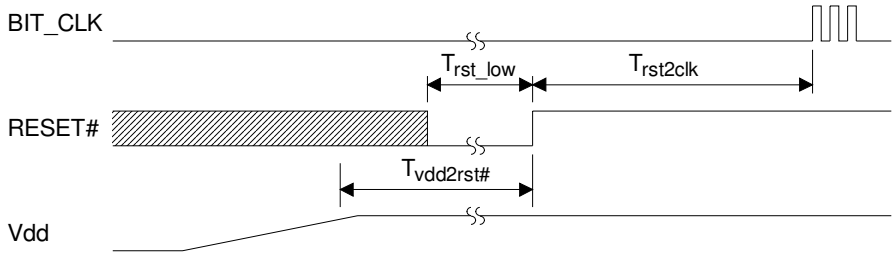


Figure 1. Power Up Timing

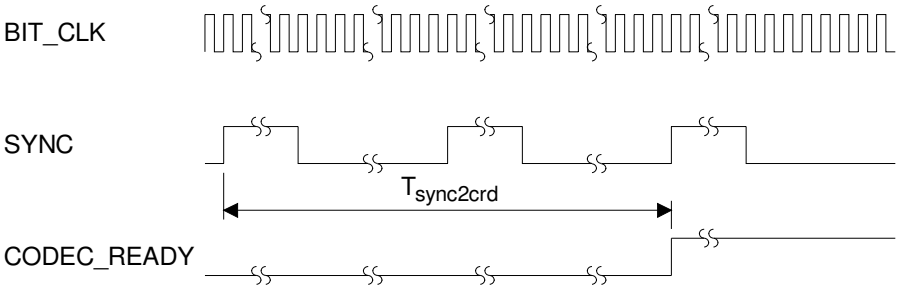


Figure 2. Codec Ready from Start-up or Fault Condition

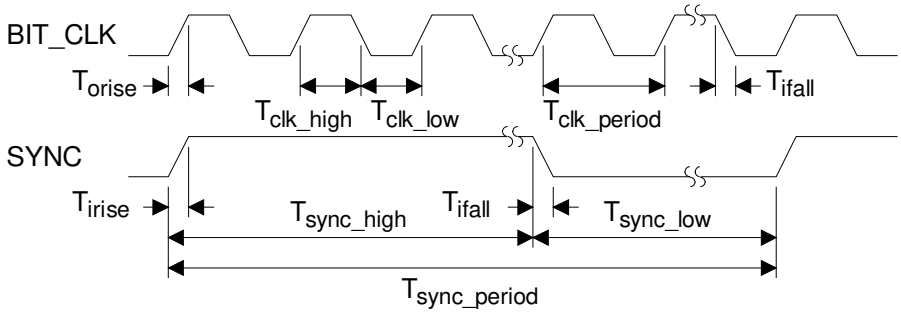


Figure 3. Clocks

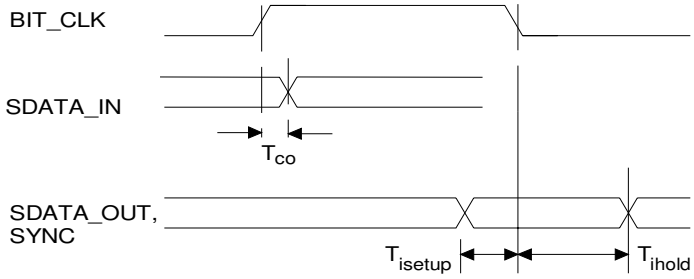


Figure 4. Data Setup and Hold

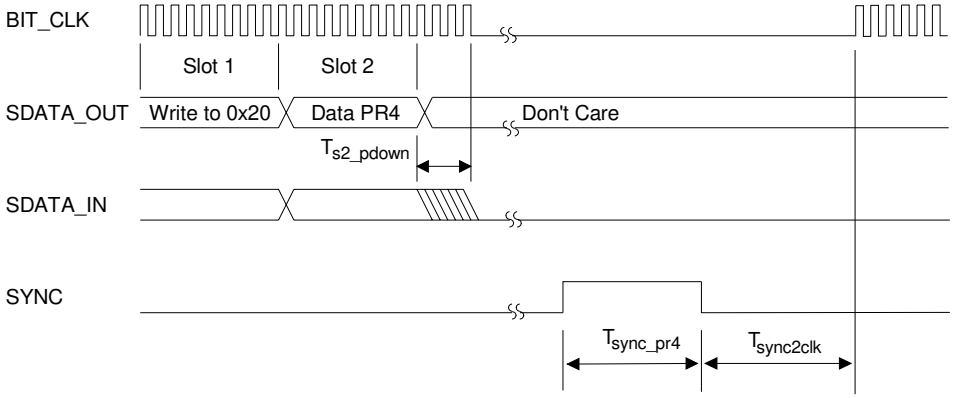


Figure 5. PR4 Powerdown and Warm Reset

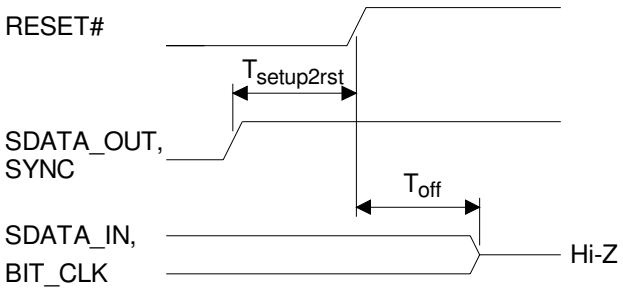


Figure 6. Test Mode

2. GENERAL DESCRIPTION

The CS4202 is a mixed-signal serial audio codec with integrated headphone power amplifier compliant with the Intel® *Audio Codec '97 Specification*, revision 2.2 [6] (referred to as AC '97). It is designed to be paired with a digital controller, typically located on the PCI bus or integrated within the system core logic chip set. The controller is responsible for all communications between the CS4202 and the remainder of the system. The CS4202 contains two distinct functional sections: digital and analog. The digital section includes the AC-link interface, S/PDIF interface, serial data port, GPIO, power management support, and Sample Rate Converters (SRCs). The analog section includes the analog input multiplexer (mux), stereo input mixer, stereo output mixer, mono output mixer, headphone amplifier, stereo Analog-to-Digital Converters (ADCs), stereo Digital-to-Analog Converters (DACs), and their associated volume controls.

2.1 AC-Link

All communication with the CS4202 is established with a 5-wire digital interface to the controller called the AC-link. This interface is shown in Figure 7. All clocking for the serial communication is synchronous to the BIT_CLK signal. BIT_CLK is generated by the primary audio codec and is used to clock the controller and any secondary audio codecs. Both input and output AC-link audio frames are organized as a sequence of 256 serial bits forming 13 groups referred to as 'slots'. During each audio frame, data is passed bi-directionally between the CS4202 and the controller. The input frame is driven from the CS4202 on the SDATA_IN line. The output frame is driven from the controller on the SDATA_OUT line. The controller is also responsible for issuing reset commands via the RESET# signal. Following a Cold Reset, the CS4202 is responsible for notifying the controller that it is ready for operation after synchronizing its internal functions. The CS4202 AC-link signals must use the same digital supply voltage as the controller, either +5 V or +3.3 V. See Section 3, *AC-Link Frame Definition*, for detailed AC-link information.

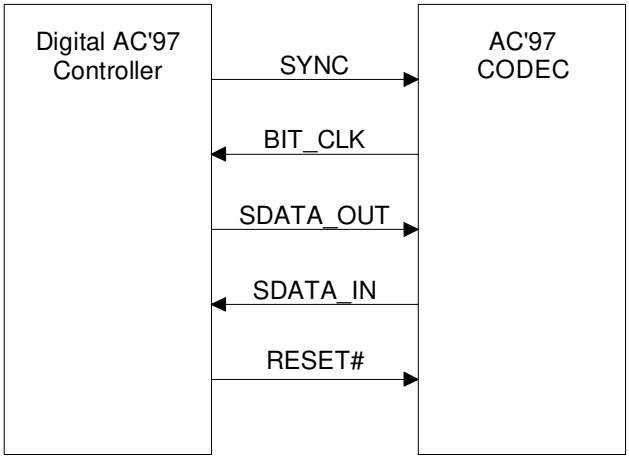


Figure 7. AC-link Connections

2.2 Control Registers

The CS4202 contains a set of AC '97 compliant control registers, and a set of Cirrus Logic defined control registers. These registers control the basic functions and features of the CS4202. Read accesses of the control registers by the AC '97 controller are accomplished with the requested register index in Slot 1 of a SDATA_OUT frame. The following SDATA_IN frame will contain the read data in Slot 2. Write operations are similar, with the register index in Slot 1 and the write data in Slot 2 of a SDATA_OUT frame. The function of each input and output frame is detailed in Section 3, *AC-Link Frame Definition*. Individual register descriptions are found in Section 4, *Register Interface*.

2.3 Sample Rate Converters

The sample rate converters (SRC) provide high accuracy digital filters supporting sample frequencies other than 48 kHz to be captured from the CS4202 or played from the controller. AC '97 requires support for two audio rates (44.1 and 48 kHz). In addition, the Intel® I/O Controller Hub (ICHx) specification [9] requires support for five more audio rates (8, 11.025, 16, 22.05, and 32 kHz). The CS4202 supports all these rates, as shown in Table 10 on page 32.

2.4 Mixers

The CS4202 input and output mixers are illustrated in Figure 8. The stereo input mixer sums together the analog inputs to the CS4202 according to the settings in the volume control registers. The stereo output mixer sums the output of the stereo input mixer with the PC_BEEP and PHONE signals. The stereo output mix is then sent to the LINE_OUT and HP_OUT pins of the CS4202. The mono output mixer generates a monophonic sum of the left and right audio channels from the stereo input mixer. The mono output mix is then sent to the MONO_OUT pin on the CS4202.

2.5 Input Mux

The input multiplexer controls which analog input is sent to the ADCs. The output of the input mux is converted to stereo 18-bit digital PCM data and transmitted to the controller by means of the AC-link SDATA_IN signal.

2.6 Volume Control

The CS4202 volume registers control analog input levels to the input mixer and analog output levels, including the master volume level. The PC_BEEP volume control uses 3 dB steps with a range of 0 dB to -45 dB attenuation. All other analog volume controls use 1.5 dB steps. The analog inputs have a mixing range of +12 dB signal gain to -34.5 dB signal attenuation. The analog output volume controls have a range of 0 dB to -46.5 dB attenuation for LINE_OUT, HP_OUT and MONO_OUT.

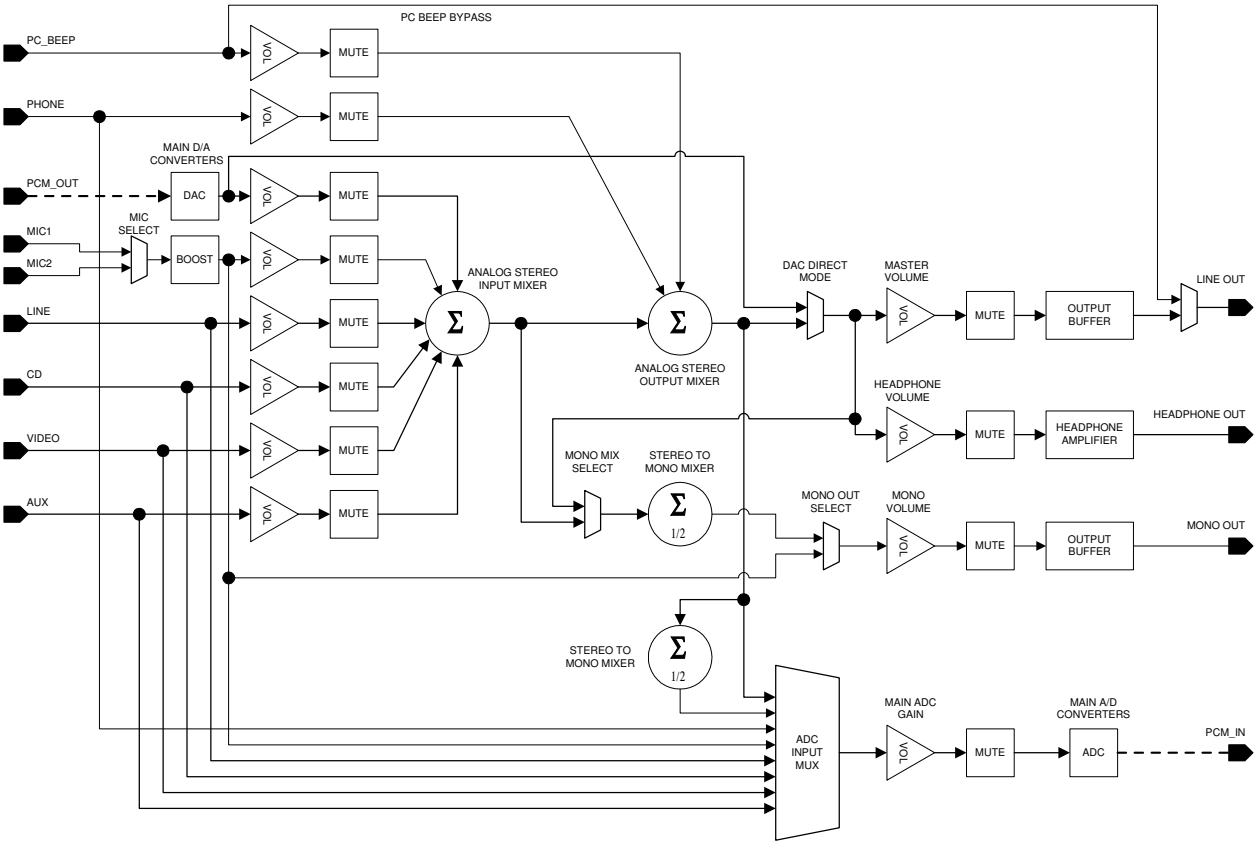


Figure 8. CS4202 Mixer Diagram

3. AC-LINK FRAME DEFINITION

The AC-link is a bi-directional serial port with data organized into frames consisting of one 16-bit and twelve 20-bit time-division multiplexed slots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-link protocol infrastructure. Slots 1 through 12 contain audio or control/status data. Both the serial data output and input frames are defined from the controller perspective, not from the CS4202 perspective.

The controller synchronizes the beginning of a frame with the assertion of the SYNC signal. Figure 9 shows the position of each bit location within the frame. The first bit position in a new serial data frame is F0 and the last bit position in the serial data frame is F255. When SYNC goes active (high) and is sampled active by the CS4202 (on the falling edge of BIT_CLK), both devices are synchronized to a new serial data frame. The data on the SDATA_OUT pin at this clock edge is the final bit of the previous frame's serial data. On the next rising edge of BIT_CLK, the first bit of Slot 0 is driven by the controller on the SDATA_OUT pin. On the next falling edge of BIT_CLK, the CS4202 latches this data in as the first bit of the frame.

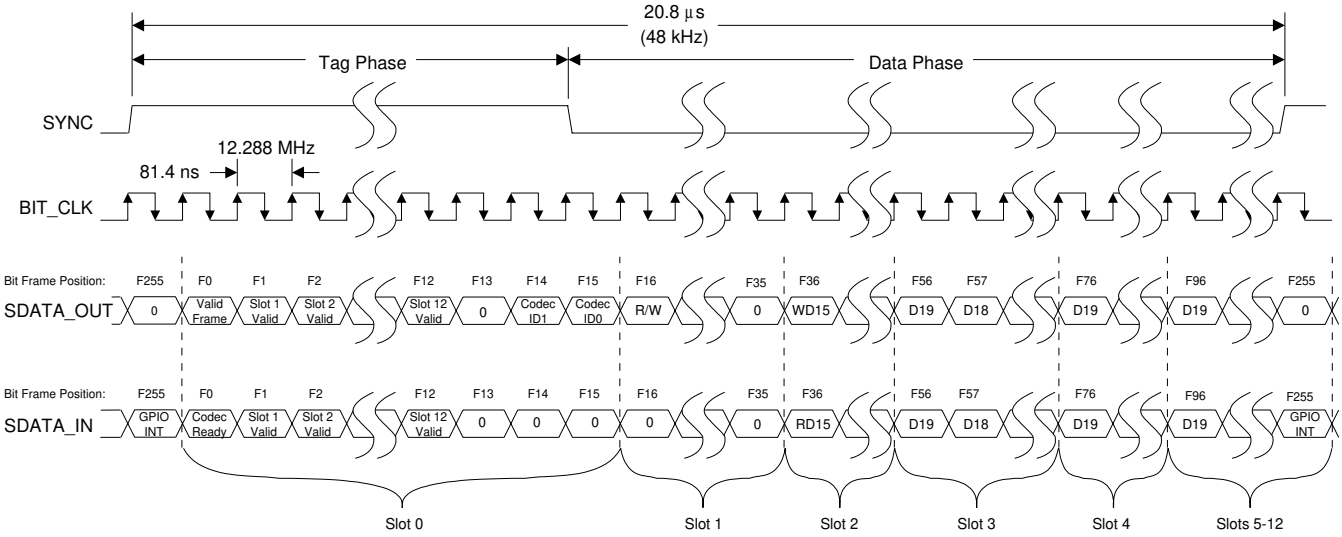


Figure 9. AC-link Input and Output Framing

3.1 AC-Link Serial Data Output Frame

In the serial data output frame, data is passed on the SDATA_OUT pin to the CS4202 from the AC '97 controller. Figure 9 illustrates the serial port timing.

The PCM playback data being passed to the CS4202 is shifted out MSB first in the most significant bits of each slot. Any PCM data from the AC '97 controller that is not 20 bits wide should be left justified in its corresponding slot and dithered or zero-padded in the unused bit positions.

Bits that are reserved should always be 'cleared' by the AC '97 controller.

3.1.1 Serial Data Output Slot Tags (Slot 0)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Valid Frame	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	Not Implem	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	Slot 9 Valid	Slot 10 Valid	Slot 11 Valid	Slot 12 Valid	Res	Codec ID1	Codec ID0

Valid Frame — The Valid Frame bit determines if any of the following slots contain either valid playback data for the CS4202 or data for read/write operations. When 'set', at least one of the other AC-link slots contains valid data. If this bit is 'clear', the remainder of the frame is ignored.

Slot 1 Valid — The Slot 1 Valid bit indicates a valid register read/write address for a primary codec.

Slot 2 Valid — The Slot 2 Valid bit indicates valid register write data for a primary codec.

Slot [3:4,6:11] Valid — The Slot [3:4,6:11] Valid bits indicate the validity of data in their corresponding serial data output slots. If a bit is 'set', the corresponding output slot contains valid data. If a bit is 'cleared', the corresponding slot will be ignored.

Slot 12 Valid — The Slot 12 Valid bit indicates if output Slot 12 contains valid GPIO control data.

Codec ID[1:0] — The Codec ID[1:0] bits determine which codec is being accessed during the current AC-link frame. Codec ID[1:0] = 00 indicates the primary codec is being accessed. Codec ID[1:0] = 01, 10, or 11 indicates one of three possible secondary codecs is being accessed. A Codec ID value of 01, 10, or 11 also indicates a valid read/write address and/or valid register write data for a secondary codec.

3.1.2 Command Address Port (Slot 1)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/$\overline{W}$	RI6	RI5	RI4	RI3	RI2	RI1	RI0	Reserved											

R/$\overline{W}$ — Read/$\overline{Write}$. When this bit is 'set', a read of the AC '97 register specified by the register index bits will occur in the AC '97 2.x audio codec. When the bit is 'cleared', a write will occur. For any read or write access to occur, the Valid Frame bit (F0) must be 'set' and the Codec ID[1:0] bits (F[14:15]) must match the Codec ID of the AC '97 2.x audio codec being accessed. Additionally, for a primary codec, the Slot 1 Valid bit (F1) must be 'set' for a read access and both the Slot 1 Valid bit (F1) and the Slot 2 Valid bit (F2) must be 'set' for a write access. For a secondary codec, both the Slot 1 Valid bit (F1) and the Slot 2 Valid bit (F2) must be 'cleared' for read and write accesses. See Figure 9 for bit frame positions.

RI[6:0] — Register Index. The RI[6:0] bits contain the 7-bit register index to the AC '97 registers in the CS4202. All registers are defined at word addressable boundaries. The RI0 bit must be 'clear' to access CS4202 registers.

3.1.3 Command Data Port (Slot 2)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	Reserved			

WD[15:0] Write Data. The WD[15:0] bits contain the 16-bit value to be written to the register. If an access is a read, this slot is ignored.

NOTE: For any write to an AC '97 register, the write is defined to be an 'atomic' access. This means that when the Slot 1 Valid bit in output Slot 0 is 'set', the Slot 2 Valid bit in output Slot 0 should always be 'set' during the same audio frame. No write access may be split across 2 frames.

3.1.4 PCM Playback Data (Slots 3-4,6-11)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD[19:0] Playback Data. The PD[19:0] bits contain the 20-bit PCM (2's complement) playback data for the left and right DACs, serial data ports, and/or the S/PDIF transmitter. Table 8 on page 30 lists a cross reference for each function and its respective slot. The mapping of a given slot to the DAC, serial data port, or S/PDIF transmitter is determined by the state of the DSA[1:0] bits in the *Extended Audio ID Register (Index 28h)* and the SPSA[1:0] bits in the *Extended Audio Status/Control Register (Index 2Ah).*

3.1.5 GPIO Pin Control (Slot12)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Implemented											GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	Reserved			

GPIO[4:0] GPIO Pin Control. The GPIO[4:0] bits control the CS4202 GPIO pins configured as outputs. Write accesses using GPIO pin control bits configured as outputs will be reflected on the GPIO pin output on the next AC-link frame. Write accesses using GPIO pin control bits configured as inputs will have no effect and are ignored. If the GPOC bit in the *Misc. Crystal Control Register (Index 60h)* is 'set', the bits in output Slot 12 are ignored and GPIO pins configured as outputs are controlled through the *GPIO Pin Status Register (Index 54h)*.

3.2 AC-Link Serial Data Input Frame

In the serial data input frame, data is passed on the SDATA_IN pin from the CS4202 to the AC '97 controller. The data format for the input frame is very similar to the output frame. Figure 9 on page 15 illustrates the serial port timing.

The PCM capture data from the CS4202 is shifted out MSB first in the most significant 18 bits of each slot. The least significant 2 bits in each slot will be 'cleared'. If the host requests PCM data from the AC '97 Controller that is less than 18 bits wide, the controller should dither and round or just round (but not truncate) to the desired bit depth.

Bits that are reserved or not implemented in the CS4202 will always be returned 'cleared'.

3.2.1 Serial Data Input Slot Tag Bits (Slot 0)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Codec Ready	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	0	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	0	0	Slot 11 Valid	Slot 12 Valid	Reserved		

Codec Ready — Codec Ready. The Codec Ready bit indicates the readiness of the CS4202 AC-link. Immediately after a Cold Reset this bit will be 'clear'. Once the CS4202 clocks and voltages are stable, this bit will be 'set'. Until the Codec Ready bit is 'set', no AC-link transactions should be attempted by the controller. The Codec Ready bit does not indicate readiness of the DACs, ADCs, Vref, or any other analog function. Those must be checked in the *Powerdown Control/Status Register (Index 26h)* by the controller before any access is made to the mixer registers. Any accesses to the CS4202 while Codec Ready is 'clear' are ignored.

Slot 1 Valid — The Slot 1 Valid bit indicates Slot 1 contains a valid read back address.

Slot 2 Valid — The Slot 2 Valid bit indicates Slot 2 contains valid register read data.

Slot [3:4,6:8,11] Valid — The Slot [3:4,6:8,11] Valid bits indicate Slot [3:4,6:8,11] contains valid capture data from the CS4202 ADCs. If a bit is 'set', the corresponding input slot contains valid data. If a bit is 'cleared', the corresponding slot will be ignored.

Slot 12 Valid — The Slot 12 Valid bit indicates Slot 12 contains valid GPIO status data.

3.2.2 Status Address Port (Slot 1)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	RI6	RI5	RI4	RI3	RI2	RI1	RI0	SR3	SR4	0	SR6	SR7	SR8	SR9	SR10	SR11	0	Reserved	

RI[6:0] — Register Index. The RI[6:0] bits echo the AC '97 register address when a register read has been requested in the previous frame. The CS4202 will only echo the register index for a read access. Write accesses will not return valid data in Slot 1.

SR[3:4,6:11] — Slot Request. If SRx is 'set', this indicates the CS4202 SRC does not need a new sample on the next AC-link frame for that particular slot. If SRx is 'clear', the SRC indicates a new sample is needed on the following frame. If the VRA bit in the *Extended Audio Status/Control Register (Index 2Ah)* is 'clear', the SR[3:4,6:11] bits are always 0. When VRA is 'set', the SRC is enabled and the SR[3:4,6:11] bits are used to request data.

3.2.3 Status Data Port (Slot 2)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	Reserved			

RD[15:0] Read Data. The RD[15:0] bits contain the register data requested by the controller from the previous read request. All read requests will return the read address in the input Slot 1 and the register data in the input Slot 2 on the following serial data frame.

3.2.4 PCM Capture Data (Slot 3-4,6-8,11)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CD17	CD16	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	0	0

CD[17:0] Capture Data. The CD [17:0] bits contain 18-bit PCM (2's complement) capture data. The data will only be valid when the respective slot valid bit is 'set' in input Slot 0. The mapping of a given slot to an ADC is determined by the state of the ASA[1:0] bits in the *AC Mode Control Register (index 5Eh)*. The definition of each slot can be found in Table 8 on page 30.

3.2.5 GPIO Pin Status (Slot 12)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	Res	BDI	Res	GPIO_INT

GPIO[4:0] GPIO Pin Status. The GPIO[4:0] bits reflect the status of the CS4202 GPIO pins configured as inputs. The pin status of GPIO pins configured as outputs will be reflected back on the GPIO[4:0] bits of input Slot 12 in the next frame. The output GPIO pins are controlled by the GPIO[4:0] pin control bits in output Slot 12.

BDI BIOS-Driver Interface. The BDI bit indicates that a BIOS event has occurred. This bit is a logic OR of all bits in the *BDI Status Register (Index 7Ah)* ANDed with their corresponding bit in the *BDI Config Register (Index 70h)*.

GPIO_INT GPIO Interrupt. The GPIO_INT bit indicates that a GPIO or BDI interrupt event has occurred. The occurrence of a GPIO interrupt is determined by the GPIO interrupt requirements as outlined in the *GPIO Pin Wakeup Mask Register (Index 52h)* description. In this case, the GPIO_INT bit is cleared by writing a '0' to the bit in the *GPIO Pin Status Register (Index 54h)* corresponding to the GPIO pin which generated the interrupt.

The occurrence of a BDI interrupt is determined by the BDI interrupt requirements as outlined in the *BDI Control Registers (Index 70h - 72h)*. In this case, the GPIO_INT bit is cleared by writing a '0' to the bit in the *BDI Status Register (Index 7Ah)* that generated the interrupt.

3.3 AC-Link Protocol Violation - Loss of SYNC

The CS4202 is designed to handle SYNC protocol violations. The following are situations where the SYNC protocol has been violated:

- The SYNC signal is not sampled high for exactly 16 BIT_CLK clock cycles at the start of an audio frame.
- The SYNC signal is not sampled high on the 256th BIT_CLK clock period after the previous SYNC assertion.
- The SYNC signal goes active high before the 256th BIT_CLK clock period after the previous SYNC assertion.

Upon loss of synchronization with the controller, the CS4202 will 'clear' the Codec Ready bit in the serial data input frame until two valid frames are detected. During this detection period, the CS4202 will ignore all register reads and writes and will discontinue the transmission of PCM capture data. In addition, if the LOSM bit in the *Misc. Crystal Control Register (Index 60h)* is 'set' (default), the CS4202 will mute all analog outputs. If the LOSM bit is 'clear', the analog outputs will not be muted.

4. REGISTER INTERFACE

Reg	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	0	0	0	0	0	0	ID8	ID7	0	0	ID4	0	0	0	0	0190h
02h	Master Volume	Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	Headphone Volume	Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono Volume	Mute	0	0	0	0	0	0	0	0	0	MM5	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	0	0	0	0	0	0	0	0	0	0	PV3	PV2	PV1	PV0	0	0000h
0Ch	Phone Volume	Mute	0	0	0	0	0	0	0	0	0	0	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	0	0	0	0	0	0	0	0	20dB	0	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	0	0	0	0	0	SL2	SL1	SL0	0	0	0	0	0	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	0	0	0	GL3	GL2	GL1	GL0	0	0	0	0	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	0	0	0	0	0	0	MIX	MS	LPBK	0	0	0	0	0	0	0	0000h
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	0	0	0	0	REF	ANL	DAC	ADC	000Fh
28h	Ext'd Audio ID	ID1	ID0	0	0	REV1	REV0	AMAP	0	0	0	DSA1	DSA0	0	SPDIF	0	VRA	x605h
2Ah	Ext'd Audio Stat/Ctrl	0	0	0	0	0	SPCV	0	0	0	0	SPSA1	SPSA0	0	SPDIF	0	VRA	0410h
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM L/R ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
3Ah	S/PDIF Control	V	DRS	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUDIO	PRO	2000h
3Ch	Ext'd Modem ID	ID1	ID0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x000h
3Eh	Ext'd Modem Stat/Ctrl	0	0	0	0	0	0	0	PRA	0	0	0	0	0	0	0	GPIO	0100h
4Ch	GPIO Pin Config.	0	0	0	0	0	0	0	0	0	0	0	GC4	GC3	GC2	GC1	GC0	001Fh
4Eh	GPIO Pin Polarity/Type	1	1	1	1	1	1	1	1	1	1	1	GP4	GP3	GP2	GP1	GP0	FFFFh
50h	GPIO Pin Sticky	0	0	0	0	0	0	0	0	0	0	0	GS4	GS3	GS2	GS1	GS0	0000h
52h	GPIO Pin Wakeup	0	0	0	0	0	0	0	0	0	0	0	GW4	GW3	GW2	GW1	GW0	0000h
54h	GPIO Pin Status	0	0	0	0	0	0	0	0	0	0	0	GI4	GI3	GI2	GI1	GI0	0000h
Cirrus Logic Defined Registers:																		
5Eh	AC Mode Control	0	0	0	0	ASPM	0	TMM	DDM	0	0	ASA1	ASA0	0	0	0	0	0000h
60h	Misc. Crystal Control	0	0	0	DPC	0	0	Reserved		10dB	CRST	0	0	GPOC	Reserved		LOSM	0003h
6Ah	Serial Port Control	SDEN	0	0	0	0	0	0	0	0	0	0	0	SDO2	SDSC	SDF1	SDF0	0000h
70h	BDI Config	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	0000h
72h	BDI Wakeup	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	0000h
7Ah	BDI Status	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	0000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4352h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	0	DID2	DID1	DID0	0	REV2	REV1	REV0	5971h

Table 1. Register Overview for the CS4202

4.1 Reset Register (Index 00h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	ID8	ID7	0	0	ID4	0	0	0	0

ID8 — 18-bit ADC Resolution. The ID8 bit is 'set', indicating this feature is present.

ID7 — 20-bit DAC resolution. The ID7 bit is 'set', indicating this feature is present.

ID4 — Headphone Out. The ID4 bit is 'set', indicating this feature is present. The state of this bit depends on the state of the HPCFG pin.

Default — 0190h. The data in this register is read-only data.

Any write to this register causes a Register Reset of the audio control *(Index 00h - 3Ah)* and Cirrus Logic defined *(Index 5Ah - 7Ah)* registers. A read from this register returns configuration information about the CS4202.

4.2 Analog Mixer Output Volume Registers (Index 02h - 04h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0

Mute — Output Mute. Setting this bit mutes the LINE_OUT_L/R or HP_OUT_L/R output signals.

ML[5:0] — Output Volume Left. These bits control the left output volume. Each step corresponds to 1.5 dB gain adjustment, with a total available range from 0 dB to -46.5 dB attenuation. Setting the ML5 bit sets the left channel attenuation to -46.5 dB by forcing ML[4:0] to a '1' state. ML[5:0] will read back 011111 when ML5 has been 'set'. See Table 2 for further details.

MR[5:0] — Output Volume Right. These bits control the right output volume. Each step corresponds to 1.5 dB gain adjustment, with a total available range from 0 dB to -46.5 dB attenuation. Setting the MR5 bit sets the right channel attenuation to -46.5 dB by forcing MR[4:0] to a '1' state. MR[5:0] will read back 011111 when MR5 has been 'set'. See Table 2 for further details.

Default — 8000h. This value corresponds to 0 dB attenuation and Mute 'set'.

If the HPCFG pin is left floating, register 02h controls the Master Output Volume and register 04h controls the Headphone Output Volume. If the HPCFG pin is tied 'low', register 02h controls the Headphone Volume and register 04h is a read-only register and always returns 0000h when 'read'.

Mx5 - Mx0 Write	Mx5 - Mx0 Read	Gain Level
000000	000000	0 dB
000001	000001	-1.5 dB
…	…	...
011111	011111	-46.5 dB
100000	011111	-46.5 dB
...	...	...
111111	011111	-46.5 dB

Table 2. Analog Mixer Output Attenuation

4.3 Mono Volume Register (Index 06h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	0	MM5	MM4	MM3	MM2	MM1	MM0

Mute — Mono Mute. Setting this bit mutes the MONO_OUT output signal.

MM[5:0] — Mono Volume Control. The MM[5:0] bits control the mono output volume. Each step corresponds to 1.5 dB gain adjustment, with a total available range from 0 dB to -46.5 dB attenuation. Setting the MM5 bit sets the mono attenuation to -46.5 dB by forcing MM[4:0] to a '1' state. MM[5:0] will read back 011111 when MM5 has been 'set'. See Table 2 on page 22 for further attenuation levels.

Default — 8000h. This value corresponds to 0 dB attenuation and Mute 'set'.

4.4 PC_BEEP Volume Register (Index 0Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	0	0	PV3	PV2	PV1	PV0	0

Mute — PC_BEEP Mute. Setting this bit mutes the PC_BEEP input signal.

PV[3:0] — PC_BEEP Volume Control. The PV[3:0] bits control the gain levels of the PC_BEEP input source to the Input Mixer. Each step corresponds to 3 dB gain adjustment, with 0000 = 0 dB. The total range is 0 dB to -45 dB attenuation.

Default — 0000h. This value corresponds to 0 dB attenuation and Mute 'clear'.

This register has no effect on the PC_BEEP volume during RESET#.

4.5 Phone Volume Register (Index 0Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	0	0	GN4	GN3	GN2	GN1	GN0

Mute — Phone Mute. Setting this bit mutes the Phone input signal.

GN[5:0] — Phone Volume Control. The GN[4:0] bits control the gain level of the Phone input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB attenuation. See Table 4 on page 25 for further attenuation levels.

Default — 8008h. This value corresponds to 0 dB attenuation and Mute 'set'.

4.6 Microphone Volume Register (Index 0Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	20dB	0	GN4	GN3	GN2	GN1	GN0

Mute — Microphone Mute. Setting this bit mutes the MIC1 or MIC2 signal. The selection of the MIC1 or MIC2 input pin is controlled by the MS bit in the *General Purpose Register (Index 20h)*.

20dB — Microphone 20 dB Boost. When 'set', the 20dB bit enables the +20 dB microphone boost block. In combination with the 10dB boost bit in the *Misc. Crystal Control Register (Index 60h)* this bit allows for variable boost from 0 dB to +30 dB in steps of 10 dB. Table 3 summarizes this behavior.

GN[4:0] — Microphone Volume Control. The GN[4:0] bits are used to control the gain level of the Microphone input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 3 for further details.

Default — 8008h. This value corresponds to 0 dB gain and Mute 'set'.

GN4 - GN0	Gain Level			
	10dB = 0, 20dB = 0	10dB = 1, 20dB = 0	10dB = 0, 20dB = 1	10dB = 1, 20dB = 1
00000	+12.0 dB	+22.0 dB	+32.0 dB	+42.0 dB
00001	+10.5 dB	+20.5 dB	+30.5 dB	+40.5 dB
…	…	...	...	...
00111	+1.5 dB	+11.5 dB	+21.5 dB	+31.5 dB
01000	0.0 dB	+10.0 dB	+20.0 dB	+30.0 dB
01001	-1.5 dB	+8.5 dB	+18.5 dB	+28.5 dB
…	…	...	...	...
11111	-34.5 dB	-24.5 dB	-14.5 dB	-4.5 dB

Table 3. Microphone Input Gain Values

4.7 Analog Mixer Input Gain Registers (Index 10h - 18h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0

Mute — Stereo Input Mute. Setting this bit mutes the respective input signal, both right and left inputs.

GL[4:0] — Left Volume Control. The GL[4:0] bits are used to control the gain level of the left analog input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 4 for further details.

GR[4:0] — Right Volume Control. The GR[4:0] bits are used to control the gain level of the right analog input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 4 for further details.

Default — 8808h. This value corresponds to 0 dB gain and Mute ‘set’.

The Analog Mixer Input Gain Registers are listed in Table 5.

Gx4 - Gx0	Gain Level
00000	+12.0 dB
00001	+10.5 dB
…	…
00111	+1.5 dB
01000	0.0 dB
01001	-1.5 dB
…	…
11111	-34.5 dB

Table 4. Analog Mixer Input Gain Values

Register Index	Function
10h	Line In Volume
12h	CD Volume
14h	Video Volume
16h	Aux Volume
18h	PCM Out Volume

Table 5. Analog Mixer Input Gain Register Index