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CS4205

CrystalClear® Audio Codec '97 for Portable Computing

Features

- Integrated Asynchronous I^2S Input Port (ZV Port)
- Integrated High-Performance Microphone Pre-Amplifier
- Integrated Digital Effects Processing for Bass and Treble Response
- Digital Docking Including an I^2S Output, 3 Synchronous I^2S Inputs
- Performance Oriented Digital Mixer
- SRS© 3D Stereo Enhancement
- On-chip PLL for use with External Clock Sources
- Dedicated Microphone Analog-to-Digital Converter
- Sample Rate Converters
- S/PDIF Digital Audio Output
- AC '97 2.1 Compliant
- PC Beep Bypass
- 20-bit Stereo Digital-to-Analog Converters
- 18-bit Stereo Analog-to-Digital Converters
- Three Analog Line-level Stereo Inputs for LINE IN, VIDEO, and AUX
- High Quality Pseudo-Differential CD Input
- Extensive Power Management Support
- Meets or Exceeds the Microsoft® PC 99 and PC 2001 Audio Performance Requirements

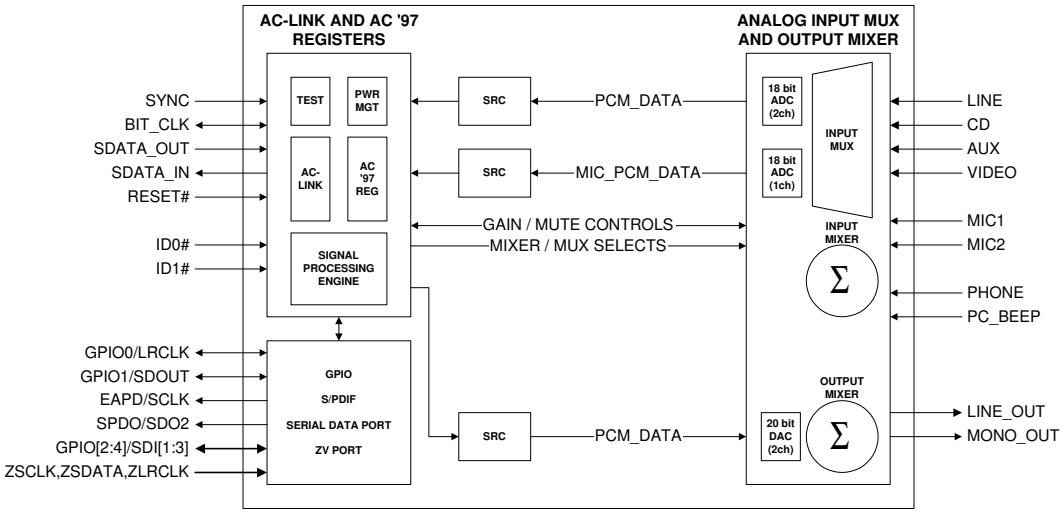
Description

The CS4205 is an AC '97 2.1 compliant stereo audio codec designed for PC multimedia systems. It uses industry leading CrystalClear® delta-sigma and mixed signal technology. The CS405 is the first Cirrus AC '97 audio codec to feature digital centric mixing and digital effects. This advanced technology and these features are designed to help enable the design of PC 99 and PC 2001 compliant high-quality audio systems for desktop, portable, and entertainment PCs.

Coupling the CS4205 with a PCI audio accelerator or core logic supporting the AC '97 interface implements a cost effective, superior quality audio solution. The CS4205 surpasses PC 99, PC 2001, and AC '97 2.1 audio quality standards.

ORDERING INFO

CS4205-KQZ, Lead Free 48-pin TQFP 9x9x1.4 mm



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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http://www.cirrus.com/corporate/contacts/sales.cfm

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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS

(Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V ±5%, DVdd = 3.3 V ±5%; 1 kHz Input Sine wave; Sample Frequency, Fs = 48 kHz; Z_{AL}=100 kΩ/ 1000 pF load for Mono and Line Outputs; C_{DL} = 18 pF load (Note 1); Measurement bandwidth is 20 Hz - 20 kHz, 18-bit linear coding for ADC functions, 20-bit linear coding for DAC functions; Mixer registers set for unity gain.

Parameter (Note 2)	Symbol	Path (Note 3)	CS4205-KQZ			Unit
			Min	Typ	Max	
Full Scale Input Voltage						
Line Inputs		A-D	0.91	1.00	-	V_{RMS}
Mic Inputs (10dB = 0, 20dB = 0)		A-D	0.91	1.00	-	V_{RMS}
Mic Inputs (10dB = 1, 20dB = 0)		A-D	0.283	0.315	-	V_{RMS}
Mic Inputs (10dB = 0, 20dB = 1)		A-D	0.091	0.10	-	V_{RMS}
Mic Inputs (10dB = 1, 20dB = 1)		A-D	0.0283	0.0315	-	V_{RMS}
Full Scale Output Voltage						
Line and Mono Outputs		D-A	0.91	1.0	1.13	V_{RMS}
Frequency Response (Note 4)	FR					
Analog Ac = ± 0.25 dB		A-A	20	-	20,000	Hz
DAC Ac = ± 0.25 dB		D-A	20	-	20,000	Hz
ADC Ac = ± 0.25 dB		A-D	20	-	20,000	Hz
Dynamic Range	DR					
Stereo Analog Inputs to LINE_OUT		A-A	90	95	-	dB FS A
Mono Analog Input to LINE_OUT		A-A	85	90	-	dB FS A
DAC Dynamic Range		D-A	85	90	-	dB FS A
ADC Dynamic Range		A-D	85	90	-	dB FS A
DAC SNR	SNR					
(-20 dB FS input w/ CCIR-RMS filter on output)		D-A	-	70	-	dB
Total Harmonic Distortion + Noise	THD+N					
(-3 dB FS input signal):						
Line Output		A-A	-	-90	-80	dB FS
DAC		D-A	-	-87	-80	dB FS
ADC (all inputs)		A-D	-	-84	-80	dB FS
Power Supply Rejection Ratio						
(1 kHz, 0.5 V_{RMS} w/ 5 V DC offset) (Note 4)			40	60	-	dB
Interchannel Isolation			70	87	-	dB
Spurious Tone (Note 4)			-	-100	-	dB FS
Input Impedance (Note 4)			10	-	-	kΩ

Notes:
1. Z_{AL} refers to the analog output pin loading and C_{DL} refers to the digital output pin loading.
2. Parameter definitions are given in Section 15, *Parameter and Term Definitions*.
3. Path refers to the signal path used to generate this data. These paths are defined in Section 15, *Parameter and Term Definitions*.
4. This specification is guaranteed by silicon characterization; it is not production tested.

ANALOG CHARACTERISTICS (Continued)

Parameter (Note 2)	Symbol	Path (Note 3)	CS4205-KQZ Min	CS4205-KQZ Typ	CS4205-KQZ Max	Unit
External Load Impedance Line Output, Mono Output			10	-	-	kΩ
Output Impedance Line Output, Mono Output (Note 4)			-	730	-	Ω
Input Capacitance (Note 4)			-	5	-	pF
Vrefout			2.3	2.4	2.5	V

MIXER CHARACTERISTICS

Parameter	Min	Typ	Max	Unit
Mixer Gain Range Span				
PC Beep	-	45.0	-	dB
Line In, Aux, CD, Video, Mic1, Mic2, Phone	-	46.5	-	dB
Mono Out, Line Out	-	46.5	-	dB
ADC Gain	-	22.5	-	dB
Step Size				
All volume controls except PC Beep	-	1.5	-	dB
PC Beep	-	3.0	-	dB

ABSOLUTE MAXIMUM RATINGS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter		Min	Typ	Max	Unit
Power Supplies	+3.3 V Digital	-0.3	-	5.5	V
	+5 V Digital	-0.3	-	5.5	V
	Analog	-0.3	-	5.5	V
Total Power Dissipation	(Supplies, Inputs, Outputs)	-	-	1.25	W
Input Current per Pin	(Except Supply Pins)	-10	-	10	mA
Output Current per Pin	(Except Supply Pins)	-15	-	15	mA
Analog Input voltage		-0.3	-	AVdd+ 0.3	V
Digital Input voltage		-0.3	-	DVdd + 0.3	V
Ambient Temperature	(Power Applied)	0	-	70	°C
Storage Temperature		-65	-	150	°C

RECOMMENDED OPERATING CONDITIONS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	+3.3 V Digital	DVdd1, DVdd2	3.135	3.3	3.465	V
	+5 V Digital	DVdd1, DVdd2	4.75	5	5.25	V
	Analog	AVdd1, AVdd2	4.75	5	5.25	V
Operating Ambient Temperature			0	-	70	°C

DIGITAL CHARACTERISTICS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
DVdd = 3.3V					
Low level input voltage	V_{il}	-	-	0.80	V
High level input voltage	V_{ih}	2.15	-	-	V
High level output voltage	V_{oh}	3.00	3.25	-	V
Low level output voltage	V_{ol}	-	0.03	0.35	V
Input Leakage Current (AC-link inputs)		-10	-	10	µA
Output Leakage Current (Tri-stated AC-link outputs)		-10	-	10	µA
Output buffer drive current BIT_CLK, SPDO/SDO2 SDATA_IN, EAPD/SCLK, GPIO0/LRCLK, GPIO1/SDOUT, GPIO2/SDI1, GPIO3/SDI2, GPIO4/SDI3 (Note 4)		- -	24 4	- -	mA mA
DVdd = 5.0 V					
Low level input voltage	V_{il}	-	-	0.80	V
High level input voltage	V_{ih}	3.25	-	-	V
High level output voltage	V_{oh}	4.50	4.95	-	V
Low level output voltage	V_{ol}	-	0.03	0.35	V
Input Leakage Current (AC-link inputs)		-10	-	10	µA
Output Leakage Current (Tri-stated AC-link outputs)		-10	-	10	µA
Output buffer drive current BIT_CLK, SPDO/SDO2 SDATA_IN, EAPD/SCLK, GPIO0/LRCLK, GPIO1/SDOUT, GPIO2/SDI1, GPIO3/SDI2, GPIO4/SDI3 (Note 4)		- -	24 4	- -	mA mA

AC '97 SERIAL PORT TIMING

Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V, DVdd = 3.3 V; C_L = 55 pF load.

Parameter	Symbol	Min	Typ	Max	Unit
RESET Timing					
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK start-up delay (XTL mode)	$T_{rst2clk}$	-	4.0	-	µs
(OSC mode)		-	4.0	-	µs
(PLL mode)		-	2.5	-	ms
1st SYNC active to CODEC READY 'set'	$T_{sync2crd}$	-	62.5	-	µs
Vdd stable to RESET# inactive	$T_{vdd2rst\#}$	100	-	-	µs
Clocks					
BIT_CLK frequency	F_{clk}	-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter (depends on XTL_IN source)		-	-	750	ps
BIT_CLK high pulse width	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width	T_{clk_low}	36	40.7	45	ns
SYNC frequency	F_{sync}	-	48	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs
Data Setup and Hold					
Output propagation delay from rising edge of BIT_CLK	T_{co}	8	10	12	ns
Input setup time from falling edge of BIT_CLK	T_{isetup}	10	-	-	ns
Input hold time from falling edge of BIT_CLK	T_{ihold}	0	-	-	ns
Input signal rise time	T_{irise}	2	-	6	ns
Input signal fall time	T_{ifall}	2	-	6	ns
Output signal rise time (Note 4)	T_{orise}	2	4	6	ns
Output signal fall time (Note 4)	T_{ofall}	2	4	6	ns
Misc. Timing Parameters					
End of Slot 2 to BIT_CLK, SDATA_IN low (PR4)	T_{s2_pdown}	-	0.2	1.0	µs
SYNC pulse width (PR4) Warm Reset	T_{sync_pr4}	1.0	-	-	µs
SYNC inactive (PR4) to BIT_CLK start-up delay	$T_{sync2clk}$	162.8	285	-	ns
Setup to trailing edge of RESET# (ATE test mode) (Note 4)	$T_{setup2rst}$	15	-	-	ns
Rising edge of RESET# to Hi-Z delay (Note 4)	T_{off}	-	-	25	ns

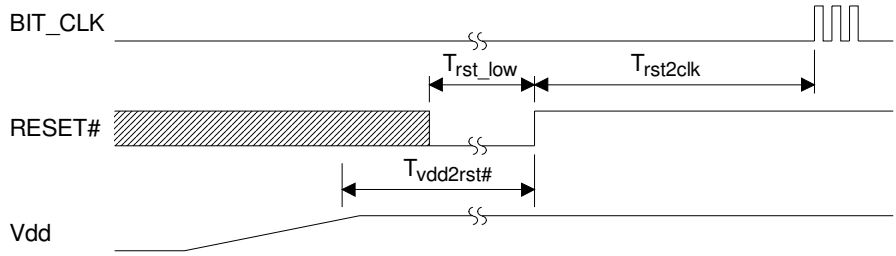

Figure 1. Power Up Timing

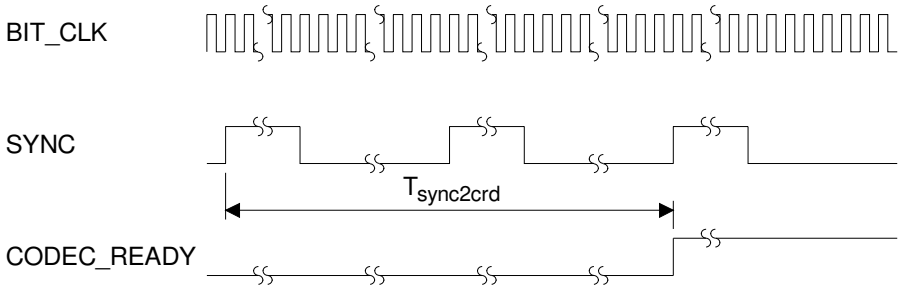

Figure 2. Codec Ready from Start-up or Fault Condition

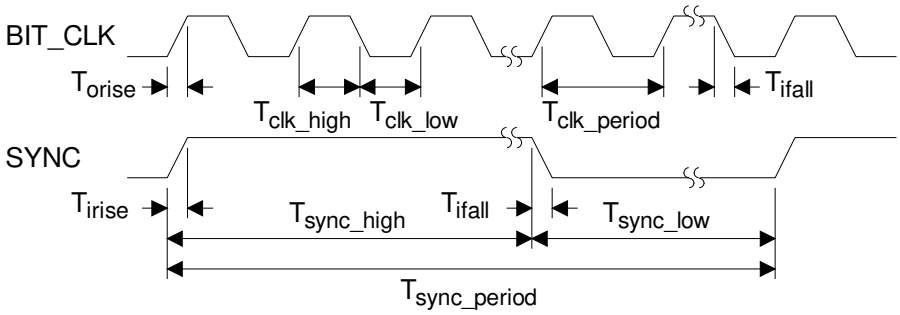

Figure 3. Clocks

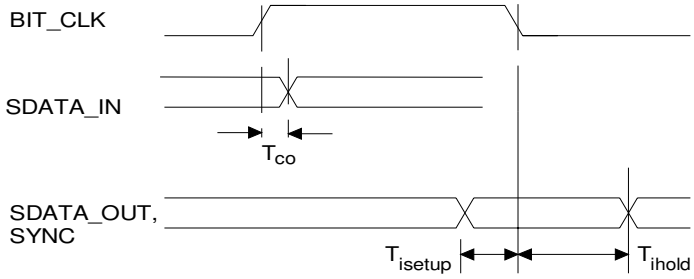

Figure 4. Data Setup and Hold

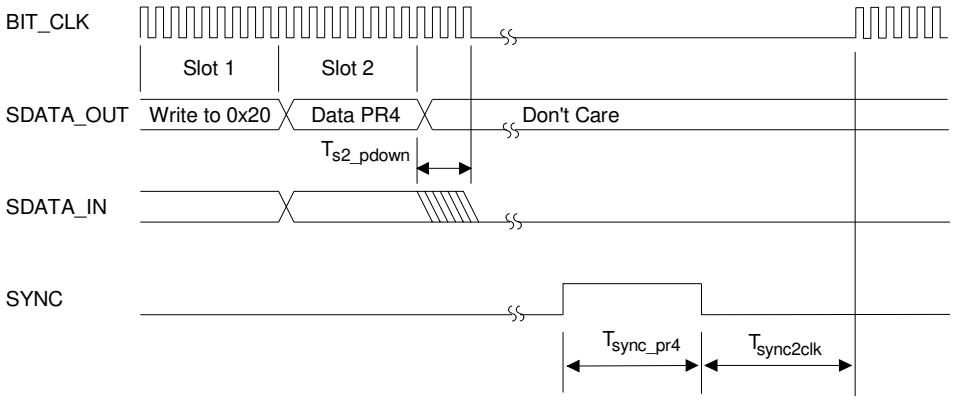

Figure 5. PR4 Powerdown and Warm Reset

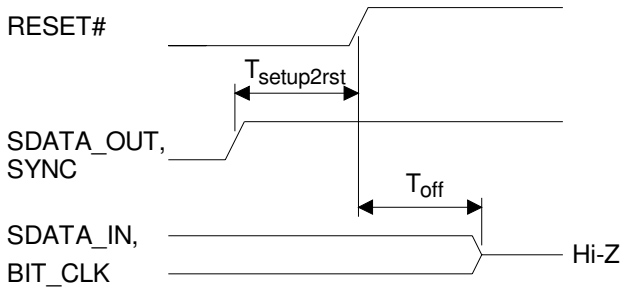

Figure 6. Test Mode

2. GENERAL DESCRIPTION

The CS4205 is a mixed-signal serial audio codec compliant with the Intel® *Audio Codec '97 Specification*, revision 2.1 [6] (referred to as AC '97). It is designed to be paired with a digital controller, typically located on the PCI bus or integrated within the system core logic chip set. The controller is responsible for all communications between the CS4205 and the remainder of the system. The CS4205 contains two distinct functional sections: digital and analog. The digital section includes the AC-link interface, S/PDIF interface, serial data port, GPIO, signal processing engine, ZV Port, power management support, and Sample Rate Converters (SRCs). The analog section includes the analog input multiplexer (mux), stereo input mixer, stereo output mixer, mono output mixer, stereo Analog-to-Digital Converters (ADCs), stereo Digital-to-Analog Converters (DACs), dedicated mono microphone ADC, and their associated volume controls.

2.1 AC-Link

All communication with the CS4205 is established with a 5-wire digital interface to the controller called the AC-link. This interface is shown in Figure 7. All clocking for the serial communication is synchronous to the BIT_CLK signal. BIT_CLK is generated by the primary audio codec and is used to clock the controller and any secondary audio codecs. Both input and output AC-link audio frames are organized as a sequence of 256 serial bits forming 13 groups referred to as 'slots'. During each audio frame, data is passed bi-directionally between the CS4205 and the controller. The input frame is driven from the CS4205 on the SDATA_IN line. The output frame is driven from the controller on the SDATA_OUT line. The controller is also responsible for issuing reset commands via the RESET# signal. Following a Cold Reset, the CS4205 is responsible for notifying the controller that it is ready for operation after synchronizing its internal functions. The CS4205 AC-link signals must use the same digital supply voltage as the controller, either +5 V or +3.3 V. See Section 4, *AC-Link Frame Definition*, for detailed AC-link information.

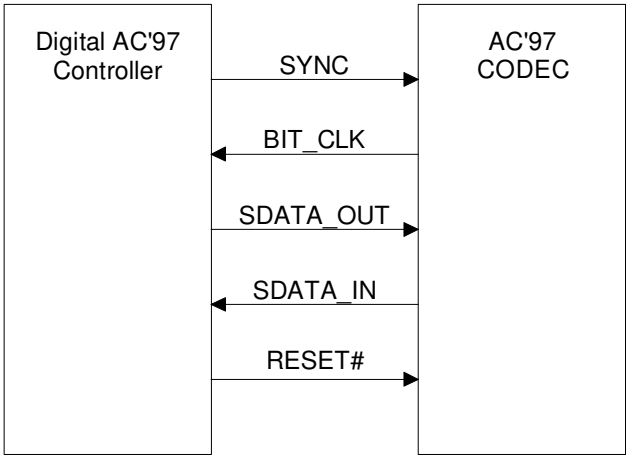

Figure 7. AC-link Connections

2.2 Control Registers

The CS4205 contains a set of AC '97 compliant control registers, and a set of Cirrus Logic defined control registers. These registers control the basic functions and features of the CS4205. Read accesses of the control registers by the AC '97 controller are accomplished with the requested register index in Slot 1 of a SDATA_OUT frame. The following SDATA_IN frame will contain the read data in Slot 2. Write operations are similar, with the register index in Slot 1 and the write data in Slot 2 of a SDATA_OUT frame. The function of each input and output frame is detailed in Section 4, *AC-Link Frame Definition*. Individual register descriptions are found in Section 5, *Register Interface*.

2.3 Sample Rate Converters

The sample rate converters (SRC) provide high accuracy digital filters supporting sample frequencies other than 48 kHz to be captured from the CS4205 or played from the controller. AC '97 requires support for two audio rates (44.1 and 48 kHz) and four modem rates (8, 9.6, 13.714, and 16 kHz). In addition, the Intel® I/O Controller Hub (ICHx) specification [9] requires support for five more audio rates (8, 11.025, 16, 22.05, and 32 kHz) and specifies two optional modem rates (24, 48kHz). The CS4205 supports all these rates, as shown in Table 12 on page 38.

2.4 Mixers

The CS4205 input and output mixers are illustrated in Figure 8. The stereo input mixer sums together the analog inputs to the CS4205 according to the settings in the volume control registers. The stereo output mixer sums the output of the stereo input mixer with the PC_BEEP and PHONE signals. The stereo output mix is then sent to the LINE_OUT pins of the CS4205. The mono output mixer generates a monophonic sum of the left and right audio channels from the stereo input mixer. The mono output mix is then sent to the MONO_OUT pin on the CS4205.

2.5 Input Mux

The input multiplexer controls which analog input is sent to the ADCs. The output of the input mux is converted to stereo 18-bit digital PCM data and transmitted to the controller by means of the AC-link SDATA_IN signal.

2.6 Volume Control

The CS4205 volume registers control analog input levels to the input mixer and analog output levels, including the master volume level. The PC_BEEP volume control uses 3 dB steps with a range of 0 dB to -45 dB attenuation. All other analog volume controls use 1.5 dB steps. The analog inputs have a mixing range of +12 dB signal gain to -34.5 dB signal attenuation. The analog output volume controls have a range of 0 dB to -46.5 dB attenuation for LINE_OUT and MONO_OUT.

2.7 Dedicated Mic Record Path

The CS4205 includes a dedicated microphone ADC that supports advanced functions such as speech recognition and internet telephony. The dedicated ADC allows recording of a microphone input independent of the input mux settings. This enables simultaneous capture of microphone and independent stereo sources.

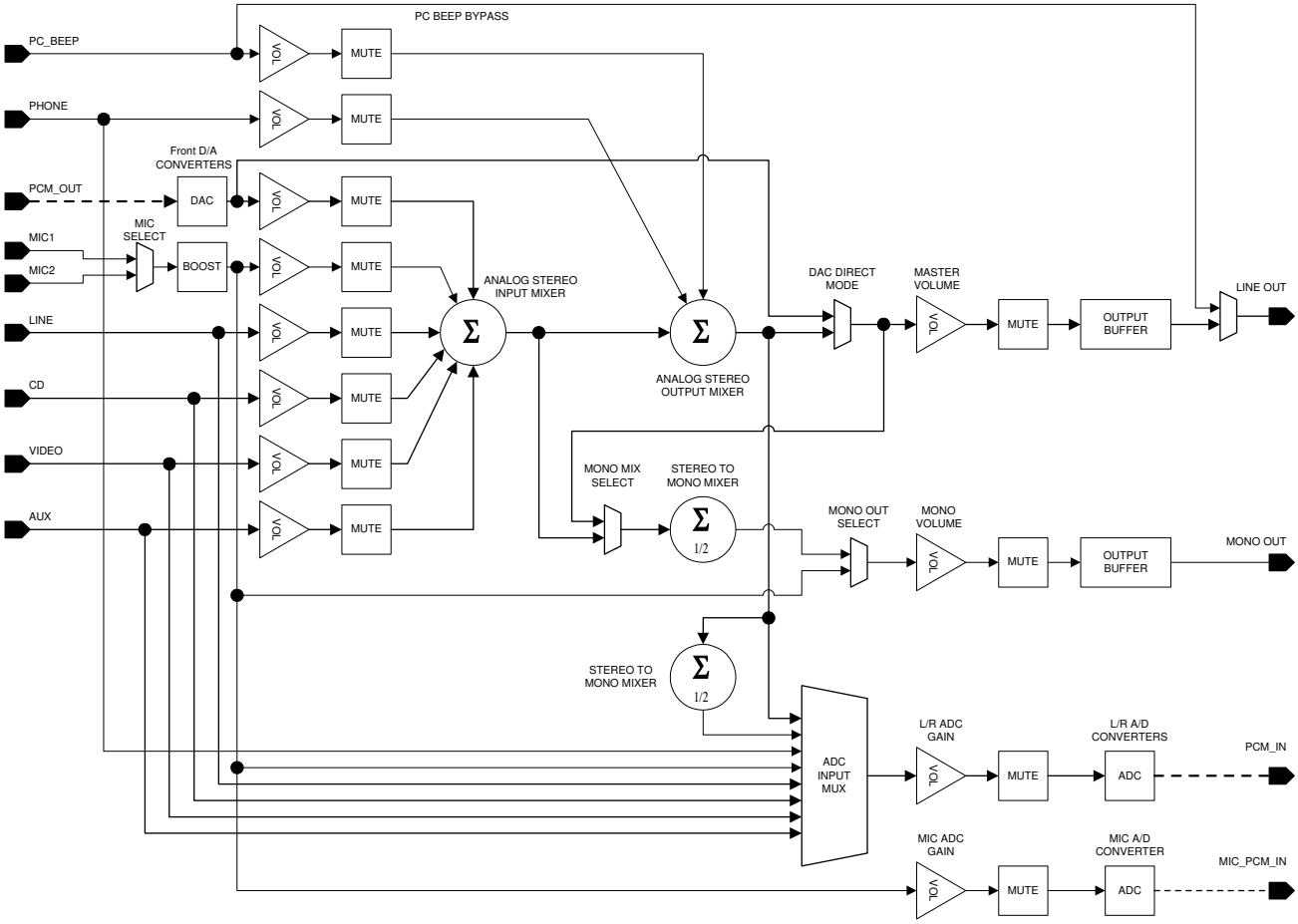

Figure 8. CS4205 Mixer Diagram

3. DIGITAL SIGNAL PATHS

The CS4205 includes a number of internal digital signal path options. Figure 9 shows the principal signal flow options through one channel of the device. Four commonly used signal flow modes are detailed in the following sections. The signal flow modes are controlled through the bits in the *AC Mode Control Register (Index 5Eh)*. The bit configuration for each detailed mode is listed in Table 1 on page 17.

3.1 Analog Centric Mode

Analog centric mode is detailed in Figure 10 on page 18. In this mode, all the digital sources are pre-mixed in the digital mixer and sent to the DACs. The DAC outputs are mixed with the analog sources in the analog mixer. The ADCs send captured data directly to the host. The ADC mux is used to select a single source or the output of the input mixer for capture. In the analog centric mode, effects processing is only available on digital sources.

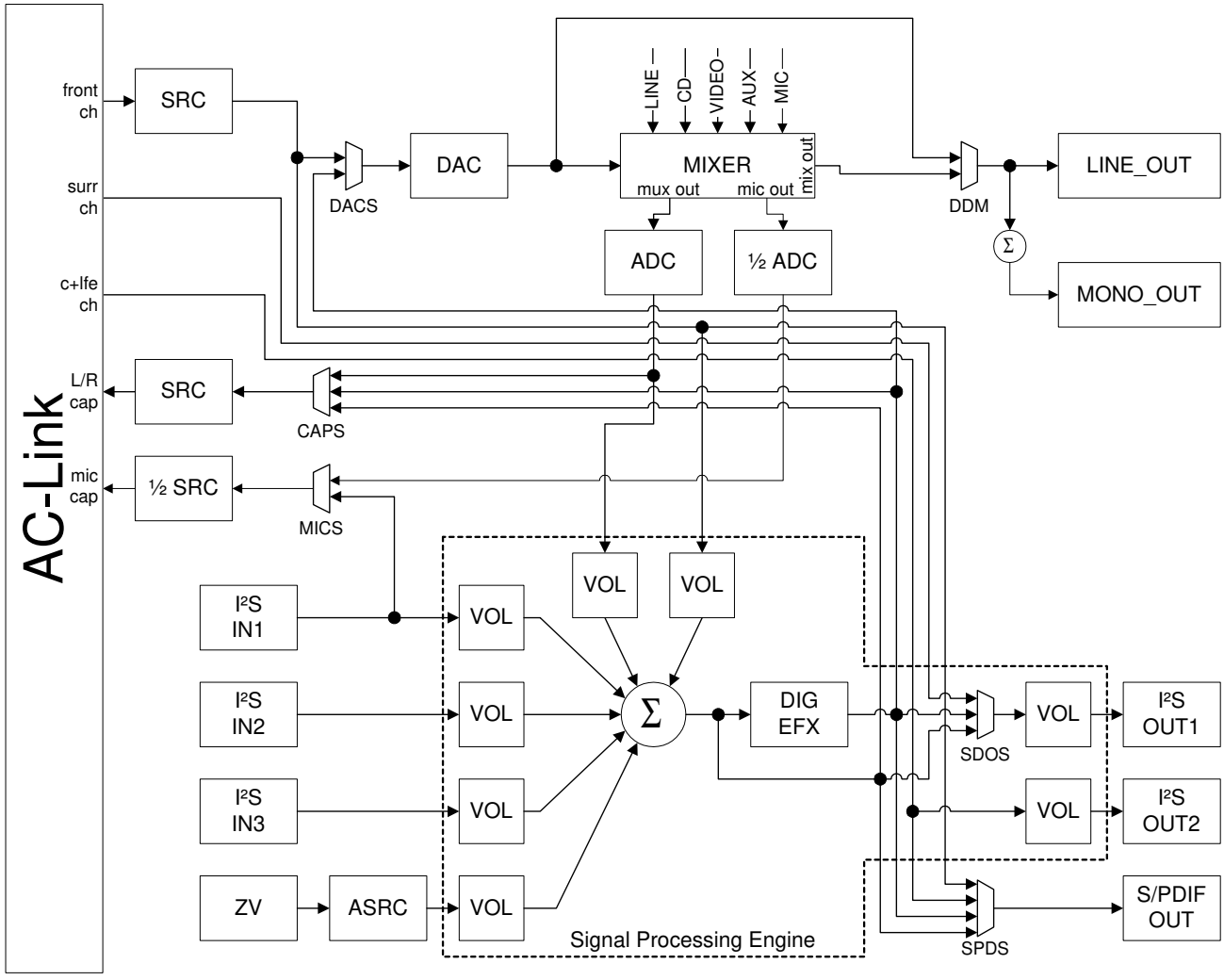

Figure 9. Digital Signal Path Overview

3.2 Digital Centric Mode

Digital centric mode is detailed in Figure 11. In this mode, the analog sources are first mixed in the analog mixer and sent to the ADCs. The ADC outputs are then mixed with the digital sources in the digital mixer. This allows effects processing on all sources and supports a "what you hear is what you record" model. The processed digital signal is sent to the DACs, bypassing the analog mixer using DAC direct mode. The ADC mux must be set to stereo mix to support this model. Consequently, only the mix can be captured by the host, rather than the individual sources.

3.3 Host Processing Mode

Host processing mode is detailed in Figure 12. This mode is similar to digital centric mode, except the output of the digital mixer is captured by the host. Any mixing with host sources and effects processing is done on the host. The processed signal is sent to the DACs, bypassing the analog mixer using DAC direct mode. In host processing mode, the playback and capture paths are completely separate inside the CS4205.

3.4 Multi-Channel Mode

Multi-channel mode is detailed in Figure 13. This mode is an extension of any of the other three modes, with the distinguishing feature that one or two additional slot pairs are routed to the serial data output ports. This allows for a complete multi-channel solution with a single AC '97 audio codec and external DACs.

AC Mode Control Bits	Analog Centric Mode	Digital Centric Mode	Host Processing Mode	Multi-Channel Mode
DACS	1	1	0	0 or 1
CAPS[1:0]	00	10	10	00,10 or 11
MICS	0 or 1	0 or 1	0 or 1	0 or 1
DDM	0	1	1	0 or 1
SDOS[1:0]	10 or 11	11	-	00
SPDS[1:0]	00, 01, 10 or 11	00, 01, 10 or 11	00 or 01	N/A

Table 1. AC Mode Control Configurations

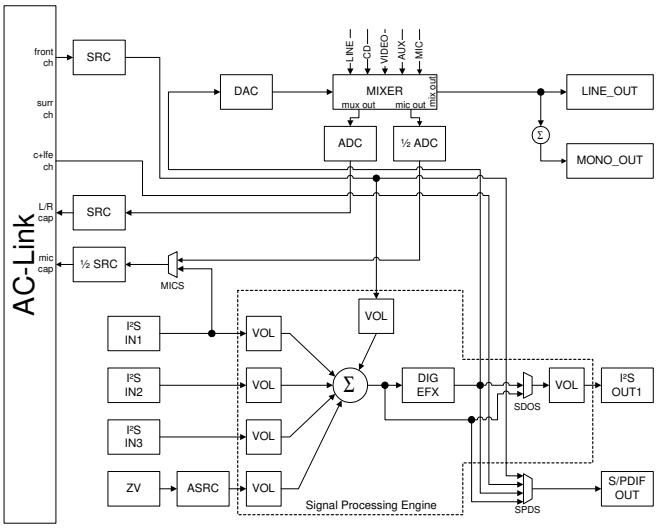

Figure 10. Analog Centric Mode

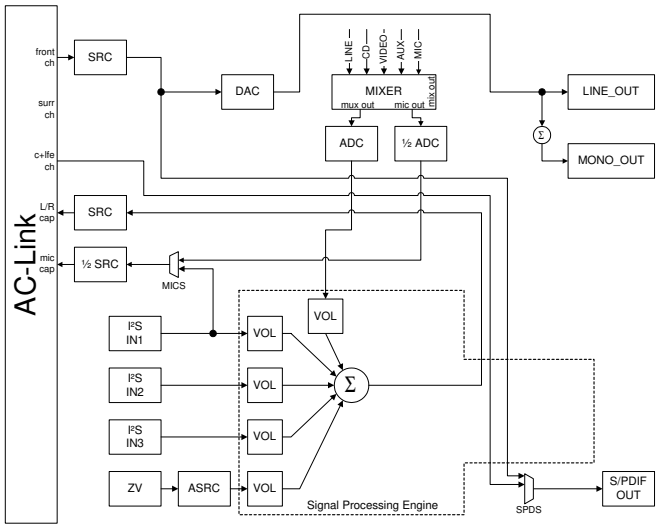

Figure 12. Host Processing Mode

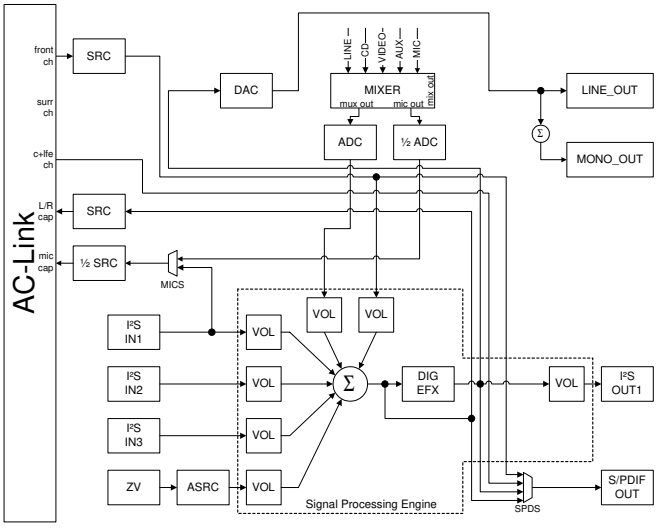

Figure 11. Digital Centric Mode

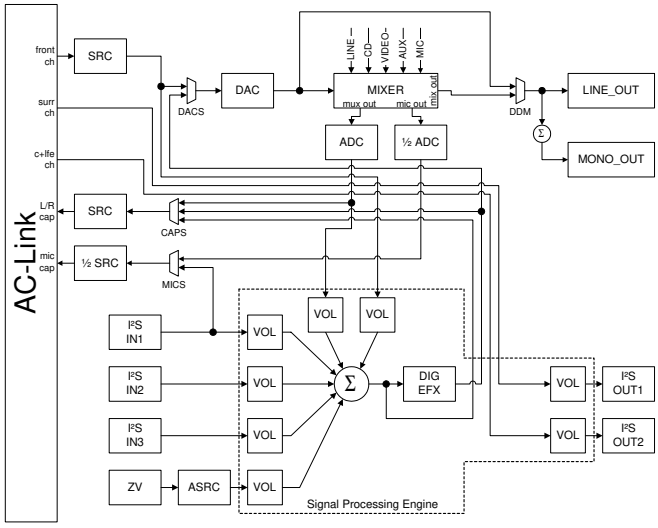

Figure 13. Multi-Channel Mode

4. AC-LINK FRAME DEFINITION

The AC-link is a bi-directional serial port with data organized into frames consisting of one 16-bit and twelve 20-bit time-division multiplexed slots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-link protocol infrastructure. Slots 1 through 12 contain audio or control/status data. Both the serial data output and input frames are defined from the controller perspective, not from the CS4205 perspective.

The controller synchronizes the beginning of a frame with the assertion of the SYNC signal. Figure 14 shows the position of each bit location within the frame. The first bit position in a new serial data frame is F0 and the last bit position in the serial data frame is F255. When SYNC goes active (high) and is sampled active by the CS4205 (on the falling edge of BIT_CLK), both devices are synchronized to a new serial data frame. The data on the SDATA_OUT pin at this clock edge is the final bit of the previous frame's serial data. On the next rising edge of BIT_CLK, the first bit of Slot 0 is driven by the controller on the SDATA_OUT pin. On the next falling edge of BIT_CLK, the CS4205 latches this data in as the first bit of the frame.

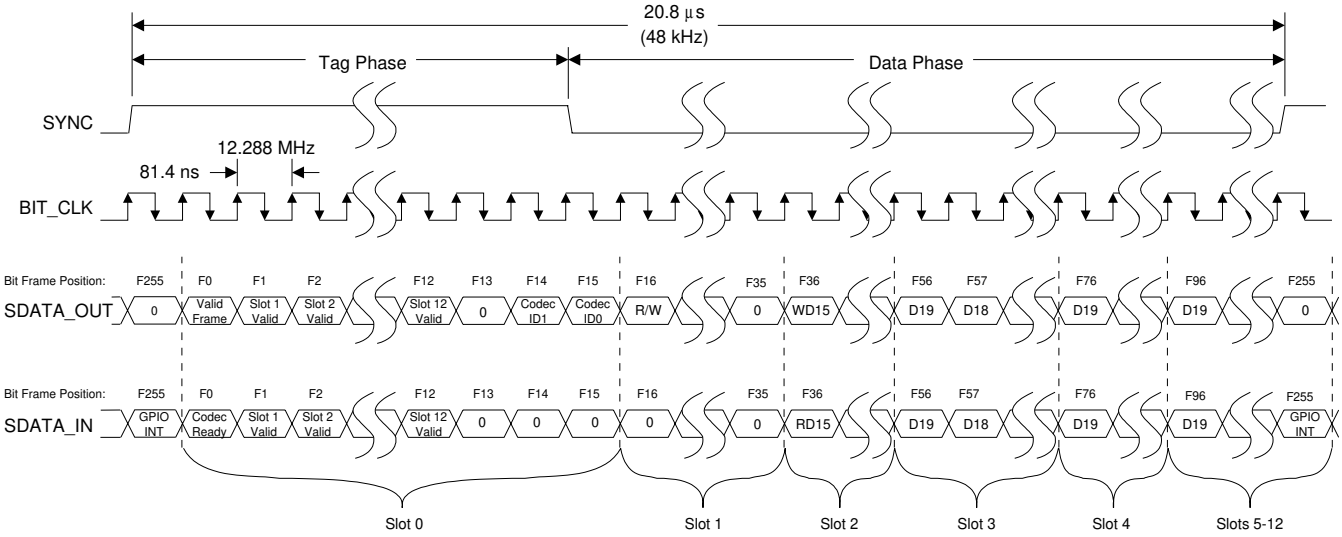

Figure 14. AC-link Input and Output Framing

4.1 AC-Link Serial Data Output Frame

In the serial data output frame, data is passed on the SDATA_OUT pin to the CS4205 from the AC '97 controller. Figure 14 illustrates the serial port timing.

The PCM playback data being passed to the CS4205 is shifted out MSB first in the most significant bits of each slot. Any PCM data from the AC '97 controller that is not 20 bits wide should be left justified in its corresponding slot and dithered or zero-padded in the unused bit positions.

Bits that are reserved should always be 'cleared' by the AC '97 controller.

4.1.1 Serial Data Output Slot Tags (Slot 0)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Valid Frame	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	Slot 5 Valid	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	Slot 9 Valid	Slot 10 Valid	Slot 11 Valid	Slot 12 Valid	Res	Codec ID1	Codec ID0

Valid Frame — The Valid Frame bit determines if any of the following slots contain either valid playback data for the CS4205 or data for read/write operations. When 'set', at least one of the other AC-link slots contains valid data. If this bit is 'clear', the remainder of the frame is ignored.

Slot 1 Valid — The Slot 1 Valid bit indicates a valid register read/write address for a primary codec.

Slot 2 Valid — The Slot 2 Valid bit indicates valid register write data for a primary codec.

Slot [3:11] Valid — The Slot [3:11] Valid bits indicate the validity of data in their corresponding serial data output slots. If a bit is 'set', the corresponding output slot contains valid data. If a bit is 'cleared', the corresponding slot will be ignored.

Slot 12 Valid — The Slot 12 Valid bit indicates if output Slot 12 contains valid GPIO control data.

Codec ID[1:0] — The Codec ID[1:0] bits determine which codec is being accessed during the current AC-link frame. Codec ID[1:0] = 00 indicates the primary codec is being accessed. Codec ID[1:0] = 01, 10, or 11 indicates one of three possible secondary codecs is being accessed. A Codec ID value of 01, 10, or 11 also indicates a valid read/write address and/or valid register write data for a secondary codec.

4.1.2 Command Address Port (Slot 1)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/$\overline{W}$	RI6	RI5	RI4	RI3	RI2	RI1	RI0	Reserved											

R/$\overline{W}$ — Read/$\overline{Write}$. When this bit is 'set', a read of the AC '97 register specified by the register index bits will occur in the AC '97 2.x audio codec. When the bit is 'cleared', a write will occur. For any read or write access to occur, the Valid Frame bit (F0) must be 'set' and the Codec ID[1:0] bits (F[14:15]) must match the Codec ID of the AC '97 2.x audio codec being accessed. Additionally, for a primary codec, the Slot 1 Valid bit (F1) must be 'set' for a read access and both the Slot 1 Valid bit (F1) and the Slot 2 Valid bit (F2) must be 'set' for a write access. For a secondary codec, both the Slot 1 Valid bit (F1) and the Slot 2 Valid bit (F2) must be 'cleared' for read and write accesses. See Figure 14 for bit frame positions.

RI[6:0] — Register Index. The RI[6:0] bits contain the 7-bit register index to the AC '97 registers in the CS4205. All registers are defined at word addressable boundaries. The RI0 bit must be 'clear' to access CS4205 registers.

4.1.3 Command Data Port (Slot 2)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	Reserved			

WD[15:0] Write Data. The WD[15:0] bits contain the 16-bit value to be written to the register. If an access is a read, this slot is ignored.

NOTE: For any write to an AC '97 register, the write is defined to be an 'atomic' access. This means that when the Slot 1 Valid bit in output Slot 0 is 'set', the Slot 2 Valid bit in output Slot 0 should always be 'set' during the same audio frame. No write access may be split across 2 frames.

4.1.4 PCM Playback Data (Slots 3-11)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD[19:0] Playback Data. The PD[19:0] bits contain the 20-bit PCM (2's complement) playback data for the left and right DACs, serial data ports, and/or the S/PDIF transmitter. Table 14 on page 43 lists a cross reference for each function and its respective slot. The mapping of a given slot to the DAC, serial data port, or S/PDIF transmitter is determined by the state of the ID[1:0] bits in the *Extended Audio ID Register (Index 28h)* and by the SM[1:0] and AMAP bits in the *AC Mode Control Register (Index 5Eh).*

4.1.5 GPIO Pin Control (Slot12)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Implemented											GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	Reserved			

GPIO[4:0] GPIO Pin Control. The GPIO[4:0] bits control the CS4205 GPIO pins configured as outputs. Write accesses using GPIO pin control bits configured as outputs will be reflected on the GPIO pin output on the next AC-link frame. Write accesses using GPIO pin control bits configured as inputs will have no effect and are ignored. If the GPOC bit in the *Misc. Crystal Control Register (Index 60h)* is 'set', the bits in output Slot 12 are ignored and GPIO pins configured as outputs are controlled through the *GPIO Pin Status Register (Index 54h)*.

4.2 AC-Link Serial Data Input Frame

In the serial data input frame, data is passed on the SDATA_IN pin from the CS4205 to the AC '97 controller. The data format for the input frame is very similar to the output frame. Figure 14 on page 19 illustrates the serial port timing.

The PCM capture data from the CS4205 is shifted out MSB first in the most significant 18 bits of each slot. The least significant 2 bits in each slot will be 'cleared'. If the host requests PCM data from the AC '97 Controller that is less than 18 bits wide, the controller should dither and round or just round (but not truncate) to the desired bit depth.

Bits that are reserved or not implemented in the CS4205 will always be returned 'cleared'.

4.2.1 Serial Data Input Slot Tag Bits (Slot 0)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Codec Ready	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	Slot 5 Valid	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	0	0	Slot 11 Valid	Slot 12 Valid	Reserved		

Codec Ready — Codec Ready. The Codec Ready bit indicates the readiness of the CS4205 AC-link. Immediately after a Cold Reset this bit will be 'clear'. Once the CS4205 clocks and voltages are stable, this bit will be 'set'. Until the Codec Ready bit is 'set', no AC-link transactions should be attempted by the controller. The Codec Ready bit does not indicate readiness of the DACs, ADCs, Vref, or any other analog function. Those must be checked in the *Powerdown Control/Status Register (Index 26h)* by the controller before any access is made to the mixer registers. Any accesses to the CS4205 while Codec Ready is 'clear' are ignored.

Slot 1 Valid — The Slot 1 Valid bit indicates Slot 1 contains a valid read back address.

Slot 2 Valid — The Slot 2 Valid bit indicates Slot 2 contains valid register read data.

Slot [3:8,11] Valid — The Slot [3:8,11] Valid bits indicate Slot [3:8,11] contains valid capture data from the CS4205 ADCs. If a bit is 'set', the corresponding input slot contains valid data. If a bit is 'cleared', the corresponding slot will be ignored.

Slot 12 Valid — The Slot 12 Valid bit indicates Slot 12 contains valid GPIO status data.

4.2.2 Status Address Port (Slot 1)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	RI6	RI5	RI4	RI3	RI2	RI1	RI0	SR3	SR4	SR5	SR6	SR7	SR8	SR9	0	SR11	0	Reserved	

RI[6:0] — Register Index. The RI[6:0] bits echo the AC '97 register address when a register read has been requested in the previous frame. The CS4205 will only echo the register index for a read access. Write accesses will not return valid data in Slot 1.

SR[3:9,11] — Slot Request. If SRx is 'set', this indicates the CS4205 SRC does not need a new sample on the next AC-link frame for that particular slot. If SRx is 'clear', the SRC indicates a new sample is needed on the following frame. If the VRA bit in the *Extended Audio Status/Control Register (Index 2Ah)* is 'clear', the SR[3:9,11] bits are always 0. When VRA is 'set', the SRC is enabled and the SR[3:9,11] bits are used to request data.

4.2.3 Status Data Port (Slot 2)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	Reserved			

RD[15:0] Read Data. The RD[15:0] bits contain the register data requested by the controller from the previous read request. All read requests will return the read address in the input Slot 1 and the register data in the input Slot 2 on the following serial data frame.

4.2.4 PCM Capture Data (Slot 3-8,11)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CD17	CD16	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	0	0

CD[17:0] Capture Data. The CD [17:0] bits contain 18-bit PCM (2's complement) capture data. The data will only be valid when the respective slot valid bit is 'set' in input Slot 0. The mapping of a given slot to an ADC is determined by the state of the ID[1:0] bits in the *Extended Audio ID Register (Index 28h)* and the SM[1:0] and AMAP bits in the *AC Mode Control Register (Index 5Eh).* The definition of each slot can be found in Table 14 on page 43.

4.2.5 GPIO Pin Status (Slot 12)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	Res	BDI	IEC	GPIO_INT

GPIO[4:0] GPIO Pin Status. The GPIO[4:0] bits reflect the status of the CS4205 GPIO pins configured as inputs. The pin status of GPIO pins configured as outputs will be reflected back on the GPIO[4:0] bits of input Slot 12 in the next frame. The output GPIO pins are controlled by the GPIO[4:0] pin control bits in output Slot 12.

BDI BIOS-Driver Interface. The BDI bit indicates that a BIOS event has occurred. This bit is a logic OR of all bits in the *BDI Status Register (Index 7Ah)* ANDed with their corresponding bit in the *BDI Config Register (Index 6Eh, Address 0Ch)*.

IEC Internal Error Condition. The IEC bit indicates that an internal error, such as an ADC over-range or a digital data overflow has occurred. This bit is a logic OR of all bits in the *IEC Status Register (Index 6Eh, Address 0Bh)*.

GPIO_INT GPIO Interrupt. The GPIO_INT bit indicates that a GPIO, BDI, or IEC interrupt event has occurred. The occurrence of a GPIO interrupt is determined by the GPIO interrupt requirements as outlined in the *GPIO Pin Wakeup Mask Register (Index 52h)* description. In this case, the GPIO_INT bit is cleared by writing a '0' to the bit in the *GPIO Pin Status Register (Index 54h)* corresponding to the GPIO pin which generated the interrupt.

The occurrence of a BDI interrupt is determined by the BDI interrupt requirements as outlined in the *BDI Control Registers (Index 6Eh, Address 0Ch - 0Dh)*. In this case, the GPIO_INT bit is cleared by writing a '0' to the bit in the *BDI Status Register (Index 7Ah)* that generated the interrupt.

The occurrence of an IEC interrupt is determined by the IEC interrupt requirements as outlined in the *Internal Error Condition Control/Status Registers (Index 6Eh, Address 09h - 0Bh)*. In this case, the GPIO_INT bit is cleared by writing a '0' to the bit in the *IEC Status Register (Index 6Eh, Address 0Bh)* corresponding to the IEC source which generated the interrupt.

4.3 AC-Link Protocol Violation - Loss of SYNC

The CS4205 is designed to handle SYNC protocol violations. The following are situations where the SYNC protocol has been violated:

- The SYNC signal is not sampled high for exactly 16 BIT_CLK clock cycles at the start of an audio frame.
- The SYNC signal is not sampled high on the 256th BIT_CLK clock period after the previous SYNC assertion.
- The SYNC signal goes active high before the 256th BIT_CLK clock period after the previous SYNC assertion.

Upon loss of synchronization with the controller, the CS4205 will 'clear' the Codec Ready bit in the serial data input frame until two valid frames are detected. During this detection period, the CS4205 will ignore all register reads and writes and will discontinue the transmission of PCM capture data. In addition, if the LOSM bit in the *Misc. Crystal Control Register (Index 60h)* is 'set' (default), the CS4205 will mute all analog outputs. If the LOSM bit is 'clear', the analog outputs will not be muted.

5. REGISTER INTERFACE

Reg	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	SE4	SE3	SE2	SE1	SE0	0	ID8	ID7	0	ID5	0	ID3	ID2	0	ID0	25ADh
02h	Master Volume	Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono Volume	Mute	0	0	0	0	0	0	0	0	0	MM5	MM4	MM3	MM2	MM1	MM0	8000h
08h	Master Tone Control	0	0	0	0	BA3	BA2	BA1	BA0	0	0	0	0	TR3	TR2	TR1	TR0	0F0Fh
0Ah	PC_BEEP Volume	Mute	0	0	0	0	0	0	0	0	0	0	PV3	PV2	PV1	PV0	0	0000h
0Ch	Phone Volume	Mute	0	0	0	0	0	0	0	0	0	0	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	0	0	0	0	0	0	0	0	20dB	0	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	0	0	0	0	0	SL2	SL1	SL0	0	0	0	0	0	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	0	0	0	GL3	GL2	GL1	GL0	0	0	0	0	GR3	GR2	GR1	GR0	8000h
1Eh	Record Gain Mic	Mute	0	0	0	0	0	0	0	0	0	0	0	GM3	GM2	GM1	GM0	8000h
20h	General Purpose	POP	ST	3D	LD	0	0	MIX	MS	LPBK	0	0	0	0	0	0	0	0000h
22h	3D Control	0	0	0	0	CR3	CR2	CR1	CR0	0	0	0	0	DP3	DP2	DP1	DP0	0000h
26h	Powerdown Ctrl/Stat	EAPD	0	PR5	PR4	PR3	PR2	PR1	PR0	0	0	0	0	REF	ANL	DAC	ADC	000Fh
28h	Ext'd Audio ID	ID1	ID0	0	0	0	0	AMAP	0	0	0	0	0	VRM	0	0	VRA	x209h
2Ah	Ext'd Audio Stat/Ctrl	0	PRL	0	0	0	0	MADC	0	0	0	0	0	VRM	0	0	VRA	4000h
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM L/R ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
34h	Mic ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
3Ch	Ext'd Modem ID	ID1	ID0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x000h
3Eh	Ext'd Modem Stat/Ctrl	0	0	0	0	0	0	0	PRA	0	0	0	0	0	0	0	GPIO	0100h
4Ch	GPIO Pin Config.	0	0	0	0	0	0	0	0	0	0	0	GC4	GC3	GC2	GC1	GC0	001Fh
4Eh	GPIO Pin Polarity/Type	1	1	1	1	1	1	1	1	1	1	1	GP4	GP3	GP2	GP1	GP0	FFFFh
50h	GPIO Pin Sticky	0	0	0	0	0	0	0	0	0	0	0	GS4	GS3	GS2	GS1	GS0	0000h
52h	GPIO Pin Wakeup	0	0	0	0	0	0	0	0	0	0	0	GW4	GW3	GW2	GW1	GW0	0000h
54h	GPIO Pin Status	0	0	0	0	0	0	0	0	0	0	0	GI4	GI3	GI2	GI1	GI0	0000h
Cirrus Logic Defined Registers:																		
5Eh	AC Mode Control	DACS	CAPS1	CAPS0	MICS	0	0	TMM	DDM	AMAP	0	SM1	SM0	SDOS1	SDOS0	SPDS1	SPDS0	0080h
60h	Misc. Crystal Control	0	0	Res	DPC	0	0	Reserved		10dB	CRST	Reserved		GPOC	Reserved		LOSM	0003h
68h	S/PDIF Control	SPEN	Val	0	Fs	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Emph	Copy	/Audio	Pro	0000h
6Ah	Serial Port Control	SDEN	0	0	0	0	0	0	0	0	SDI3	SDI2	SDI1	SDO2	SDSC	SDF1	SDF0	0000h
6Ch	Special Feature Addr	0	0	0	0	0	0	0	0	0	0	0	0	A3	A2	A1	A0	0000h
6Eh	Special Feature Data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	8000h
7Ah	BDI Status	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	0000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4352h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	0	DID2	DID1	DID0	1	REV2	REV1	REV0	5959h

Table 2. Register Overview for the CS4205