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CS4207

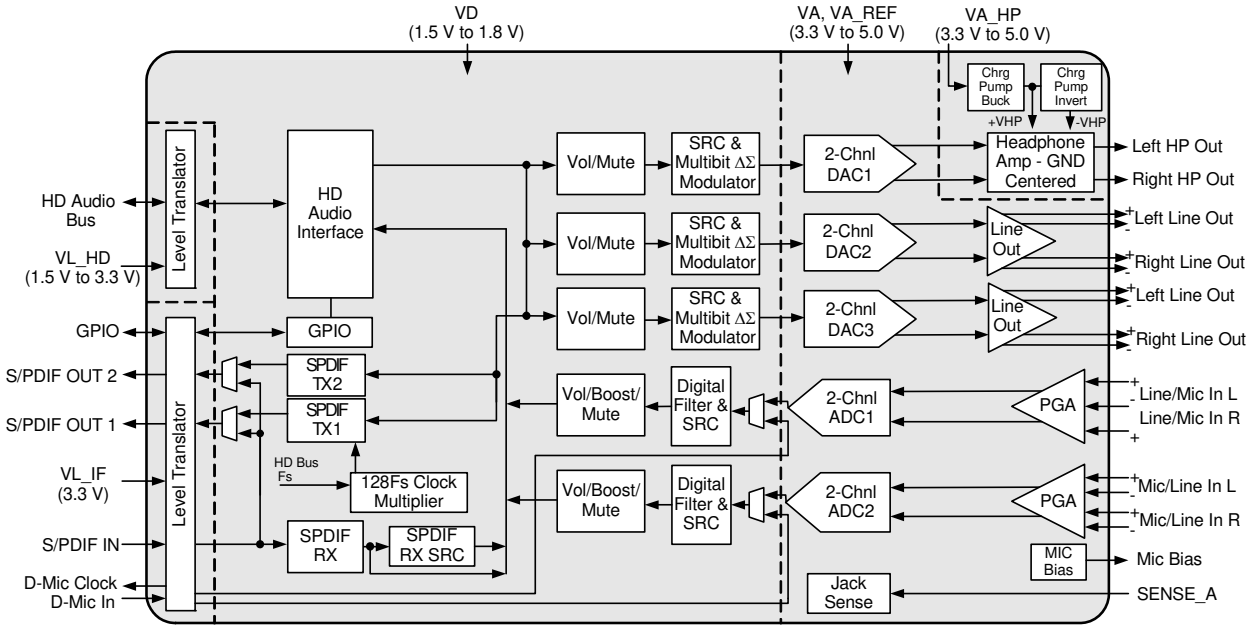
Low-power, 4-in / 6-out HD Audio Codec with Headphone Amp

DIGITAL to ANALOG FEATURES

- DAC1 (Headphone)
  - 101 dB Dynamic Range (A-wtd)
  - -89 dB THD+N
- Headphone Amplifier - GND Centered
  - Integrated Negative-voltage Regulator
  - No DC-blocking Capacitor Required
  - 50 mW Power/Channel into 16 Ω
- DAC2 & DAC3 (Line Outs)
  - 110 dB Dynamic Range (A-wtd)
  - -94 dB THD+N
  - Differential Balanced or Single-ended
- Each DAC Supports 32 kHz to 192 kHz Sample Rates Independently.
- Digital Volume Control
  - +6.0 dB to -57.5 dB in 0.5 dB Steps
  - Zero Cross and/or Soft Ramp Transitions
- Independent Support of D0 and D3 Power States for Each DAC
- Fast D3 to D0 Transition
  - Audio Playback in Less Than 50 ms

ANALOG to DIGITAL FEATURES

- ADC1 & ADC2
  - 105 dB Dynamic Range (A-wtd)
  - -88 dB THD+N
  - Differential Balanced or Single-ended Inputs
  - Analog Programmable Gain Amplifier (PGA) ±12 dB, 1.0 dB Steps, with Zero Cross Transitions and Mute
- MIC Inputs
  - Pre-amplifier with Selectable 0 dB, +10 dB, +20 dB, and +30 dB Gain Settings
  - Programmable, Low-noise MIC Bias Level
- Each ADC Supports 8 kHz to 96 kHz Sample Rates Independently
- Additional Digital Attenuation Control
  - -13.0 dB to -51.0 dB in 1.0 dB steps
  - Zero Cross and/or Soft Ramp Transitions
- Digital Interface for Two Dual Digital Mic Inputs
- Independent Support of D0 and D3 Power States for Each ADC



Digital Audio Interface Receiver

- Complete EIAJ CP1201, IEC 60958, S/PDIF Compatible Receiver
- 32 kHz to 192 kHz Sample Rate Range
- Automatic Detection of Compressed Audio Streams
- Integrated Sample Rate Converter
  - 128 dB Dynamic Range
  - -120 dB THD+N
  - Supports Sample Rates up to 192 kHz
  - 1:1 Input/Output Sample Rate Ratios

Digital Audio Interface Transmitters

- Two Independent EIAJ CP1201, IEC-60958, S/PDIF Compatible Transmitters
- 32 kHz to 192 kHz Sample Rate Range

System Features

- Very Low D3 Power Dissipation of <7 mW
  - Jack Detect Active in D3
  - HDA BITCLK Not Required for D3 State
- Jack Detect Does Not Require HDA Bus BITCLK
- All Configuration Settings are Preserved in D3 State
- Pop/Click Suppression in State Transitions
- Detects Wake Event and Generates Power State Change Request when HDA Bus Controller is in D3
- Variable Power Supplies
  - 1.5 V to 1.8 V Digital Core Voltage
  - 3.3 V to 5.0 V Analog Core Voltage
  - 3.3 V to 5.0 V Headphone Drivers
  - 1.5 V to 3.3 V HD Bus Interface Logic
  - 3.3 V Interface Logic levels for GPIO, S/PDIF, and Digital Mic
- Individual Power-down Managed
  - ADCs, DACs, PGAs, Headphone Driver, S/PDIF Receiver, and Transmitters

General Description

The CS4207 is a highly integrated multi-channel low-power HD Audio Codec featuring 192 kHz DACs, 96 kHz ADCs, 192 kHz S/PDIF Transmitters and Receiver, Microphone pre-amp and bias voltage, and a ground centered Headphone driver. Based on multi-bit, delta-sigma modulation, it allows infinite sample rate adjustment between 32 kHz and 192 kHz.

The ADC input path allows control of a number of features. The microphone input path includes a selectable programmable-gain pre-amplifier stage and a low-noise MIC bias voltage supply. A PGA is available for line and microphone inputs and provides analog gain with soft ramp and zero cross transitions. The ADC also features an additional digital volume attenuator with soft ramp transitions.

The stereo headphone amplifier is powered from a separate internally generated positive supply, with an integrated charge pump providing a negative supply. This allows a ground-centered analog output with a wide signal swing and eliminates external DC-blocking capacitors.

The integrated digital audio interface receiver and transmitters utilize a 24-bit, high-performance, monolithic CMOS stereo asynchronous sample rate converter to clock align the PCM samples to/from the S/PDIF interfaces. Auto detection of non-PCM encoded data disables the sample rate conversion to preserve bit accuracy of the data.

In addition to its many features, the CS4207 operates from a low-voltage analog and digital core, making this part ideal for portable systems that require low power consumption in a minimal amount of space.

The CS4207 is available in a 48-pin WQFN package in both Automotive (-40°C to +105°C) and Commercial (-40°C to +85°C) grades. The CS4207 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on p 147 for complete ordering information.

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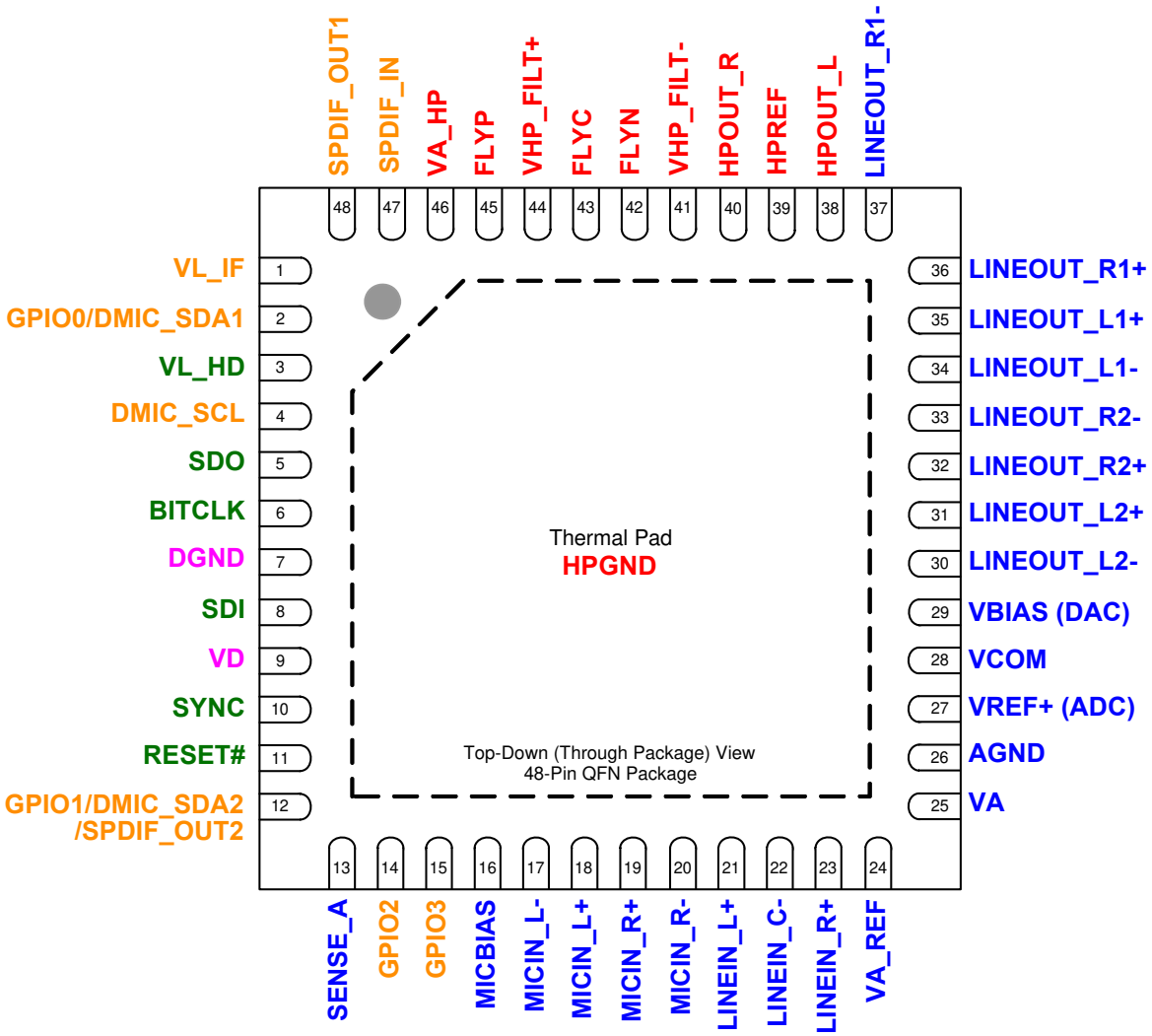
1. PIN DESCRIPTIONS

1.1 CS4207 48-pin QFN Pinout:



Pin Name	QFN	Pin Description
VL_IF	1	**Digital Interface Signal Level** (*Input*) - Digital supply for the GPIO, S/PDIF and Digital Mic interfaces. Refer to the Recommended Operating Conditions for appropriate voltages.
GPIO0/ DMIC_SDA1	2	**General Purpose I/O** (*Input/Output*) - General purpose input or output line, or **Digital Mic Data Input** (*Input*) - The first data input line from a digital microphone.
VL_HD	3	**Digital Interface Signal Level** (*Input*) - Digital supply for the HD Audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
DMIC_SCL	4	**Digital Mic Clock** (*Output*) - The high speed clock output to the digital microphone.
SDO	5	**Serial Data Input** (*Input*) - Serial data input stream from the HD Audio Bus.
BITCLK	6	**Bit Clock** (*Input*) - 24 MHz bit clock from the HD Audio Bus.
DGND	7	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
SDI	8	**Serial Data Output** *(Input/Output*) - Serial data output stream to the HD Audio Bus.
VD	9	**Digital Power** (*Input*) - Positive power for the internal digital section.
SYNC	10	**Sync Clock** (*Input*) - 48 kHz sync clock from the HD Audio Bus.

Pin Name	QFN	Pin Description
RESET#	11	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
GPIO1/ DMIC_SDA2/ SPDIF_OUT2	12	**General Purpose I/O** (*Input/Output*) - General purpose input or output line, or **Digital Mic Data Input** (*Input*) - The second data input line from a digital microphone, or **S/PDIF Output** (*Output*) - Output from internal S/PDIF Transmitter.
SENSE_A	13	**Jack Sense Pin** (*Input/Output*) - Jack sense detect.
GPIO2	14	**General Purpose I/O** (*Input/Output*) - General purpose input or output lines.
GPIO3	15	**General Purpose I/O** (*Input/Output*) - General purpose input or output lines.
MICBIAS	16	**Microphone Bias** (*Output*) - Provides a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
MICIN_L- MICIN_L+ MICIN_R+ MICIN_R-	17 18 19 20	**Microphone Input Left/Right** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
LINEIN_L+ LINEIN_C- LINEIN_R+	21 22 23	**Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
VA_REF VA	24 25	**Analog Power** (*Input*) - Positive power for the internal analog section. VA_REF is the return pin for the VBIAS cap.
AGND	26	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
VREF+	27	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal ADCs.
VCOM	28	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
VBIAS	29	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal DACs.
LINEOUT_L2- LINEOUT_L2+ LINEOUT_R2+ LINEOUT_R2- LINEOUT_L1- LINEOUT_L1+ LINEOUT_R1+ LINEOUT_R1-	30 31 32 33 34 35 36 37	**Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table
HPOUT_L HPOUT_R	38 40	**Analog Headphone Output** *(Output)* **-** The full-scale output level is specified in the DAC Analog Characteristics specification table.
HPREF	39	**Pseudo Diff. Headphone Reference** (*Input*) - Ground reference for the headphone amplifiers.
VHP_FILT-	41	**Inverting Charge Pump Filter Connection** *(Output)* **-** Power supply from the inverting charge pump that provides the negative rail for the headphone amplifier.
FLYN	42	**Charge Pump Cap Negative Node** *(Output)* **-** Negative node for the inverting charge pump's flying capacitor.
FLYC	43	**Charge Pump Cap Common Node** *(Output)* **-** Common positive node for the step-down and inverting charge pumps' flying capacitor.
VHP_FILT+	44	**Non-Inverting Charge Pump Filter Connection** *(Output)* **-** Power supply from the step-down charge pump that provides the positive rail for the headphone amplifier.
FLYP	45	**Charge Pump Cap Positive Node** *(Output)* **-** Positive node for the step-down charge pump's flying capacitor.
VA_HP	46	**Analog Power For Headphone** *(Input)* **-** Positive power for the internal analog headphone section.
SPDIF_IN	47	**S/PDIF Input** (*Input*) - Input to internal S/PDIF Receiver.
SPDIF_OUT1	48	**S/PDIF Output** (*Output*) - Output from internal S/PDIF Transmitter.
HPGND	TP	**HP Ground** (*Input*) - Ground reference for the internal headphone section. See "QFN Thermal Pad" on page 144 for more information.

1.2 Digital I/O Pin Characteristics

Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

Power Supply	Pin Name SW/(HW)	I/O	Driver	Receiver
VL_HD	RESET#	Input	-	1.5 V - 3.3 V
	SDO	Input	-	1.5 V - 3.3 V
	BITCLK	Input	-	1.5 V - 3.3 V
	SDI (Note 1)	Input/Output	1.5 V - 3.3 V	1.5 V - 3.3 V
	SYNC	Input	-	1.5 V - 3.3 V
VA	SENSE_A	Input	-	3.3 V - 5.0 V
VL_IF	GPIO1/ DMIC_SDA2	Input/Output	3.3 V	3.3 V
	GPIO2	Input/Output	3.3 V	3.3 V
	GPIO3	Input/Output	3.3 V	3.3 V
	SPDIF_IN	Input	-	3.3 V
	SPDIF_OUT	Output	3.3 V	-
	GPIO0/ DMIC_SDA1	Input/Output	3.3 V	3.3 V
	DMIC_SCL	Output	3.3 V	-

Notes:

1. SDI output functionality also requires the VA and VL_IF rails to be at nominal levels.

2. TYPICAL CONNECTION DIAGRAMS

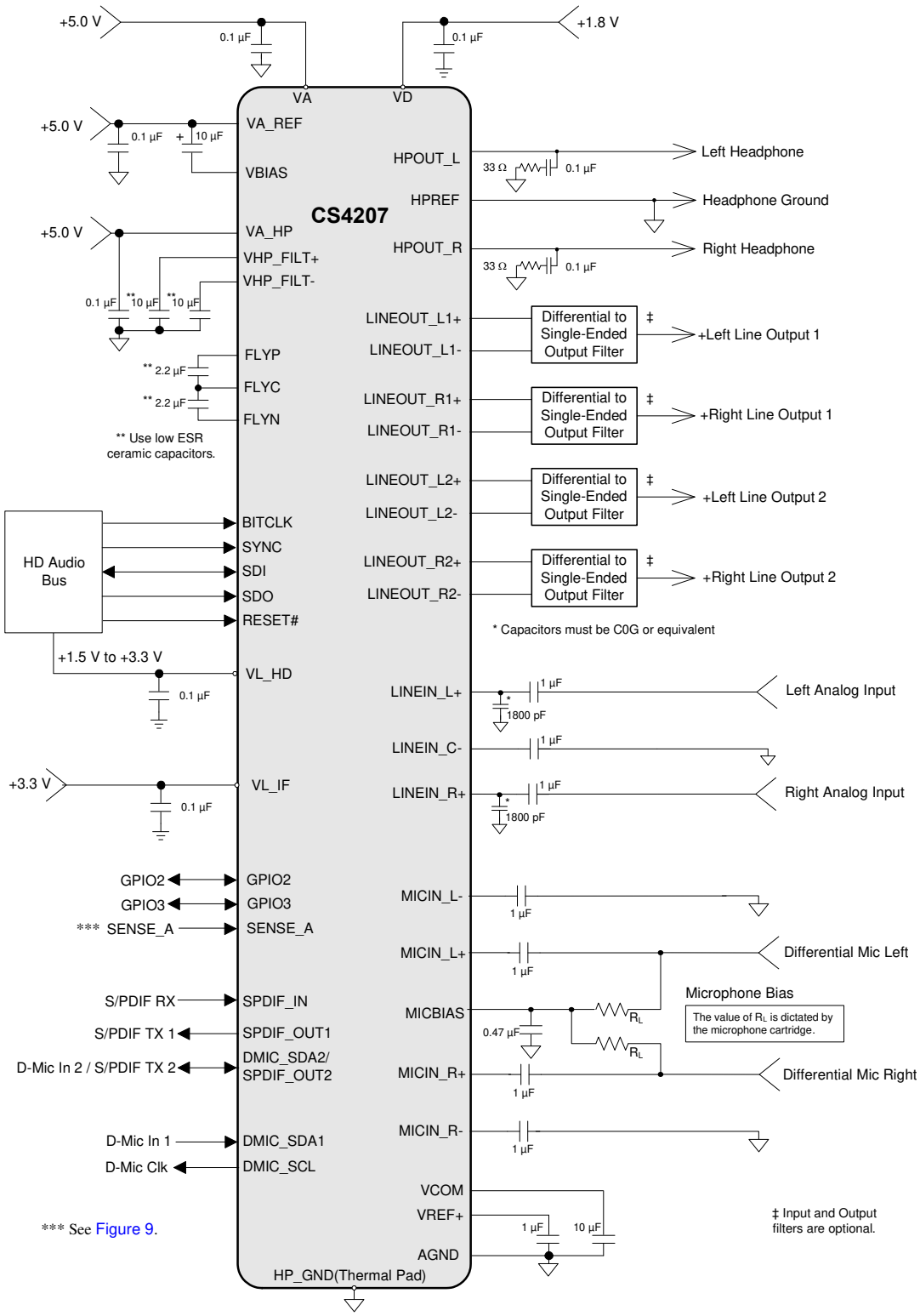


Figure 1. Typical Connection Diagram - Desktop System

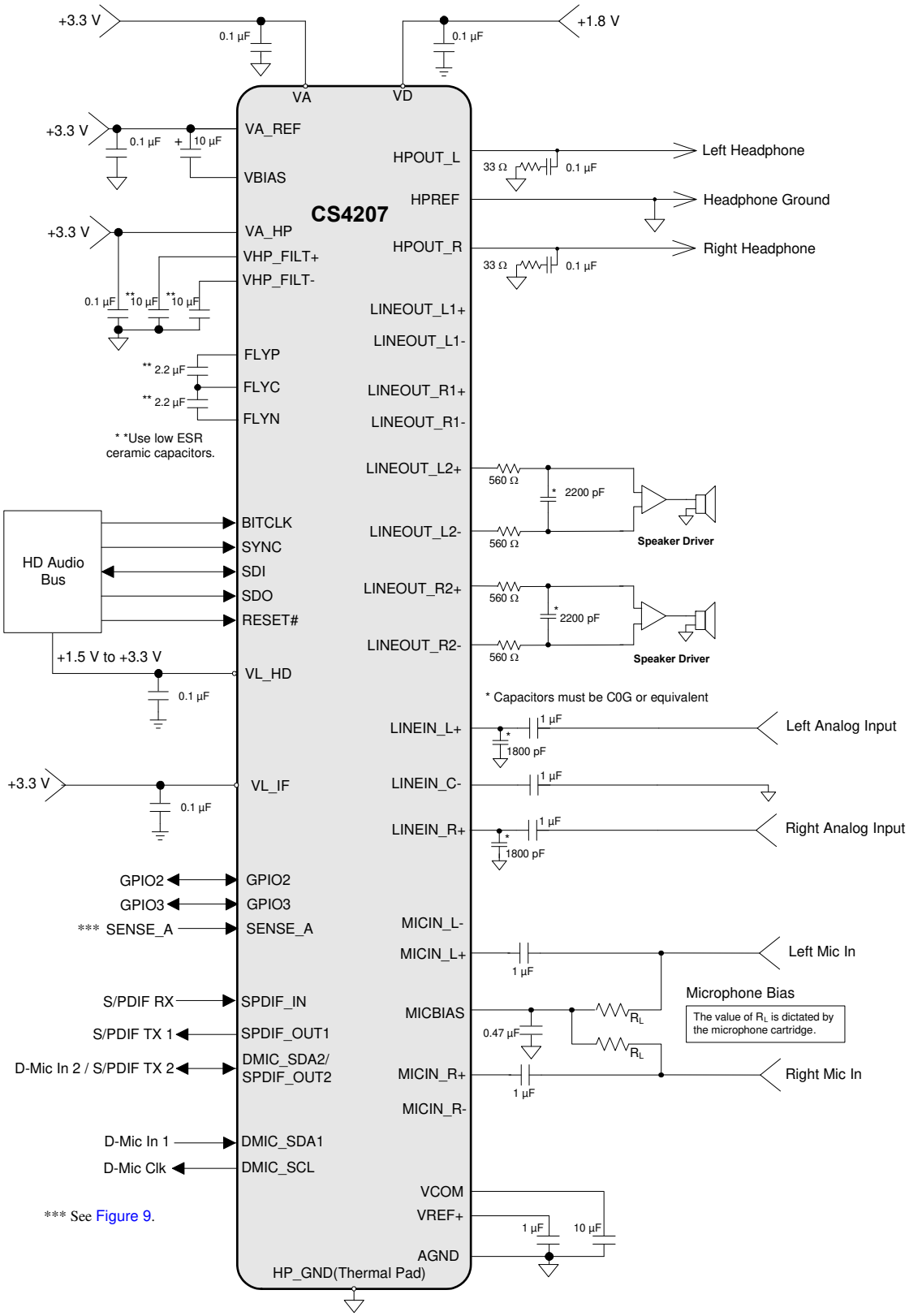


Figure 2. Typical Connection Diagram - Portable System

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply (Note 1)				
Analog Core	VA	2.97	5.25	V
DAC Reference	VA_REF	2.97	5.25	V
Headphone Amplifier	VA_HP	2.97	5.25	V
Digital Core	VD	1.42	1.89	V
HD Audio Bus Interface	VL_HD	1.42	3.47	V
GPIO, S/PDIF and Digital Mic Interface	VL_IF	2.97	3.47	V
Ambient Temperature Commercial - CNZ	T_A	-40	+85	°C
Ambient Temperature Automotive - DNZ	T_A	-40	+105	°C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply Analog Core	VA	-0.3	5.5	V
DAC Reference	VA_REF	-0.3	5.5	V
Headphone Amplifier	VA_HP	-0.3	5.5	V
Digital Core	VD	-0.3	3.0	V
HD Audio Interface	VL_HD	-0.3	4.0	V
GPIO, S/PDIF and Digital Mic Interface	VL_IF	-0.3	4.0	V
Input Current (Note 2)	I_{in}	-	±10	mA
Analog Input Voltage (Note 3)	V_{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage (Note 3) HD Audio Interface	V_{IND}	-0.3	VL_HD+0.4	V
GPIO, S/PDIF and Digital Mic Interface	V_{IND}	-0.3	VL_IF+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	+115	°C
Storage Temperature	T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. The device will operate properly over the full range of the analog, digital and interface supplies.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to digital full-scale): 1 kHz through passive input filter; VA_HP = VA; VL_HD = VL_IF = 3.3; VD = 1.8 V; T_A = +25°C; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 4)	VA, VA_REF = 5.0 V (Differential/Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V (Differential/Single-ended) Min	Typ	Max	Unit
Line In to PGA to ADC (ADC1 or ADC2; differential perf. characteristics only valid for ADC2)							
Dynamic Range							
PGA Setting: 0 dB A-weighted	99/96	105/102	-	95/93	101/99	-	dB
unweighted	96/93	102/99	-	92/90	98/96	-	dB
PGA Setting: +12 dB A-weighted	95/86	101/92	-	92/83	98/89	-	dB
unweighted	92/83	98/89	-	89/80	95/86	-	dB
Total Harmonic Distortion + Noise							
PGA Setting: 0 dB -1 dBFS	-	-88/-88	-82/-82	-	-95/-92	-89/-86	dB
-60 dBFS	-	-42/-39	-36/-33	-	-38/-36	-32/-30	dB
PGA Setting: +12 dB -1 dBFS	-	-88/-88	-82/-82	-	-92/-86	-86/-80	dB
Mic In to PGA to ADC (+20 dB) (ADC1 or ADC2; differential perf. characteristics only valid for ADC2)							
Dynamic Range							
A-weighted	86/78	92/84	-	83/75	89/81	-	dB
unweighted	83/75	89/81	-	80/72	86/78	-	dB
Total Harmonic Distortion + Noise							
-1 dBFS	-	-89/-82	-83/-76	-	-86/-78	-80/-72	dB
Other Analog Characteristics							
DC Accuracy							
Interchannel Gain Mismatch	-	0.2	-	-	0.2	-	dB
Gain Drift	-	±100	-	-	±100	-	ppm/°C
Offset Error High Pass Filter On	-	352	-	-	352	-	LSB
Interchannel Isolation	-	90	-	-	90	-	dB
HP Amp to Analog Input Isolation							
R_L = 10 kΩ	-	100	-	-	100	-	dB
R_L = 16 Ω	-	70	-	-	70	-	dB
Full-scale Input Voltage - Line In/Mic In (Differential Inputs) PGA(0dB)	1.58•VA	1.66•VA	1.74•VA	1.58•VA	1.66•VA	1.74•VA	Vpp
Full-scale Input Voltage - Line In PGA (0dB) (Single-ended Inputs)	0.79•VA	0.83•VA	0.87•VA	0.79•VA	0.83•VA	0.87•VA	Vpp
PGA (+12dB)		0.21•VA			0.21•VA		Vpp
Full-scale Input Voltage - Mic In PGA+Boost(0dB)	0.79•VA	0.83•VA	0.87•VA	0.79•VA	0.83•VA	0.87•VA	Vpp
(Single-ended Inputs) PGA+Boost(+20dB)		0.08•VA			0.08•VA		Vpp
Input Impedance (Note 5)							
Mic In (Differential or Pseudo-Diff)	-	43.5	-	-	43.5	-	kΩ
Line In (Pseudo-Diff, PGA = -12/0/+12 dB)	-	93/99/103	-	-	93/99/103	-	kΩ
Mic/Line In (Single-Ended, PGA = -12/0/+12 dB)	-	27/33/37	-	-	27/33/37	-	kΩ
Common Mode Rejection (Differential Inputs)	-	60	-	-	60	-	dB

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to digital full-scale): 1 kHz through passive input filter; VA_HP = VA; VL_HD = VL_IF = 3.3; VD = 1.8 V; T_A = -40 to +85°C; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 4)		VA, VA_REF = 5.0 V (Differential/Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V (Differential/Single-ended) Min	Typ	Max	Unit
Line In to PGA to ADC (ADC1 or ADC2; differential perf. characteristics only valid for ADC2)								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	99/96	105/102	-	95/93	101/99	-	dB
	unweighted	96/93	102/99	-	92/90	98/96	-	dB
PGA Setting: +12 dB	A-weighted	95/86	101/92	-	92/83	98/89	-	dB
	unweighted	92/83	98/89	-	89/80	95/86	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-88/-88	-82/-82	-	-95/-92	-89/-86	dB
	-60 dBFS	-	-42/-39	-36/-33	-	-38/-36	-32/-30	dB
PGA Setting: +12 dB	-1 dBFS	-	-88/-88	-82/-82	-	-92/-86	-86/-80	dB
Mic In to PGA to ADC (+20 dB) (ADC1 or ADC2; differential perf. characteristics only valid for ADC2)								
Dynamic Range								
	A-weighted	86/78	92/84	-	83/75	89/81	-	dB
	unweighted	83/75	89/81	-	80/72	86/78	-	dB
Total Harmonic Distortion + Noise								
	-1 dBFS	-	-89/-82	-83/-76	-	-86/-78	-80/-72	dB
Other Analog Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	High Pass Filter On	-	352	-	-	352	-	LSB
Interchannel Isolation		-	90	-	-	90	-	dB
HP Amp to Analog Input Isolation								
	R_L = 10 kΩ	-	100	-	-	100	-	dB
	R_L = 16 Ω	-	70	-	-	70	-	dB
Full-scale Input Voltage - Line In/Mic In (Differential Inputs)	PGA(0dB)	1.58•VA	1.66•VA	1.74•VA	1.58•VA	1.66•VA	1.74•VA	Vpp
Full-scale Input Voltage - Line In (Single-ended Inputs)	PGA(0dB)	0.79•VA	0.83•VA	0.87•VA	0.79•VA	0.83•VA	0.87•VA	Vpp
	PGA(+12dB)		0.21•VA			0.21•VA		Vpp
Full-scale Input Voltage - Mic In								
	PGA+Boost(0dB)	0.79•VA	0.83•VA	0.87•VA	0.79•VA	0.83•VA	0.87•VA	Vpp
(Single-ended Inputs)	PGA+Boost(+20dB)		0.08•VA			0.08•VA		Vpp
Input Impedance (Note 5)		-		-	-		-	
	Mic In (Differential or Pseudo-Diff)		43.5			43.5		kΩ
	Line In (Pseudo-Diff, PGA = -12/0/+12 dB)		93/99/103			93/99/103		kΩ
	Mic/Line In (Single-Ended, PGA = -12/0/+12 dB)		27/33/37			27/33/37		kΩ
Common Mode Rejection (Differential Inputs)		-	60	-	-	60	-	dB

4. Referred to the typical full-scale voltage. Applies to all THD+N and Dynamic Range values in the table.
5. Measured between [LINE/MIC]IN_[L/R]+ and [LINE/MIC]IN_[C/L/R]- for differential and pseudo-differential inputs, and between [LINE/MIC]IN_[L/R]+ and AGND for single-ended inputs.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 6)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	.4535	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay		-	7.6/Fs	-	s
***High-Pass Filter Characteristics* (48 kHz Fs)**					
Frequency Response	-3.0 dB -0.13 dB	- -	3.6 24.2	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0.17	dB
Filter Settling Time		-	10^5/Fs	0	s

6. Response is clock dependent and will scale with Fs.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; VD = 1.8 V; VL_HD = VL_IF = 3.3V; T_A = +25°C; Measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output and test load R_L = 16 Ω, C_L = 10 pF for the headphone output (see Figure 3); DAC Gain = 0 dB).

Parameter (Note 4)		VA, VA_REF = 5.0 V VA_HP = 5.0 V (Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V VA_HP = 3.3 V (Single-ended) Min	Typ	Max	Unit
DAC1; R_L = 16 Ω; DAC Gain = -5 dB								
Dynamic Range								
18 to 24-Bit	A-weighted	95	101	-	93	99	-	dB
	unweighted	92	98	-	90	96	-	dB
16-Bit	A-weighted	-	93	-	-	93	-	dB
	unweighted	-	90	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-89	-83	-	-93	-87	dB
	-20 dB	-	-78	-72	-	-76	-70	dB
	-60 dB	-	-38	-32	-	-36	-30	dB
16-Bit	0 dB	-	-89	-	-	-90	-	dB
	-20 dB	-	-70	-	-	-70	-	dB
	-60 dB	-	-30	-	-	-30	-	dB
DAC1; R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	100	106	-	98	104	-	dB
	unweighted	97	103	-	95	101	-	dB
16-Bit	A-weighted	-	96	-	-	96	-	dB
	unweighted	-	93	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-88	-82	-	-90	-84	dB
	-20 dB	-	-83	-77	-	-81	-75	dB
	-60 dB	-	-43	-37	-	-41	-35	dB
16-Bit	0 dB	-	-88	-	-	-90	-	dB
	-20 dB	-	-73	-	-	-73	-	dB
	-60 dB	-	-33	-	-	-33	-	dB
Other Characteristics for DAC1; R_L = 16 Ω or 10 kΩ								
Full-scale Output Voltage, R_L = 10 kΩ		0.80•VA	0.84•VA	0.88•VA	0.80•VA	0.84•VA	0.88•VA	Vpp
Output Power, THD+N = -75 dB, R_L = 16 Ω		-	38	-	-	17	-	mW_{rms}
Output Power, THD+N = 1%, R_L = 16 Ω		-	50	-	-	23	-	mW_{rms}
Output Power,THD+N = 10%, R_L = 16 Ω		-	74	-	-	35	-	mW_{rms}
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Output Offset Voltage	DAC to HPOUT	-	2	4	-	2	4	mV
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 7)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 7)	-	-	150	-	-	150	pF
Output Impedance		-	300	-	-	300	-	mΩ

Parameter (Note 4)		VA, VA_REF = 5.0 V (Differential/Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V (Differential/Single-ended) Min	Typ	Max	Unit
DAC2/DAC3; R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	104/100	110/106	-	101/97	107/103	-	dB
	unweighted	101/97	107/103	-	98/94	104/100	-	dB
16-Bit	A-weighted	-	96	-	-	96	-	dB
	unweighted	-	93	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-94/-91	-88/-85	-	-96/-94	-90/-88	dB
	-20 dB	-	-87/-83	-81/-77	-	-84/-80	-78/-74	dB
	-60 dB	-	-47/-43	-41/-37	-	-44/-40	-38/-34	dB
16-Bit	0 dB	-	-92	-	-	-92	-	dB
	-20 dB	-	-73	-	-	-73	-	dB
	-60 dB	-	-33	-	-	-33	-	dB
Other Characteristics for DAC2/DAC3; R_L = 10 kΩ								
Full-scale Output Voltage		1.60•VA/ 0.80•VA	1.68•VA/ 0.84•VA	1.76•VA/ 0.88•VA	1.60•VA/ 0.80•VA	1.68•VA/ 0.84•VA	1.76•VA/ 0.88•VA	Vpp
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 7)	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)	(Note 7)	-	-	100	-	-	100	pF
Output Impedance		-	100	-	-	100	-	Ω

7. See Figure 3 and Figure 4. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity.

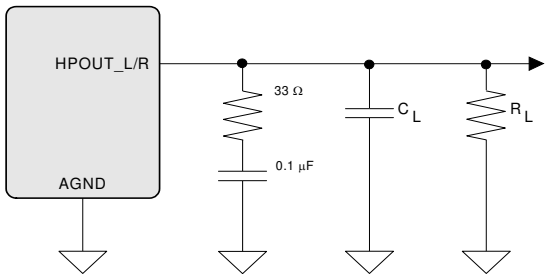


Figure 3. Output Test Load, Headphone Out

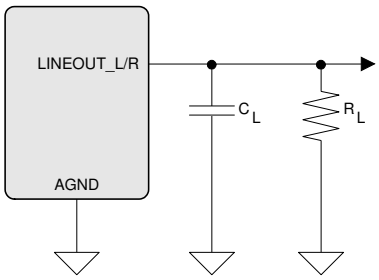


Figure 4. Output Test Load, Line Out

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; VD = 1.8 V; VL_HD = VL_IF = 3.3V; T_A = -40 to +85°C; Measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output and test load R_L = 16 Ω, C_L = 10 pF for the headphone output (see Figure 5); DAC Gain = 0 dB).

Parameter (Note 4)		VA, VA_REF = 5.0 V VA_HP = 5.0 V (Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V VA_HP = 3.3 V (Single-ended) Min	Typ	Max	Unit
DAC1; R_L = 16 Ω; DAC Gain = -5 dB								
Dynamic Range								
18 to 24-Bit	A-weighted	95	101	-	93	99	-	dB
	unweighted	92	98	-	90	96	-	dB
16-Bit	A-weighted	-	93	-	-	93	-	dB
	unweighted	-	90	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-89	-83	-	-93	-87	dB
	-20 dB	-	-78	-72	-	-76	-70	dB
	-60 dB	-	-38	-32	-	-36	-30	dB
16-Bit	0 dB	-	-89	-	-	-90	-	dB
	-20 dB	-	-70	-	-	-70	-	dB
	-60 dB	-	-30	-	-	-30	-	dB
DAC1; R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	100	106	-	98	104	-	dB
	unweighted	97	103	-	95	101	-	dB
16-Bit	A-weighted	-	96	-	-	96	-	dB
	unweighted	-	93	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-88	-82	-	-90	-84	dB
	-20 dB	-	-83	-77	-	-81	-75	dB
	-60 dB	-	-43	-37	-	-41	-35	dB
16-Bit	0 dB	-	-88	-	-	-90	-	dB
	-20 dB	-	-73	-	-	-73	-	dB
	-60 dB	-	-33	-	-	-33	-	dB
Other Characteristics for DAC1; R_L = 16 Ω or 10 kΩ								
Full-scale Output Voltage, R_L = 10 kΩ		0.80•VA	0.84•VA	0.88•VA	0.80•VA	0.84•VA	0.88•VA	Vpp
Output Power, THD+N = -75 dB, R_L = 16 Ω		-	38	-	-	17	-	mW_{rms}
Output Power, THD+N = 1%, R_L = 16 Ω		-	50	-	-	23	-	mW_{rms}
Output Power,THD+N = 10%, R_L = 16 Ω		-	74	-	-	35	-	mW_{rms}
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Output Offset Voltage	DAC to HPOUT	-	2	5	-	2	5	mV
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 8)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 8)	-	-	150	-	-	150	pF
Output Impedance		-	300	-	-	300	-	mΩ

Parameter (Note 4)		VA, VA_REF = 5.0 V (Differential/Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V (Differential/Single-ended) Min	Typ	Max	Unit
DAC2/DAC3; R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	104/100	110/106	-	101/97	107/103	-	dB
	unweighted	101/97	107/103	-	98/94	104/100	-	dB
16-Bit	A-weighted	-	96	-	-	96	-	dB
	unweighted	-	93	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-94/-91	-88/-85	-	-96/-94	-88/-88	dB
	-20 dB	-	-87/-83	-81/-77	-	-84/-80	-78/-74	dB
	-60 dB	-	-47/-43	-41/-37	-	-44/-40	-38/-34	dB
16-Bit	0 dB	-	-92	-	-	-92	-	dB
	-20 dB	-	-73	-	-	-73	-	dB
	-60 dB	-	-33	-	-	-33	-	dB
Other Characteristics for DAC2/DAC3; R_L = 10 kΩ								
Full-scale Output Voltage		1.60•VA/ 0.80•VA	1.68•VA/ 0.84•VA	1.76•VA/ 0.88•VA	1.60•VA/ 0.80•VA	1.68•VA/ 0.84•VA	1.76•VA/ 0.88•VA	Vpp
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 8)	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)	(Note 8)	-	-	100	-	-	100	pF
Output Impedance		-	100	-	-	100	-	Ω

8. See Figure 5 and Figure 6. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity.

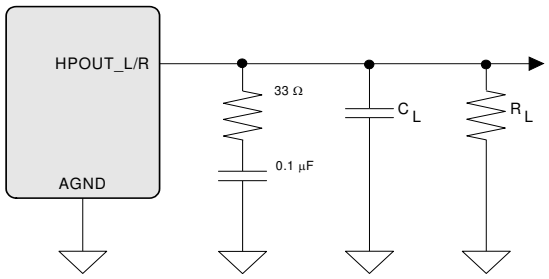


Figure 5. Output Test Load, Headphone Out

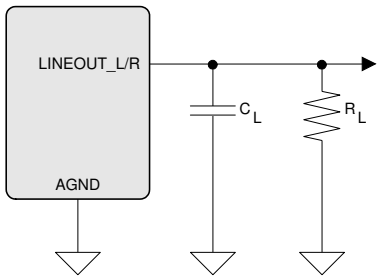


Figure 6. Output Test Load, Line Out

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter		Min	Typ	Max	Unit
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
Passband	to -0.01 dB corner	0	-	21792	Hz
	to -3 dB corner	0	-	23952	Hz
StopBand		-	26256	-	Hz
StopBand Attenuation (Note 9)		-	102	-	dB
Total Group Delay		-	0.196	-	ms

9. Measurement Bandwidth is from Stopband to 100 kHz.

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Min	Typ	Max	Units
VCOM Characteristics					
Nominal Voltage		-	0.5•VA	-	V
Output Impedance		-	23	-	kΩ
DC Current Source/Sink (Note 10)		-	-	10	µA
VHP_FILT+ Characteristics					
Nominal Voltage		-	0.5•VA_HP	-	V
VHP_FILT- Characteristics					
Nominal Voltage		-	-0.5•VA_HP	-	V
MIC BIAS Characteristics					
Nominal Voltage	VREFE = 000b	-	Hi-Z	-	V
	VREFE = 001b	-	0.5•VA	-	V
	VREFE = 010b	-	GND	-	V
	VREFE = 100b	-	0.8•VA	-	V
DC Current Source	(VA=5.0V)	-	5	-	mA
	(VA=3.3V)	-	3	-	mA
Power Supply Rejection Ratio (PSRR) (Note 11)	1 kHz	-	60	-	dB

10. The DC current draw represents the allowed current draw from the VCOM pin due to typical leakage through electrolytic de-coupling capacitors.
11. Valid with the recommended capacitor values on VBIAS. Increasing the capacitance will also increase the PSRR.

DIGITAL MICROPHONE INTERFACE CHARACTERISTICS

Test conditions: Inputs: Logic 0 = GND = 0 V, Logic 1 = VL_IF; T_A = +25 °C; C_{LOAD} = 30 pF.

Parameters		Symbol	Min	Typ	Max	Units
DMIC_SCL Period (Fs_{ADC} >= 44.1 kHz)	(Note 12)	t_P	-	8 • T_cyc	-	ns
DMIC_SCL Period (Fs_{ADC} <= 32.0 kHz)	(Note 12)	t_P	-	12 • T_cyc	-	ns
DMIC_SCL Duty Cycle		-	45	-	55	%
DMIC_SCL Rise Time	(Note 13)	t_r	-	-	10	ns
DMIC_SCL Fall Time	(Note 13)	t_f	-	-	10	ns
DMIC_SDA Setup Time Before DMIC_SCL Rising Edge		$t_{s(SD-CLKR)}$	40	-	-	ns
DMIC_SDA Hold Time After DMIC_SCL Rising Edge		$t_{h(CLKR-SD)}$	5	-	-	ns
DMIC_SDA Setup Time Before DMIC_SCL Falling Edge		$t_{s(SD-CLKF)}$	40	-	-	ns
DMIC_SDA Hold Time After DMIC_SCL Falling Edge		$t_{h(CLKF-SD)}$	6	-	-	ns

Notes:

12. The output clock frequency will follow the Bit Clock (BITCLK) frequency divided by 8 or 12, depending on the sample rate of the ADC. Any deviation of the Bit Clock source from the nominal supported rates will be directly imparted to the output clock rate by the same factor (e.g. +100 ppm offset in the frequency of BIT-CLK will become a +100 ppm offset in DMIC_SCL). For the nominal value of T_cyc reference HDA024-A (see Note 4 in "References" on page 147).
13. Rise and fall times are measured from 0.1 • VL_IF to 0.9 • VL_IF.

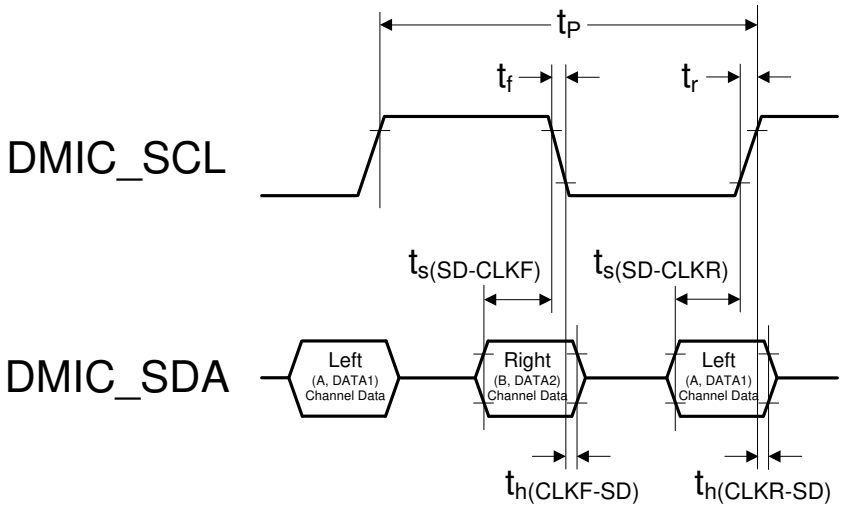


Figure 7. Digital MIC Interface Timing

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 14)	Symbol	Min	Max	Units
Input Leakage Current	I_{in}	-	±10	µA
Input Pin Capacitance	C_{in}	-	7.5	pF
VL_HD = 1.5 V				
High-Level Input Voltage	V_{IH}	0.60•VL_HD	-	V
Low-Level Input Voltage	V_{IL}	-	0.40•VL_HD	V
High-Level Output Voltage (I_{OUT} = -500 µA)	V_{OH}	0.90•VL_HD	-	V
Low-Level Output Voltage (I_{OUT} = 1500 µA)	V_{OL}	-	0.10•VL_HD	V
VL_HD = 3.3 V				
High-Level Input Voltage	V_{IH}	0.65•VL_HD	-	V
Low-Level Input Voltage	V_{IL}	-	0.35•VL_HD	V
High-Level Output Voltage (I_{OUT} = -500 µA)	V_{OH}	0.90•VL_HD	-	V
Low-Level Output Voltage (I_{OUT} = 1500 µA)	V_{OL}	-	0.10•VL_HD	V
VL_IF = 3.3 V				
High-Level Input Voltage	V_{IH}	0.65•VL_IF	-	V
Low-Level Input Voltage	V_{IL}	-	0.35•VL_IF	V
High-Level Output Voltage (I_{OH} = -100 µA)	V_{OH}	VL_IF - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)	V_{OL}	-	0.2	V

14. See "Digital I/O Pin Characteristics" on p 10 for HD Audio I/F and control power rails.

HD AUDIO BUS SPECIFICATIONS & CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
BITCLK Period	T_{CYC}	41.163	41.67	42.171	ns
BITCLK High Time	T_{HIGH}	17.50		24.16	ns
BITCLK Low Time	T_{LOW}	17.50		24.16	ns
BITCLK Jitter			150	500	ps
SDI Valid After BITCLK Rising	T_{TCO}	3		11	ns
SDO Setup Time	T_{SU}	5			ns
SDO Hold Time	T_{H}	5			ns

S/PDIF TRANSMITTER/RECEIVER SPECIFICATIONS & CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Transmitter Specifications & Characteristics					
AES3 Transmitter Output Jitter	$T_{JIT(rms)}$	meets IEC 60958-3			ps
Receiver Specifications & Characteristics					
PLL Clock Recovery Sample Rate Range	f_{rec}				kHz
Input Jitter Tolerance	$T_{JIT(rms)}$	meets IEC 60958-3			ps

POWER CONSUMPTION

(This table represents the power consumption for individual circuit blocks within the codec) (See (Note 15))

	Individual Block Operation	VA/ VA_HP	Typical Current (mA) i_{VA}	i_{VA_HP}	i_{VD} VD =1.8V	i_{VL_HD} VL_HD =3.3V	i_{VL_IF} VL_IF =3.3V	Total Power for individual block (mW)
1	Codec D3 State- unsolicited response capable (Note 16)	3.3 5.0	0.94 1.20	0.00 0.00	3.34	0.07	0.00	**9.35** **12.24**
2	ADC1 or ADC2 with PGA operation and Pseudo-Diff Inputs	3.3 5.0	5.47 6.23	0.00 0.00	7.27	0.17	0.00	**31.70** **44.80**
3	DAC1 with Headphone/Line Out (Note 17)	3.3 5.0	11.08 14.06	1.51 1.76	8.79	0.06	0.00	**57.57** **95.12**
4	DAC2 or DAC3 with Differential Line Out (Note 18)	3.3 5.0	10.72 13.59	0.00 0.00	8.72	0.06	0.00	**51.27** **83.84**
5	S/PDIF transmitter with SRC function	3.3 5.0	0.84 1.10	0.00 0.00	8.90	0.07	0.23	**19.78** **22.51**
6	S/PDIF receiver with SRC function	3.3 5.0	0.84 1.10	0.00 0.00	12.67	0.10	0.00	**25.91** **28.64**

15. Unless otherwise noted, test conditions are as follows: All zeros input, sample rate = 48 kHz; No load.
16. RESET# held HI, all HDA Bus clocks and data lines are running; HDA Interface running with support for unsolicited responses; All converters are in D3 state.
17. Full-scale single-ended output signal into a 10 kΩ load.
18. Full-scale differential output signal into a 10 kΩ load.

(The following table demonstrates the total power consumption for typical system operation. These total codec power numbers are derived from the individual block power consumption numbers in the previous table.)

	Typical Codec Operation	Power States ADC1	ADC2	DAC1	DAC2	DAC3	S/PDIF_OUT	S/PDIF_IN	VA/ VA_HP	Active Blocks	Total Codec Power (mW)
1	Stereo Record from Line In 1 (PGA/ADC1)	D0	D3	D3	D3	D3	D3	D3	3.3 5.0	HDA Interface + unsolicited response + ADC1	**41.04** **57.04**
2	Stereo Playback to Headphone (No Load)	D3	D3	D0	D3	D3	D3	D3	3.3 5.0	HDA Interface + unsolicited response + DAC1	**66.91** **107.36**
3	Stereo Playback to Headphone Out and S/PDIF Out	D3	D3	D0	D3	D3	D0	D3	3.3 5.0	HDA Interface + unsolicited response + DAC1+ S/PDIF OUT	**86.69** **129.87**
4	Receive from S/PDIF and Playback to S/PDIF Out	D3	D3	D3	D3	D3	D0	D0	3.3 5.0	HDA Interface + unsolicited response + S/PDIF IN/OUT	**55.04** **63.39**
5	Stereo Record & Playback Line In 1 / Line Out 1	D0	D3	D3	D0	D3	D3	D3	3.3 5.0	HDA Interface + unsolicited response + ADC1 + DAC2	**92.31** **140.88**

4. CODEC RESET AND INITIALIZATION

4.1 Link Reset

A Link Reset is a system controller generated assertion of the HD Audio Bus RESET# signal. A Link reset will cause some of the HD Audio bus interface logic to be initialized. Following a Link Reset, the CS4207 will perform the Codec Initialization request sequence. Many of the codec settings will remain unchanged following a Link Reset. See "Register Settings Across Reset Conditions" section on page 29 for more details.

When the codec has detected a Link Reset condition, all converter widgets and pin widgets will transition to a low power operating mode, if previously in D0. The actual power states reported will remain unchanged, i.e. if in D0 or D3 prior to Link Reset, the widget stays in D0 or D3. If enabled, presence detection will continue to sense any impedance changes and issue a power state change request to the Link prior to asserting an Unsolicited Response.

4.2 Function Group Reset

Because the CS4207 supports the Extended Power State Support (EPSS), a single occurrence of the **Function Group Reset** command will **NOT** cause the Audio Function unit and all associated widgets to initialize to the power-on reset values (as described in the HD Audio Specification, Rev. 1.0). When the CS4207 receives a single Function Group Reset verb, the codec will issue a response to the verb to acknowledge receipt, and reset each input/output converter widget's Stream Number and Lowest Channel Number to the default (0h). No other settings are modified. See "Register Settings Across Reset Conditions" section on page 29 for more details.

The CS4207 will respond to the newly created "Double Function Group Reset" (as defined in HDA015-B, March 1, 2007) and will reset most of the register settings to their power on defaults. This "Double Function Group Reset" will not affect the HD Audio bus interface logic or the unique codec physical address, which must be reset with the link RESET# signal. Therefore, the codec will not initiate a Codec Initialization sequence on the link. In addition, the Configuration Default settings will not be reset with a "Double Function Group Reset".

This new reset condition is created by sending two Function Group resets back to back. The "Double Function Group Reset" is defined as two (2) Function Group Reset verbs received without any other intervening verbs. The Function Group Reset verbs are not required to be received in sequential frames, but there must not be any other verbs received in frames between the receipt of the Function Group Reset verbs. There are no implied time outs between the time the first Function Group Reset is received and the second Function Group Reset verb.

4.3 Codec Initialization

Immediately following the completion of a Link Reset sequence, the CS4207 will initiate a codec initialization sequence. The purpose of this initialization sequence is to acquire a unique address by which the codec can thereafter be referenced with Commands on the SDO signal. During this sequence, the Controller provides the codec with a unique address using its attached SDI signal.

If the CS4207 codec is in a low power D3 state and enabled to support a presence detect event, it will retain its unique address while in that low power state. If RESET# is de-asserted high, and BITCLK and SYNC are running at the time of a presence detect event, the codec will signal an unsolicited response.

When put into the D3 low power state and enabled to support a presence detect event, with the link in the reset state (RESET# is asserted low), the CS4207 will post the occurrence of a wake event and request a power state change by signaling a power state change request and initialization request. It will reestablish the connection with the controller by performing a "Codec Initialization request".