Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CIRRUS LOGIC®

CS4228A

24-Bit, 96 kHz Surround Sound Codec

Features

- Six 24-bit D/A converters
  - 100 dB dynamic range
  - -90 dB THD+N
- Two 24-bit A/D converters
  - 97 dB dynamic range
  - -88 dB THD+N
- Sample rates up to 100 kHz
- Pop-free digital output volume controls
  - 90.5 dB range, 0.5 dB resolution (182 levels)
  - Variable smooth ramp rate, 0.125 dB steps
- Mute control pin for off-chip muting circuits
- On-chip anti-alias and output filters
- De-emphasis filters for 32, 44.1 and 48 kHz

Description

The CS4228A codec provides two analog-to-digital and six digital-to-analog Delta-Sigma converters, along with volume controls, in a compact 28-pin SSOP device. Combined with an IEC958 (SPDIF) receiver (like the CS8414) and surround sound decoder (such as one of the CS492x or CS493xx families), it is ideal for use in DVD player, A/V receiver and car audio systems supporting multiple standards such as Dolby Digital AC-3®, AAC™, DTS®, Dolby ProLogic®, THX®, and other multi-channel formats.

A flexible serial audio interface allows operation in Left Justified, Right Justified, I²S, or One Line Data modes.

ORDERING INFORMATION

CS4228A-KS	-10° to +70°C	28-pin SSOP
CDB4228A		Evaluation Board

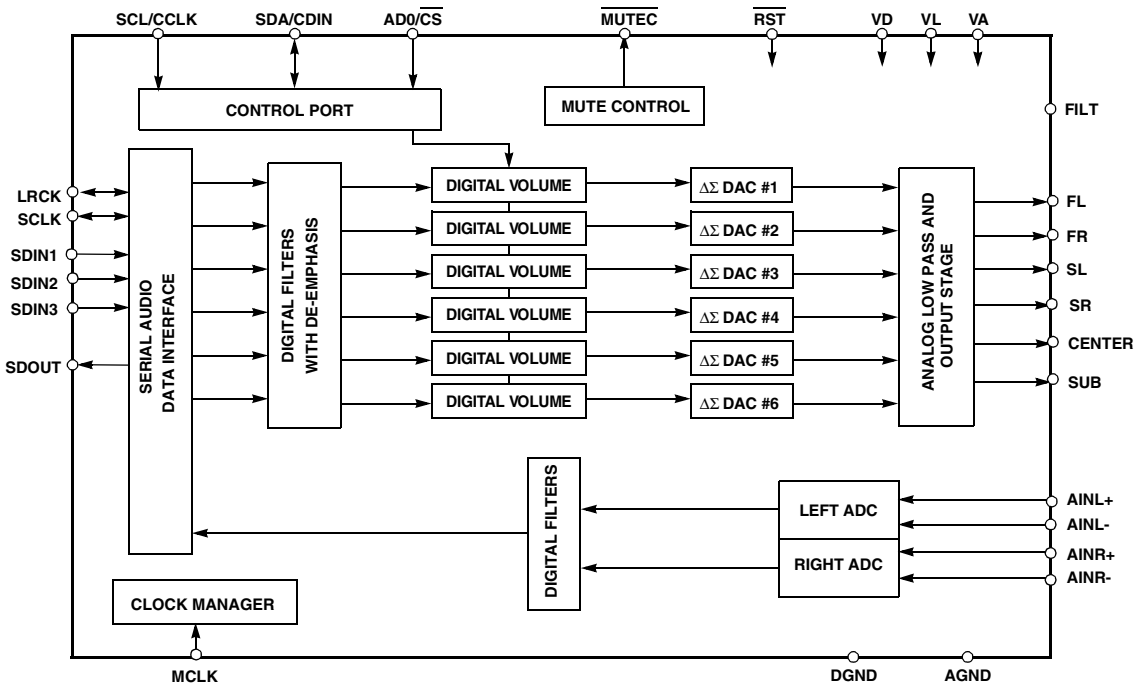


TABLE OF CONTENTS

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to www.cirrus.com

LIST OF FIGURES

LIST OF TABLES

1. CHARACTERISTICS AND SPECIFICATIONS

(Min/Max performance characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics are derived from measurements taken at T_A = 25°C, VA = 5.0V, VD = 5.0V)

SPECIFIED OPERATING CONDITIONS ((AGND, DGND = 0V; all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supply	Digital	VD	4.75	5.0	5.25	V
	Analog	VA	4.75	5.0	5.25	V
	Interface	VL	3.0*	-	5.25	V
	VD - VL (Note 12)		-	-	2.00	V
Specified Temperature Range	(-KS)	T_A	-10	-	70	°C

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supply	Digital	VD	-0.3	6.0	V
	Analog	VA	-0.3	6.0	V
	Interface	VL	-0.3	6.0	V
	VD - VL		-	2.0	V
Input Current	(Note 1)		-	±10	mA
Analog Input Voltage	(Note 2)		-0.7	VA + 0.7	V
Digital Input Voltage	Input Pins		-0.7	VL + 2.5	V
	Bidirectional Pins (Notes 2 and 3)		-0.7	VL + 0.7	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Notes: 1. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

2. The maximum over or under voltage is limited by the input current.

3. Bidirectional pins configured as inputs.

Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

ANALOG CHARACTERISTICS (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 15 pF)

Parameter	Symbol	Base Rate Mode Min	Base Rate Mode Typ	Base Rate Mode Max	High Rate Mode Min	High Rate Mode Typ	High Rate Mode Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB) Differential Input; unless otherwise specified.								
Dynamic Range, -60 dBFS input (A weighted)		91	97	-	91	97	-	dB
(unweighted)			94	-		94	-	dB
Total Harmonic Distortion + Noise (Note 4)	THD+N	-	-88	-83	-	-88	-83	dB
Interchannel Isolation		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Offset Error (with high pass filter)		-	-	0	-	-	0	LSB
Full Scale Input Voltage (Differential):		5.24	5.66	6.09	5.24	5.66	6.09	Vp-p
Gain Drift		-	100	-	-	100	-	ppm/°C
Input Resistance		10	-	-	10	-	-	kΩ
Input Capacitance		-	-	15	-	-	15	pF
A/D Decimation Filter Characteristics								
Passband (Note 5)		0.022	-	21.77	0.022	-	43.54	kHz
Passband Ripple		-	-	0.01	-	-	0.05	dB
Stopband (Note 5)		30.0	-	6114	72.41	-	6071	kHz
Stopband Attenuation (Note 6)		80	-	-	45	-	-	dB
Group Delay	t_{gd}	-	17/Fs	-	-	17/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0	-	-	0	µs
High Pass Filter Characteristics								
Frequency Response: -3 dB (Note 7)		-	3.4	-	-	3.4	-	Hz
-0.13 dB		-	20	-	-	20	-	Hz
Phase Deviation @ 20 Hz (Note 7)		-	10	-	-	10	-	Degree
Passband Ripple		-	-	0	-	-	0	dB

Notes:
4. Referenced to typical full-scale differential input voltage (2 Vrms). Tested at -1 dBFS
5. Filter characteristics scale with output sample rate.
6. The analog modulator samples the input at 128 times Fs. For example, to obtain an output sample rate of 48 kHz the input must be sampled at 6.144 MHz. There is no rejection of input signals which are multiples of the sampling frequency (n × 6.144 MHz ±20.0 kHz where n = 0,1,2,3...).
7. High Pass Filter characteristics are specified for Fs=44.1 kHz.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Base Rate Mode Min	Base Rate Mode Typ	Base Rate Mode Max	High Rate Mode Min	High Rate Mode Typ	High Rate Mode Max	Units
Analog Output Characteristics - Minimum Attenuation, 10 kΩ, 10 pF load; unless otherwise specified.								
Dynamic Range, -60 dBFS input (A weighted)		93	100	-	93	100	-	dB
(unweighted)		-	97	-	-	97	-	dB
Total Harmonic Distortion + Noise (unweighted)	THD+N	-	-90	-83	-	-90	-83	dB
Interchannel Isolation		-	95	-	-	95	-	dB
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Offset Voltage		-	10	-	-	10	-	mV
Full Scale Output Voltage		3.42	3.7	3.98	3.42	3.7	3.98	Vp-p
Gain Drift		-	100	-	-	100	-	ppm/°C
Analog Output Load								
Minimum Load Resistance:		-	10	-	-	10	-	kΩ
Maximum Load Capacitance:		-	100	-	-	100	-	pF
Combined Digital and Analog Filter Characteristics								
Frequency Response 10 Hz to 20 kHz			±0.1			±0.1		dB
Deviation from Linear Phase		-	±0.5	-	-	±0.5	-	Degrees
Passband: to 0.01 dB corner (Notes 8, 9)		0	-	21.77	0	-	43.54	kHz
Passband Ripple (Note 9)		-	-	±0.01	-	-	±0.01	dB
Stopband (Notes 8, 9)		26.2	-	-	62.5	-	-	kHz
Stopband Attenuation (Notes 8, 10)		70	-	-	65	-	-	dB
Group Delay (Fs = Input Word Rate)	tgd	-	29/Fs	-	-	17/Fs	-	s
Analog Loopback Performance								
Signal-to-noise Ratio (CCIR-2K weighted, -20 dB FS input)	CCIR-2K	-	90	-	-	90	-	dB

8. The passband and stopband edges scale with frequency. For input word rates, Fs, other than 44.1 kHz, the 0.01 dB passband edge is 0.4535×Fs and the stopband edge is 0.5465×Fs.
9. Digital filter characteristics.
10. Measurement bandwidth is 10 Hz to 3 Fs.

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current	normal operation, V_A= V_D =V_L =5V					
(Note 11, Note 12)	BRM	I_A	-	35	42	mA
		I_D	-	78	105	mA
		I_L	-	0.3	2	mA
	power-down state (all supplies) (Note 13)					
	BRM	I_A	-	0.2	1	mA
		I_D	-	0.4	15	mA
		I_L	-	0.2	0.5	mA
Power Dissipation	(Note 11)					
V_A= V_D = V_L = 5V	normal operation		-	567	715	mW
	power-down (Note 13)		-	4	12.5	mW
Package Thermal Resistance	TSSOP (-KS)	θ_{JA}	-	56	-	°C/Watt
		θ_{JC}	-	37	-	°C/Watt
Power Supply Rejection Ratio	(1 kHz, 10 mV_{rms})	PSRR	-	50	-	dB

Notes: 11. Current consumption increases with increasing FS and increasing MCLK. Variance between speed modes is small.

12. VD current consumption increases (ID normal and ID_pdn) when VD - VL > 1.5V. When VD - VL = 1.7V, I_D typically increases by 2 mA and when VD - VL = 2V, I_D typically increases by 12 mA.

13. Power down mode is defined as $\overline{RST}$ pin = Low with clocks running.

DIGITAL CHARACTERISTICS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
High-level Input Voltage	VL=5V	V_{IH}	0.7 x VL	-	V
Low-level Input Voltage		V_{IL}	-	0.3 x VL	V
High-level Input Voltage	VL=3.3V	V_{IH}	2.2	-	V
Low-level Input Voltage		V_{IL}	-	1.0	V
High-level Output Voltage at					
VL = 5V	I_0 = -2.0 mA	V_{OH}	VL - 1.0	-	V
	I_0 = -100 µA	V_{OH}	VL - 0.7	-	V
VL = 3.3V	I_0 = -2.0 mA	V_{OH}	2.3	-	V
Low-level Output Voltage at					
VL = 5V	I_0 = 2.0 mA	V_{OL}	-	0.4	V
	I_0 = 100 µA	V_{OL}	-	0.2	V
VL = 3.3V	I_0 = -2.0 mA	V_{OL}	-	0.4	V
Input Leakage Current	(Digital Inputs)		-	10	µA
Output Leakage Current	(High-Impedance Digital Outputs)		-	10	µA

SWITCHING CHARACTERISTICS (Inputs: Logic 0 = 0V, Logic 1 = VL)

Parameter		Symbol	Min	Typ	Max	Units
Audio ADC's and DAC's Sample Rate	BRM	Fs	30	-	50	kHz
	HRM		60	-	100	kHz
MCLK Frequency	(Note 14)		3.84	-	25.6	MHz
MCLK Duty Cycle	BRM					
	MCLK =128, 384 Fs		40	50	60	%
	MCLK = 256, 512 Fs		40	50	60	%
	HRM					
	MCLK = 64, 192 Fs		40	50	60	%
	MCLK = 128, 256 Fs		40	50	60	%
$\overline{\text{RST}}$ Low Time	(Note 15)		1	-	-	ms
SCLK Falling Edge to SDOUT Output Valid	(Note 16)	t_{dpd}		-	50	ns
LRCK Edge to MSB Valid		t_{lrpd}		-	20	ns
SDIN Setup Time Before SCLK Rising Edge		t_{ds}		-	10	ns
SDIN Hold Time After SCLK Rising Edge		t_{dh}		-	30	ns
SCLK Period BRM	(Note 17)	t_{sck}	$\frac{1}{(128)Fs}$	-	-	ns
SCLK Period HRM	(Note 17)	t_{sck}	$\frac{1}{(64)Fs}$	-	-	ns
Master Mode						
SCLK Falling to LRCK Edge		t_{mslr}		$\pm$10	-	ns
SCLK Duty Cycle				50	-	%
Slave Mode						
SCLK High Time		t_{sckh}	50	-	-	ns
SCLK Low Time		t_{sckl}	50	-	-	ns
SCLK rising to LRCK Edge		t_{lrckd}	25	-	-	ns
LRCK Edge to SCLK Rising		t_{lrcks}	25	-	-	ns

Notes: 14. See CI1:0 register on page 22 for settings.

15. After powering up the CS4228A, $\overline{\text{RST}}$ should be held low for 1 ms after the power supplies and clocks are settled.

16. Scales with sample rate Fs. 50 ns valid at 48 kHz, more time at slower Fs and less time at faster Fs.

17. See DCK1:0 register on page 25 for settings.

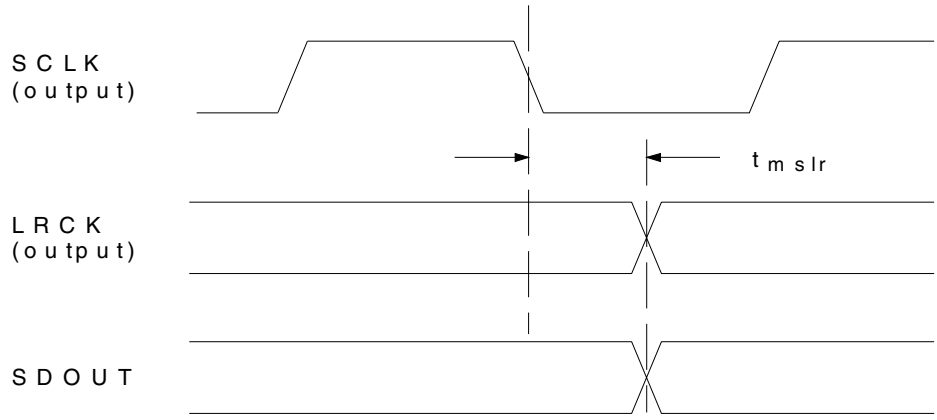


Figure 1. Serial Audio Port Master Mode Timing

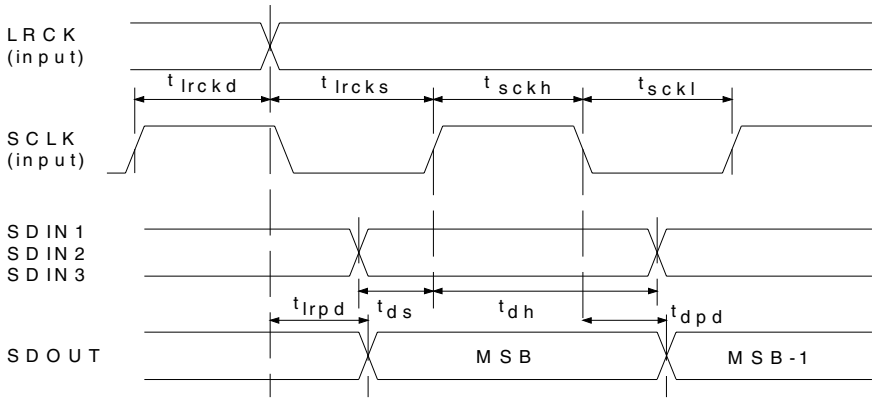


Figure 2. Serial Audio Port Slave Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT (Inputs: Logic 0 = 0V, Logic 1 = VL)

Parameter		Symbol	Min	Max	Units
SPI Mode (SDOUT > 47 kΩ to GND)					
CCLK Clock Frequency		f_{sck}	-	6	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0		µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20		ns
CCLK Low Time		t_{scl}	66		ns
CCLK High Time		t_{sch}	66		ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40		ns
CCLK Rising to DATA Hold Time	(Note 18)	t_{dh}	15		ns
Rise Time of CCLK and CDIN	(Note 19)	t_{r2}		30	ns
Fall Time of CCLK and CDIN	(Note 19)	t_{f2}		100	ns

Notes: 18. Data must be held for sufficient time to bridge the transition time of CCLK.

19. For F_{SCK} < 1 MHz

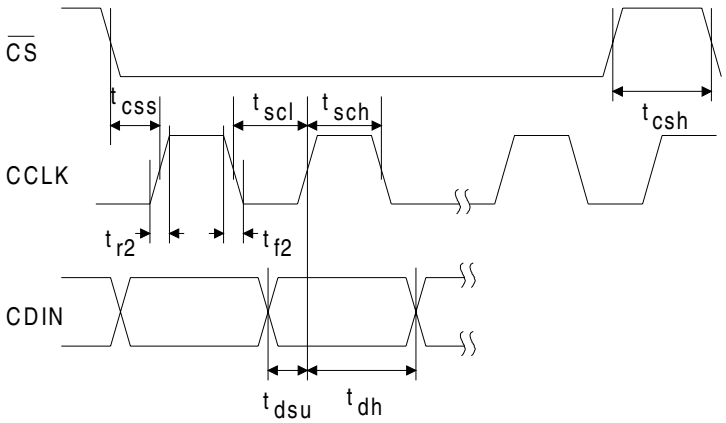


Figure 3. SPI Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT (Inputs: Logic 0 = 0V, Logic 1 = VL)

Parameter	Symbol	Min	Max	Units
I²C Mode (SDOUT < 47 kΩ to ground)				
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7		µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0		µs
Clock Low Time	t_{low}	4.7		µs
Clock High Time	t_{high}	4.0		µs
Setup Time for Repeated Start Condition	t_{sust}	4.7		µs
SDA Hold Time from SCL Falling (Note 20)	t_{hdd}	0		µs
SDA Setup Time to SCL Rising	t_{sud}	250		ns
Rise Time of Both SDA and SCL Lines (Note 21)	t_r		30	ns
Fall Time of Both SDA and SCL Lines	t_f		300	ns
Setup Time for Stop Condition	t_{susp}	4.7		µs

Notes: 20. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

21. Pin 11 (SCL/CCLK) of the CS4228A does not have sufficient hysteresis to enable the use of standard two-wire mode configurations with a resistor pull-up. This issue can be worked around by placing a Schmitt Trigger buffer, for example a 74VHC14, on the SCL line just prior to the CS4228A. See Figure 5. This will not affect the operation of the bus in either mode, as pin 6 is an input only.

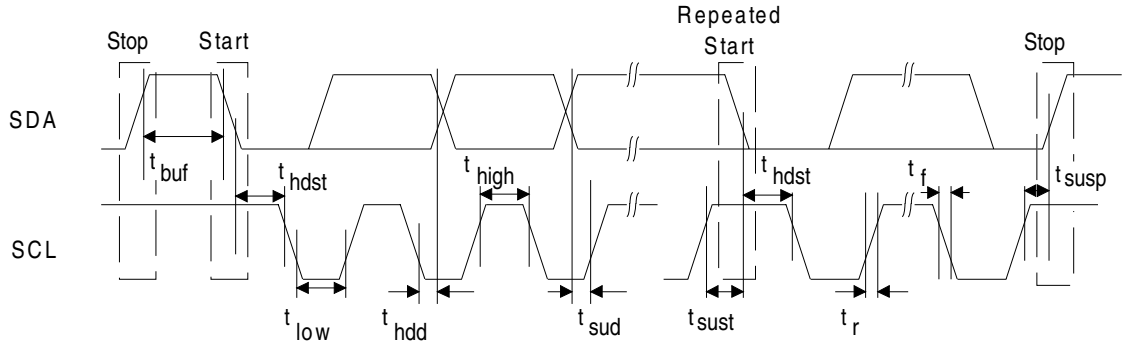


Figure 4. I²C Control Port Timing

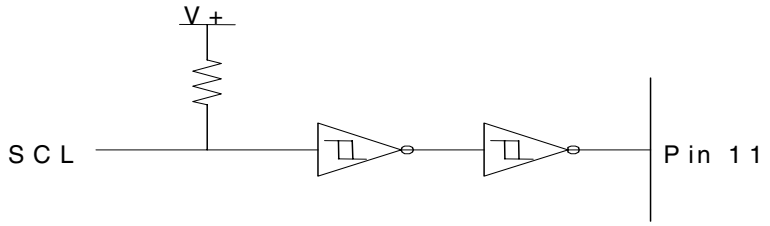


Figure 5. I²C Mode SCL Buffer Example

2. TYPICAL CONNECTION DIAGRAM

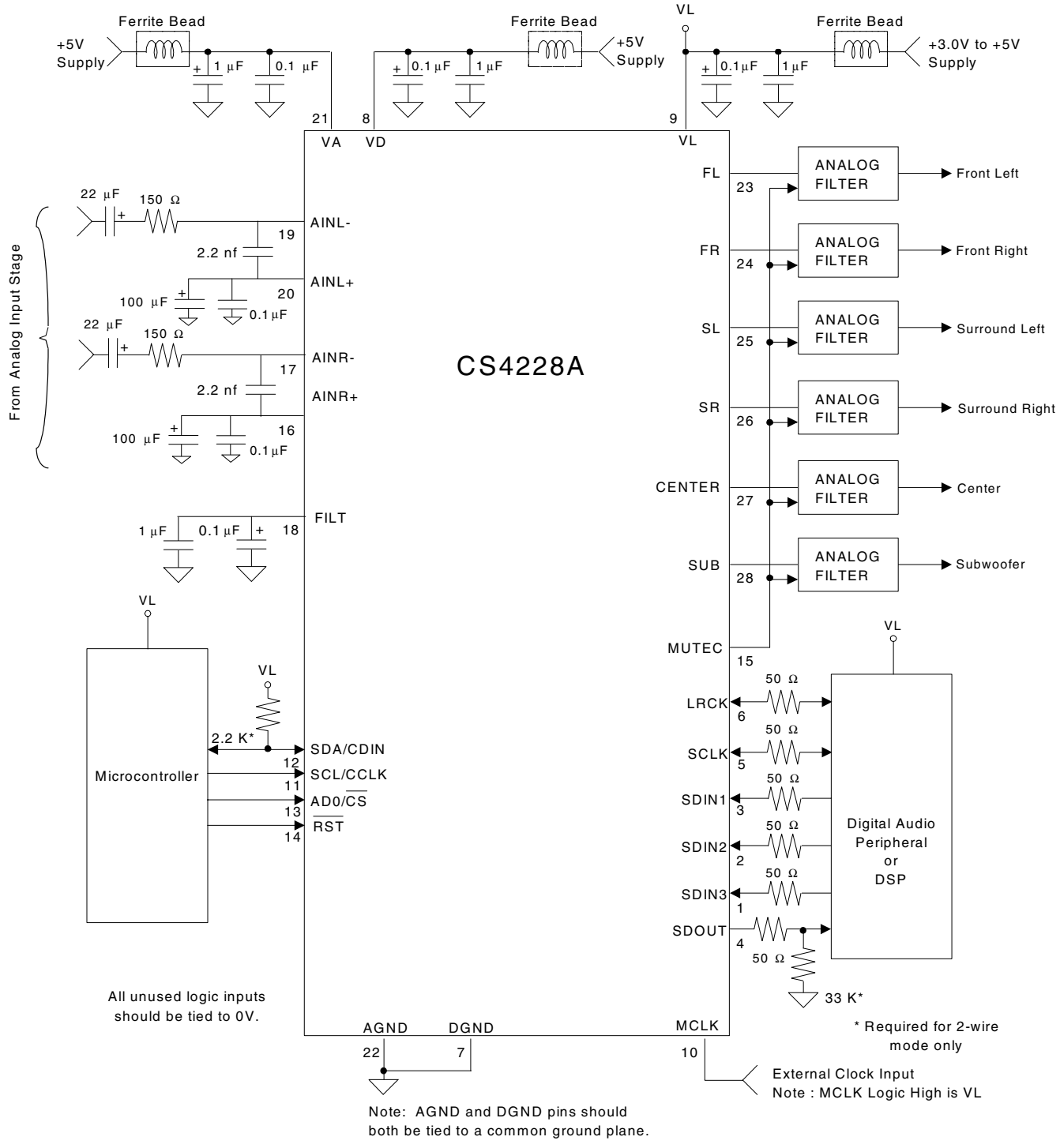


Figure 6. Recommended Connection Diagram

3. FUNCTIONAL DESCRIPTION

3.1 Overview

The CS4228A is a 24-bit audio codec comprised of 2 analog-to-digital converters (ADC) and 6 digital-to-analog converters (DAC), all implemented using single-bit delta-sigma techniques. Other functions integrated with the codec include independent digital volume controls for each DAC, digital DAC de-emphasis filters, ADC high-pass filters, an on-chip voltage reference, and a flexible serial audio interface. All functions are configured through a serial control port operable in SPI mode and in I^2C mode. Figure 6 shows the recommended connections for the CS4228A.

3.2 Analog Inputs

3.2.1 Line Level Inputs

AINR+, AINR-, AINL+, and AINL- are the line level analog inputs (See Figure 6). These pins are internally biased to a DC operating voltage of approximately 2.3 VDC. AC coupling the inputs preserves this bias and minimizes signal distortion. Figure 6 shows operation with a single-ended input source. This source may be supplied to either the positive or negative input as long as the unused input is connected to ground through capacitors as shown. When operated with single-ended inputs, distortion will increase at input levels higher than -1 dBFS. Figure 7 shows an example of a differential input circuit.

Muting of the stereo ADC is possible through the ADC Control Byte.

The ADC output data is in 2's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively.

3.2.2 High Pass Filter

Digital high pass filters in the signal path after the ADCs remove any DC offsts present on the analog inputs. The high pass filter helps prevent audible "clicks" when switching between audio sources downstream from the ADCs. The high pass filter response, given in "High Pass Filter Characteristics", scales linearly with sample rate. Thus, for High Rate Mode, the -3 dB frequency at a 96 kHz sample rate will be equal to 96/44.1 times that at a sample rate of 44.1 kHz.

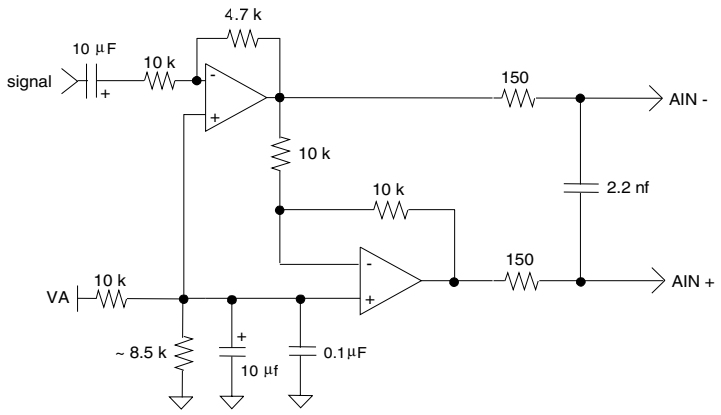


Figure 7. Optional Line Input Buffer

The high pass filters can be disabled by setting the HPF bit in the ADC Control register. When asserted, any DC present at the analog inputs will be represented in the ADC outputs. The high pass filter may also be "frozen" using the HPFZ bit in the ADC Control register. In this condition, it will remember the DC offset present at the ADC inputs at the moment the HPFZ bit was asserted, and will continue to remove this DC level from the ADC outputs. This is useful in cases where it is desirable to eliminate a fixed DC offset while still maintaining full frequency response down to DC.

3.3 Analog Outputs

3.3.1 Line Level Outputs

The CS4228A contains on-chip buffer amplifiers capable of producing line level outputs. These amplifiers are biased to a quiescent DC level of approximately 2.3V. This bias, as well as variations in offset voltage, are removed using off-chip AC load coupling.

The delta-sigma conversion process produces high frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low pass filter. For most applications, a simple passive filter as shown in Figure 8 can be used. Note that this circuit also serves to block the DC present at the outputs. Figure 9 gives an example of a filter which can be used in applications where greater out of band attenuation is desired. The 2-pole Butterworth filter has a -3 dB frequency of 50 kHz, a passband attenuation of 0.1 dB at 20 kHz, providing optimal out-of-band filtering for sample rates from 44.1 kHz to 96 kHz. The filter has and a gain of 1.56, providing a 2 Vrms output signal.

3.3.2 Digital Volume Control

Each DAC's output level is controlled via the Digital Volume Control register operating over the range of 0 to 90.5 dB attenuation with 0.5 dB resolution. Volume control changes do not occur instantaneously. Instead they ramp in increments of 0.125 dB at a variable rate controlled by the RMP1:0 bits in the Digital Volume Control register.

Each output can be independently muted via mute control bits MUT6-1 in the DAC Mute1 Control register. When asserted, MUT attenuates the corresponding DAC to its maximum value (90.5 dB). When MUT is deasserted, the corresponding DAC

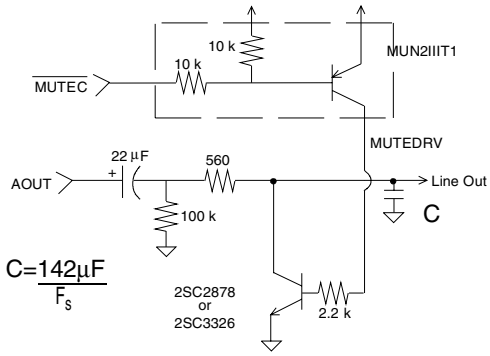
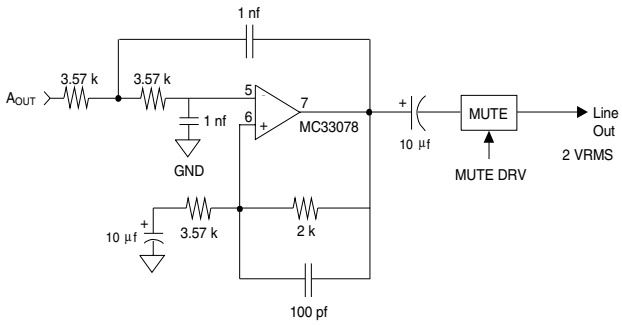


Figure 8. Passive Output Filter with Mute



2-Pole Butterworth Filter

Figure 9. Butterworth Output Filter with Mute

returns to the attenuation level set in the Digital Volume Control register. The attenuation is ramped up and down at the rate specified by the RMP1:0 bits.

To achieve complete digital attenuation of an incoming signal, Hard Mute controls are provided. When asserted, Hard Mute will send zero data to a corresponding pair of DACs. Hard Mute is not ramped, so it should only be asserted after setting the two corresponding MUT bits to prevent high frequency transients from appearing on the DAC outputs. Hard Mute is controlled by the HMUTE56/34/12 bits in the DAC Mute2 Control register.

3.4 Mute Control

The Mute Control pin is typically connected to an external mute control circuit as shown in Figure 8 and Figure 9. The Mute Control pin is asserted during power up, power down, and when serial port clock errors are present. The pin can also be controlled by the user via the control port, or automatically asserted when zero data is present on all six DAC inputs. To prevent large transients on the output, it is desirable to mute the DAC outputs before the Mute Control pin is asserted. Please see the $\overline{\text{MUTEC}}$ pin in the Pin Descriptions section for more information.

3.5 Clock Generation

The master clock, MCLK, is supplied to the CS4228A from an external clock source. If MCLK stops for 10 µs, the CS4228A will enter Power Down Mode in which the supply current is reduced as specified under “Power Supply”. In all modes it is required that the number of MCLK periods per SCLK and LRCK period be constant.

3.5.1 Clock Source

The CS4228A internal logic requires an external master clock, MCLK, that operates at multiples of the sample rate frequency, Fs. The MCLK/Fs ratio is determined by the CI1:0 bits in the CODEC Clock Mode register.

3.5.2 Synchronization

The serial port is internally synchronized with MCLK. If from one LRCK cycle to the next, the number of MCLK cycles per LRCK cycle changes by more than 32, the CS4228A will undergo an internal reset of its data paths in an attempt to resynchronize. Consequently, it is advisable to mute the DACs and clear the $\overline{\text{DIGPDN}}$ bit when changing from one clock source to another to avoid the output of undesirable audio signals as the device resynchronizes. It is adviseable to ensure that MCLK complies with the Switching Characteristics at all times when switching clock sources without resetting the part.

3.6 Digital Interfaces

3.6.1 Serial Audio Interface Signals

The serial audio data is presented in 2's complement binary form with the MSB first in all formats. The serial interface clock, SCLK, is used for both transmitting and receiving audio data. SCLK can be generated by the CS4228A (master mode) or it can be input from an external source (slave mode). Mode selection is made with the DMS1:0 bits in the Serial Port Mode register. The number of SCLK cycles in one sample period can be set using the DCK1:0 bits as detailed in the Serial Port Mode register.

The Left/Right clock (LRCK) is used to indicate left and right data frames and the start of a new sample period. It may be an output of the CS4228A (master mode), or it may be generated by an external source (slave mode). The frequency of LRCK is the same as the system sample rate, Fs.

SDIN1, SDIN2, and SDIN3 are the data input pins. SDOUT, the data output pin, carries data from the two 24-bit ADC's. The serial audio port may also be operated in One Line Data Mode in which all 6

channels of DAC data is input on SDIN1 and the stereo ADC data is output on SDOUT. Table 1 outlines the serial port input to DAC channel allocations.

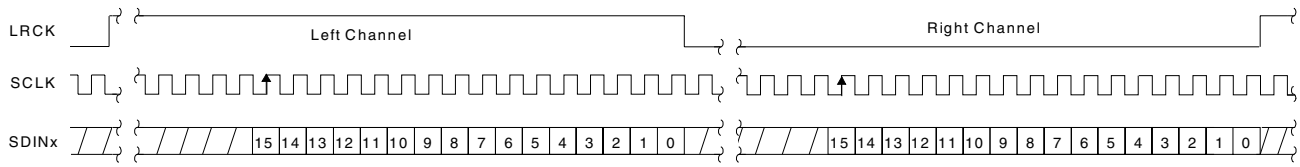
DAC Inputs		
SDIN1	left channel	DAC #1
	right channel	DAC #2
	single line	All 6 DAC channels (BRM)
SDIN2	left channel	DAC #3
	right channel	DAC #4
SDIN3	left channel	DAC #5
	right channel	DAC #6

Table 1. Serial Audio Port Input Channel Allocations

3.6.2 Serial Audio Interface Formats

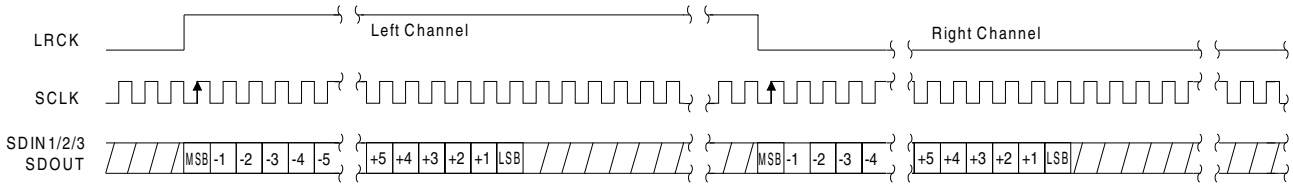
The digital audio port supports 6 formats, shown in Figure 10, 11, 12 and 13. These formats are selected using the DDF2:0 bits in the Serial Port Mode register.

In One Line Data Mode, all 6 DAC channels are input on SDIN1. One Line Data Mode is only available in BRM. See Figure 13 for channel allocations.



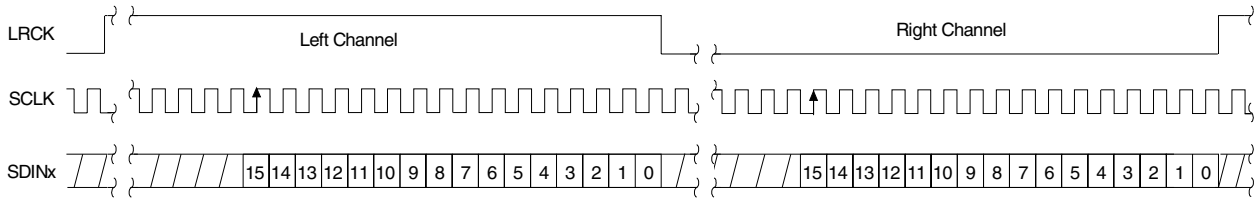
I2S Mode, Data Valid on Rising Edge of SCLK		
Bits/Sample	SCLK Rate(s)	Notes
16	32, 48, 64, 128 Fs 32, 64 Fs	BRM, 48 Fs available in slave mode only HRM
18 to 24	48, 64, 128 Fs 64 Fs	BRM, 48 Fs available in slave mode only HRM

Figure 10. I²S Serial Audio Formats



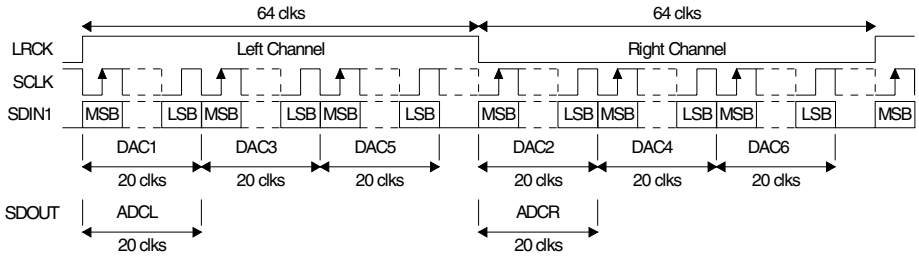
Left Justified Mode, Data Valid on Rising Edge of SCLK		
Bits/Sample	SCLK Rate(s)	Notes
16	32, 48, 64, 128 Fs 32, 64 Fs	BRM, 48 Fs available in slave mode only HRM
18 to 24	48, 64, 128 Fs 64 Fs	BRM, 48 Fs available in slave mode only HRM

Figure 11. Left Justified Serial Audio Formats



Right Justified Mode, Data Valid on Rising Edge of SCLK		
Bits/Sample	SCLK Rate(s)	Notes
16	32, 48, 64, 128 Fs 32, 64 Fs	BRM, 48 Fs available in slave mode only HRM
20	48, 64, 128 Fs 64 Fs	BRM, 48 Fs available in slave mode only HRM
24	48, 64, 128 Fs 64 Fs	BRM, 48 Fs available in slave mode only HRM

Figure 12. Right Justified Serial Audio Formats



One Line Data Mode, Data Valid on Rising Edge of SCLK		
Bits/Sample	SCLK Rate(s)	Notes
20	128 Fs	6 inputs, 2 outputs, BRM only

Figure 13. One Line Data Serial Audio Format

3.7 Control Port Signals

Internal registers are accessed through the control port. The control port may be operated asynchronously with respect to audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no register access is required.

The control port has 2 operating modes: SPI mode and I^2C mode. In both modes the CS4228A operates as a slave device. Mode selection is determined by the state of the SDOUT pin when $\overline{RST}$ transitions from low to high: high for SPI, low for I^2C mode. SDOUT is internally pulled high to VL. A resistive load from SDOUT to GND of less than 47 kΩ will enable I^2C mode after a hardware reset.

3.7.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS4228A chip select signal, CCLK is the control port bit clock input, and CDIN is the input data line. There is no data output line, therefore all registers are write-only in SPI mode. Data is clocked in on the rising edge of CCLK.

Figure 13 shows the operation of the control port in SPI mode. The first 7 bits on CDIN, after $\overline{CS}$ goes low, form the chip address (0010000). The eighth bit is a read/write indicator (R/$\overline{W}$), which should always be low to write. The next 8 bits set the Memory Address Pointer (MAP) which is the address of the register that is to be written. The following bytes contain the data which will be placed into the registers designated by the MAP.

The CS4228A has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is zero, then the MAP will stay constant for successive writes. If INCR is 1, then the MAP will increment after each byte is written, allowing block reads, or writes, of successive registers.

3.7.2 I^2C Mode

In I^2C mode, SDA is a bidirectional data line. Data is clocked into and out of the port by the SCL clock. The signal timing is shown in Figure 15 and 16. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low.

The first byte sent to the CS4228A after a Start condition consists of a 7 bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The AD0 pin determines the LSB of the chip address field. The upper 6 bits of the address field must be 00100 and the seventh bit must match AD0. If the operation is to be a write, the second byte is the Memory Address Ponter (MAP), which selects the register to be written. The succeeding byte(s) are data. If the operation is to be a read, the second byte is sent from the chip to the controller and contains the contents of the register pointed to by the current value of the MAP.

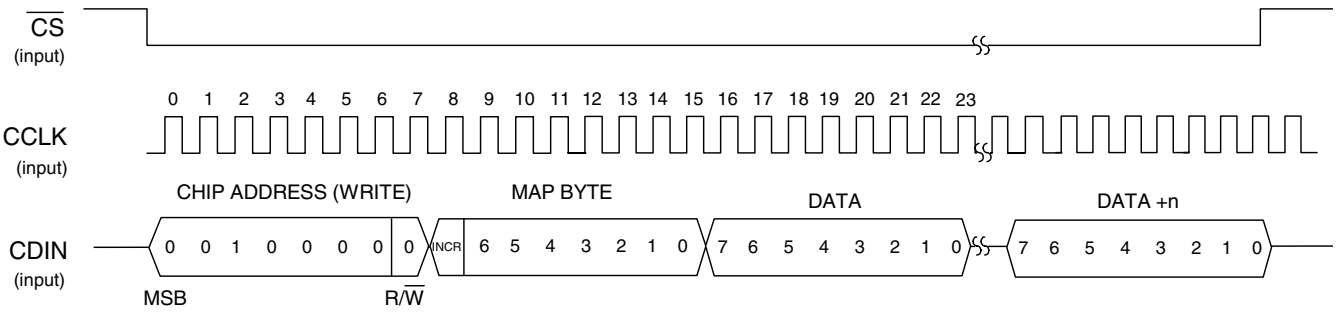


Figure 14. Control Port Timing, SPI Slave Mode Write

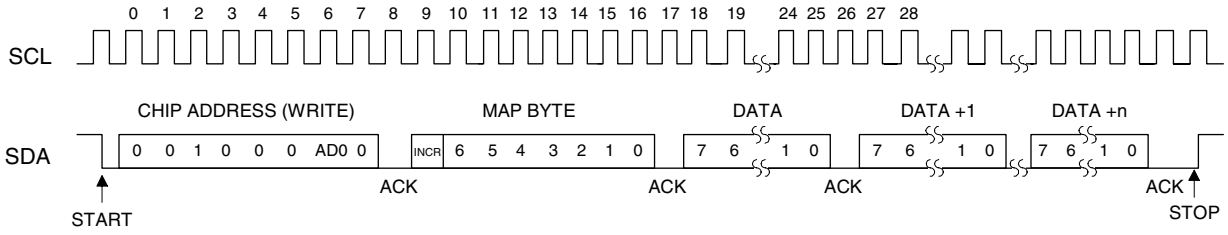


Figure 15. Control Port Timing, I²C Slave Mode Write

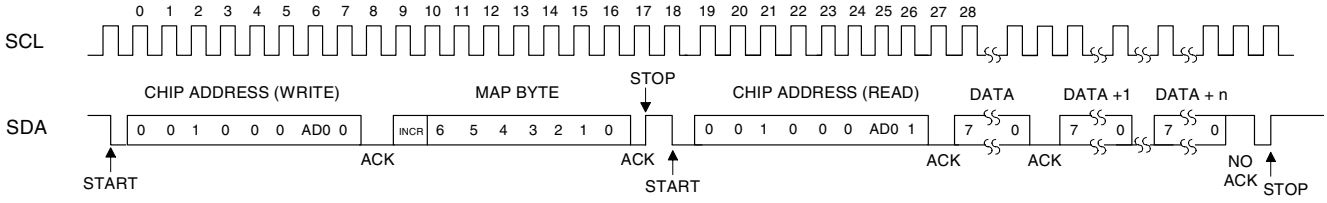


Figure 16. Control Port Timing, I²C Slave Mode Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 16, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 001000x0 chip address & write operation.

Receive acknowledge bit.

Send MAP byte, auto increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 001000x1 chip address & read operation.

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

3.8 Control Port Bit Definitions

All registers are read/write, except the Chip Status register which is read-only. For more detailed information, see the bit definition tables.

3.9 Power-up/Reset/Power Down Mode

Upon power up, the user should hold $\overline{RST} = 0$ until the power supplies and clocks stabilize. In this state, the control registers are reset to their default settings, and the device remains in a low power mode in which the control port is inactive. The part may be held in a low power reset state by clearing the $\overline{DIGPDN}$ bit in the Chip Control register. In this state, the digital portions of the CODEC are in reset, but the control port is active and the desired register settings can be loaded. Normal operation is achieved by setting the $\overline{DIGPDN}$ bit to 1, at which time the CODEC powers up and normal operation begins.

The CS4228A will enter a stand-by mode if the master clock source stops for approximately 10 µs or if the number of MCLK cycles per LRCK period varies by more than 32. Should this occur, the control registers retain their settings.

The CS4228A will mute the analog outputs, assert the $\overline{\text{MUTEC}}$ pin and enter the Power Down Mode if the supply drops below approximately 4V.

3.10 Power Supply, Layout, and Grounding

The CS4228A requires careful attention to power supply and grounding details. VA is normally supplied from the system 5 VDC analog supply. VD is from a 5 VDC digital supply. VL should be from the supply used for the devices digitally interfacing with the CS4228A. Attention should be placed on the VL and VD power up sequence such that the VD supply is applied at the same time or after VL supply is applied (see "Specified Operating Conditions" on page 4).

AGND and DGND pins should both be tied to a solid ground plane surrounding the CS4228A. The system analog and digital ground planes should not be separated under normal circumstances. A solid ground plane underneath the part is recommended.

Decoupling capacitors should be mounted and routed in such a way as to minimize the circuit path length from the CS4228A supply pin or FILT pin, through the capacitor, and back to the applicable CS4228A AGND or DGND pin. The small value ceramic capacitors should be closest to the part. In some cases, ferrite beads in the VL, VD and VA supply lines, and low-value resistances (~ 50 Ω) in series with the LRCK, SCLK, SDIN and SDOUT lines can help reduce coupling of digital signals into the analog portions of the CS4228A.

Both capacitors on the FILT pin should be as close to the CS4228A as possible. Any noise that couples onto the FILT pin will couple directly onto all of the analog outputs. Please see the CDB4228 evaluation board data sheet for recommended layout of the decoupling components.

4. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
MAP	Memory Address Pointer	INCR	Reserved	Reserved	MAP4	MAP3	MAP2	MAP1	MAP0
		1	0	0	0	0	0	0	1
0x01	CODEC Clock Mode	HRM	Reserved	Reserved	Reserved	CI1	CI0	Reserved	Reserved
	default=0x04	0	0	0	0	0	1	0	0
0x02	Chip Control	$\overline{\text{DIGPDN}}$	Reserved	Reserved	ADCPDN	DACPDN56	DACPDN34	DACPDN12	Reserved
	default=0x80	1	0	0	0	0	0	0	0
0x03	ADC Control	MUTL	MUTR	HPF	HPFZ	Reserved	Reserved	Reserved	Reserved
	default=0x00	0	0	0	0	0	0	0	0
0x04	DAC Mute1 Control	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1	RMP1	RMP0
	default=0xFC	1	1	1	1	1	1	0	0
0x05	DAC Mute2 Control	MUTEC	MUTCZ	Reserved	Reserved	HMUTE56	HMUTE34	HMUTE12	Reserved
	default=0x80	1	0	0	0	0	0	0	0
0x06	DAC De-emphasis Control	DEMS1	DEMS0	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1
	default=0x80	1	0	0	0	0	0	0	0
0x07	DAC 1 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x08	DAC 2 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x09	DAC 3 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x0A	DAC 4 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x0B	DAC 5 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x0C	DAC 6 Volume Cntrl	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
	default=0x00	0	0	0	0	0	0	0	0
0x0D	Serial Port Mode	DCK1	DCK0	DMS1	DMS0	Reserved	DDF2	DDF1	DDF0
	default=0x84	1	0	0	0	0	1	0	0
0x0E	Chip Status	CLKERR	ADCOVL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	read only	X	X	0	0	0	0	0	0
		7	6	5	4	3	2	1	0

Table 2. User Registers

5. REGISTER DESCRIPTIONS

All registers are read/write except for Chip Status, which is read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in the tables underneath each bit's label. Default values are also marked in the text with an asterisk.

5.1 Memory Address Pointer (MAP)

Not a register

7	6	5	4	3	2	1	0
INCR	RESERVED		MAP4	MAP3	MAP2	MAP1	MAP0
1	0	0	0	0	0	0	1

INCR — memory address pointer auto increment control
- 0 - MAP is not incremented automatically.
- *1 - internal MAP is automatically incremented after each read or write.

MAP4:0 — Memory address pointer (MAP). Sets the register address that will be read or written by the control port.

5.2 CODEC Clock Mode

Address 0x01

7	6	5	4	3	2	1	0
HRM	RESERVED			CI1	CI0	RESERVED	
0	0	0	0	0	1	0	0

HRM — Sets the sample rate mode for the ADCs and DACs
- *0 - Base Rate Mode (BRM) supports sample rates up to 50 kHz
- 1 - High Rate Mode (HRM) supports sample rates up to 100 kHz. Typically used for 96 kHz sample rate.

CI1:0 — Specifies the ratio of MCLK to the sample rate of the ADCs and DACs (Fs)

CI1:0	BRM (Fs)	HRM (Fs)
0	128	64
*1	256	128
2	384	192
3	512	256

5.3 Chip Control

Address 0x02

7	6	5	4	3	2	1	0
$\overline{\text{DIGPDN}}$	RESERVED		ADCPDN	DACPDN56	DACPDN34	DACPDN12	RESERVED
1	0	0	0	0	0	0	0

$\overline{\text{DIGPDN}}$ — Power down the digital portions of the CODEC
- 0 - Digital power down.
- *1 - Normal operation

ADCPDN — Power down the analog section of the ADC
- *0 - Normal
- 1 - ADC power down.

DACPDN12 Power down the analog section of DAC 1 and 2
*0 - Normal
1 - Power down DAC 1 and 2.

DACPDN34 Power down the analog section of DAC 3 and 4
*0 - Normal
1 - Power down DAC 3 and 4.

DACPDN56 Power down the analog section of DAC 5 and 6
*0 - Normal
1 - Power down DAC 5 and 6.

5.4 ADC Control

Address 0x03

7	6	5	4	3	2	1	0
MUTL	MUTR	HPF	HPFZ	RESERVED			
0	0	0	0	0	0	0	0

MUTL, MUTR ADC left and right channel mute control
*0 - Normal
1 - Selected ADC output muted

HPF ADC DC offset removal. See “High Pass Filter” for more information
*0 - Enabled
1 - Disabled

HPFZ ADC DC offset averaging freeze. See “High Pass Filter” for more information
*0 - Normal. The DC offset average is dynamically calculated and subtracted from incoming ADC data.
1 - Freeze. The DC offset average is frozen at the current value and subtracted from incoming ADC data. Allows passthru of DC information.

5.5 DAC Mute1 Control

Address 0x04

7	6	5	4	3	2	1	0
MUT6	MUT5	MUT4	MUT3	MUT2	MUT1	RMP1	RMP0
1	1	1	1	1	1	0	0

MUT6 - MUT1 Mute control for DAC6 - DAC1 respectively. When asserted, the corresponding DAC is digitally attenuated to its maximum value (90.5 dB). When deasserted, the corresponding DAC attenuation value returns to the value stored in the corresponding Digital Volume Control register. The attenuation value is ramped up and down at the rate specified by RMP1:0.
0 - Normal output level
*1 - Selected DAC output fully attenuated.

RMP1:0 Attenuation ramp rate.
*0 - 0.5 dB change per 4 LRCKs
1 - 0.5 dB change per 8 LRCKs
2 - 0.5 dB change per 16 LRCKs
3 - 0.5 dB change per 32 LRCKs

5.6 DAC Mute2 Control

Address 0x05

7	6	5	4	3	2	1	0
MUTEC	MUTCZ	RESERVED		HMUTE56	HMUTE34	HMUTE12	RESERVED
1	0	0	0	0	0	0	0

MUTEC — Controls the $\overline{\text{MUTEC}}$ pin
- 0 - Normal operation
- *1 - $\overline{\text{MUTEC}}$ pin asserted low

MUTCZ — Automatically asserts the $\overline{\text{MUTEC}}$ pin on consecutive zeros. When enabled, 512 consecutive zeros on all six DAC inputs will cause the $\overline{\text{MUTEC}}$ pin to be asserted low. A single non-zero value on any DAC input will cause the $\overline{\text{MUTEC}}$ pin to deassert.
- *0 - Disabled
- 1 - Enabled

HMUTE56/34/12 — Hard mute the corresponding DAC pair. When asserted, zero data is sent to the corresponding DAC pair causing an instantaneous mute. To prevent high frequency transients on the outputs, a DAC pair should be fully attenuated by asserting the corresponding MUT6-MUT1 bits in the DAC Mute Control register or by writing 0xFF to the corresponding Digital Volume Control registers before asserting HMUTE.
- *0 - Normal operation
- 1 - DAC pair is muted

5.7 DAC De-emphasis Control

Address 0x06

7	6	5	4	3	2	1	0
DEMS1	DEMS0	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1
1	0	0	0	0	0	0	0

DEMS1:0 — Selects the DAC de-emphasis response curve.
- 0 - Reserved
- 1 - De-emphasis for 48 kHz
- *2 - De-emphasis for 44.1 kHz
- 3 - De-emphasis for 32 kHz

DEM6 - DEM1 — De-emphasis control for DAC6 - DAC1 respectively
- *0 - De-emphasis off
- 1 - De-emphasis on

5.8 Digital Volume Control

Addresses 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C

7	6	5	4	3	2	1	0
VOLn							
0	0	0	0	0	0	0	0

VOL6 - VOL1 — Address 0x0C - 0x07 sets the attenuation level for DAC 6 - DAC1 respectively. The attenutation level is ramped up and down at the rate specified by RMP1:0 in the DAC Volume Control Setup register.
0 - 181 represents 0 to 90.5 dB of attenuation in 0.5 dB steps.

5.9 Serial Port Mode

Address 0x0D

7	6	5	4	3	2	1	0
DCK1	DCK0	DMS1	DMS0	RESERVED	DDF2	DDF1	DFF0
1	0	0	0	0	1	0	0

DCK1:0 Sets the number of Serial Clocks (SCLK) per Fs period (LRCLK)

DCK1:0	BRM (Fs)	HRM (Fs)
0	32 (1)	(3)
1	48 (2)	(3)
2	*64	32 (1)
3	128	64

Notes: 1. All formats will default to 16 bits
2. Slave mode only
3. Invalid mode

DMS1:0 Sets the master/slave mode of the serial audio port
- *0 - Slave (External LRCLK, SCLK)
- 1 - Reserved
- 2 - Reserved
- 3 - Master (No 48 Fs SCLK in BRM)

DDF2:0 Serial Port Data Format
- 0 - Right Justified, 24-bit
- 1 - Right Justified, 20-bit
- 2 - Right Justified, 16-bit
- 3 - Left Justified, maximum 24-bit
- *4 - I^2S compatible, maximum 24-bit
- 5 - One-line Data Mode, available in BRM only
- 6 - Reserved
- 7 - Reserved

5.10 Chip Status

Address 0x0E

7	6	5	4	3	2	1	0
CLKERR	ADCOVL	RESERVED					
X	X	0	0	0	0	0	0

CLKERR Clocking system status, read only
- 0 - No Error
- 1 - No MCLK is present, or a request for clock change is in progress

ADCOVL ADC overflow bit, read only
- 0 - No overflow
- 1 - ADC overflow has occurred