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CS42325

10-In, 6-Out, 2 Vrms Audio CODEC with Headphone

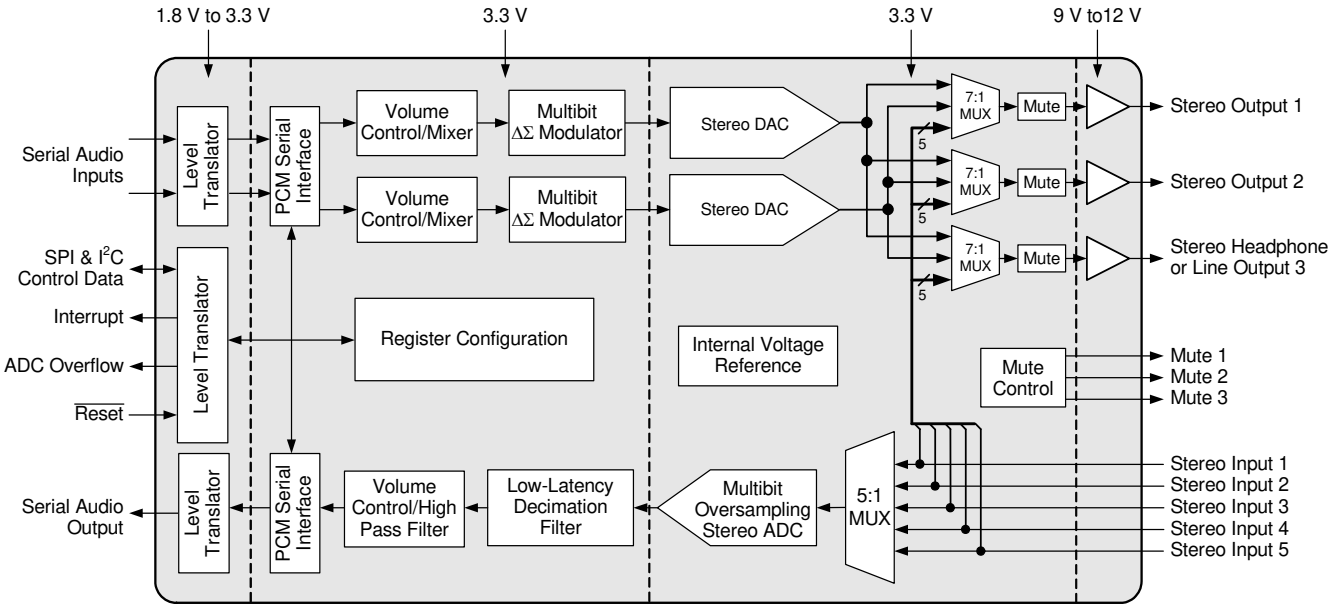
D/A Features

- Dual 24-bit Stereo DACs
- 100 dB Dynamic Range (A-Wtd)
- -90 dB THD+N
- Integrated Line Driver
  - 2 Vrms Output
  - Single-Ended Outputs
- Integrated Headphone Driver
  - 2 x 10 mW into 32 Ω
- Stereo 7:1 Output Multiplexer
- Volume Control with Soft Ramp
  - 0.5 dB Step Size
  - Zero Crossing Click-Free Transitions
- Selectable Serial Audio Interface Formats
  - Left- or Right-Justified, Up to 24-bit
  - I²S Up to 24-bit
- Selectable 50/15 μs De-Emphasis
- Internal Analog Mute
- Control Output for External Muting
- Popguard® Technology

A/D Features

- Single 24-bit Stereo ADC
- Stereo 5:1 Input Multiplexer
- 2 Vrms Single-Ended Inputs
- 95 dB Dynamic Range (A-Wtd)
- -88 dB THD+N
- Digital Volume Control with Soft Ramp
  - 0.5 dB Step Size
- Selectable Serial Audio Interface Formats
  - Left-Justified
  - I²S
- High-Pass Filter or DC Offset Calibration

See System Features, General Description, and Ordering information on page 2.



Advance Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

System Features

- High Performance 24-bit Converters
  - Multi-bit Delta-Sigma Modulator
  - Up to 96 kHz Sampling Rates
- Direct Interface with 1.8 V to 3.3 V Logic Levels
- Supports Asynchronous Serial Port Operation
  - Two Independent Clock Domains
  - ADC, DAC1, and DAC2 can be Independently Assigned to the Two Clock Domains
  - Each Serial Port Supports Master or Slave Operation
- Internal Digital Loopback
- +3.3 V Analog Power Supply
- +3.3 V Digital Power Supply
- +9 V to +12 V High-Voltage Power Supply
- Hardware or Software Mode Configuration
  - Supports I²C® and SPI™ Software Interface

General Description

The CS42325 is a highly integrated stereo audio CODEC. The CS42325 performs stereo analog-to-digital (A/D) and up to four channels of digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 96 kHz.

A 5:1 stereo input multiplexer is included for selecting between line-level inputs. The output of the input multiplexer is followed by an advanced 3rd-order, multi-bit delta-sigma modulator and digital filtering/decimation. Sampled data is transmitted by the serial audio interface at rates from 4 kHz to 96 kHz, in either Slave or Master Mode.

The D/A converter is based on a 5th-order multi-bit delta-sigma modulator with an ultra-linear low-pass filter and offers a volume control that operates with a 0.5 dB step size. It incorporates selectable soft ramp and zero crossing transition functions to eliminate clicks and pops.

An integrated 7:1 stereo output multiplexer on each of the three stereo 2 Vrms line-level outputs is used to select any of the 5 stereo analog inputs, for analog bypass support, or the outputs of the 2 internal DACs. Each 2 Vrms output can be muted with the selectable analog mute function. Analog output 3 has a built in headphone driver and can be used either as a line output or headphone output.

Standard 50/15 µs de-emphasis is available for a 44.1 kHz sample rate for compatibility with digital audio programs mastered using the 50/15 µs pre-emphasis technique.

Integrated digital level translators allow easy interfacing between the CS42325 and other devices operating over a wide range of logic levels.

The CS42325 is available in a 48-pin LQFP package in Commercial (-40°C to +85°C) and Automotive (-40°C to +105°C) grades. The CDB42325 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "Ordering information" on page 71 for complete details.

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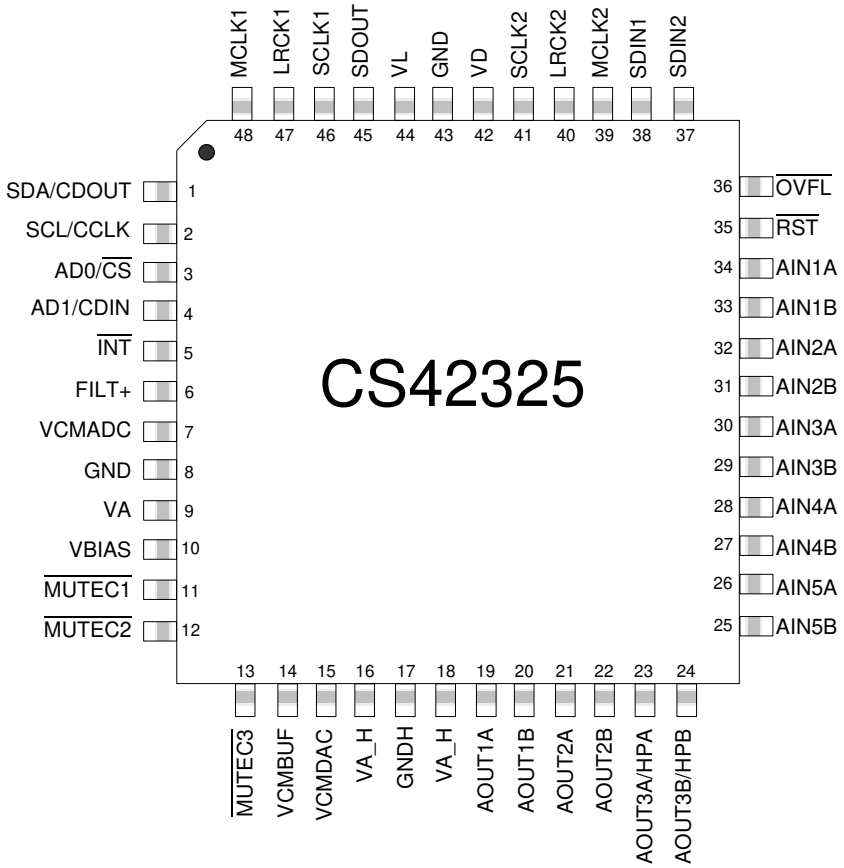
1. PIN DESCRIPTIONS

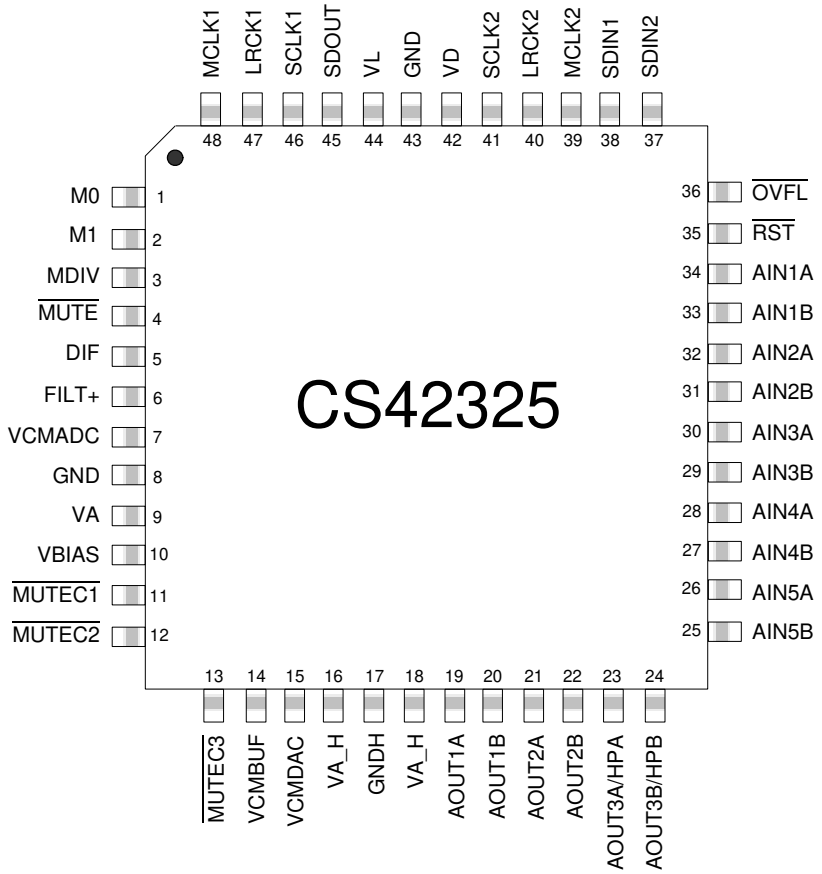
1.1 Software Mode



Pin Name	#	Pin Description
SDA/CDOUT	1	**I²C Format SDA** (*Input/Output*) - Acts as an input/output data pin. An external pull-up resistor is required for I²C control port operation. **SPI Format CDOUT** (*Output*) - Acts as an output only data pin.
SCL/CCLK	2	**I²C Format, SCL** (*Input*) - Serial clock for the serial control port. An external pull-up resistor is required for I²C control port operation. **SPI Format, CCLK** (*Input*) - Serial clock for the serial control port.
AD0/$\overline{CS}$	3	**I²C Format, AD0** (*Input*) - Forms the device address input AD[0]. **SPI Format, CS** (*Input*) - Acts as the active low chip select input.
AD1/CDIN	4	**I²C Format, AD1** (*Input*) - Forms the device address input AD[1]. **SPI Format, CDIN** (*Input*) - Becomes the input data pin.
$\overline{INT}$	5	**Interrupt** (*Output*) - Indicates an interrupt condition has occurred.
FILT+	6	**FILT+** (*Output*) - Full-scale reference voltage for ADC.
VCMADC	7	**ADC Common-Mode Voltage** (*Output*) - Filter connections for the ADC internal quiescent reference voltage.
GND	8	**Analog Ground** (*Input*) - Analog ground reference.
VA	9	**Analog Power** *(Input)* - Positive power for the internal analog section.
VBIAS	10	**Bias Voltage** (*Output*) - Positive reference voltage for the internal DAC.

$\overline{\text{MUTEC1}}$	11	**Mute Control 1** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.
$\overline{\text{MUTEC2}}$	12	**Mute Control 2** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.
$\overline{\text{MUTEC3}}$	13	**Mute Control 3** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.
VCMBUF	14	**VCMBUF** (*Output*) - Internally buffered VCMDAC
VCMDAC	15	**DAC Common-Mode Voltage** (*Output*) - Filter connections for the DAC internal quiescent reference voltage.
VA_H	16 18	**Analog High Voltage Power** *(Input)* - Positive power for the internal output buffer section.
GNDH	17	**Analog Ground** (*Input*) - Ground reference for high-voltage section.
AOUT1A, AOUT1B AOUT2A, AOUT2B	19, 20 21, 22	**Line Level Analog Audio Outputs** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.
AOUT3A/HPA AOUT3B/HPB	23 24	**Line Level/Headphone Analog Audio Outputs** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.
AIN5B, AIN5A AIN4B, AIN4A AIN3B, AIN3A AIN2B, AIN2A AIN1B, AIN1A	25, 26 27, 28 29, 30 31, 32 33, 34	**Stereo Analog Inputs 1-5** (*Input*) - The full-scale input level is specified in the ADC Analog Characteristics specification table.
$\overline{\text{RST}}$	35	**Reset** (*Input*) - The device enters a low-power mode when this pin is driven low.
$\overline{\text{OVFL}}$	36	**ADC Overflow** (*Output*) - Indicates an ADC overflow condition is present.
SDIN2 SDIN1	37 38	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
MCLK2	39	**Master Clock 2** (*Input*) - Optional asynchronous clock source for the DAC's delta-sigma modulators.
LRCK2	40	**Serial Port 2 Left/Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio input data line.
SCLK2	41	**Serial Port 2 Serial Bit Clock** *(Input/Output)* - Serial bit clock for serial audio interface 2.
VD	42	**Digital Power** (*Input*) - Positive power for the internal digital section.
GND	43	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VL	44	**Digital Interface Power** (*Input*) - Determines the required signal level for the control and serial port interfaces as shown in "I/O Power Rails" on page 12. Refer to the"Recommended Operating Conditions" on page 13 for appropriate voltages.
SDOUT	45	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
SCLK1	46	**Serial Port 1 Serial Bit Clock** *(Input/Output)* - Serial bit clock for serial audio interface 1.
LRCK1	47	**Serial Port 1 Left/Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio output data line.
MCLK1	48	**Master Clock 1** (*Input*) - Clock source for the ADC's delta-sigma modulators. By default, this signal also clocks the DAC's delta-sigma modulators.

1.2 Hardware Mode



Pin Name	#	Pin Description
M0, M1	1, 2	**Mode Selection** (*Input*) - Determines the operational mode of the device.
MDIV	3	**MCLK Divider** (*Input*) - Setting this pin high places a divide-by-2 circuit in the MCLK path to the core device circuitry.
$\overline{\text{MUTE}}$	4	**$\overline{\text{MUTE}}$** (*Input*) - Engages the internal digital mute and activates the $\overline{\text{MUTECx}}$ pins
DIF	5	**DIF** (*Input*) - Sets the serial audio interface format. Setting DIF high selects I²S audio format and low selects LJ audio format.
FILT+	6	**FILT+** (*Output*) - Full-scale reference voltage for ADC.
VCMADC	7	**ADC Common-Mode Voltage** (*Output*) - Filter connections for the ADC internal quiescent reference voltage.
GND	8	**Analog Ground** (*Input*) - Analog ground reference.
VA	9	**Analog Power** *(Input)* - Positive power for the internal analog section.
VBIAS	10	**Bias Voltage** (*Output*) - Positive reference voltage for the internal DAC.
$\overline{\text{MUTEC1}}$	11	**Mute Control 1** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.
$\overline{\text{MUTEC2}}$	12	**Mute Control 2** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.

$\overline{\text{MUTEC3}}$	13	**Mute Control 3** (*Output*) - Active-low mute output can drive external circuitry to eliminate the clicks and pops associated with any single-rail output. This pin will become a high-impedance output during power-down mode or when an invalid MCLK to LRCK ratio is detected.
VCMBUF	14	**VCMBUF** (*Output*) - Internally buffered VCMDAC
VCMDAC	15	**DAC Common-Mode Voltage** (*Output*) - Filter connections for the DAC internal quiescent reference voltage.
VA_H	16, 18	**Analog High Voltage Power** *(Input)* - Positive power for the internal output buffer section.
GNDH	17	**Analog Ground** (*Input*) - Ground reference for high-voltage section.
AOUT1A, AOUT1B AOUT2A, AOUT2B	19, 20 21, 22	**Line Level Analog Audio Outputs** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.
AOUT3A/HPA AOUT3B/HPB	23 24	**Line Level/Headphone Analog Audio Outputs** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.
AIN5B, AIN5A AIN4B, AIN4A AIN3B, AIN3A AIN2B, AIN2A AIN1B, AIN1A	25, 26 27, 28 29, 30 31, 32 33, 34	**Stereo Analog Inputs 1-5** (*Input*) - The full-scale input level is specified in the ADC Analog Characteristics specification table.
$\overline{\text{RST}}$	35	**Reset** (*Input*) - The device enters a low-power mode when this pin is driven low.
$\overline{\text{OVFL}}$	36	**ADC Overflow** (*Output*) - Indicates an ADC overflow condition is present.
SDIN2 SDIN1	37 38	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
MCLK2	39	**Master Clock 2** (*Input*) - Optional asynchronous clock source for the DAC's delta-sigma modulators.
LRCK2	40	**Serial Port 2 Left/Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio input data line.
SCLK2	41	**Serial Port 2 Serial Bit Clock** *(Input/Output)* - Serial bit clock for serial audio interface 2.
VD	42	**Digital Power** (*Input*) - Positive power for the internal digital section.
GND	43	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VL	44	**Digital Interface Power** (*Input*) - Determines the required signal level for the control and serial port interfaces as shown in "I/O Power Rails" on page 12. Refer to the"Recommended Operating Conditions" on page 13 for appropriate voltages
SDOUT	45	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
SCLK1	46	**Serial Port 1 Serial Bit Clock** *(Input/Output)* - Serial bit clock for serial audio interface 1.
LRCK1	47	**Serial Port 1 Left Right/Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio output data line.
MCLK1	48	**Master Clock 1** (*Input*) - Clock source for the ADC's delta-sigma modulators. By default, this signal also clocks the DAC's delta-sigma modulators.

1.3 Digital I/O Pin Characteristics

The logic level for each input should adhere to the corresponding power rail and should not exceed the maximum ratings.

Power Supply	Pin Number	Pin Name	I/O	Driver	Receiver
Software Mode					
VL	1	SDA CDOUT	Input/Output Hi-Z/Output	1.8 V - 3.3 V, Open Drain 1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V, with Hysteresis
	2	SCL CCLK	Input	-	1.8 V - 3.3 V, with Hysteresis
	3	AD0 $\overline{CS}$	Input	-	1.8 V - 3.3 V, with Hysteresis
	4	AD1 CDIN	Input	-	1.8 V - 3.3 V, with Hysteresis
	5	INT	Output	1.8 V - 3.3 V, Open Drain	1.8 V - 3.3 V, with Hysteresis
Hardware Mode					
VL	1	M0	Input	-	1.8 V - 3.3 V, with Hysteresis
	2	M1	Input	-	1.8 V - 3.3 V, with Hysteresis
	3	MDIV	Input	-	1.8 V - 3.3 V, with Hysteresis
	4	MUTE	Input	-	1.8 V - 3.3 V, with Hysteresis
	5	DIF	Input	-	1.8 V - 3.3 V, with Hysteresis
All Modes					
VL	35	$\overline{RST}$	Input	-	1.8 V - 3.3 V
	47 40	LRCK1 LRCK2	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
	46 41	SCLK1 SCLK2	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
	48 39	MCLK1 MCLK2	Input	-	1.8 V - 3.3 V
	38 37	SDIN1 SDIN2	Input	-	1.8 V - 3.3 V
	45	SDOUT	Output	1.8 V - 3.3 V, CMOS	-
	36	OVFL	Output	1.8 V - 3.3 V, Open Drain	-
VA_H	11 12 13	MUTEC1 MUTEC2 MUTEC3	Output	9.0 V - 12.0 V	-

Table 1. I/O Power Rails

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = GNDH = 0 V; All voltages with respect to ground.

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Analog	VA	3.13	3.3	3.47	V
	Digital	VD	3.13	3.3	3.47	V
	Logic	VL	1.71	3.3	3.47	V
	High Voltage Analog	VA_H	8.55	9.0	12.60	V
Ambient Operating Temperature (Power Applied)						
	Commercial(-CQZ)	T_A	-40	-	+85	°C
	Automotive(-DQZ)		-40	-	+105	°C

ABSOLUTE MAXIMUM RATINGS

GND = GNDH = 0 V; All voltages with respect to ground. (Note 1)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	VA	-0.3	+4.50	V
	Digital	VD	-0.3	+4.50	V
	Logic	VL	-0.3	+4.50	V
	High Voltage Analog	VA_H	-0.3	+17.0	V
Input Current	(Note 2)	I_{in}	-10	+10	mA
Analog Input Voltage		V_{INA}	GND - 0.3	VA_H + 0.3	V
Digital Input Voltage	Logic	V_{IND}	-0.3	VL + 0.4	V
Ambient Operating Temperature (Power Applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes: 1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

ADC ANALOG CHARACTERISTICS - COMMERCIAL (-CQZ)

Test Conditions (unless otherwise specified): VA = VD = VL = 3.3 V, VA_H = 9 V, GND = GNDH = 0 V; T_A = 25° C; 997 Hz Input Sine Wave. Decoupling capacitors, filter capacitors, and recommended input filter as shown in Figure 7 on page 26 and Figure 8 on page 27; Fs = 48 kHz or 96 kHz; Synchronous Mode; Measurement Bandwidth 10 Hz to 20 kHz,

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Dynamic Range	A-weighted		89	95	-	dB
	unweighted		86	92	-	dB
Total Harmonic Distortion + Noise	(Note 3)					
	-1 dB	THD+N	-	-88	-80	dB
	-20 dB		-	-72	-	dB
	-60 dB		-	-32	-	dB
Double-Speed Mode						
Dynamic Range	A-weighted		89	95	-	dB
	unweighted		86	92	-	dB
Total Harmonic Distortion + Noise	(Note 3)					
	-1 dB	THD+N	-	-88	-80	dB
	-20 dB		-	-72	-	dB
	-60 dB		-	-32	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-5	-	+5	%
Gain Drift			-	±100	-	ppm/°C
Analog Input Characteristics						
Full-scale Input Voltage			0.576•VA	0.606•VA	0.636•VA	V_{rms}
Input Impedance			-	200	-	kΩ
Maximum Interchannel Input Impedance Mismatch			-	2	-	%
Interchannel Isolation	(1 kHz)		-	-90	-	dB

Note: 3. Referred to the typical line-level full-scale input voltage.

ADC ANALOG CHARACTERISTICS - AUTOMOTIVE (-DQZ)

Test Conditions (unless otherwise specified): VA = 3.13 V to 3.47 V, VD = 3.13 V to 3.47 V, VL = 1.71 V to 3.47 V, VA_H = 8.55 V to 12.60 V, GND = GNDH = 0 V; T_A = -40° C to +85° C; 997 Hz Input Sine Wave. Decoupling capacitors, filter capacitors, and recommended input filter as shown in Figure 7 on page 26 and Figure 8 on page 27; Fs = 48 kHz or 96 kHz; Synchronous Mode; Measurement Bandwidth 10 Hz to 20 kHz,

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Dynamic Range	A-weighted		85	95	-	dB
	unweighted		82	92	-	dB
Total Harmonic Distortion + Noise	(Note 3)					
	-1 dB	THD+N	-	-88	-78	dB
	-20 dB		-	-72	-	dB
	-60 dB		-	-32	-	dB
Double-Speed Mode						
Dynamic Range	A-weighted		85	95	-	dB
	unweighted		82	92	-	dB
Total Harmonic Distortion + Noise	(Note 3)					
	-1 dB	THD+N	-	-88	-78	dB
	-20 dB		-	-72	-	dB
	-60 dB		-	-32	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-5	-	+5	%
Gain Drift			-	±100	-	ppm/°C
Analog Input Characteristics						
Full-scale Input Voltage			0.576•VA	0.606•VA	0.636•VA	V_{rms}
Input Impedance			-	200	-	kΩ
Maximum Interchannel Input Impedance Mismatch			-	2	-	%
Interchannel Isolation	(1 kHz)		-	-90	-	dB

Note: 4. Referred to the typical line-level full-scale input voltage.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 5)			Symbol	Min	Typ	Max	Unit
Single-Speed Mode							
Passband	(-0.1 dB)			0	-	0.489	Fs
Passband Ripple				-	-	0.035	dB
Stopband				0.569	-	-	Fs
Stopband Attenuation				70	-	-	dB
Total Group Delay			t_{gd}	-	12/Fs	-	s
Double-Speed Mode							
Passband	(-0.1 dB)			0	-	0.489	Fs
Passband Ripple				-	-	0.025	dB
Stopband				0.5604	-	-	Fs
Stopband Attenuation				69	-	-	dB
Total Group Delay			t_{gd}	-	9/Fs	-	s
High-Pass Filter Characteristics							
Frequency Response	-3.0 dB -0.13 dB	 (Note 6)		-	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	(Note 6)		-	10	-	Deg
Passband Ripple				-	-	0	dB
Filter Settling Time					10^5/Fs		s

Notes: 5. Response is clock dependent and will scale with sample rate (Fs). Note that the response plots (Figures 23 to 30) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

6. Response shown is for Fs = 48 kHz.

DAC ANALOG CHARACTERISTICS - COMMERCIAL (-CQZ)

Test Conditions (unless otherwise specified): VA = VD = VL = 3.3 V, VA_H = 9 V, GND = GNDH = 0 V; T_A = 25° C; 997 Hz Full-Scale Output Sine Wave. Decoupling capacitors, Filter capacitors, and Recommended output filter as shown in Figure 7 on page 26 and Figure 8 on page 27; Fs = 48 kHz or 96 kHz; Synchronous Mode; Measurement Bandwidth 10 Hz to 20 kHz,

Parameter			Symbol	Min	Typ	Max	Unit
R_L = 5 kΩ							
Dynamic Range		(Note 7)					
	18 to 24-Bit	A-weighted		94	100	-	dB
		unweighted		91	97	-	dB
	16-Bit	A-weighted		88	93	-	dB
		unweighted		85	90	-	dB
Total Harmonic Distortion + Noise		(Note 7)					
	18 to 24-Bit	0 dB		-	-90	-84	dB
		-20 dB		-	-77	-73	dB
		-60 dB	THD+N	-	-37	-33	dB
	16-Bit	0 dB		-	-87	-82	dB
		-20 dB		-	-73	-68	dB
		-60 dB		-	-30	-25	dB
Interchannel Isolation		(1 kHz)		-	-100	-	dB
R_L = 32 Ω							
Dynamic Range		(Note 7)					
	18 to 24-Bit	A-weighted		94	100	-	dB
		unweighted		91	97	-	dB
	16-Bit	A-weighted		88	93	-	dB
		unweighted		85	90	-	dB
Total Harmonic Distortion + Noise		(Note 7)					
	18 to 24-Bit	0 dB		-	-40	-34	dB
		-3 dB		-	-54	-48	dB
		-20 dB	THD+N	-	-77	-73	dB
		-60 dB		-	-37	-33	dB
	16-Bit	0 dB		-	-40	-34	dB
		-20 dB		-	-73	-68	dB
		-60 dB		-	-30	-25	dB
Interchannel Isolation		(1 kHz)		-	-80	-	dB
Other Characteristics for R_L = 32Ω or 5 kΩ							
Full-Scale Output Voltage		(Note 8)		1.9	2.0	2.1	V_{rms}
Max current draw from an AOUT1x or AOUT2x pin			I_{OUT}	-	575	-	µA
AC-Load Resistance (AOUT1x and AOUT2x)		(Note 9)	R_L	5	-	-	kΩ
AC-Load Resistance (AOUT3x/HPx)		(Note 9)	R_L	16	-	-	Ω
Load Capacitance		(Note 9)	C_L	-	-	100	pF
Output Impedance			Z_{OUT}	40	50	60	Ω
Interchannel Gain Mismatch				-	0.1	0.25	dB
Gain Drift				-	100	-	ppm/°C

Notes: 7. One-half LSB of triangular PDF dither added to data.

8. Does not account for attenuation due to Z_{OUT}.

9. See Figures 1 and 2 on page 19. R_L and C_L reflect the minimum resistance and maximum capacitance allowed in order to maintain stability in the internal op-amp. C_L affects the dominant pole of the internal output amp; increasing C_L beyond 100 pF can cause the internal op-amp to become unstable.

DAC ANALOG CHARACTERISTICS - AUTOMOTIVE (-DQZ)

Test Conditions (unless otherwise specified): VA = 3.13 V to 3.47 V, VD = 3.13 V to 3.47 V, VL = 1.71 V to 3.47 V, VA_H = 8.55 V to 12.60 V, GND = GNDH = 0 V; T_A = -40° C to +85° C; 997 Hz Full-Scale Output Sine Wave. Decoupling capacitors, filter capacitors, and recommended output filter as shown in Figure 7 on page 26 and Figure 8 on page 27; Fs = 48 kHz or 96 kHz; Synchronous Mode; Measurement Bandwidth 10 Hz to 20 kHz,

Parameter			Symbol	Min	Typ	Max	Unit
R_L = 5 kΩ							
Dynamic Range		(Note 7)					
	18 to 24-Bit	A-weighted		90	100	-	dB
		unweighted		87	97	-	dB
	16-Bit	A-weighted		83	93	-	dB
		unweighted		80	90	-	dB
Total Harmonic Distortion + Noise		(Note 7)					
	18 to 24-Bit	0 dB		-	-90	-80	dB
		-20 dB		-	-77	-67	dB
		-60 dB	THD+N	-	-37	-27	dB
	16-Bit	0 dB		-	-87	-77	dB
		-20 dB		-	-77	-67	dB
		-60 dB		-	-37	-27	dB
Interchannel Isolation		(1 kHz)		-	-100	-	dB
R_L = 32 Ω							
Dynamic Range		(Note 7)					
	18 to 24-Bit	A-weighted		90	100	-	dB
		unweighted		87	97	-	dB
	16-Bit	A-weighted		83	93	-	dB
		unweighted		80	90	-	dB
Total Harmonic Distortion + Noise		(Note 7)					
	18 to 24-Bit	0 dB		-	-40	-20	dB
		-3 dB		-	-54	-44	dB
		-20 dB	THD+N	-	-77	-67	dB
		-60 dB		-	-37	-27	dB
	16-Bit	0 dB		-	-40	-30	dB
		-20 dB		-	-73	-63	dB
		-60 dB		-	-30	-20	dB
Interchannel Isolation		(1 kHz)		-	-80	-	dB
Other Characteristics for R_L = 32 Ω or 5 kΩ							
Full-Scale Output Voltage		(Note 8)		1.9	2.0	2.1	V_{rms}
Max current draw from an AOUT1x or AOUT2x pin			I_{OUT}	-	575	-	µA
AC-Load Resistance (AOUT1x and AOUT2x)		(Note 9)	R_L	5	-	-	kΩ
AC-Load Resistance (AOUT3x/HPx)		(Note 9)	R_L	16	-	-	Ω
Load Capacitance		(Note 9)	C_L	-	-	100	pF
Output Impedance			Z_{OUT}	40	50	60	Ω
Interchannel Gain Mismatch				-	0.1	0.25	dB
Gain Drift				-	100	-	ppm/°C

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 10)		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Passband (Note 11)	to -0.01 dB corner to -3 dB corner		0 0	- -	.454 .499	Fs Fs
Frequency Response (10 Hz to 20 kHz)			-0.01	-	+0.01	dB
StopBand			0.547	-	-	Fs
StopBand Attenuation	(Note 11)		102	-	-	dB
Group Delay		tgd	-	9.4/Fs	-	s
De-emphasis Error (Note 12)	Fs = 44.1 kHz		-	-	+/-0.14	dB
Double-Speed Mode						
Passband (Note 11)	to -0.01 dB corner to -3 dB corner		0 0	- -	.43 .499	Fs Fs
Frequency Response (10 Hz to 20 kHz)			-0.01	-	+0.01	dB
StopBand			.583	-	-	Fs
StopBand Attenuation	(Note 11)		80	-	-	dB
Group Delay		tgd	-	4.6/Fs	-	s

Notes: 10. Response is clock-dependent and will scale with Fs. Note that the amplitude vs. frequency plots of this data (Figures 31 to 42) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

11. For Single-Speed Mode, the measurement bandwidth is from StopBand to 3 Fs.
For Double-Speed Mode, the measurement bandwidth is from StopBand to 3 Fs.

12. De-emphasis is available only in Single-Speed Mode.

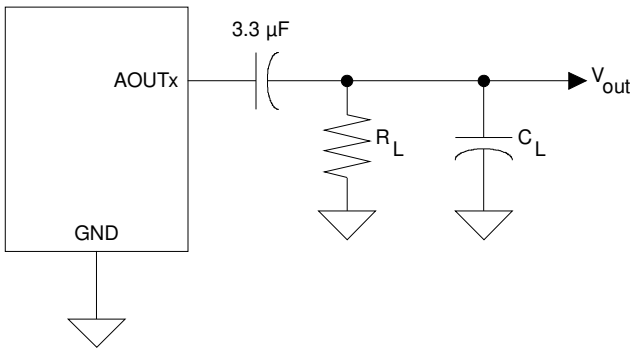


Figure 1. Equivalent Analog Output Load

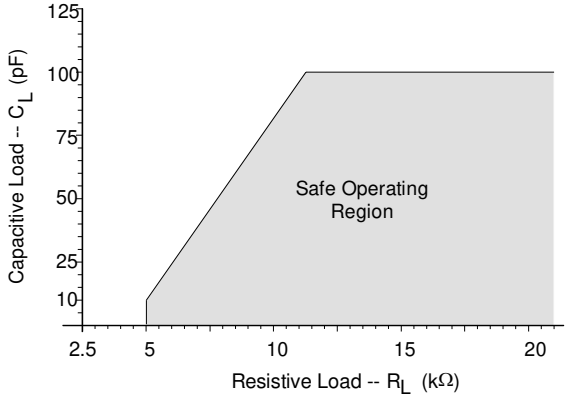


Figure 2. Maximum Analog Line Output Loading

ANALOG PASS-THRU CHARACTERISTICS

Test Conditions (unless otherwise specified): VA = VD = VL = 3.3 V; VA_H = 9 V; GND = GNDH = 0 V; T_A = 25° C; Input test signal is a 1 kHz sine wave; Measurement Bandwidth is 10 Hz to 20 kHz; Synchronous Mode.

Parameter	Symbol	Min	Typ	Max	Unit
Analog Input to Analog Output Characteristics (Gain=0dB), R_L = 5 kΩ					
Dynamic Range					
A-weighted		89	95	-	dB
unweighted		86	92	-	dB
Total Harmonic Distortion + Noise (Note 3)					
0 dB	THD+N	-	-87	-81	dB
-3 dB		-	-93	-	dB
Frequency Response 10 Hz to 20 kHz		-	±0.1	-	dB
Analog Input to Analog Output Characteristics (Gain=0dB), R_L = 32 Ω					
Dynamic Range					
A-weighted		89	95	-	dB
unweighted		86	92	-	dB
Total Harmonic Distortion + Noise (Note 3)					
0 dB	THD+N	-	-40	-34	dB
-3 dB		-	-54	-	dB
Frequency Response 10 Hz to 20 kHz		-3.0	-	+0.5	dB
Analog Characteristics, R_L = 5 kΩ and R_L = 32 Ω					
Max Input Voltage		-	2.0	-	V_{rms}
Max Output Voltage (Note 8)		-	2.0	-	V_{rms}
Max current draw from an AOUT1x or AOUT2x pin	I_{OUT}	-	575	-	µA
AC-Load Resistance (AOUT1x and AOUT2x) (Note 9)	R_L	5	-	-	kΩ
AC-Load Resistance (AOUT3x/HPx) (Note 9)	R_L	16	-	-	Ω
Load Capacitance (Note 9)	C_L	-	-	100	pF
Output Impedance	Z_{OUT}	40	50	60	Ω
Interchannel Isolation (1 kHz)		-	-90	-	dB

Note: 13. Referred to the typical line-level full-scale input voltage.

DC ELECTRICAL CHARACTERISTICS

GND = GNDH = 0 V; all voltages with respect to ground. MCLK1=12.288 MHz; MCLK2=static; Fs=48 kHz; Master Mode; R_L = 5 kΩ.

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current (Normal Operation)	VA_H = 9 V	I_{A_H}	-	24	32	mA
	VA = 3.3 V	I_A	-	19	25	mA
	VD = 3.3 V	I_D	-	22	29	mA
	VL = 3.3 V	I_L	-	10	13	mA
Power Supply Current	VA _H= 9 V	I_{PD}	-	0	-	µA
(Power-Down Mode) (Note 14)	VL=VD=VA=3.3 V		-	200	-	µA
Power Consumption (Normal Operation)	VA_H = 9 V	-	-	216	289	mW
	VL=VD=VA = 3.3 V	-	-	169	225	mW
(Power-Down Mode)	All supplies	-	-	0.7	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 15)	PSRR	-	60	-	dB
Reference Voltages						
VCMADC Nominal Voltage		VCMADC	-	0.5•VA	-	V
VCMDAC Nominal Voltage		VCMDAC	-	4	-	V
DC Current from VCMADC or VCMDAC	(Note 16)	I_{CM}	-	-	1	µA
VCMADC or VCMDAC Output Impedance		Z_{CM}	-	23	-	kΩ
FILT+ Nominal Voltage		FILT+	-	VA	-	V
VBIAS Nominal Voltage		VBIAS	-	VA-0.8	-	V

Notes: 14. Power-Down Mode is defined as $\overline{RST}$ = Low, with all clock and data lines held static low and no analog input.

15. Valid with the recommended capacitor values on FILT+, VCMDAC, VCMADC and VCMBUF as shown in Figure 7 on page 26 and Figure 8 on page 27.

16. The DC current draw represents the allowed current draw due to typical leakage through the electrolytic de-coupling capacitors.

DIGITAL INTERFACE CHARACTERISTICS

Parameters (Note 17)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	0.7•VL	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.2•VL	V
High-Level Output Voltage at I_o=2 mA	Digital Interface	V_{OH}	VL-1.0	-	-	V
	$\overline{MUTEC1}$/$\overline{MUTEC2}$/$\overline{MUTEC3}$	V_{OH}	VA_H-1.0	-	-	V
Low-Level Output Voltage at I_o=2 mA	Digital Interface	V_{OL}	-	-	0.4	V
	$\overline{MUTEC1}$/$\overline{MUTEC2}$/$\overline{MUTEC3}$	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-10	-	+10	µA
Input Capacitance			-	-	1	pF
Maximum $\overline{MUTEC1}$/$\overline{MUTEC2}$/$\overline{MUTEC3}$ Drive Current			-	3	-	mA
Minimum $\overline{OVFL}$ Active Time			$\frac{10^6}{LRCKX}$			µs

Note: 17. Digital Interface signals include all pins sourced from the VL supply as shown in "I/O Power Rails" on page 12.

SWITCHING CHARACTERISTICS - SERIAL AUDIO

Logic '0' = GND = GNDH = 0 V; Logic '1' = VL; C_L = 20 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock (MCLKx = MCLK1, MCLK2)						
MCLKx Frequency MCLKx Duty Cycle			1.024 40	- 50	41.4720 60	MHz %
Sample Rates						
	Single-Speed Mode Double-Speed Mode	-	4 50	-	54 108	kHz
Master Mode						
SCLKx Frequency SCLKx Period SCLKx Duty Cycle (Note 18)	 1/(128*108 kHz) 	- t_{PERIOD} $t_{HIGH} \div t_{PERIOD}$	64•Fs 72.3 40	- - 50	64•Fs - 60	Hz ns %
LRCKx setup LRCKx hold	before SCLK rising after SCLK rising	t_{SETUP1} t_{HOLD1}	20 20	-	-	ns
SDOUT setup SDOUT hold	before SCLK rising after SCLK rising	t_{SETUP2} t_{HOLD2}	10 10	-	-	ns
Slave Mode						
SCLKx Frequency (Note 19) SCLKx Period SCLKx Duty Cycle	 1/(128•108 kHz) 	- t_{PERIOD} $t_{HIGH} \div t_{PERIOD}$	- 72.3 40	64•Fs - 50	- - 60	Hz ns %
LRCKx setup LRCKx hold	before SCLK rising after SCLK rising	t_{SETUP1} t_{HOLD1}	20 20	-	-	ns
SDOUT setup SDOUT hold	before SCLK rising after SCLK rising	t_{SETUP2} t_{HOLD2}	10 10	-	-	ns

Notes: 18. Duty cycle of generated SCLKx in Master Mode depends on duty cycle of the corresponding MCLKx as specified under "System Clocking" on page 28.

19. In Slave Mode, the SCLK/LRCK ratio can be set according to preference. However, specified performance is guaranteed only when using the ratios in Section 4.2.1 Master Mode on page 30 and Section 4.2.2 Slave Mode on page 30.

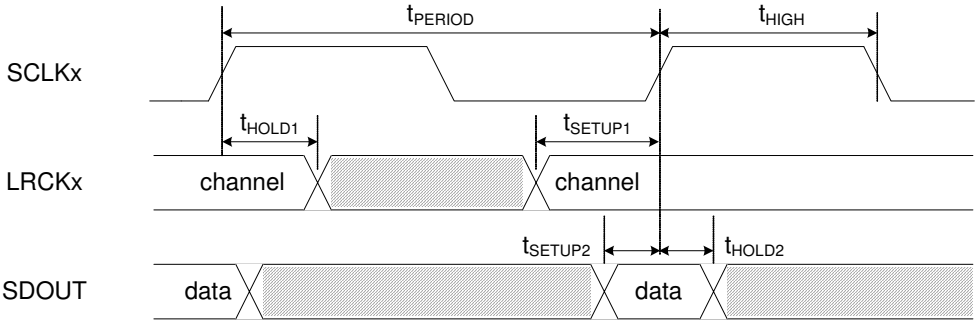


Figure 3. Serial Input Timing

SWITCHING CHARACTERISTICS - SERIAL AUDIO (CONT.)

Logic '0' = GND = GNDH = 0 V; Logic '1' = VL; C_L = 20 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Master Mode						
SDINx setup SDINx hold	before SCLK rising after SCLK rising	t_{SETUP3} t_{HOLD3}	10 10	-	-	ns
Slave Mode						
SDINx setup SDINx hold	before SCLK rising after SCLK rising	t_{SETUP3} t_{HOLD3}	10 10	-	-	ns

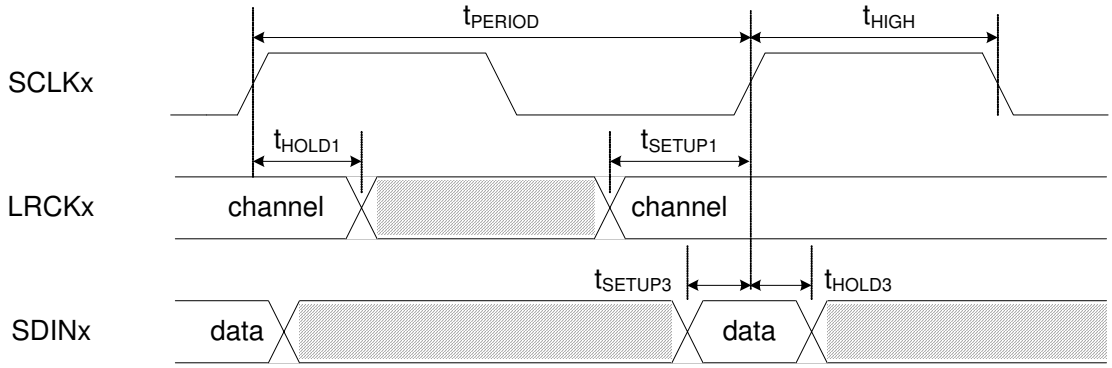


Figure 4. Serial Output Timing

SWITCHING CHARACTERISTICS - SOFTWARE MODE - I²C FORMAT

Inputs: Logic '0' = GND = GNDH = 0 V, Logic '1' = VL, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note Note:)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Note: 20. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

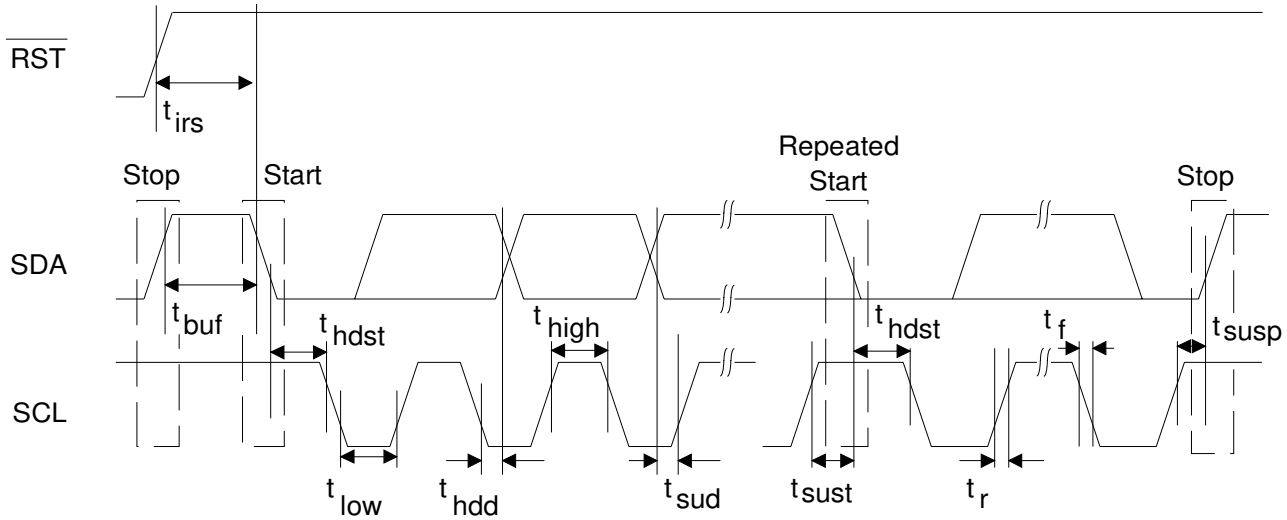


Figure 5. Software Mode Timing - I²C Format

SWITCHING CHARACTERISTICS - SOFTWARE MODE - SPI FORMAT

Inputs: Logic '0' = GND = GNDH = 0 V; Logic '1' = VLC; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to CS Falling	t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling (Note 21)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions	t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 22)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 23)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 23)	t_{f2}	-	100	ns
Transition Time from CCLK to CDOUT Valid (Note 24)	t_{r2}	-	100	ns
Time from CS rising to CDOUT High-Z	t_{f2}	-	100	ns

Notes: 21. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

22. Data must be held for sufficient time to bridge the transition time of CCLK.

23. For F_{SCK} < 1 MHz.

24. CDOUT should *not* be sampled during this time.

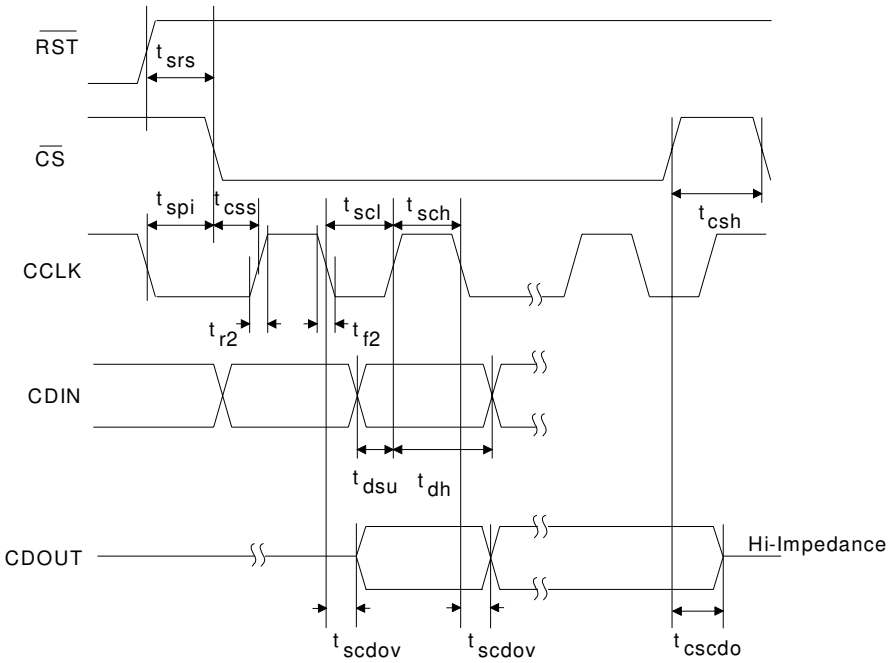


Figure 6. Software Mode Timing - SPI Mode