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CS42426

114 dB, 192 kHz 6-Ch Codec with PLL

Features

- Six 24-bit D/A, two 24-bit A/D Converters
- 114 dB DAC / 114 dB ADC Dynamic Range
- -100 dB THD+N
- System Sampling Rates up to 192 kHz
- Integrated Low-Jitter PLL for Increased System Jitter Tolerance
- PLL Clock or System Clock Selection
- 7 Configurable General-Purpose Outputs
- ADC High-Pass Filter for DC Offset Calibration
- Expandable ADC Channels and One-Line Mode Support
- Digital Output Volume Control with Soft Ramp
- Digital +/-15 dB Input Gain Adjust for ADC
- Differential Analog Architecture
- Supports Logic Levels between 1.8 V and 5 V

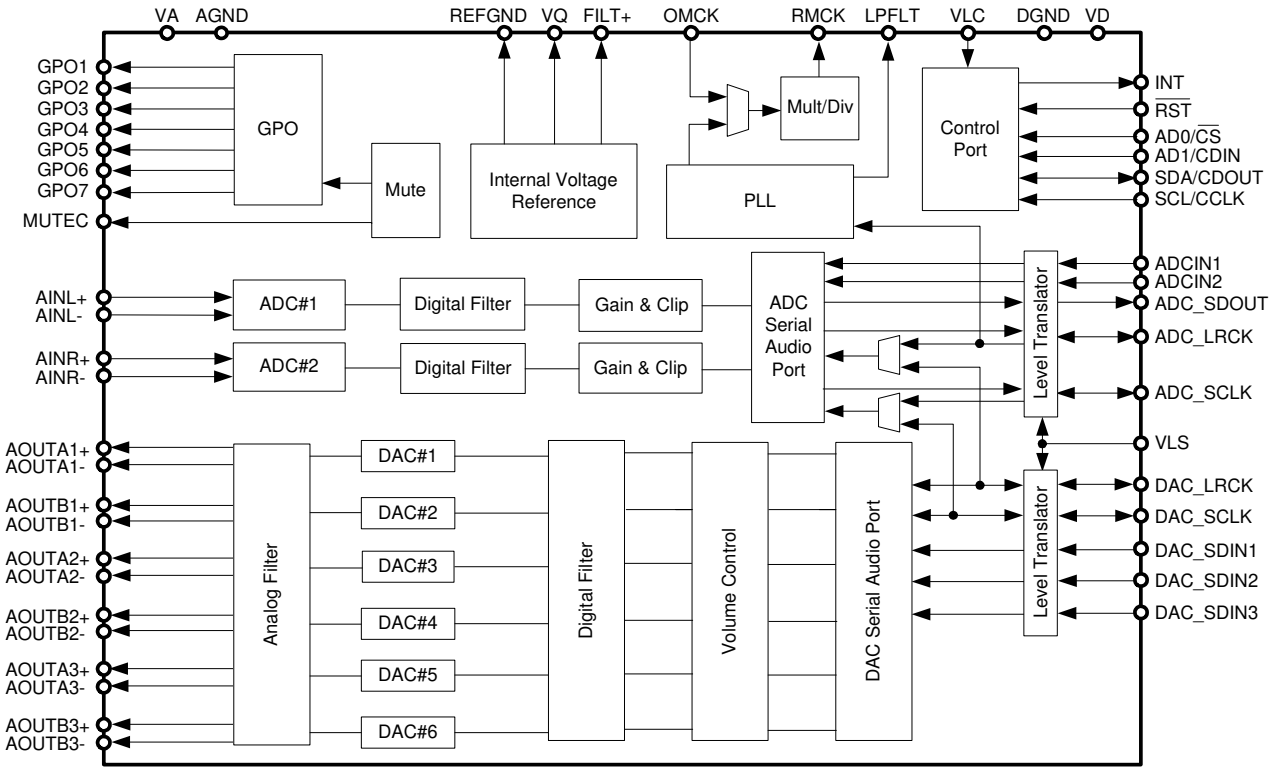
General Description

The CS42426 codec provides two analog-to-digital and six digital-to-analog delta-sigma converters, as well as an integrated PLL.

The CS42426 integrated PLL provides a low-jitter system clock. The internal stereo ADC is capable of independent channel gain control for single-ended or differential analog inputs. All six channels of DAC provide digital volume control and differential analog outputs. The general-purpose outputs may be driven high or low, or mapped to a variety of DAC mute controls or ADC overflow indicators.

The CS42426 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, digital speaker and automotive audio systems.

The CS42426 is available in a 64-pin LQFP package in both Commercial (-10° to +70° C) and Automotive (-40° to +85° C) grades. The CDB42428 Customer Demonstration board is also available for device evaluation. Refer to "Ordering Information" on page 71.



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1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25° C.)

SPECIFIED OPERATING CONDITIONS

(AGND=DGND=0, all voltages with respect to ground; OMCK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supply	Analog	VA	4.75	5.0	5.25	V
	Digital	VD	3.13	3.3	5.25	V
	Serial Port Interface	VLS	1.8	5.0	5.25	V
	Control Port Interface	VLC	1.8	5.0	5.25	V
Ambient Operating Temperature (power applied)	CS42426-CQZ	T_A	-10	-	+70	°C
	CS42426-DQZ		-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	Serial Port Interface	VLS	-0.3	6.0	V
	Control Port Interface	VLC	-0.3	6.0	V
Input Current	(Note 1)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 2)	V_{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage	Serial Port Interface	V_{IND-S}	-0.3	VLS+ 0.4	V
(Note 2)	Control Port Interface	V_{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature(power applied)					
	CS42426-CQZ	T_A	-20	+85	°C
	CS42426-DQZ	T_A	-50	+95	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
2. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS

(T_A = 25° C; VA = 5 V, VD = 3.3 V, Logic "0" = DGND =AGND = 0 V; Logic "1" = VLS = VLC = 5 V; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Full-scale input sine wave, 997 Hz.; PDN_PLL = 1; OMCK = 12.288 MHz; Single-Speed Mode DAC_SCLK = 3.072 MHz; Double-Speed Mode DAC_SCLK = 6.144 MHz; Quad-Speed Mode DAC_SCLK = 12.288 MHz.)

Parameter	Symbol	CS42426-CQZ Min	CS42426-CQZ Typ	CS42426-CQZ Max	CS42426-DQZ Min	CS42426-DQZ Typ	CS42426-DQZ Max	Unit
Single-Speed Mode (Fs=48 kHz)								
Dynamic Range A-weighted		108	114	-	106	114	-	dB
unweighted		105	111	-	103	111	-	dB
Total Harmonic Distortion + Noise								
(Note 3) -1 dB	THD+N	-	-100	-94	-	-100	-92	dB
-20 dB		-	-91	-	-	-91	-	dB
-60 dB		-	-51	-	-	-51	-	dB
Double-Speed Mode (Fs=96 kHz)								
Dynamic Range A-weighted		108	114	-	106	114	-	dB
unweighted		105	111	-	103	111	-	dB
40 kHz bandwidth unweighted		-	108	-	-	108	-	dB
Total Harmonic Distortion + Noise								
(Note 3) -1 dB		-	-100	-94	-	-100	-92	dB
-20 dB	THD+N	-	-91	-	-	-91	-	dB
-60 dB		-	-51	-	-	-51	-	dB
40 kHz bandwidth -1 dB		-	-97	-	-	-97	-	dB
Quad-Speed Mode (Fs=192 kHz)								
Dynamic Range A-weighted		108	114	-	106	114	-	dB
unweighted		105	111	-	103	111	-	dB
40 kHz bandwidth unweighted		-	108	-	-	108	-	dB
Total Harmonic Distortion+ Noise								
(Note 3) -1 dB		-	-100	-94	-	-100	-92	dB
-20 dB	THD+N	-	-91	-	-	-91	-	dB
-60 dB		-	-51	-	-	-51	-	dB
40 kHz bandwidth -1 dB		-	-97	-	-	-97	-	dB
Dynamic Performance for All Modes								
Interchannel Isolation		-	110	-	-	110	-	dB
Interchannel Phase Deviation		-	0.0001	-	-	0.0001	-	Degree
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	+/-100	-	-	+/-100	-	ppm/°C
Offset Error HPF_FREEZE disabled		-	0	-	-	0	-	LSB
HPF_FREEZE enabled		-	100	-	-	100	-	LSB
Analog Input								
Full-scale Differential Input Voltage		1.05 VA	1.10 VA	1.16 VA	0.99 VA	1.10 VA	1.21 VA	Vpp
Input Impedance (Differential) (Note 4)		17	-	-	17	-	-	kΩ
Common Mode Rejection Ratio	CMRR	-	82	-	-	82	-	dB

Notes:

3. Referred to the typical full-scale voltage.
4. Measured between AIN+ and AIN-

A/D DIGITAL FILTER CHARACTERISTICS

Parameter			Symbol	Min	Typ	Max	Unit
Single-Speed Mode (2 to 50 kHz sample rates)							
Passband	(-0.1 dB)	(Note 5)		0	-	0.47	Fs
Passband Ripple				-	-	±0.035	dB
Stopband		(Note 5)		0.58	-	-	Fs
Stopband Attenuation				-95	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	12/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0.0	µs
Double-Speed Mode (50 to 100 kHz sample rates)							
Passband	(-0.1 dB)	(Note 5)		0	-	0.45	Fs
Passband Ripple				-	-	±0.035	dB
Stopband		(Note 5)		0.68	-	-	Fs
Stopband Attenuation				-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	9/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0.0	µs
Quad-Speed Mode (100 to 192 kHz sample rates)							
Passband	(-0.1 dB)	(Note 5)		0	-	0.24	Fs
Passband Ripple				-	-	±0.035	dB
Stopband		(Note 5)		0.78	-	-	Fs
Stopband Attenuation				-97	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	5/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0.0	µs
High-Pass Filter Characteristics							
Frequency Response	-3.0 dB -0.13 dB	 (Note 6)		-	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	(Note 6)		-	10	-	Deg
Passband Ripple				-	-	0	dB
Filter Setting Time				-	10^5/Fs	-	s

Notes:

5. The filter frequency response scales precisely with Fs.
6. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

ANALOG OUTPUT CHARACTERISTICS

(T_A = 25° C; VA = 5 V, VD = 3.3 V, Logic "0" = DGND =AGND = 0 V; Logic "1" = VLS = VLC = 5V; Measurement Bandwidth 10 Hz to 20 kHz unless otherwise specified.; Full-scale output 997 Hz sine wave, Test load R_L = 3 kΩ, C_L = 30 pF; PDN_PLL = 1; OMCK = 12.288 MHz; Single-Speed Mode, DAC_SCLK = 3.072 MHz; Double-Speed Mode, DAC_SCLK = 6.144 MHz; Quad-Speed Mode, DAC_SCLK = 12.288 MHz.)

Parameter	Symbol	CS42426-CQZ Min	CS42426-CQZ Typ	CS42426-CQZ Max	CS42426-DQZ Min	CS42426-DQZ Typ	CS42426-DQZ Max	Unit
Dynamic performance for all modes								
Dynamic Range (Note 7)								
24-bit A-Weighted		108	114	-	106	114	-	dB
unweighted		105	111	-	103	111	-	dB
16-bit A-Weighted		-	97	-	-	97	-	dB
(Note 8) unweighted		-	94	-	-	94	-	dB
Total Harmonic Distortion + Noise								
24-bit 0 dB		-	-100	-94	-	-100	-92	dB
-20 dB		-	-91	-	-	-91	-	dB
-60 dB	THD+N	-	-51	-	-	-51	-	dB
16-bit 0 dB		-	-94	-	-	-94	-	dB
(Note 8) -20 dB		-	-74	-	-	-74	-	dB
-60 dB		-	-34		-	-34	-	dB
Idle Channel Noise/Signal-to-Noise Ratio (A-Weighted)		-	114	-	-	114	-	dB
Interchannel Isolation (1 kHz)		-	90	-	-	90	-	dB
Analog Output Characteristics for all modes								
Unloaded Full-Scale Differential Output Voltage	V_{FS}	.89 VA	.94 VA	.99 VA	.84 VA	.94 VA	1.04 VA	Vpp
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	300	-	-	300	-	ppm/°C
Output Impedance	Z_{OUT}	-	150	-	-	150	-	Ω
AC-Load Resistance	R_L	3	-	-	3	-	-	kΩ
Load Capacitance	C_L	-	-	30	-	-	30	pF

Notes:

7. One-half LSB of triangular PDF dither is added to data.
8. Performance limited by 16-bit quantization noise.

D/A DIGITAL FILTER CHARACTERISTICS

Parameter		Fast Roll-Off Min	Fast Roll-Off Typ	Fast Roll-Off Max	Slow Roll-Off Min	Slow Roll-Off Typ	Slow Roll-Off Max	Unit
Combined Digital and On-chip Analog Filter Response - Single-Speed Mode - 48 kHz								
Passband (Note 9)	to -0.01 dB corner	0	-	0.4535	0	-	0.4166	Fs
	to -3 dB corner	0	-	0.4998	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	-0.01	-	+0.01	dB
StopBand		0.5465	-	-	0.5834	-	-	Fs
StopBand Attenuation	(Note 10)	90	-	-	64	-	-	dB
Group Delay		-	12/Fs	-	-	6.5/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.41/Fs		-	±0.14/Fs	s
De-emphasis Error (Note 11)	Fs = 32 kHz	-	-	±0.23	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	-	-	±0.09	dB
Combined Digital and On-chip Analog Filter Response - Double-Speed Mode - 96 kHz								
Passband (Note 9)	to -0.01 dB corner	0	-	0.4166	0	-	0.2083	Fs
	to -3 dB corner	0	-	0.4998	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	-0.01	-	0.01	dB
StopBand		0.5834	-	-	0.7917	-	-	Fs
StopBand Attenuation	(Note 10)	80	-	-	70	-	-	dB
Group Delay		-	4.6/Fs	-	-	3.9/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.03/Fs		-	±0.01/Fs	s
Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode - 192 kHz								
Passband (Note 9)	to -0.01 dB corner	0	-	0.1046	0	-	0.1042	Fs
	to -3 dB corner	0	-	0.4897	0	-	0.4813	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	-0.01	-	0.01	dB
StopBand		0.6355	-	-	0.8683	-	-	Fs
StopBand Attenuation	(Note 10)	90	-	-	75	-	-	dB
Group Delay		-	4.7/Fs	-	-	4.2/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.01/Fs		-	±0.01/Fs	s

Notes:

9. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 39 to 62) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
10. Single- and Double-Speed Mode Measurement Bandwidth is from stopband to 3 Fs.
    Quad-Speed Mode Measurement Bandwidth is from stopband to 1.34 Fs.
11. De-emphasis is available only in Single-Speed Mode.

SWITCHING CHARACTERISTICS

(For CQZ, T_A = -10 to +70° C; For DQZ, T_A = -40 to +85° C;
VA = 5 V, VD =VLC= 3.3 V, VLS = 1.8 V to 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VLS, C_L = 30 pF)

Parameters	Symbol	Min	Typ	Max	Units
$\overline{RST}$ Pin Low Pulse Width (Note 12)		1	-	-	ms
PLL Clock Recovery Sample Rate Range		30	-	200	kHz
RMCK Output Jitter (Note 14)		-	200	-	ps RMS
RMCK Output Duty Cycle (Note 15)		45	50	55	%
OMCK Frequency (Note 13)		1.024	-	25.600	MHz
OMCK Duty Cycle (Note 13)		40	50	60	%
DAC_SCLK, ADC_SCLK Duty Cycle		45	50	55	%
DAC_LRCK, ADC_LRCK Duty Cycle		45	50	55	%
Master Mode					
RMCK to DAC_SCLK, ADC_SCLK active edge delay	t_{smd}	0	-	15	ns
RMCK to DAC_LRCK, ADC_LRCK delay	t_{lmd}	0	-	15	ns
Slave Mode					
DAC_SCLK, ADC_SCLK Falling Edge to ADC_SDOUT, ADC_SDOUT Output Valid	t_{dpd}		-	(Note 16)	ns
DAC_LRCK, ADC_LRCK Edge to MSB Valid	t_{lrpd}		-	26.5	ns
DAC_SDIN Setup Time Before DAC_SCLK Rising Edge	t_{ds}	10	-	-	ns
DAC_SDIN Hold Time After DAC_SCLK Rising Edge	t_{dh}	30	-	-	ns
DAC_SCLK, ADC_SCLK High Time	t_{sckh}	20	-	-	ns
DAC_SCLK, ADC_SCLK Low Time	t_{sckl}	20	-	-	ns
DAC_SCLK, ADC_SCLK falling to DAC_LRCK, SAI_LRCK Edge	t_{lrck}	-25	-	+25	ns

Notes:

12. After powering-up the CS42426, $\overline{RST}$ should be held low after the power supplies and clocks are settled.
13. See Table 1 on page 24 for suggested OMCK frequencies
14. Limit the loading on RMCK to 1 CMOS load if operating above 24.576 MHz.
15. Not valid when RMCK_DIV in "Clock Control (address 06h)" on page 48 is set to Multiply by 2.
16. 76.5 ns for Single-Speed and Double-Speed modes, 23 ns for Quad-Speed Mode.

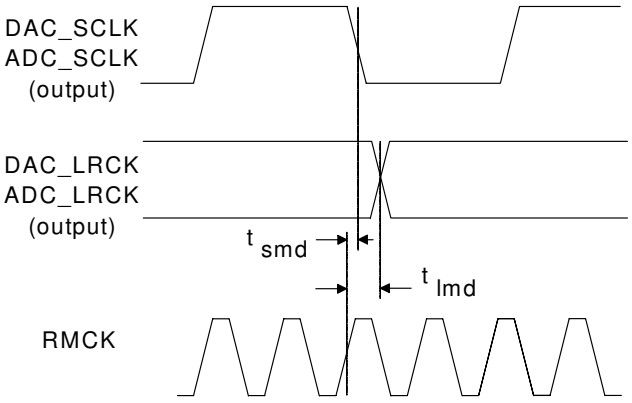


Figure 1. Serial Audio Port Master Mode Timing

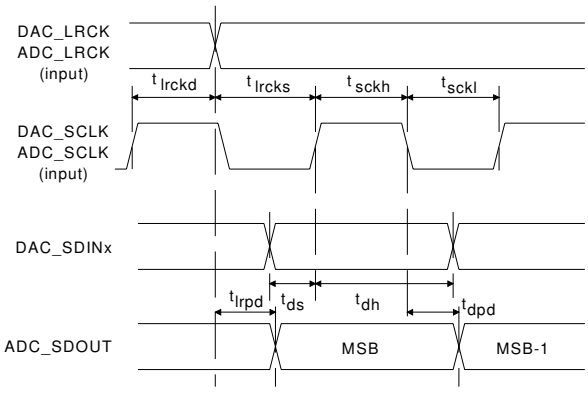


Figure 2. Serial Audio Port Slave Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(For CQZ, T_A = -10 to +70° C; For DQZ, T_A = -40 to +85° C; VA = 5 V, VD =VLS= 3.3 V; VLC = 1.8 V to 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 17)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling (Note 18)	t_{ack}	-	(Note 19)	ns

Notes:

17. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.
18. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.
19. $\frac{15}{256 \times Fs}$ for Single-Speed Mode, $\frac{15}{128 \times Fs}$ for Double-Speed Mode, $\frac{15}{64 \times Fs}$ for Quad-Speed Mode

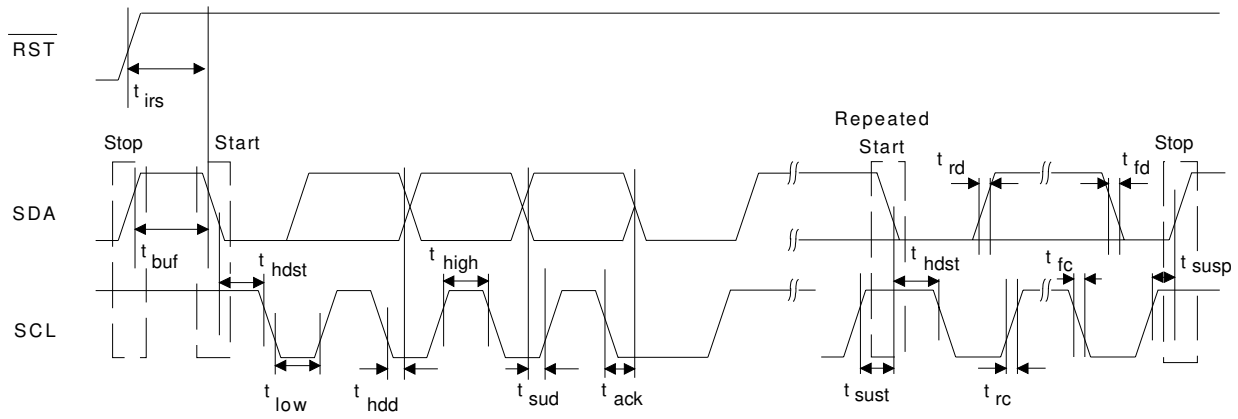


Figure 3. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI™ FORMAT

(For CQZ, T_A = -10 to +70° C; For DQZ, T_A = -40 to +85° C; VA = 5 V, VD =VLS= 3.3 V; VLC = 1.8 V to 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Typ	Max	Units
CCLK Clock Frequency		f_{sck}	0	-	6.0	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	-	ns
CCLK Low Time		t_{scl}	66	-	-	ns
CCLK High Time		t_{sch}	66	-	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	-	ns
CCLK Rising to DATA Hold Time	(Note 20)	t_{dh}	15	-	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	-	50	ns
Rise Time of CDOUT		t_{r1}	-	-	25	ns
Fall Time of CDOUT		t_{f1}	-	-	25	ns
Rise Time of CCLK and CDIN	(Note 21)	t_{r2}	-	-	100	ns
Fall Time of CCLK and CDIN	(Note 21)	t_{f2}	-	-	100	ns

Notes:

20. Data must be held for sufficient time to bridge the transition time of CCLK.
21. For f_{sck} <1 MHz.

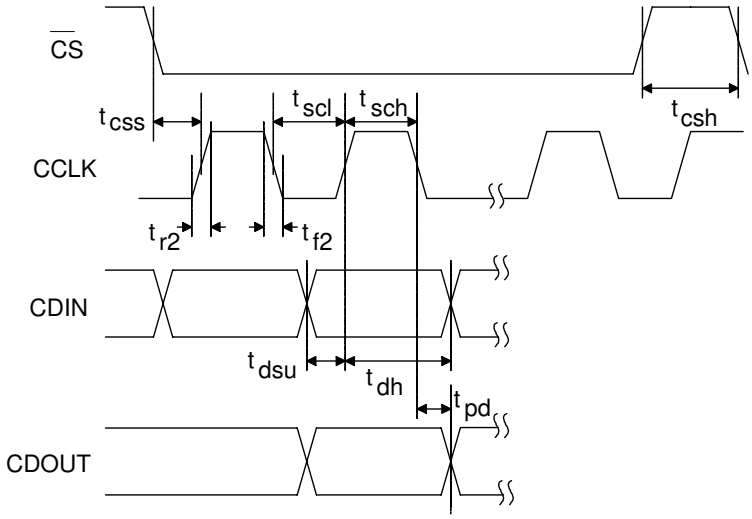


Figure 4. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(T_A = 25° C; AGND=DGND=0, all voltages with respect to ground; OMCK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Current	normal operation, VA = 5 V	I_A	-	75	-	mA
(Note 22)	VD = 5 V	I_D	-	85	-	mA
	VD = 3.3 V	I_D	-	51	-	mA
	Interface current, VLC=5 V (Note 23)	I_{LC}	-	250	-	µA
	VLS=5 V	I_{LS}	-	13	-	mA
	power-down state (all supplies) (Note 24)	I_{pd}	-	250	-	µA
Power Consumption	(Note 22)					
VA=5 V, VD=VLS=VLC=3.3 V	normal operation		-	587	650	mW
	power-down (Note 24)		-	1.25	-	mW
VA=5 V, VD=VLS=VLC=5 V	normal operation		-	866	960	mW
	power-down (Note 24)		-	1.25	-	mW
Power Supply Rejection Ratio (Note 25)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB
VQ Nominal Voltage			-	2.7	-	V
VQ Output Impedance			-	50	-	kΩ
VQ Maximum allowable DC current			-	0.01	-	mA
FILT+ Nominal Voltage			-	5.0	-	V
FILT+ Output Impedance			-	35	-	kΩ
FILT+ Maximum allowable DC current			-	0.01	-	mA

Notes:

22. Current consumption increases with increasing FS and increasing OMCK. Max values are based on highest FS and highest OMCK. Variance between speed modes is negligible.
23. I_{LC} measured with no external loading on the SDA pin.
24. Power-Down Mode is defined as $\overline{RST}$ pin = Low with all clock and data lines held static.
25. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 5.

DIGITAL INTERFACE CHARACTERISTICS

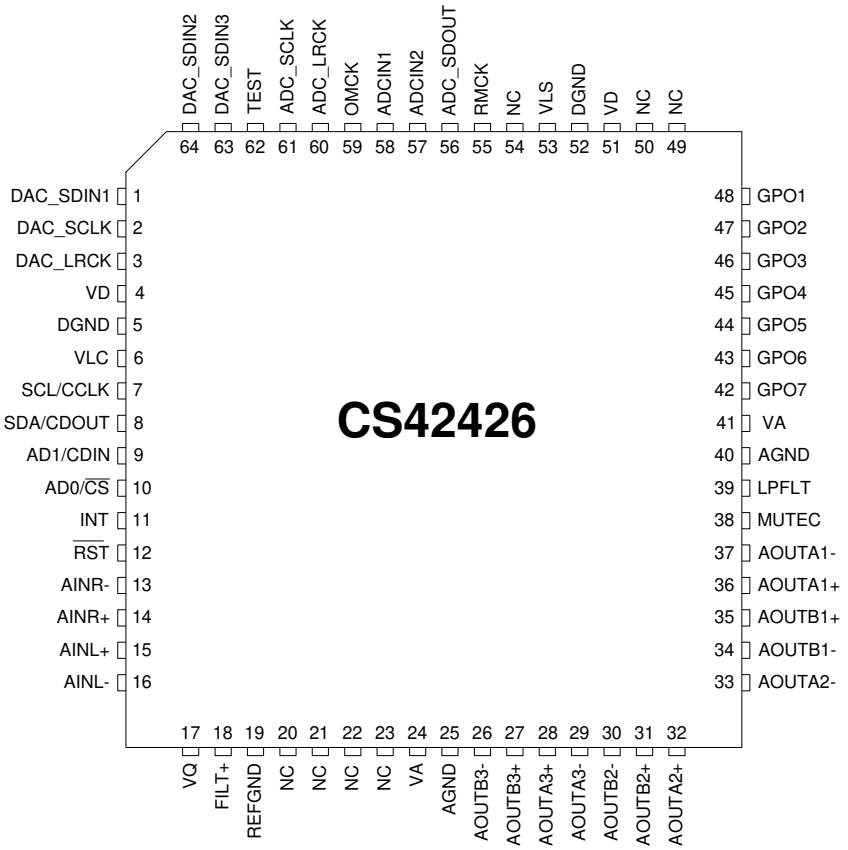
(For CQZ, T_A = +25° C; For DQZ, T_A = -40 to +85° C)

Parameters (Note 26)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Serial Port	V_{IH}	0.7xVLS	-	-	V
	Control Port		0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.2xVLS	V
	Control Port		-	-	0.2xVLC	V
High-Level Output Voltage at I_o=2 mA	(Note 27) Serial Port	V_{OH}	VLS-1.0	-	-	V
	Control Port		VLC-1.0	-	-	V
	MUTEC, GPOx		VA-1.0	-	-	V
Low-Level Output Voltage at I_o=2 mA (Note 27) Serial Port, Control Port, MUTEC, GPOx		V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
MUTEC Drive Current			-	3	-	mA

Notes:

26. Serial Port signals include: RMCK, OMCK, ADC_SCLK, ADC_LRCK, DAC_SCLK, DAC_LRCK, ADC_SDOUT, DAC_SDIN1-3, ADCIN1/2
    Control Port signals include: SCL/CCLK, SDA/CDOUT, AD0/$\overline{CS}$, AD1/CDIN, INT, $\overline{RST}$
27. When operating RMCK above 24.576 MHz, limit the loading on the signal to 1 CMOS load.

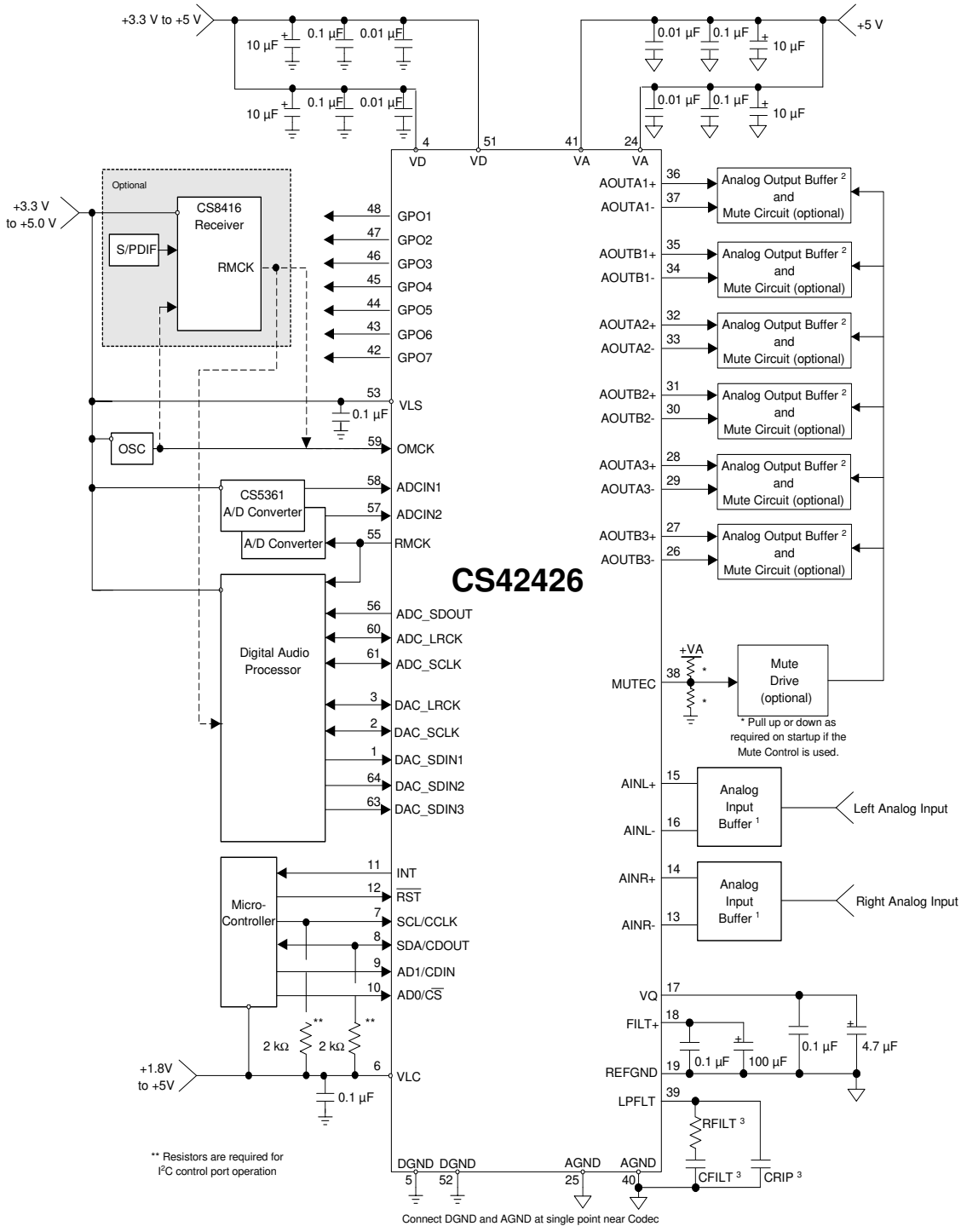
2. PIN DESCRIPTIONS



Pin Name	#	Pin Description
DAC_SDIN1 DAC_SDIN2 DAC_SDIN3	1 64 63	**DAC Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
DAC_SCLK	2	**DAC Serial Clock** *(Input/Output)* - Serial clock for the DAC serial audio interface.
DAC_LRCK	3	**DAC Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the DAC serial audio data line.
VD	4 51	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	5 52	**Digital Ground** (*Input*) - Ground reference. Should be connected to digital ground.
VLC	6	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port.
SCL/CCLK	7	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I²C mode as shown in the Typical Connection Diagram.
SDA/CDOUT	8	**Serial Control Data** (*Input/Output*) **-** SDA is a data I/O line in I²C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	9	**Address Bit 1 (I²C)/Serial Control Data (SPI)** (*Input*) - AD1 is a chip address pin in I²C mode; CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{CS}$	10	**Address Bit 0 (I²C)/Control Port Chip Select (SPI)** *(Input*) **-** AD0 is a chip address pin in I²C mode; $\overline{CS}$ is the chip select signal in SPI mode.
INT	11	**Interrupt** *(Output*) - The CS42426 will generate an interrupt condition as per the Interrupt Mask register. See "Interrupts" on page 37 for more details.

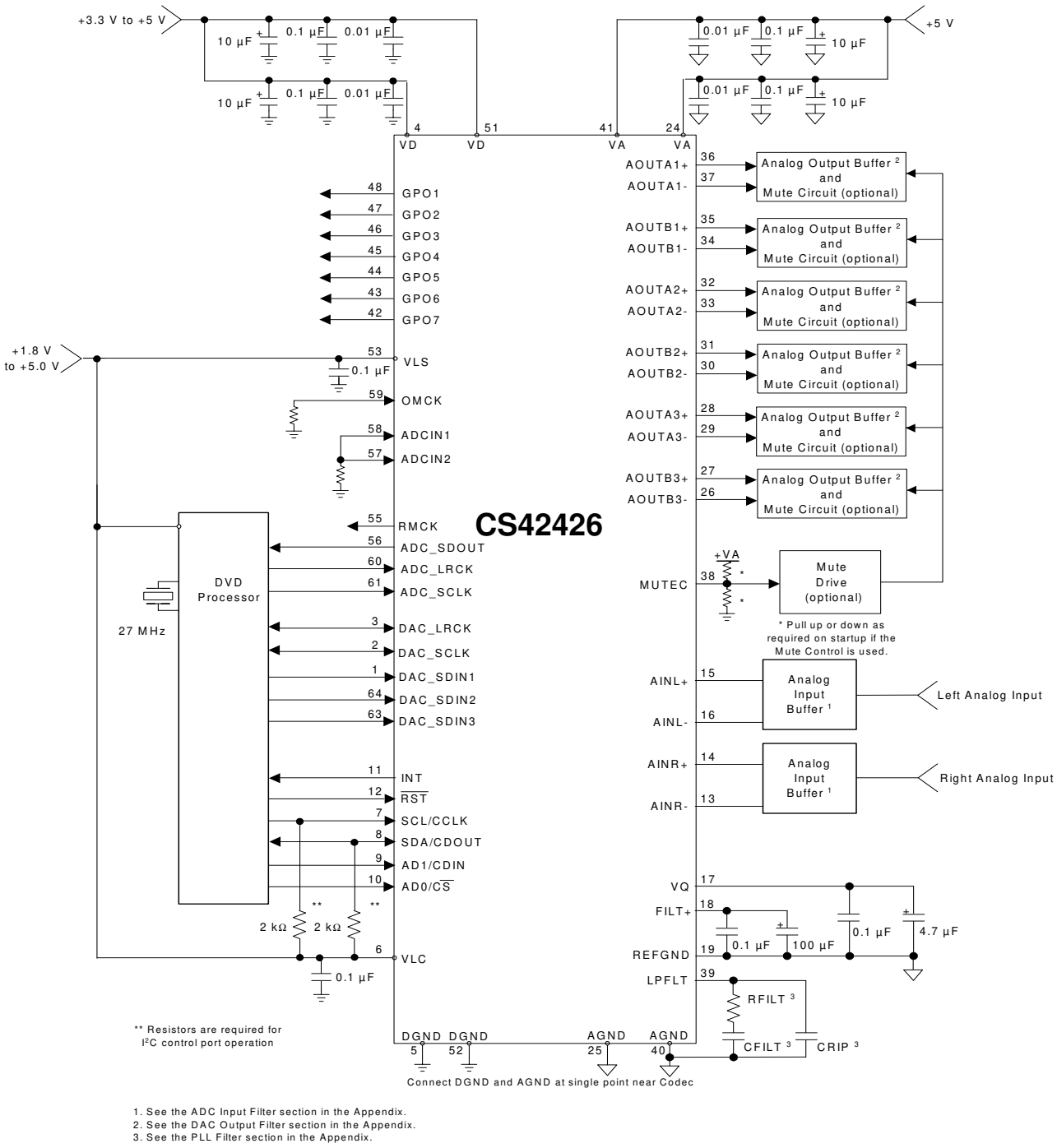
$\overline{\text{RST}}$	12	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
AINR- AINR+	13 14	**Differential Right Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
AINL+ AINL-	15 16	**Differential Left Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins.
VQ	17	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
REFGND	19	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
AOUTA1 +,- AOUTB1 +,- AOUTA2 +,- AOUTB2 +,- AOUTA3 +,- AOUTB3 +,-	36,37 35,34 32,33 31,30 28,29 27,26	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VA	24 41	**Analog Power** (*Input*) - Positive power supply for the analog section.
AGND	25 40	**Analog Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MUTEC	38	**Mute Control** (*Output*) - The Mute Control pin outputs high impedance following an initial power-on condition or whenever the PDN bit is set to a '1', forcing the codec into power-down mode. The signal will remain in a high impedance state as long as the part is in power-down mode. The Mute Control pin goes to the selected "active" state during reset, muting, or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
LPFLT	39	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and ground.
GPO7 GPO6 GPO5 GPO4 GPO3 GPO2 GPO1	42 43 44 45 46 47 48	**General Purpose Output** (*Output*) - These pins can be configured as general purpose output pins, an ADC overflow interrupt or Mute Control outputs according to the General Purpose Pin Control registers.
VLS	53	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial port interfaces.
RMCK	55	**Recovered Master Clock** (*Output*) - Recovered master clock output from the External Clock Reference (OMCK, pin 59) or the PLL which is locked to the incoming ADC_LRCK.
ADC_SDOUT	56	**ADC Serial Data Output** (*Output*) - Output for two's complement serial audio PCM data from the output of the internal and external ADCs.
ADCIN1 ADCIN2	58 57	**External ADC Serial Input** (*Input*) - The CS42426 provides for up to two external stereo analog to digital converter inputs to provide a maximum of six channels on one serial data output line when the CS42426 is placed in One-Line Mode.
OMCK	59	**External Reference Clock** (*Input*) - External clock reference that must be within the ranges specified in the register "OMCK Frequency (OMCK Freqx)" on page 48.
ADC_LRCK	60	**ADC Left/Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the ADC serial audio data line.
ADC_SCLK	61	**ADC Serial Clock** *(Input/Output)* - Serial clock for the ADC serial audio interface.
TEST	62	**Test Pin** (*Input*) - This pin must be connected to DGND.

3. TYPICAL CONNECTION DIAGRAMS



1. See the ADC Input Filter section in the Appendix.
2. See the DAC Output Filter section in the Appendix.
3. See the PLL Filter section in the Appendix.

Figure 5. Typical Connection Diagram



1. See the ADC Input Filter section in the Appendix.
2. See the DAC Output Filter section in the Appendix.
3. See the PLL Filter section in the Appendix.

Figure 6. Typical Connection Diagram using the PLL

4. APPLICATIONS

4.1 Overview

The CS42426 is a highly integrated mixed-signal 24-bit audio codec comprised of 2 analog-to-digital converters (ADC), implemented using multi-bit delta-sigma techniques, and 6 digital-to-analog converters (DAC). Other functions integrated within the codec include independent digital volume controls for each DAC, digital de-emphasis filters for DAC, digital gain control for ADC channels, ADC high-pass filters, and an on-chip voltage reference. All serial data is transmitted through one configurable serial audio interface for the ADC with enhanced one-line modes of operation, allowing up to 6 channels of serial audio data on one data line. All functions are configured through a serial control port operable in SPI mode or in I²C mode. Figure 5 and Figure 6 show the recommended connections for the CS42426.

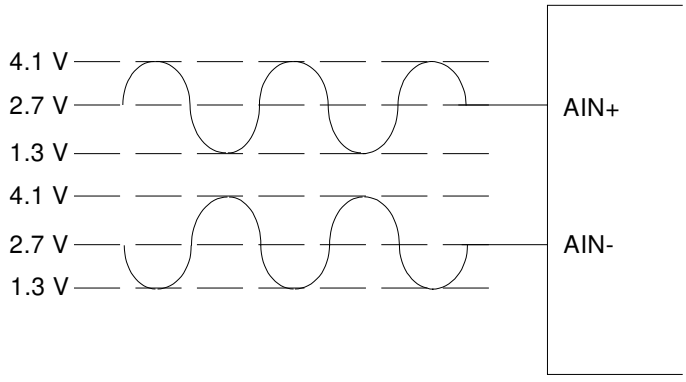
The CS42426 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the FM bits in register "Functional Mode (address 03h)" on page 43. Single-Speed Mode (SSM) supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed Mode (DSM) supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed Mode (QSM) supports input sample rates up to 192 kHz and uses an oversampling ratio of 32x.

Using the integrated PLL, a low-jitter clock is recovered from the ADC LRCK input signal. The recovered clock or an externally supplied clock attached to the OMCK pin can be used as the System Clock.

4.2 Analog Inputs

4.2.1 Line-Level Inputs

AINR+, AINR-, AINL+, and AINL- are the line-level differential analog inputs. The analog signal must be externally biased to VQ, approximately 2.7 V, before being applied to these inputs. The level of the signal can be adjusted for the left and right ADC independently through the ADC Left and Right Channel Gain Control Registers on page 55. The ADC output data is in two's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively and cause the ADC Overflow bit in the register "Interrupt Status (address 20h) (Read Only)" on page 56 to be set to a '1'. The GPO pins may also be configured to indicate an overflow condition has occurred in the ADC. See "General-Purpose Pin Control (addresses 29h to 2Fh)" on page 58 for proper configuration. Figure 7 shows the full-scale analog input levels. See "ADC Input Filter" on page 61 for a recommended input buffer.



Full-Scale Input Level= (AIN+) - (AIN-)= 5.6 Vpp

Figure 7. Full-Scale Analog Input

4.2.2 High-Pass Filter and DC Offset Calibration

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. The high-pass filter can be independently enabled and disabled. If the HPF_Freeze bit is set during normal operation, the current value of the DC offset for the corresponding channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS42426 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

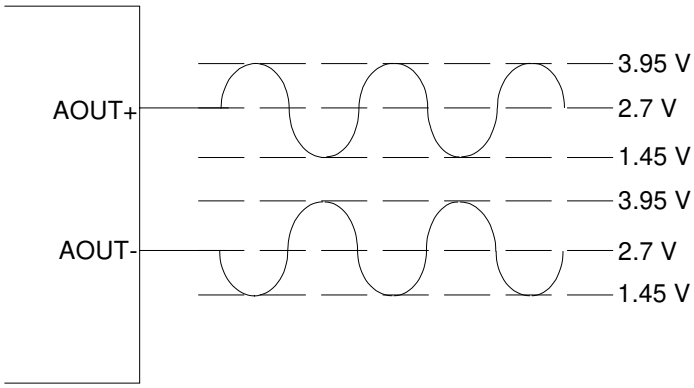
The high-pass filters are controlled using the HPF_FREEZE bit in the register "Misc Control (address 05h)" on page 46.

4.3 Analog Outputs

4.3.1 Line-Level Outputs and Filtering

The CS42426 contains on-chip buffer amplifiers capable of producing line-level differential outputs. These amplifiers are biased to a quiescent DC level of approximately VQ.

The delta-sigma conversion process produces high-frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low-pass filter. See "DAC Output Filter" on page 61 for a recommended output buffer. This filter configuration accounts for the normally differing AC loads on the AOUT+ and AOUT- differential output pins. It also shows an AC coupling configuration which minimizes the number of required AC coupling capacitors. Figure 8 shows the full-scale analog output levels.



Full-Scale Output Level= (AIN+) - (AIN-)= 5 Vpp

Figure 8. Full-Scale Output

4.3.2 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS42426 incorporates selectable interpolation filters for each mode of operation. A "fast" and a "slow" roll-off filter is available in Single-, Double-, and Quad-Speed Modes. These filters have been designed to accommodate a variety of musical tastes and styles. The FILT_SEL bit found in the register "Misc Control (address 05h)" on page 46 selects which filter is used. Filter response plots can be found in Figures 39 to 62.

4.3.3 Digital Volume and Mute Control

Each DAC's output level is controlled via the Volume Control registers operating over the range of 0 to -127 dB attenuation with 0.5 dB resolution. See "Volume Control (addresses 0Fh, 10h, 11h, 12h, 13h, 14h)" on page 53. Volume control changes are programmable to ramp in increments of 0.125 dB at the rate controlled by the SZC[1:0] bits in the Digital Volume Control register. See "Volume Transition Control (address 0Dh)" on page 51.

Each output can be independently muted via mute control bits in the register "Channel Mute (address 0Eh)" on page 52. When enabled, each XX_MUTE bit attenuates the corresponding DAC to its maximum value (-127 dB). When the XX_MUTE bit is disabled, the corresponding DAC returns to the attenuation level set in the Volume Control register. The attenuation is ramped up and down at the rate specified by the SZC[1:0] bits.

The Mute Control pin, MUTEC, is typically connected to an external mute control circuit. The Mute Control pin outputs high impedance during Power-Up or in Power-Down Mode by setting the PDN bit in the register "Power Control (address 02h)" on page 43 to a '1'. Once out of Power-Down Mode, the pin can be controlled by the user via the control port, or automatically asserted high when zero data is present on all DAC inputs, or when serial port clock errors are present. To prevent large transients on the output, it is desirable to mute the DAC outputs before the Mute Control pin is asserted. Please see the MUTEC pin in the Pin Descriptions section for more information.

Each of the GPO1-GPO7 can be programmed to provide a hardware MUTE signal to individual circuits. Each pin can be programmed as an output, with specific muting capabilities as defined by the function bits in the register "General-Purpose Pin Control (addresses 29h to 2Fh)" on page 58.

4.3.4 ATAPI Specification

The CS42426 implements the channel-mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 14 on page 54 and Figure 9 for additional information.

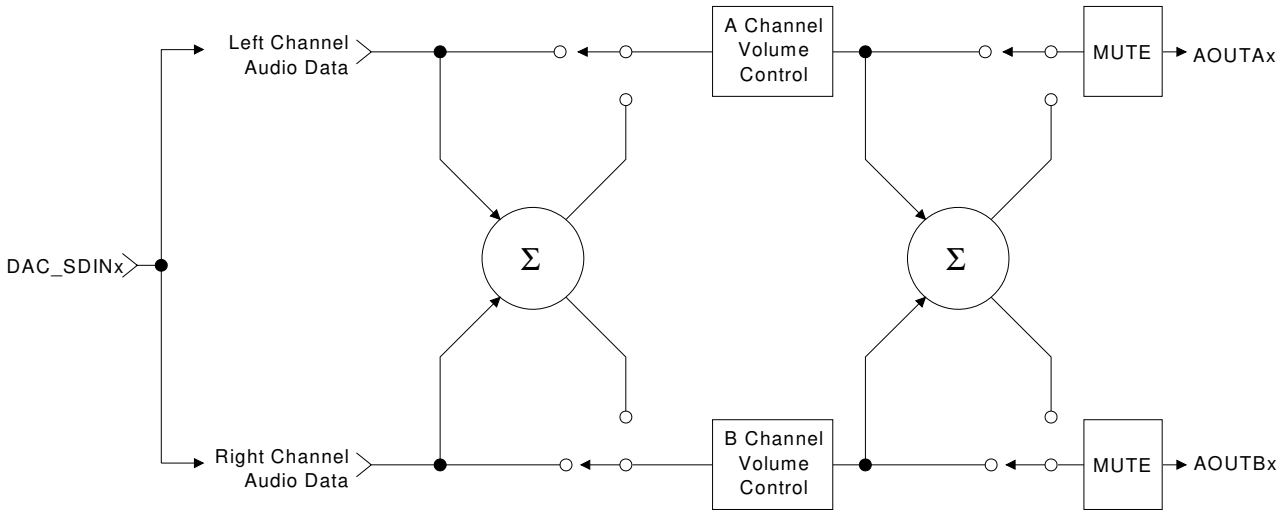


Figure 9. ATAPI Block Diagram (x = channel pair 1, 2, 3)

4.4 Clock Generation

The clock generation for the CS42426 is shown in the figure below. The internal MCLK is derived from the output of the PLL or a master clock source attached to OMCK. The mux selection is controlled by the SW_CTRLx bits and can be configured to manual switch mode only, or automatically switch on loss of PLL lock to the other source input.

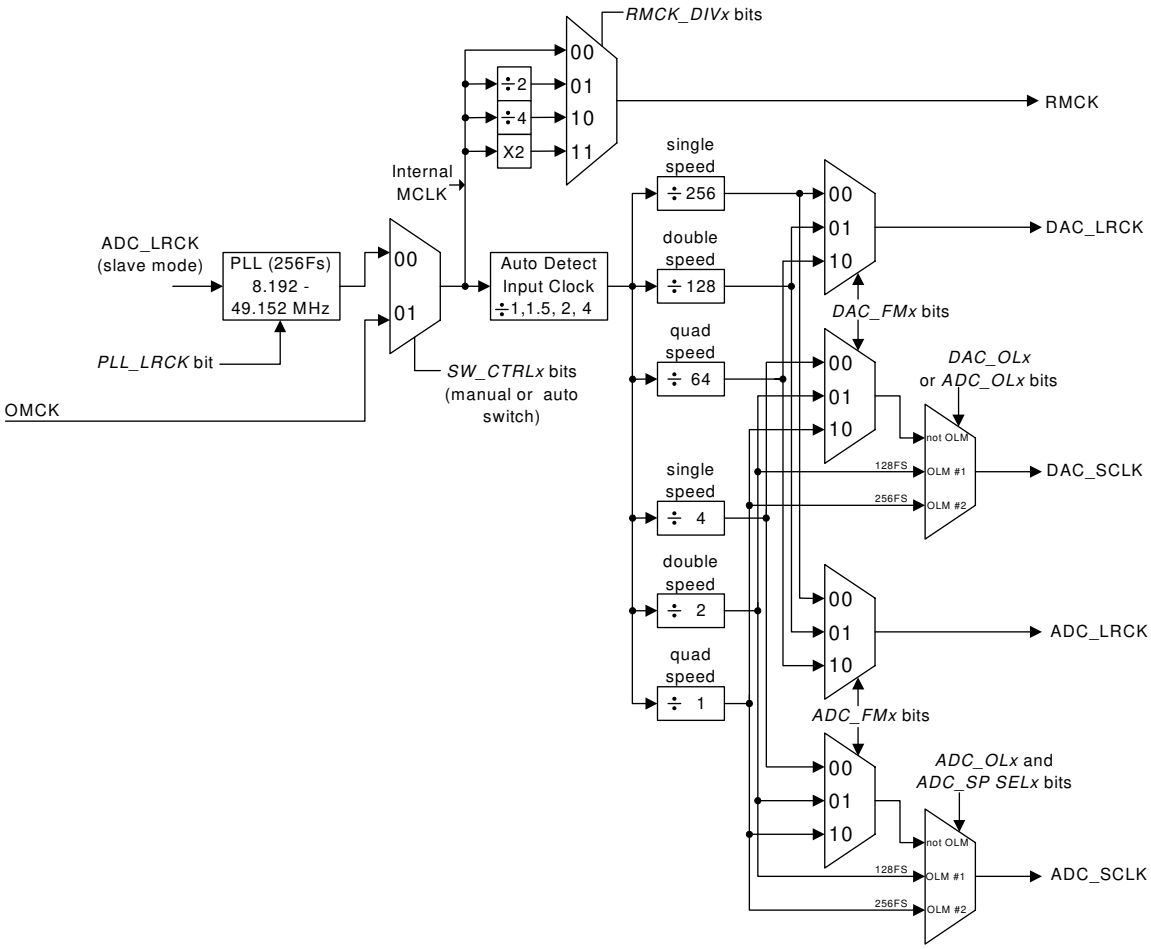


Figure 10. Clock Generation

4.4.1 PLL and Jitter Attenuation

The PLL can be configured to lock onto the incoming ADC_LRCK signal from the ADC Serial Port and generate the required internal master clock frequency. There are some applications where low jitter in the recovered clock, presented on the RMCK pin, is important. For this reason, the PLL has been designed to have good jitter-attenuation characteristics. By setting the PLL_LRCK bit to a '1' in the register "Clock Control (address 06h)" on page 48, the PLL will lock to the incoming ADC_LRCK and generate an output master clock (RMCK) of 256Fs. Table 2 shows the output of the PLL with typical input Fs values for ADC_LRCK.

See "Appendix B: PLL Filter" on page 62 for more information concerning PLL operation, required filter components, optimal layout guidelines, and jitter-attenuation characteristics.

4.4.2 OMCK System Clock Mode

A special clock-switching mode is available that allows the clock that is input through the OMCK pin to be used as the internal master clock. This feature is controlled by the SW_CTRLx bits in register "Clock Control (address 06h)" on page 48. An advanced auto-switching mode is also implemented to maintain master clock functionality. The clock auto-switching mode allows the clock input through OMCK to be used as a clock in the system without any disruption when the PLL loses lock, for example, when the LRCK is removed from ADC_LRCK. This clock-switching is done glitch-free. A clock adhering to the specifications detailed in the Switching Characteristics table on page 11 must be applied to the OMCK pin at all times that the FRC_PLL_LK bit is set to '0' (See "Force PLL Lock (FRC_PLL_LK)" on page 49).

Sample Rate (kHz)	OMCK (MHz)								
	Single-Speed (4 to 50 kHz)			Double-Speed (50 to 100 kHz)			Quad-Speed (100 to 192 kHz)		
	256x	384x	512x	128x	192x	256x	64x	96x	128x
48	12.2880	18.4320	24.5760	-	-	-	-	-	-
96	-	-	-	12.2880	18.4320	24.5760	-	-	-
192	-	-	-	-	-	-	12.2880	18.4320	24.5760

Table 1. Common OMCK Clock Frequencies

4.4.3 Master Mode

In Master Mode, the serial interface timings are derived from an external clock attached to OMCK or from the output of the PLL with an input reference to the ADC_LRCK input from the ADC serial port. The DAC Serial Port and ADC Serial Port can both be masters only when OMCK is used as the clock source. When using the PLL output, the ADC Serial Port must be slave and the DAC Serial Port can operate in Master Mode. Master clock selection and operation is configured with the SW_CTRL1:0 bits in the Clock Control Register (See "Clock Control (address 06h)" on page 48).

4.4.4 Slave Mode

In Slave Mode, DAC_LRCK, DAC_SCLK and/or ADC_LRCK and ADC_SCLK operate as inputs. The Left/Right clock signal must be equal to the sample rate, Fs, and must be synchronously derived from the supplied master clock, OMCK, or must be synchronous to the supplied ADC_LRCK used as the input to the PLL. In this latter scenario, the PLL output becomes the internal master clock. The supported PLL output frequencies are shown in Table 2.

Sample Rate (kHz)	PLL Output (MHz)		
	Single-Speed (4 to 50kHz)	Double-Speed (50 to 100kHz)	Quad-Speed (100 to 192kHz)
	256x	256x	256x
32	8.1920	-	-
44.1	11.2896	-	-
48	12.2880	-	-
64	-	16.3840	-
88.2	-	22.5792	-
96	-	24.5760	-
176.4	-	-	45.1584
192	-	-	49.1520

The serial bit clock, DAC_SCLK and/or ADC_SCLK, must be synchronous to the corresponding DAC_LRCK/ADC_LRCK and be equal to 128x, 64x, 48x or 32x Fs, depending on the interface format selected and desired speed mode.

When the device is clocked from OMCK, the frequency of OMCK must be at least twice the frequency of the fastest Slave Mode, SCLK. For example, if both serial ports are in Slave Mode with one SCLK running at 32x Fs and the other at 64x Fs, the slowest OMCK signal that can be used to clock the device is 128x Fs.

When either serial port is in Slave Mode, its respective LRCK signal must be present for proper device operation.

In Slave Mode, One-Line Mode #1 is supported; One-Line Mode #2 is not.

The sample rate to OMCK ratios and OMCK frequency requirements for Slave Mode operation are shown in Table 1. Refer to Table 3 for required clock ratios.

	Single-Speed	Double-Speed	Quad-Speed	One-Line Mode #1
OMCK/LRCK Ratio	256x, 384x, 512x	128x, 192x, 256x	64x, 96x, 128x	256x
SCLK/LRCK Ratio	32x, 48x, 64x, 128x	32x, 48x, 64x	32x, 48x, 64x	128x

Table 3. Slave Mode Clock Ratios

4.5 Digital Interfaces

4.5.1 Serial Audio Interface Signals

The CS42426 interfaces to an external Digital Audio Processor via two independent serial ports, the DAC serial port, DAC_SP, and the ADC serial port, ADC_SP. The digital output of the internal ADCs use the ADC_SDOUT pin and can be configured to use either the ADC or DAC serial port timings.These configuration bits and the selection of Single-, Double- or Quad-Speed Mode for DAC_SP and ADC_SP are found in register “Functional Mode (address 03h)” on page 43.

The serial interface clocks, ADC_SCLK for ADC_SP and DAC_SCLK for DAC_SP, are used for transmitting and receiving audio data. Either ADC_SCLK or DAC_SCLK can be generated by the CS42426 (Master Mode), or it can be input from an external source (Slave Mode). Master or Slave Mode selection is made using bits DAC_SP M/$\overline{S}$ and ADC_SP M/$\overline{S}$ in register “Misc Control (address 05h)” on page 46.

The Left/Right clock (ADC_LRCK or DAC_LRCK) is used to indicate left and right data frames and the start of a new sample period. It may be an output of the CS42426 (Master Mode), or it may be generated by an external source (Slave Mode). As described in later sections, particular modes of operation do allow the sample rate, Fs, of the ADC_SP and the DAC_SP to be different, but must be multiples of each other.

The serial data interface format selection (Left/Right-Justified, I²S or One-Line Mode) for the ADC serial port data out pin, ADC_SDOUT, and the DAC input pins, DAC_SDIN1:3, is configured using the appropriate bits in the register “Interface Formats (address 04h)” on page 45. The serial audio data is presented in two's complement binary form with the MSB first in all formats.

DAC_SDIN1, DAC_SDIN2, and DAC_SDIN3 are the serial data input pins supplying the internal DAC. ADC_SDOUT, the ADC data output pin, carries data from the two internal 24-bit ADCs and, when configured for one-line mode, up to four additional ADC channels attached externally to the signals ADCIN1 and ADCIN2 (typically two CS5361 stereo ADCs). When operated in One-Line Mode, 6 channels of DAC data are input on DAC_SDIN1 and 6 channels of ADC data are output on ADC_SDOUT. Table 4 on page 26 outlines the serial port channel allocations.