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## 114 dB, 192 kHz 8-Ch Codec with PLL

### Features

- ◆ Eight 24-bit D/A, two 24-bit A/D Converters
- ◆ 114 dB DAC / 114 dB ADC Dynamic Range
- ◆ -100 dB THD+N
- ◆ System Sampling Rates up to 192 kHz
- ◆ Integrated Low-Jitter PLL for Increased System Jitter Tolerance
- ◆ PLL Clock or System Clock Selection
- ◆ 7 Configurable General-Purpose Outputs
- ◆ ADC High-Pass Filter for DC Offset Calibration
- ◆ Expandable ADC Channels and One-Line Mode Support
- ◆ Digital Output Volume Control with Soft Ramp
- ◆ Digital +/-15 dB Input Gain Adjust for ADC
- ◆ Differential Analog Architecture
- ◆ Supports Logic Levels between 1.8 V and 5 V

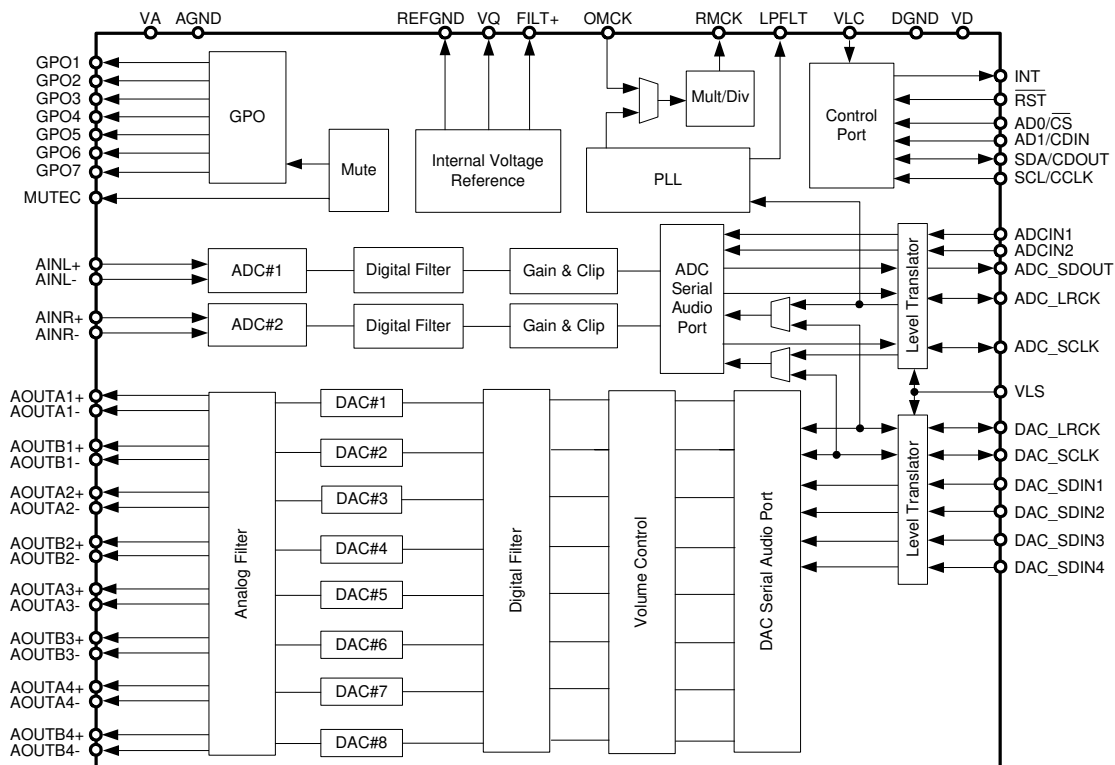
### General Description

The CS42428 codec provides two analog-to-digital and eight digital-to-analog delta-sigma converters, as well as an integrated PLL.

The CS42428 integrated PLL provides a low-jitter system clock. The internal stereo ADC is capable of independent channel gain control for single-ended or differential analog inputs. All eight channels of DAC provide digital volume control and differential analog outputs. The general-purpose outputs may be driven high or low, or mapped to a variety of DAC mute controls or ADC overflow indicators.

The CS42428 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, digital speaker and automotive audio systems.

The CS42428 is available in a 64-pin LQFP package in both Commercial (-10° to 70° C) and Automotive (-40° to 85° C) grades. The CDB42428 Customer Demonstration board is also available for device evaluation. Refer to ["Ordering Information" on page 71](#).



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**TABLE OF CONTENTS**

<b>1. CHARACTERISTICS AND SPECIFICATIONS .....</b>	<b>6</b>
SPECIFIED OPERATING CONDITIONS .....	6
ABSOLUTE MAXIMUM RATINGS .....	6
ANALOG INPUT CHARACTERISTICS .....	7
A/D DIGITAL FILTER CHARACTERISTICS .....	8
ANALOG OUTPUT CHARACTERISTICS .....	9
D/A DIGITAL FILTER CHARACTERISTICS .....	10
SWITCHING CHARACTERISTICS .....	11
SWITCHING CHARACTERISTICS - CONTROL PORT - I <sup>2</sup> C FORMAT .....	12
SWITCHING CHARACTERISTICS - CONTROL PORT - SPI™ FORMAT .....	13
DC ELECTRICAL CHARACTERISTICS .....	14
DIGITAL INTERFACE CHARACTERISTICS .....	15
<b>2. PIN DESCRIPTIONS .....</b>	<b>16</b>
<b>3. TYPICAL CONNECTION DIAGRAMS .....</b>	<b>18</b>
<b>4. APPLICATIONS .....</b>	<b>20</b>
4.1 Overview .....	20
4.2 Analog Inputs .....	20
4.2.1 Line-Level Inputs .....	20
4.2.2 High-Pass Filter and DC Offset Calibration .....	21
4.3 Analog Outputs .....	21
4.3.1 Line-Level Outputs and Filtering .....	21
4.3.2 Interpolation Filter .....	21
4.3.3 Digital Volume and Mute Control .....	22
4.3.4 ATAPI Specification .....	22
4.4 Clock Generation .....	23
4.4.1 PLL and Jitter Attenuation .....	23
4.4.2 OMCK System Clock Mode .....	24
4.4.3 Master Mode .....	24
4.4.4 Slave Mode .....	24
4.5 Digital Interfaces .....	25
4.5.1 Serial Audio Interface Signals .....	25
4.5.2 Serial Audio Interface Formats .....	27
4.5.3 ADCIN1/ADCIN2 Serial Data Format .....	30
4.5.4 One-Line Mode (OLM) Configurations .....	31
4.5.4.1 OLM Config #1 .....	31
4.5.4.2 OLM Config #2 .....	32
4.5.4.3 OLM Config #3 .....	33
4.5.4.4 OLM Config #4 .....	34
4.6 Control Port Description and Timing .....	35
4.6.1 SPI Mode .....	35
4.6.2 I <sup>2</sup> C Mode .....	36
4.7 Interrupts .....	37
4.8 Reset and Power-Up .....	37
4.9 Power Supply, Grounding, and PCB Layout .....	38
<b>5. REGISTER QUICK REFERENCE .....</b>	<b>39</b>
<b>6. REGISTER DESCRIPTION .....</b>	<b>42</b>
6.1 Memory Address Pointer (MAP) .....	42
6.2 Chip I.D. and Revision Register (address 01h) (Read Only) .....	42
6.3 Power Control (address 02h) .....	43
6.4 Functional Mode (address 03h) .....	43
6.5 Interface Formats (address 04h) .....	45
6.6 Misc Control (address 05h) .....	46

6.7 Clock Control (address 06h) .....	48
6.8 OMCK/PLL_CLK Ratio (address 07h) (Read Only) .....	49
6.9 Clock Status (address 08h) (Read Only) .....	50
6.10 Volume Transition Control (address 0Dh) .....	51
6.11 Channel Mute (address 0Eh) .....	52
6.12 Volume Control (addresses 0Fh, 10h, 11h, 12h, 13h, 14h, 15h, 16h) .....	53
6.13 Channel Invert (address 17h) .....	53
6.14 Mixing Control Pair 1 (Channels A1 & B1)(address 18h) Mixing Control Pair 2 (Channels A2 & B2)(address 19h) Mixing Control Pair 3 (Channels A3 & B3)(address 1Ah) Mixing Control Pair 4 (Channels A4 & B4)(address 1Bh) .....	53
6.15 ADC Left Channel Gain (address 1Ch) .....	55
6.16 ADC Right Channel Gain (address 1Dh) .....	55
6.17 Interrupt Control (address 1Eh) .....	55
6.18 Interrupt Status (address 20h) (Read Only) .....	56
6.19 Interrupt Mask (address 21h) .....	57
6.20 Interrupt Mode MSB (address 22h) Interrupt Mode LSB (address 23h) .....	57
6.21 Mute Pin Control (address 28h) .....	57
6.22 General-Purpose Pin Control (addresses 29h to 2Fh) .....	58
<b>7. PARAMETER DEFINITIONS .....</b>	<b>60</b>
<b>8. APPENDIX A: EXTERNAL FILTERS .....</b>	<b>61</b>
8.1 ADC Input Filter .....	61
8.2 DAC Output Filter .....	61
<b>9. APPENDIX B: PLL FILTER .....</b>	<b>62</b>
9.1 External Filter Components .....	62
9.1.1 General .....	62
9.1.2 Capacitor Selection .....	62
9.1.3 Circuit Board Layout .....	63
<b>10. APPENDIX C: ADC FILTER PLOTS .....</b>	<b>64</b>
<b>11. APPENDIX D: DAC FILTER PLOTS .....</b>	<b>66</b>
<b>12. PACKAGE DIMENSIONS .....</b>	<b>70</b>
THERMAL CHARACTERISTICS .....	70
<b>13. ORDERING INFORMATION .....</b>	<b>71</b>
<b>14. REFERENCES .....</b>	<b>71</b>
<b>15. REVISION HISTORY .....</b>	<b>72</b>

## LIST OF FIGURES

Figure 1. Serial Audio Port Master Mode Timing .....	11
Figure 2. Serial Audio Port Slave Mode Timing .....	11
Figure 3. Control Port Timing - I <sup>2</sup> C Format .....	12
Figure 4. Control Port Timing - SPI Format .....	13
Figure 5. Typical Connection Diagram .....	18
Figure 6. Typical Connection Diagram using the PLL .....	19
Figure 7. Full-Scale Analog Input .....	20
Figure 8. Full-Scale Output .....	21
Figure 9. ATAPI Block Diagram (x = channel pair 1, 2, 3, 4) .....	22
Figure 10. Clock Generation .....	23
Figure 11. Right-Justified Serial Audio Formats .....	27
Figure 12. I <sup>2</sup> S Serial Audio Formats .....	28
Figure 13. Left-Justified Serial Audio Formats .....	28
Figure 14. One Line Mode #1 Serial Audio Format .....	29
Figure 15. One Line Mode #2 Serial Audio Format .....	29

Figure 16.ADCIN1/ADCIN2 Serial Audio Format .....	30
Figure 17.OLM Configuration #1 .....	31
Figure 18.OLM Configuration #2 .....	32
Figure 19.OLM Configuration #3 .....	33
Figure 20.OLM Configuration #4 .....	34
Figure 21.Control Port Timing in SPI Mode .....	35
Figure 22.Control Port Timing, I <sup>2</sup> C Write .....	36
Figure 23.Control Port Timing, I <sup>2</sup> C Read .....	36
Figure 24.Recommended Analog Input Buffer .....	61
Figure 25.Recommended Analog Output Buffer .....	61
Figure 26.Recommended Layout Example .....	63
Figure 27.Single-Speed Mode Stopband Rejection .....	64
Figure 28.Single-Speed Mode Transition Band .....	64
Figure 29.Single-Speed Mode Transition Band (Detail) .....	64
Figure 30.Single-Speed Mode Passband Ripple .....	64
Figure 31.Double-Speed Mode Stopband Rejection .....	64
Figure 32.Double-Speed Mode Transition Band .....	64
Figure 33.Double-Speed Mode Transition Band (Detail) .....	65
Figure 34.Double-Speed Mode Passband Ripple .....	65
Figure 35.Quad-Speed Mode Stopband Rejection .....	65
Figure 36.Quad-Speed Mode Transition Band .....	65
Figure 37.Quad-Speed Mode Transition Band (Detail) .....	65
Figure 38.Quad-Speed Mode Passband Ripple .....	65
Figure 39.Single-Speed (fast) Stopband Rejection .....	66
Figure 40.Single-Speed (fast) Transition Band .....	66
Figure 41.Single-Speed (fast) Transition Band (detail) .....	66
Figure 42.Single-Speed (fast) Passband Ripple .....	66
Figure 43.Single-Speed (slow) Stopband Rejection .....	66
Figure 44.Single-Speed (slow) Transition Band .....	66
Figure 45.Single-Speed (slow) Transition Band (detail) .....	67
Figure 46.Single-Speed (slow) Passband Ripple .....	67
Figure 47.Double-Speed (fast) Stopband Rejection .....	67
Figure 48.Double-Speed (fast) Transition Band .....	67
Figure 49.Double-Speed (fast) Transition Band (detail) .....	67
Figure 50.Double-Speed (fast) Passband Ripple .....	67
Figure 51.Double-Speed (slow) Stopband Rejection .....	68
Figure 52.Double-Speed (slow) Transition Band .....	68
Figure 53.Double-Speed (slow) Transition Band (detail) .....	68
Figure 54.Double-Speed (slow) Passband Ripple .....	68
Figure 55.Quad-Speed (fast) Stopband Rejection .....	68
Figure 56.Quad-Speed (fast) Transition Band .....	68
Figure 57.Quad-Speed (fast) Transition Band (detail) .....	69
Figure 58.Quad-Speed (fast) Passband Ripple .....	69
Figure 59.Quad-Speed (slow) Stopband Rejection .....	69
Figure 60.Quad-Speed (slow) Transition Band .....	69
Figure 61.Quad-Speed (slow) Transition Band (detail) .....	69
Figure 62.Quad-Speed (slow) Passband Ripple .....	69

---

**LIST OF TABLES**

Table 1. Common OMCK Clock Frequencies .....	24
Table 2. Common PLL Output Clock Frequencies.....	24
Table 3. Slave Mode Clock Ratios .....	25
Table 4. Serial Audio Port Channel Allocations .....	26
Table 5. DAC De-Emphasis .....	44
Table 6. Digital Interface Formats .....	45
Table 7. ADC One-Line Mode.....	45
Table 8. DAC One-Line Mode.....	45
Table 9. RMCK Divider Settings .....	48
Table 10. OMCK Frequency Settings .....	48
Table 11. Master Clock Source Select.....	49
Table 12. PLL Clock Frequency Detection.....	50
Table 13. Example Digital Volume Settings .....	53
Table 14. ATAPI Decode .....	54
Table 15. Example ADC Input Gain Settings .....	55
Table 16. PLL External Component Values .....	62

## 1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and  $T_A = 25^\circ \text{C}$ .)

### SPECIFIED OPERATING CONDITIONS

(AGND=DGND=0, all voltages with respect to ground; OMCK=12.288 MHz; Master Mode)

Parameter	Symbol	Min	Typ	Max	Units	
DC Power Supply	Analog	VA	4.75	5.0	5.25	V
	Digital	VD	3.13	3.3	5.25	V
	Serial Port Interface	VLS	1.8	5.0	5.25	V
	Control Port Interface	VLC	1.8	5.0	5.25	V
Ambient Operating Temperature (power applied)	CS42428-CQZ	$T_A$	-10	-	+70	$^\circ\text{C}$
	CS42428-DQZ	$T_A$	-40	-	+85	$^\circ\text{C}$

### ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units	
DC Power Supply	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	Serial Port Interface	VLS	-0.3	6.0	V
	Control Port Interface	VLC	-0.3	6.0	V
Input Current	(Note 1) $I_{in}$	-	$\pm 10$	mA	
Analog Input Voltage	(Note 2) $V_{IN}$	AGND-0.7	VA+0.7	V	
Digital Input Voltage	Serial Port Interface	$V_{IND-S}$	-0.3	VLS+ 0.4	V
	Control Port Interface	$V_{IND-C}$	-0.3	VLC+ 0.4	V
Ambient Operating Temperature(power applied)	CS42428-CQZ	$T_A$	-20	+85	$^\circ\text{C}$
	CS42428-DQZ	$T_A$	-50	+95	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65	+150	$^\circ\text{C}$	

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

#### Notes:

- Any pin except supplies. Transient currents of up to  $\pm 100$  mA on the analog input pins will not cause SCR latch-up.
- The maximum over/under voltage is limited by the input current.

## ANALOG INPUT CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ ;  $V_A = 5\text{ V}$ ,  $V_D = 3.3\text{ V}$ , Logic “0” = DGND = AGND = 0 V; Logic “1” = VLS = VLC = 5 V; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Full-scale input sine wave, 997 Hz.; PDN\_PLL = 1; OMCK = 12.288 MHz; Single-Speed Mode DAC\_SCLK = 3.072 MHz; Double-Speed Mode DAC\_SCLK = 6.144 MHz; Quad-Speed Mode DAC\_SCLK = 12.288 MHz.)

Parameter	Symbol	CS42428-CQZ			CS42428-DQZ			Unit
		Min	Typ	Max	Min	Typ	Max	
Single-Speed Mode (Fs=48 kHz)								
Dynamic Range	A-weighted	108	114	-	106	114	-	dB
	unweighted	105	111	-	103	111	-	dB
Total Harmonic Distortion + Noise (Note 3)	-1 dB	-	-100	-94	-	-100	-92	dB
	-20 dB	-	-91	-	-	-91	-	dB
	-60 dB	-	-51	-	-	-51	-	dB
Double-Speed Mode (Fs=96 kHz)								
Dynamic Range	A-weighted	108	114	-	106	114	-	dB
	unweighted	105	111	-	103	111	-	dB
	40 kHz bandwidth unweighted	-	108	-	-	108	-	dB
Total Harmonic Distortion + Noise (Note 3)	-1 dB	-	-100	-94	-	-100	-92	dB
	-20 dB	-	-91	-	-	-91	-	dB
	-60 dB	-	-51	-	-	-51	-	dB
	40 kHz bandwidth -1 dB	-	-97	-	-	-97	-	dB
Quad-Speed Mode (Fs=192 kHz)								
Dynamic Range	A-weighted	108	114	-	106	114	-	dB
	unweighted	105	111	-	103	111	-	dB
	40 kHz bandwidth unweighted	-	108	-	-	108	-	dB
Total Harmonic Distortion+ Noise (Note 3)	-1 dB	-	-100	-94	-	-100	-92	dB
	-20 dB	-	-91	-	-	-91	-	dB
	-60 dB	-	-51	-	-	-51	-	dB
	40 kHz bandwidth -1 dB	-	-97	-	-	-97	-	dB
<b>Dynamic Performance for All Modes</b>								
Interchannel Isolation		-	110	-	-	110	-	dB
Interchannel Phase Deviation		-	0.0001	-	-	0.0001	-	Degree
<b>DC Accuracy</b>								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	+/-100	-	-	+/-100	-	ppm/°C
Offset Error	HPF_FREEZE disabled	-	0	-	-	0	-	LSB
	HPF_FREEZE enabled	-	100	-	-	100	-	LSB
<b>Analog Input</b>								
Full-scale Differential Input Voltage		1.05 VA	1.10 VA	1.16 VA	0.99 VA	1.10 VA	1.21 VA	Vpp
Input Impedance (Differential) (Note 4)		17	-	-	17	-	-	kΩ
Common Mode Rejection Ratio	CMRR	-	82	-	-	82	-	dB

### Notes:

3. Referred to the typical full-scale voltage.
4. Measured between AIN+ and AIN-



**A/D DIGITAL FILTER CHARACTERISTICS**

Parameter	Symbol	Min	Typ	Max	Unit
<b>Single-Speed Mode (2 to 50 kHz sample rates)</b>					
Passband (-0.1 dB) (Note 5)		0	-	0.47	Fs
Passband Ripple		-	-	±0.035	dB
Stopband (Note 5)		0.58	-	-	Fs
Stopband Attenuation		-95	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	$t_{gd}$	-	12/Fs	-	s
Group Delay Variation vs. Frequency	$\Delta t_{gd}$	-	-	0.0	µs
<b>Double-Speed Mode (50 to 100 kHz sample rates)</b>					
Passband (-0.1 dB) (Note 5)		0	-	0.45	Fs
Passband Ripple		-	-	±0.035	dB
Stopband (Note 5)		0.68	-	-	Fs
Stopband Attenuation		-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	$t_{gd}$	-	9/Fs	-	s
Group Delay Variation vs. Frequency	$\Delta t_{gd}$	-	-	0.0	µs
<b>Quad-Speed Mode (100 to 192 kHz sample rates)</b>					
Passband (-0.1 dB) (Note 5)		0	-	0.24	Fs
Passband Ripple		-	-	±0.035	dB
Stopband (Note 5)		0.78	-	-	Fs
Stopband Attenuation		-97	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	$t_{gd}$	-	5/Fs	-	s
Group Delay Variation vs. Frequency	$\Delta t_{gd}$	-	-	0.0	µs
<b>High-Pass Filter Characteristics</b>					
Frequency Response -3.0 dB		-	1	-	Hz
-0.13 dB (Note 6)		-	20	-	Hz
Phase Deviation @ 20 Hz (Note 6)		-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Setting Time		-	$10^5/Fs$	-	s

**Notes:**

5. The filter frequency response scales precisely with Fs.
6. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

## ANALOG OUTPUT CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ ;  $V_A = 5\text{ V}$ ,  $V_D = 3.3\text{ V}$ , Logic “0” = DGND =AGND = 0 V; Logic “1” = VLS = VLC = 5V; Measurement Bandwidth 10 Hz to 20 kHz unless otherwise specified.; Full-scale output 997 Hz sine wave, Test load  $R_L = 3\text{ k}\Omega$ ,  $C_L = 30\text{ pF}$ ; PDN\_PLL = 1; OMCK = 12.288 MHz; Single-Speed Mode, DAC\_SCLK = 3.072 MHz; Double-Speed Mode, DAC\_SCLK = 6.144 MHz; Quad-Speed Mode, DAC\_SCLK = 12.288 MHz.)

Parameter	Symbol	CS42428-CQZ			CS42428-DQZ			Unit
		Min	Typ	Max	Min	Typ	Max	
<b>Dynamic performance for all modes</b>								
Dynamic Range (Note 7)								
24-bit A-Weighted		108	114	-	106	114	-	dB
unweighted		105	111	-	103	111	-	dB
16-bit A-Weighted		-	97	-	-	97	-	dB
(Note 8) unweighted		-	94	-	-	94	-	dB
Total Harmonic Distortion + Noise								
24-bit								
0 dB		-	-100	-94	-	-100	-92	dB
-20 dB		-	-91	-	-	-91	-	dB
-60 dB	THD+N	-	-51	-	-	-51	-	dB
16-bit								
0 dB		-	-94	-	-	-94	-	dB
(Note 8) -20 dB		-	-74	-	-	-74	-	dB
-60 dB		-	-34	-	-	-34	-	dB
Idle Channel Noise/Signal-to-Noise Ratio (A-Weighted)		-	114	-	-	114	-	dB
Interchannel Isolation (1 kHz)		-	90	-	-	90	-	dB
<b>Analog Output Characteristics for all modes</b>								
Unloaded Full-Scale Differential Output Voltage	$V_{FS}$	.89 VA	.94 VA	.99 VA	.84 VA	.94 VA	1.04 VA	Vpp
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	300	-	-	300	-	ppm/°C
Output Impedance	$Z_{OUT}$	-	150	-	-	150	-	$\Omega$
AC-Load Resistance	$R_L$	3	-	-	3	-	-	k $\Omega$
Load Capacitance	$C_L$	-	-	30	-	-	30	pF

**Notes:**

7. One-half LSB of triangular PDF dither is added to data.
8. Performance limited by 16-bit quantization noise.

**D/A DIGITAL FILTER CHARACTERISTICS**

Parameter	Fast Roll-Off			Slow Roll-Off			Unit	
	Min	Typ	Max	Min	Typ	Max		
<b>Combined Digital and On-chip Analog Filter Response - Single-Speed Mode - 48 kHz</b>								
Passband (Note 9)	to -0.01 dB corner	0	-	0.4535	0	-	0.4166	Fs
	to -3 dB corner	0	-	0.4998	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz	-0.01	-	+0.01	-0.01	-	+0.01		dB
StopBand	0.5465	-	-	0.5834	-	-		Fs
StopBand Attenuation (Note 10)	90	-	-	64	-	-		dB
Group Delay	-	12/Fs	-	-	6.5/Fs	-		s
Passband Group Delay Deviation 0 - 20 kHz	-	-	±0.41/Fs	-	-	±0.14/Fs		s
De-emphasis Error (Note 11) (Relative to 1 kHz)	Fs = 32 kHz	-	-	±0.23	-	-	±0.23	dB
	Fs = 44.1 kHz	-	-	±0.14	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	-	-	±0.09	dB
<b>Combined Digital and On-chip Analog Filter Response - Double-Speed Mode - 96 kHz</b>								
Passband (Note 9)	to -0.01 dB corner	0	-	0.4166	0	-	0.2083	Fs
	to -3 dB corner	0	-	0.4998	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz	-0.01	-	0.01	-0.01	-	0.01		dB
StopBand	0.5834	-	-	0.7917	-	-		Fs
StopBand Attenuation (Note 10)	80	-	-	70	-	-		dB
Group Delay	-	4.6/Fs	-	-	3.9/Fs	-		s
Passband Group Delay Deviation 0 - 20 kHz	-	-	±0.03/Fs	-	-	±0.01/Fs		s
<b>Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode - 192 kHz</b>								
Passband (Note 9)	to -0.01 dB corner	0	-	0.1046	0	-	0.1042	Fs
	to -3 dB corner	0	-	0.4897	0	-	0.4813	Fs
Frequency Response 10 Hz to 20 kHz	-0.01	-	0.01	-0.01	-	0.01		dB
StopBand	0.6355	-	-	0.8683	-	-		Fs
StopBand Attenuation (Note 10)	90	-	-	75	-	-		dB
Group Delay	-	4.7/Fs	-	-	4.2/Fs	-		s
Passband Group Delay Deviation 0 - 20 kHz	-	-	±0.01/Fs	-	-	±0.01/Fs		s

**Notes:**

9. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 39 to 62) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
10. Single- and Double-Speed Mode Measurement Bandwidth is from stopband to 3 Fs.  
Quad-Speed Mode Measurement Bandwidth is from stopband to 1.34 Fs.
11. De-emphasis is available only in Single-Speed Mode.

## SWITCHING CHARACTERISTICS

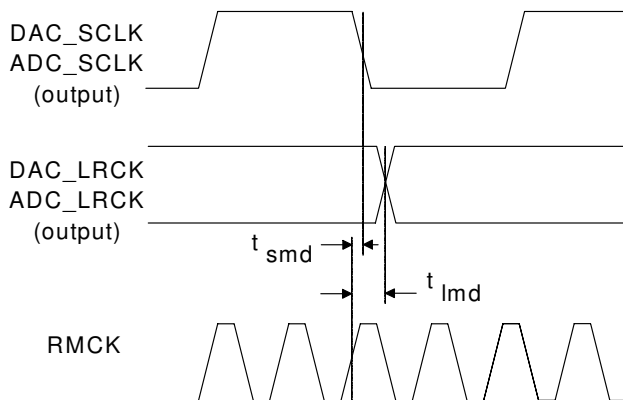
(For CQZ,  $T_A = -10$  to  $+70^\circ\text{C}$ ; For DQZ,  $T_A = -40$  to  $+85^\circ\text{C}$ ;

$V_A = 5\text{V}$ ,  $V_D = V_{LC} = 3.3\text{V}$ ,  $V_{LS} = 1.8\text{V}$  to  $5.25\text{V}$ ; Inputs: Logic 0 = DGND, Logic 1 = V<sub>LS</sub>,  $C_L = 30\text{pF}$ )

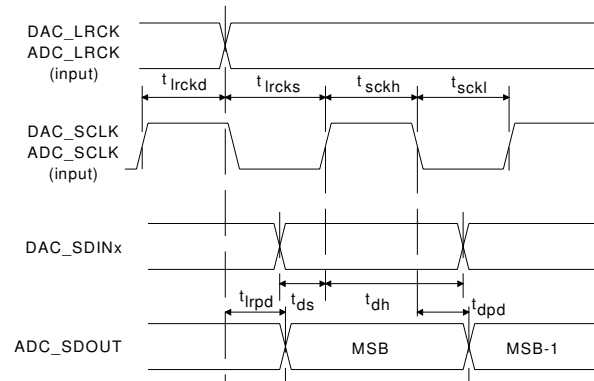
Parameters	Symbol	Min	Typ	Max	Units
$\overline{\text{RST}}$ Pin Low Pulse Width (Note 12)		1	-	-	ms
PLL Clock Recovery Sample Rate Range		30	-	200	kHz
RMCK Output Jitter (Note 14)		-	200	-	ps RMS
RMCK Output Duty Cycle (Note 15)		45	50	55	%
OMCK Frequency (Note 13)		1.024	-	25.600	MHz
OMCK Duty Cycle (Note 13)		40	50	60	%
DAC_SCLK, ADC_SCLK Duty Cycle		45	50	55	%
DAC_LRCK, ADC_LRCK Duty Cycle		45	50	55	%
<b>Master Mode</b>					
RMCK to DAC_SCLK, ADC_SCLK active edge delay	$t_{\text{smd}}$	0	-	15	ns
RMCK to DAC_LRCK, ADC_LRCK delay	$t_{\text{lmd}}$	0	-	15	ns
<b>Slave Mode</b>					
DAC_SCLK, ADC_SCLK Falling Edge to ADC_SDOUT, ADC_SDOUT Output Valid	$t_{\text{dpd}}$		-	(Note 16)	ns
DAC_LRCK, ADC_LRCK Edge to MSB Valid	$t_{\text{l rpd}}$		-	26.5	ns
DAC_SDIN Setup Time Before DAC_SCLK Rising Edge	$t_{\text{ds}}$	10	-	-	ns
DAC_SDIN Hold Time After DAC_SCLK Rising Edge	$t_{\text{dh}}$	30	-	-	ns
DAC_SCLK, ADC_SCLK High Time	$t_{\text{sckh}}$	20	-	-	ns
DAC_SCLK, ADC_SCLK Low Time	$t_{\text{sckl}}$	20	-	-	ns
DAC_SCLK, ADC_SCLK falling to DAC_LRCK, SAI_LRCK Edge	$t_{\text{l rck}}$	-25	-	+25	ns

### Notes:

12. After powering-up the CS42428,  $\overline{\text{RST}}$  should be held low after the power supplies and clocks are settled.
13. See [Table 1 on page 24](#) for suggested OMCK frequencies
14. Limit the loading on RMCK to 1 CMOS load if operating above 24.576 MHz.
15. Not valid when RMCK\_DIV in “Clock Control (address 06h)” on [page 48](#) is set to Multiply by 2.
16. 76.5 ns for Single-Speed and Double-Speed modes, 23 ns for Quad-Speed Mode.



**Figure 1. Serial Audio Port Master Mode Timing**



**Figure 2. Serial Audio Port Slave Mode Timing**

## SWITCHING CHARACTERISTICS - CONTROL PORT - I<sup>2</sup>C FORMAT

(For CQZ, T<sub>A</sub> = -10 to +70° C; For DQZ, T<sub>A</sub> = -40 to +85° C; V<sub>A</sub> = 5 V, V<sub>D</sub> = V<sub>LS</sub> = 3.3 V; V<sub>LC</sub> = 1.8 V to 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, C<sub>L</sub> = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f <sub>scl</sub>	-	100	kHz
RST Rising Edge to Start	t <sub>irs</sub>	500	-	ns
Bus Free Time Between Transmissions	t <sub>buf</sub>	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t <sub>hdst</sub>	4.0	-	μs
Clock Low time	t <sub>low</sub>	4.7	-	μs
Clock High Time	t <sub>high</sub>	4.0	-	μs
Setup Time for Repeated Start Condition	t <sub>sust</sub>	4.7	-	μs
SDA Hold Time from SCL Falling	t <sub>hdd</sub>	0	-	μs
SDA Setup time to SCL Rising	t <sub>sud</sub>	250	-	ns
Rise Time of SCL and SDA	t <sub>rc</sub>	-	1	μs
Fall Time SCL and SDA	t <sub>fc</sub>	-	300	ns
Setup Time for Stop Condition	t <sub>susp</sub>	4.7	-	μs
Acknowledge Delay from SCL Falling	t <sub>ack</sub>	-	(Note 19)	ns

### Notes:

17. Data must be held for sufficient time to bridge the transition time, t<sub>fc</sub>, of SCL.
18. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.
19.  $\frac{15}{256 \times F_s}$  for Single-Speed Mode,  $\frac{15}{128 \times F_s}$  for Double-Speed Mode,  $\frac{15}{64 \times F_s}$  for Quad-Speed Mode

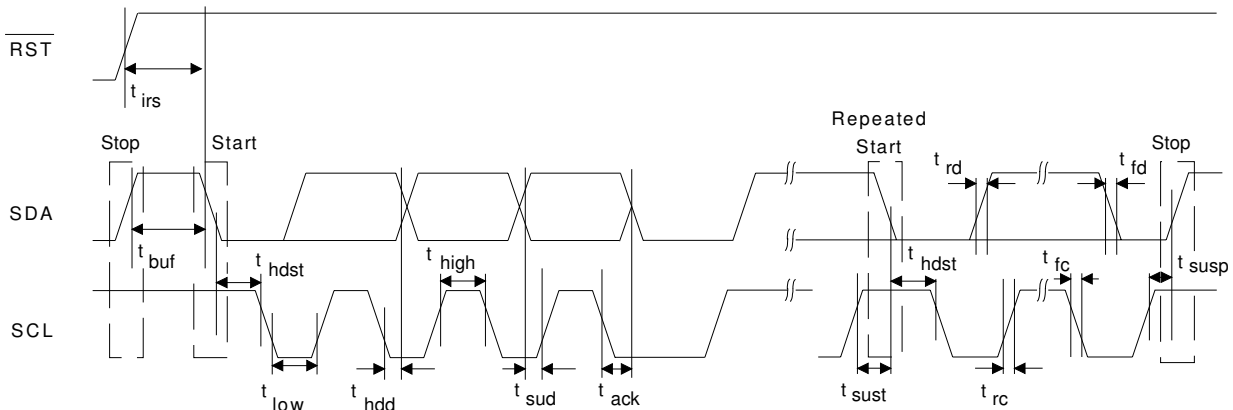


Figure 3. Control Port Timing - I<sup>2</sup>C Format

## SWITCHING CHARACTERISTICS - CONTROL PORT - SPI™ FORMAT

(For CQZ,  $T_A = -10$  to  $+70^\circ\text{C}$ ; For DQZ,  $T_A = -40$  to  $+85^\circ\text{C}$ ;  $V_A = 5\text{ V}$ ,  $V_D = V_{LS} = 3.3\text{ V}$ ;  $V_{LC} = 1.8\text{ V}$  to  $5.25\text{ V}$ ; Inputs: Logic 0 = DGND, Logic 1 = VLC,  $C_L = 30\text{ pF}$ )

Parameter	Symbol	Min	Typ	Max	Units
CCLK Clock Frequency	$f_{sck}$	0	-	6.0	MHz
$\overline{\text{CS}}$ High Time Between Transmissions	$t_{csh}$	1.0	-	-	$\mu\text{s}$
$\overline{\text{CS}}$ Falling to CCLK Edge	$t_{css}$	20	-	-	ns
CCLK Low Time	$t_{scl}$	66	-	-	ns
CCLK High Time	$t_{sch}$	66	-	-	ns
CDIN to CCLK Rising Setup Time	$t_{dsu}$	40	-	-	ns
CCLK Rising to DATA Hold Time	$t_{dh}$	15	-	-	ns
CCLK Falling to CDOUT Stable	$t_{pd}$	-	-	50	ns
Rise Time of CDOUT	$t_{r1}$	-	-	25	ns
Fall Time of CDOUT	$t_{f1}$	-	-	25	ns
Rise Time of CCLK and CDIN	$t_{r2}$	-	-	100	ns
Fall Time of CCLK and CDIN	$t_{f2}$	-	-	100	ns

### Notes:

20. Data must be held for sufficient time to bridge the transition time of CCLK.

21. For  $f_{sck} < 1\text{ MHz}$ .

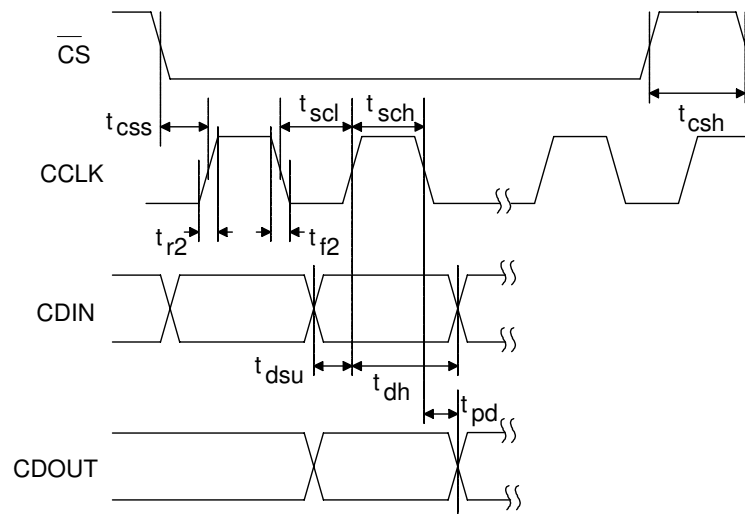


Figure 4. Control Port Timing - SPI Format

## DC ELECTRICAL CHARACTERISTICS

(T<sub>A</sub> = 25° C; AGND=DGND=0, all voltages with respect to ground; OMCK=12.288 MHz; Master Mode)

Parameter	Symbol	Min	Typ	Max	Units	
Power Supply Current (Note 22)	normal operation, V <sub>A</sub> = 5 V	I <sub>A</sub>	-	75	-	mA
	VD = 5 V	I <sub>D</sub>	-	85	-	mA
	VD = 3.3 V	I <sub>D</sub>	-	51	-	mA
	Interface current, V <sub>LC</sub> =5 V (Note 23)	I <sub>LC</sub>	-	250	-	μA
	V <sub>LS</sub> =5 V	I <sub>LS</sub>	-	13	-	mA
	power-down state (all supplies) (Note 24)	I <sub>pd</sub>	-	250	-	μA
Power Consumption (Note 22)	VA=5 V, VD=VLS=VLC=3.3 V		-	587	650	mW
	normal operation		-	1.25	-	mW
	power-down (Note 24)		-	866	960	mW
	VA=5 V, VD=VLS=VLC=5 V		-	1.25	-	mW
Power Supply Rejection Ratio (Note 25)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB
VQ Nominal Voltage		-	2.7	-	V	
VQ Output Impedance		-	50	-	kΩ	
VQ Maximum allowable DC current		-	0.01	-	mA	
FILT+ Nominal Voltage		-	5.0	-	V	
FILT+ Output Impedance		-	35	-	kΩ	
FILT+ Maximum allowable DC current		-	0.01	-	mA	

### Notes:

22. Current consumption increases with increasing FS and increasing OMCK. Max values are based on highest FS and highest OMCK. Variance between speed modes is negligible.
23. I<sub>LC</sub> measured with no external loading on the SDA pin.
24. Power-Down Mode is defined as  $\overline{RST}$  pin = Low with all clock and data lines held static.
25. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 5.

## DIGITAL INTERFACE CHARACTERISTICS

(For CQZ,  $T_A = +25^\circ\text{C}$ ; For DQZ,  $T_A = -40$  to  $+85^\circ\text{C}$ )

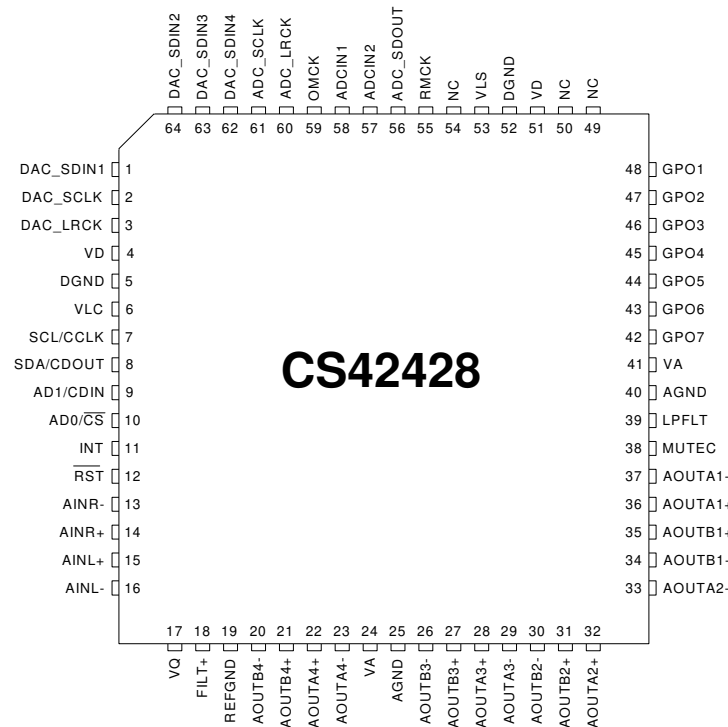
Parameters (Note 26)	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Serial Port	0.7xVLS	-	-	V
	Control Port	0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	-	-	0.2xVLS	V
	Control Port	-	-	0.2xVLC	V
High-Level Output Voltage at $I_o=2\text{ mA}$	(Note 27) Serial Port	VLS-1.0	-	-	V
	Control Port	VLC-1.0	-	-	V
	MUTE $\overline{\text{C}}$ , GPO $\overline{\text{x}}$	VA-1.0	-	-	V
Low-Level Output Voltage at $I_o=2\text{ mA}$	(Note 27)	-	-	0.4	V
Serial Port, Control Port, MUTE $\overline{\text{C}}$ , GPO $\overline{\text{x}}$	$V_{OL}$	-	-	0.4	V
Input Leakage Current	$I_{in}$	-	-	$\pm 10$	$\mu\text{A}$
Input Capacitance		-	8	-	pF
MUTE $\overline{\text{C}}$ Drive Current		-	3	-	mA

### Notes:

26. Serial Port signals include: RMCK, OMCK, ADC\_SCLK, ADC\_LRCK, DAC\_SCLK, DAC\_LRCK, ADC\_SDO $\overline{\text{U}}$ T, DAC\_SDIN1-4, ADCIN1/2  
 Control Port signals include: SCL/CCLK, SDA/CDOUT, AD0/ $\overline{\text{CS}}$ , AD1/CDIN, INT,  $\overline{\text{RST}}$
27. When operating RMCK above 24.576 MHz, limit the loading on the signal to 1 CMOS load.



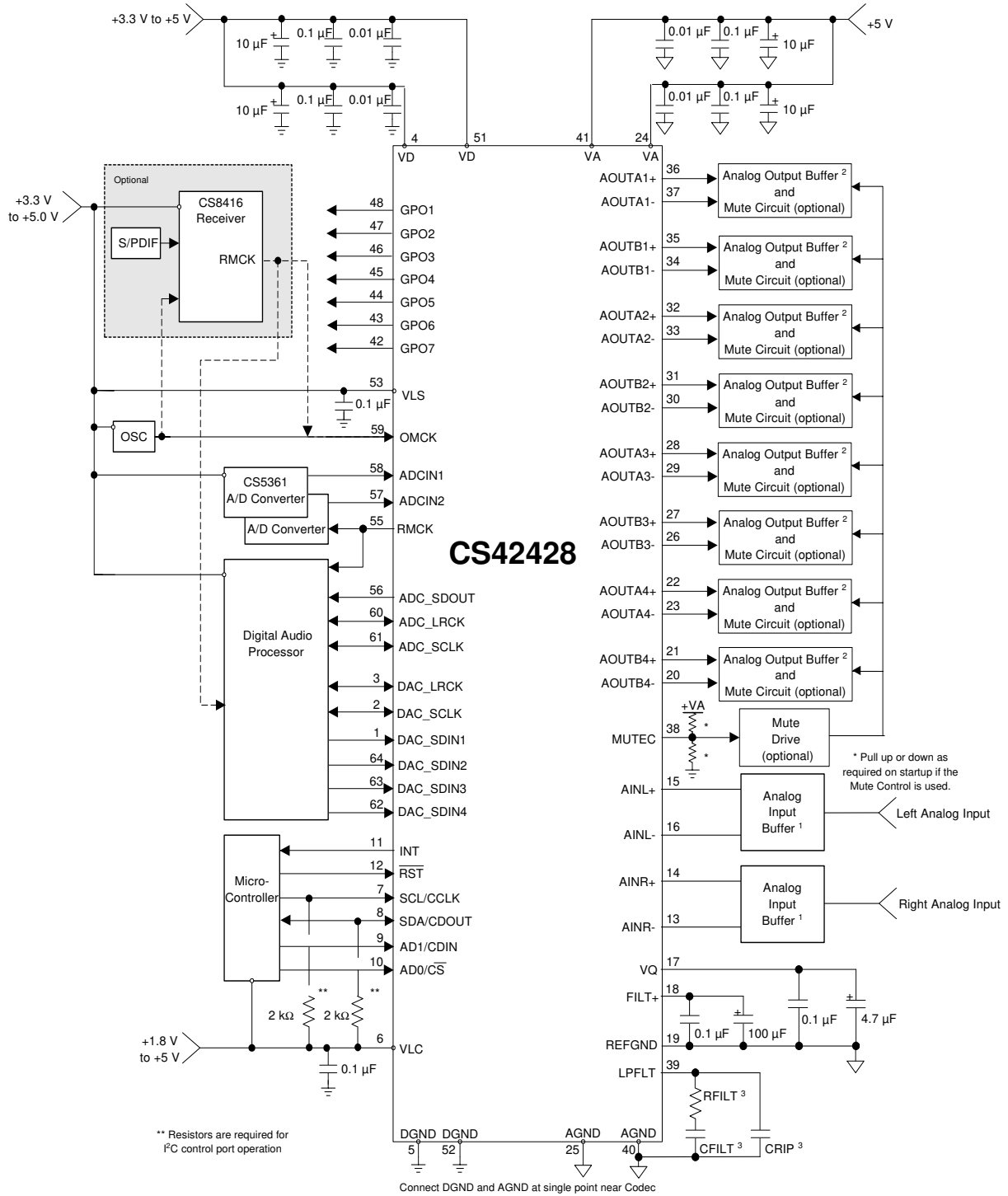
## 2. PIN DESCRIPTIONS



Pin Name	#	Pin Description
DAC_SDIN1	1	
DAC_SDIN2	64	<b>DAC Serial Audio Data Input (Input)</b> - Input for two's complement serial audio data.
DAC_SDIN3	63	
DAC_SDIN4	62	
DAC_SCLK	2	
DAC_LRCK	3	<b>DAC Left Right Clock (Input/Output)</b> - Determines which channel, Left or Right, is currently active on the DAC serial audio data line.
VD	4 51	<b>Digital Power (Input)</b> - Positive power supply for the digital section.
DGND	5 52	<b>Digital Ground (Input)</b> - Ground reference. Should be connected to digital ground.
VLC	6	<b>Control Port Power (Input)</b> - Determines the required signal level for the control port.
SCL/CCLK	7	<b>Serial Control Port Clock (Input)</b> - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I <sup>2</sup> C mode as shown in the Typical Connection Diagram.
SDA/CDOUT	8	<b>Serial Control Data (Input/Output)</b> - SDA is a data I/O line in I <sup>2</sup> C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	9	<b>Address Bit 1 (I<sup>2</sup>C)/Serial Control Data (SPI) (Input)</b> - AD1 is a chip address pin in I <sup>2</sup> C mode; CDIN is the input data line for the control port interface in SPI mode.
AD0/ $\overline{\text{CS}}$	10	<b>Address Bit 0 (I<sup>2</sup>C)/Control Port Chip Select (SPI) (Input)</b> - AD0 is a chip address pin in I <sup>2</sup> C mode; $\overline{\text{CS}}$ is the chip select signal in SPI mode.
INT	11	<b>Interrupt (Output)</b> - The CS42428 will generate an interrupt condition as per the Interrupt Mask register. See " <a href="#">Interrupts</a> " on page 37 for more details.

$\overline{\text{RST}}$	12	<b>Reset (Input)</b> - The device enters a low power mode and all internal registers are reset to their default settings when low.
AINR- AINR+	13 14	<b>Differential Right Channel Analog Input (Input)</b> - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
AINL+ AINL-	15 16	<b>Differential Left Channel Analog Input (Input)</b> - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins.
VQ	17	<b>Quiescent Voltage (Output)</b> - Filter connection for internal quiescent reference voltage.
FILT+	18	<b>Positive Voltage Reference (Output)</b> - Positive reference voltage for the internal sampling circuits.
REFGND	19	<b>Reference Ground (Input)</b> - Ground reference for the internal sampling circuits.
AOUTA1 +,- AOUTB1 +,- AOUTA2 +,- AOUTB2 +,- AOUTA3 +,- AOUTB3 +,- AOUTA4 +,- AOUTB4 +,-	36,37 35,34 32,33 31,30 28,29 27,26 22,23 21,20	<b>Differential Analog Output (Output)</b> - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VA	24 41	<b>Analog Power (Input)</b> - Positive power supply for the analog section.
AGND	25 40	<b>Analog Ground (Input)</b> - Ground reference. Should be connected to analog ground.
MUTE <sub>C</sub>	38	<b>Mute Control (Output)</b> - The Mute Control pin outputs high impedance following an initial power-on condition or whenever the PDN bit is set to a '1', forcing the codec into power-down mode. The signal will remain in a high impedance state as long as the part is in power-down mode. The Mute Control pin goes to the selected "active" state during reset, muting, or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
LPFLT	39	<b>PLL Loop Filter (Output)</b> - An RC network should be connected between this pin and ground.
GPO7 GPO6 GPO5 GPO4 GPO3 GPO2 GPO1	42 43 44 45 46 47 48	<b>General Purpose Output (Output)</b> - These pins can be configured as general purpose output pins, an ADC overflow interrupt or Mute Control outputs according to the General Purpose Pin Control registers.
VLS	53	<b>Serial Port Interface Power (Input)</b> - Determines the required signal level for the serial port interfaces.
RMCK	55	<b>Recovered Master Clock (Output)</b> - Recovered master clock output from the External Clock Reference (OMCK, pin 59) or the PLL which is locked to the incoming ADC_LRCK.
ADC_SDO <sub>UT</sub>	56	<b>ADC Serial Data Output (Output)</b> - Output for two's complement serial audio PCM data from the output of the internal and external ADCs.
ADCIN1 ADCIN2	58 57	<b>External ADC Serial Input (Input)</b> - The CS42428 provides for up to two external stereo analog to digital converter inputs to provide a maximum of six channels on one serial data output line when the CS42428 is placed in One-Line Mode.
OMCK	59	<b>External Reference Clock (Input)</b> - External clock reference that must be within the ranges specified in the register " <a href="#">OMCK Frequency (OMCK Freqx)</a> " on page 48.
ADC_LRCK	60	<b>ADC Left/Right Clock (Input/Output)</b> - Determines which channel, Left or Right, is currently active on the ADC serial audio data line.
ADC_SCLK	61	<b>ADC Serial Clock (Input/Output)</b> - Serial clock for the ADC serial audio interface.

### 3. TYPICAL CONNECTION DIAGRAMS



1. See the ADC Input Filter section in the Appendix.  
 2. See the DAC Output Filter section in the Appendix.  
 3. See the PLL Filter section in the Appendix.

Figure 5. Typical Connection Diagram

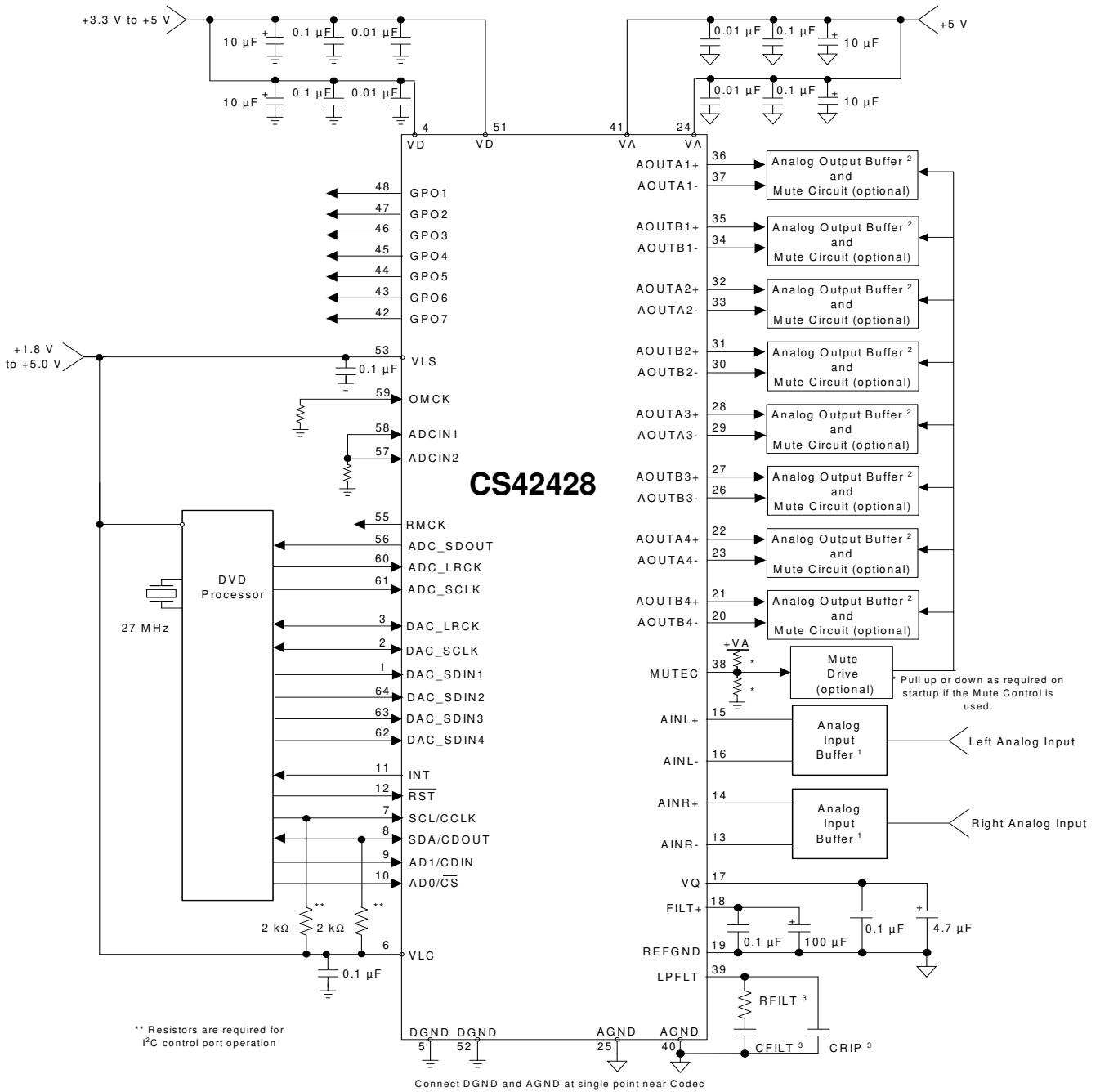


Figure 6. Typical Connection Diagram using the PLL

## 4. APPLICATIONS

### 4.1 Overview

The CS42428 is a highly integrated mixed-signal 24-bit audio codec comprised of 2 analog-to-digital converters (ADC), implemented using multi-bit delta-sigma techniques, and 8 digital-to-analog converters (DAC). Other functions integrated within the codec include independent digital volume controls for each DAC, digital de-emphasis filters for DAC, digital gain control for ADC channels, ADC high-pass filters, and an on-chip voltage reference. All serial data is transmitted through one configurable serial audio interface for the ADC with enhanced one-line modes of operation, allowing up to 6 channels of serial audio data on one data line. All functions are configured through a serial control port operable in SPI mode or in I<sup>2</sup>C mode. [5](#) and [6](#) show the recommended connections for the CS42428.

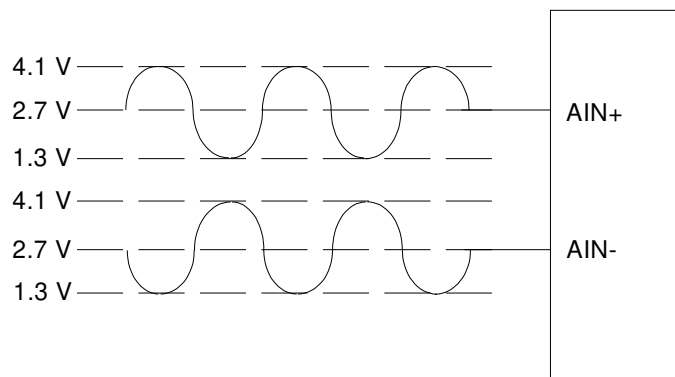
The CS42428 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the FM bits in register “[Functional Mode \(address 03h\)](#)” on [page 43](#). Single-Speed Mode (SSM) supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed Mode (DSM) supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed Mode (QSM) supports input sample rates up to 192 kHz and uses an oversampling ratio of 32x.

Using the integrated PLL, a low-jitter clock is recovered from the ADC LRCK input signal. The recovered clock or an externally supplied clock attached to the OMCK pin can be used as the System Clock.

### 4.2 Analog Inputs

#### 4.2.1 Line-Level Inputs

AINR+, AINR-, AINL+, and AINL- are the line-level differential analog inputs. The analog signal must be externally biased to V<sub>Q</sub>, approximately 2.7 V, before being applied to these inputs. The level of the signal can be adjusted for the left and right ADC independently through the ADC Left and Right Channel Gain Control Registers on [page 55](#). The ADC output data is in two’s complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFFH or 800000H, respectively and cause the ADC Overflow bit in the register “[Interrupt Status \(address 20h\) \(Read Only\)](#)” on [page 56](#) to be set to a ‘1’. The GPO pins may also be configured to indicate an overflow condition has occurred in the ADC. See “[General-Purpose Pin Control \(addresses 29h to 2Fh\)](#)” on [page 58](#) for proper configuration. [Figure 7](#) shows the full-scale analog input levels. See “[ADC Input Filter](#)” on [page 61](#) for a recommended input buffer.



$$\text{Full-Scale Input Level} = (\text{AIN}+) - (\text{AIN}-) = 5.6 \text{ Vpp}$$

**Figure 7. Full-Scale Analog Input**

### 4.2.2 High-Pass Filter and DC Offset Calibration

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. The high-pass filter can be independently enabled and disabled. If the HPF\_Freeze bit is set during normal operation, the current value of the DC offset for the corresponding channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS42428 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

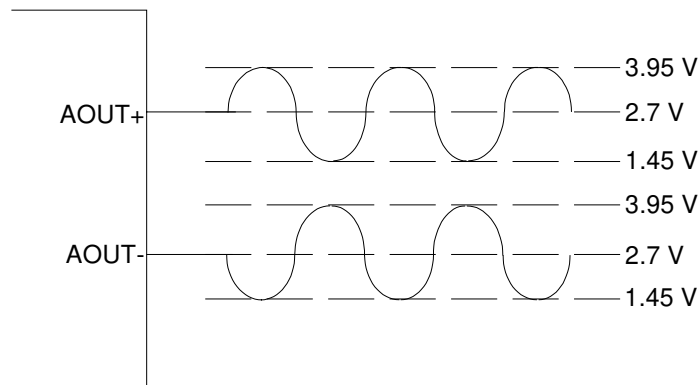
The high-pass filters are controlled using the HPF\_FREEZE bit in the register [“Misc Control \(address 05h\)”](#) on page 46.

## 4.3 Analog Outputs

### 4.3.1 Line-Level Outputs and Filtering

The CS42428 contains on-chip buffer amplifiers capable of producing line-level differential outputs. These amplifiers are biased to a quiescent DC level of approximately V<sub>Q</sub>.

The delta-sigma conversion process produces high-frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low-pass filter. See [“DAC Output Filter”](#) on page 61 for a recommended output buffer. This filter configuration accounts for the normally differing AC loads on the AOUT+ and AOUT- differential output pins. It also shows an AC coupling configuration which minimizes the number of required AC coupling capacitors. [Figure 8](#) shows the full-scale analog output levels.



Full-Scale Output Level= (AIN+) - (AIN-)= 5 V<sub>pp</sub>

**Figure 8. Full-Scale Output**

### 4.3.2 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS42428 incorporates selectable interpolation filters for each mode of operation. A “fast” and a “slow” roll-off filter is available in Single-, Double-, and Quad-Speed Modes. These filters have been designed to accommodate a variety of musical tastes and styles. The FILT\_SEL bit found in the register [“Misc Control \(address 05h\)”](#) on page 46 selects which filter is used. Filter response plots can be found in [Figures 39 to 62](#).

### 4.3.3 Digital Volume and Mute Control

Each DAC's output level is controlled via the Volume Control registers operating over the range of 0 to -127 dB attenuation with 0.5 dB resolution. See [“Volume Control \(addresses 0Fh, 10h, 11h, 12h, 13h, 14h, 15h, 16h\)” on page 53](#). Volume control changes are programmable to ramp in increments of 0.125 dB at the rate controlled by the SZC[1:0] bits in the Digital Volume Control register. See [“Volume Transition Control \(address 0Dh\)” on page 51](#).

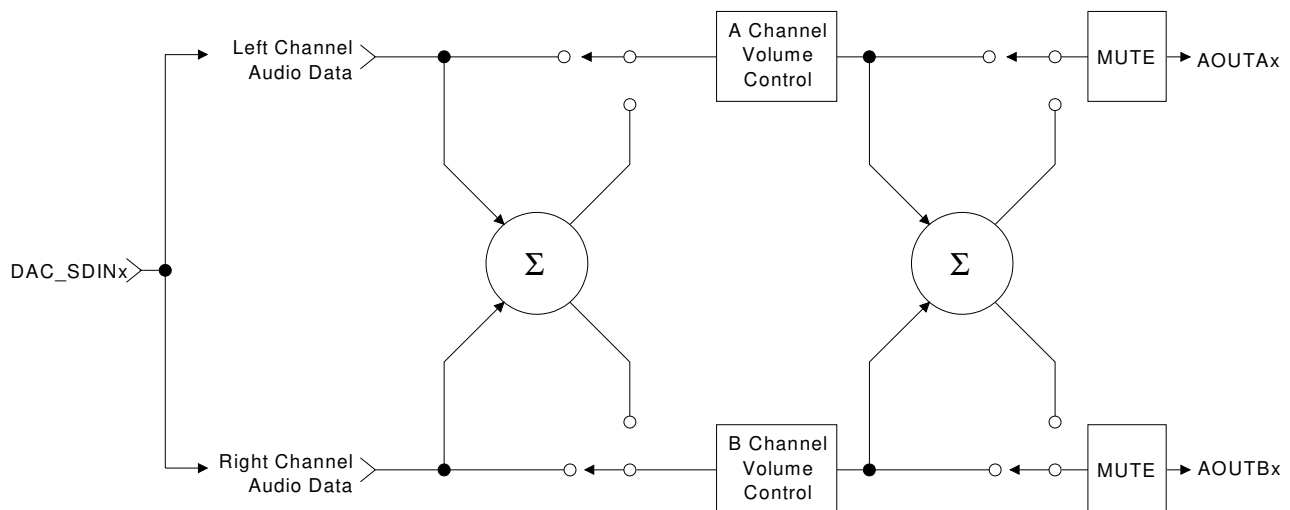
Each output can be independently muted via mute control bits in the register [“Channel Mute \(address 0Eh\)” on page 52](#). When enabled, each XX\_MUTE bit attenuates the corresponding DAC to its maximum value (-127 dB). When the XX\_MUTE bit is disabled, the corresponding DAC returns to the attenuation level set in the Volume Control register. The attenuation is ramped up and down at the rate specified by the SZC[1:0] bits.

The Mute Control pin, MUTE<sub>C</sub>, is typically connected to an external mute control circuit. The Mute Control pin outputs high impedance during Power-Up or in Power-Down Mode by setting the PDN bit in the register [“Power Control \(address 02h\)” on page 43](#) to a ‘1’. Once out of Power-Down Mode, the pin can be controlled by the user via the control port, or automatically asserted high when zero data is present on all DAC inputs, or when serial port clock errors are present. To prevent large transients on the output, it is desirable to mute the DAC outputs before the Mute Control pin is asserted. Please see the MUTE<sub>C</sub> pin in the Pin Descriptions section for more information.

Each of the GPO1-GPO7 can be programmed to provide a hardware MUTE signal to individual circuits. Each pin can be programmed as an output, with specific muting capabilities as defined by the function bits in the register [“General-Purpose Pin Control \(addresses 29h to 2Fh\)” on page 58](#).

### 4.3.4 ATAPI Specification

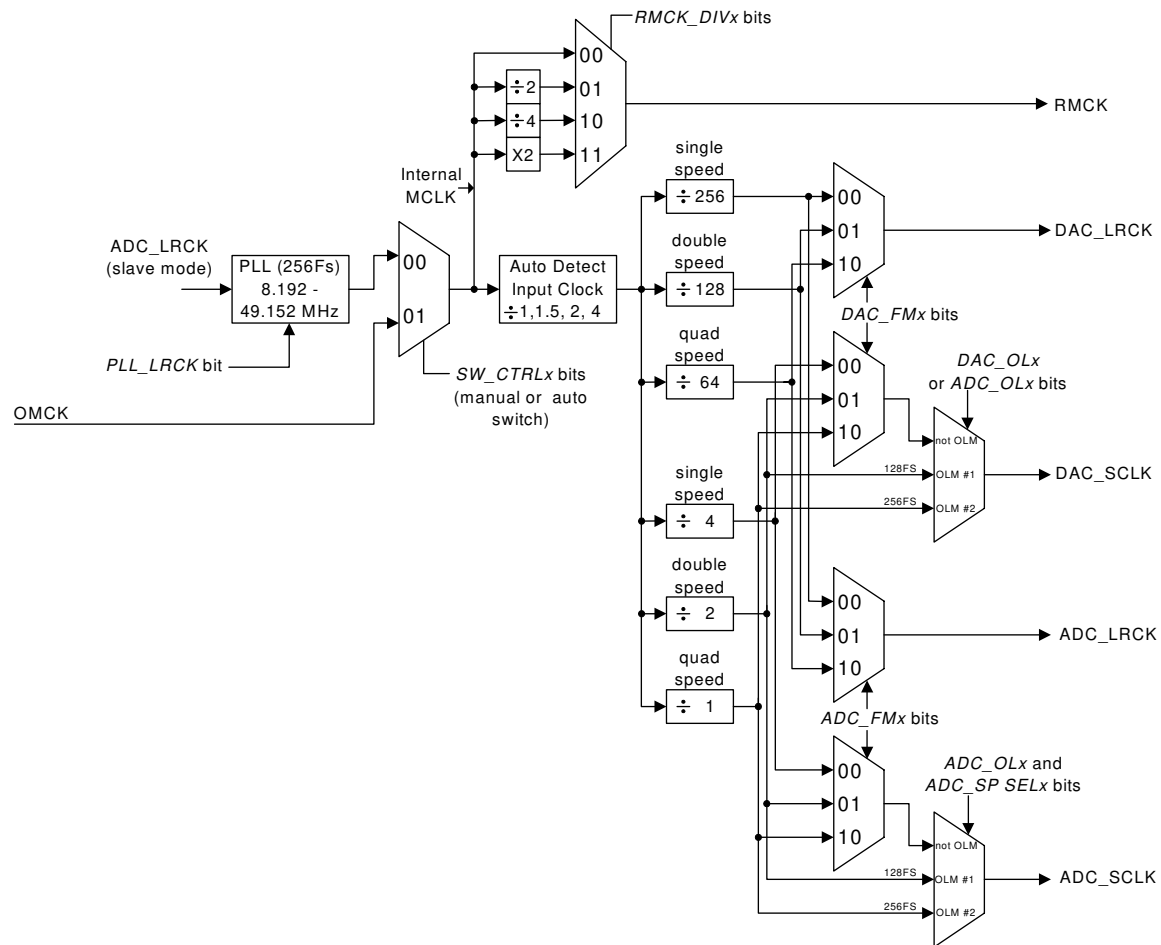
The CS42428 implements the channel-mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to [Table 14 on page 54](#) and [Figure 9](#) for additional information.



**Figure 9. ATAPI Block Diagram (x = channel pair 1, 2, 3, 4)**

## 4.4 Clock Generation

The clock generation for the CS42428 is shown in the figure below. The internal MCLK is derived from the output of the PLL or a master clock source attached to OMCK. The mux selection is controlled by the SW\_CTRLx bits and can be configured to manual switch mode only, or automatically switch on loss of PLL lock to the other source input.



**Figure 10. Clock Generation**

### 4.4.1 PLL and Jitter Attenuation

The PLL can be configured to lock onto the incoming ADC\_LRCK signal from the ADC Serial Port and generate the required internal master clock frequency. There are some applications where low jitter in the recovered clock, presented on the RMCK pin, is important. For this reason, the PLL has been designed to have good jitter-attenuation characteristics. By setting the PLL\_LRCK bit to a '1' in the register [“Clock Control \(address 06h\)” on page 48](#), the PLL will lock to the incoming ADC\_LRCK and generate an output master clock (RMCK) of 256Fs. [Table 2](#) shows the output of the PLL with typical input Fs values for ADC\_LRCK.

See [“Appendix B: PLL Filter” on page 62](#) for more information concerning PLL operation, required filter components, optimal layout guidelines, and jitter-attenuation characteristics.



#### 4.4.2 OMCK System Clock Mode

A special clock-switching mode is available that allows the clock that is input through the OMCK pin to be used as the internal master clock. This feature is controlled by the SW\_CTRLx bits in register “Clock Control (address 06h)” on page 48. An advanced auto-switching mode is also implemented to maintain master clock functionality. The clock auto-switching mode allows the clock input through OMCK to be used as a clock in the system without any disruption when the PLL loses lock, for example, when the LRCK is removed from ADC\_LRCK. This clock-switching is done glitch-free. A clock adhering to the specifications detailed in the Switching Characteristics table on page 11 must be applied to the OMCK pin at all times that the FRC\_PLL\_LK bit is set to ‘0’ (See “Force PLL Lock (FRC\_PLL\_LK)” on page 49).

Sample Rate (kHz)	OMCK (MHz)								
	Single-Speed (4 to 50 kHz)			Double-Speed (50 to 100 kHz)			Quad-Speed (100 to 192 kHz)		
	256x	384x	512x	128x	192x	256x	64x	96x	128x
48	12.2880	18.4320	24.5760	-	-	-	-	-	-
96	-	-	-	12.2880	18.4320	24.5760	-	-	-
192	-	-	-	-	-	-	12.2880	18.4320	24.5760

Table 1. Common OMCK Clock Frequencies

#### 4.4.3 Master Mode

In Master Mode, the serial interface timings are derived from an external clock attached to OMCK or from the output of the PLL with an input reference to the ADC\_LRCK input from the ADC serial port. The DAC Serial Port and ADC Serial Port can both be masters only when OMCK is used as the clock source. When using the PLL output, the ADC Serial Port must be slave and the DAC Serial Port can operate in Master Mode. Master clock selection and operation is configured with the SW\_CTRL1:0 bits in the Clock Control Register (See “Clock Control (address 06h)” on page 48).

#### 4.4.4 Slave Mode

In Slave Mode, DAC\_LRCK, DAC\_SCLK and/or ADC\_LRCK and ADC\_SCLK operate as inputs. The Left/Right clock signal must be equal to the sample rate, Fs, and must be synchronously derived from the supplied master clock, OMCK, or must be synchronous to the supplied ADC\_LRCK used as the input to the PLL. In this latter scenario, the PLL output becomes the internal master clock. The supported PLL output frequencies are shown in Table 2.

Sample Rate (kHz)	PLL Output (MHz)		
	Single-Speed (4 to 50kHz)	Double-Speed (50 to 100kHz)	Quad-Speed (100 to 192kHz)
	256x	256x	256x
32	8.1920	-	-
44.1	11.2896	-	-
48	12.2880	-	-
64	-	16.3840	-
88.2	-	22.5792	-
96	-	24.5760	-
176.4	-	-	45.1584
192	-	-	49.1520

The serial bit clock, DAC\_SCLK and/or ADC\_SCLK, must be synchronous to the corresponding DAC\_LRCK/ADC\_LRCK and be equal to 128x, 64x, 48x or 32x Fs, depending on the interface format selected and desired speed mode.

When the device is clocked from OMCK, the frequency of OMCK must be at least twice the frequency of the fastest Slave Mode, SCLK. For example, if both serial ports are in Slave Mode with one SCLK running at 32x Fs and the other at 64x Fs, the slowest OMCK signal that can be used to clock the device is 128x Fs.

When either serial port is in Slave Mode, its respective LRCK signal must be present for proper device operation.

In Slave Mode, One-Line Mode #1 is supported; One-Line Mode #2 is not.

The sample rate to OMCK ratios and OMCK frequency requirements for Slave Mode operation are shown in [Table 1](#). Refer to [Table 3](#) for required clock ratios.

	Single-Speed	Double-Speed	Quad-Speed	One-Line Mode #1
OMCK/LRCK Ratio	256x, 384x, 512x	128x, 192x, 256x	64x, 96x, 128x	256x
SCLK/LRCK Ratio	32x, 48x, 64x, 128x	32x, 48x, 64x	32x, 48x, 64x	128x

**Table 3. Slave Mode Clock Ratios**

## 4.5 Digital Interfaces

### 4.5.1 Serial Audio Interface Signals

The CS42428 interfaces to an external Digital Audio Processor via two independent serial ports, the DAC serial port, DAC\_SP, and the ADC serial port, ADC\_SP. The digital output of the internal ADCs use the ADC\_SDOUT pin and can be configured to use either the ADC or DAC serial port timings. These configuration bits and the selection of Single-, Double- or Quad-Speed Mode for DAC\_SP and ADC\_SP are found in register [“Functional Mode \(address 03h\)”](#) on page 43.

The serial interface clocks, ADC\_SCLK for ADC\_SP and DAC\_SCLK for DAC\_SP, are used for transmitting and receiving audio data. Either ADC\_SCLK or DAC\_SCLK can be generated by the CS42428 (Master Mode), or it can be input from an external source (Slave Mode). Master or Slave Mode selection is made using bits DAC\_SP M/S and ADC\_SP M/S in register [“Misc Control \(address 05h\)”](#) on page 46.

The Left/Right clock (ADC\_LRCK or DAC\_LRCK) is used to indicate left and right data frames and the start of a new sample period. It may be an output of the CS42428 (Master Mode), or it may be generated by an external source (Slave Mode). As described in later sections, particular modes of operation do allow the sample rate, Fs, of the ADC\_SP and the DAC\_SP to be different, but must be multiples of each other.

The serial data interface format selection (Left/Right-Justified, I<sup>2</sup>S or One-Line Mode) for the ADC serial port data out pin, ADC\_SDOUT, and the DAC input pins, DAC\_SDIN1:4, is configured using the appropriate bits in the register [“Interface Formats \(address 04h\)”](#) on page 45. The serial audio data is presented in two's complement binary form with the MSB first in all formats.

DAC\_SDIN1, DAC\_SDIN2, DAC\_SDIN3 and DAC\_SDIN4 are the serial data input pins supplying the internal DAC. ADC\_SDOUT, the ADC data output pin, carries data from the two internal 24-bit ADCs and, when configured for one-line mode, up to four additional ADC channels attached externally to the signals ADCIN1 and ADCIN2 (typically two CS5361 stereo ADCs). When operated in One-Line Mode, 6 channels of DAC data are input on DAC\_SDIN1, two additional DAC channels on DAC\_SDIN4, and 6 channels of ADC data are output on ADC\_SDOUT. [Table 4 on page 26](#) outlines the serial port channel allocations.