Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CS42432

108 dB, 192 kHz 4-In, 6-Out TDM CODEC

FEATURES

- Four 24-bit A/D, Six 24-bit D/A Converters
- ADC Dynamic Range
  - 105 dB Differential
  - 102 dB Single-Ended
- DAC Dynamic Range
  - 108 dB Differential
  - 105 dB Single-Ended
- ADC/DAC THD+N
  - -98 dB Differential
  - -95 dB Single-Ended
- Compatible with Industry-Standard Time Division Multiplexed (TDM) Serial Interface
- DAC Sampling Rates up to 192 kHz
- ADC Sampling Rates up to 96 kHz
- Programmable ADC High-Pass Filter for DC Offset Calibration
- Logarithmic Digital Volume Control
- Hardware Mode or Software I²C™ & SPI™
- Supports Logic Levels Between 5 V and 1.8 V

GENERAL DESCRIPTION

The CS42432 CODEC provides four multi-bit analog-to-digital and six multi-bit digital-to-analog delta-sigma converters. The CODEC is capable of operation with either differential or single-ended inputs and outputs, in a 52-pin MQFP package.

Four fully differential, or single-ended, inputs are available on stereo ADC1 and ADC2. Digital volume control is provided for each ADC channel, with selectable overflow detection.

All six DAC channels provide digital volume control and can operate with differential or single-ended outputs.

An auxiliary serial input is available for an additional two channels of PCM data.

The CS42432 is available in a 52-pin MQFP package in Commercial (-10°C to +70°C) and Automotive (-40°C to +105°C) grades. The CDB42438 Customer Demonstration Board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 58 for complete ordering information.

The CS42432 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, and automotive audio systems.

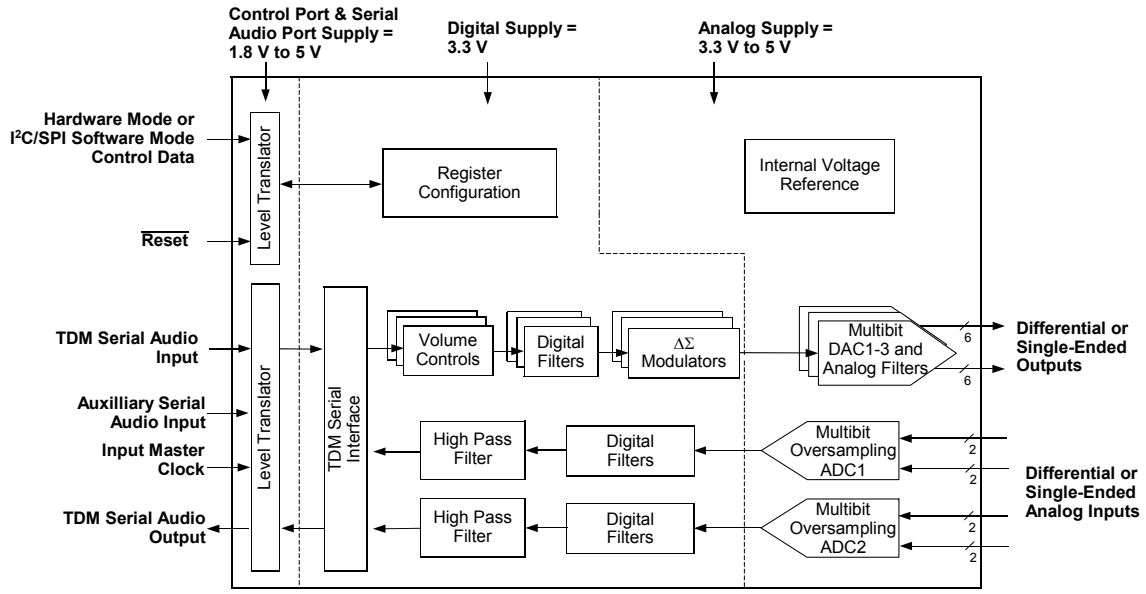
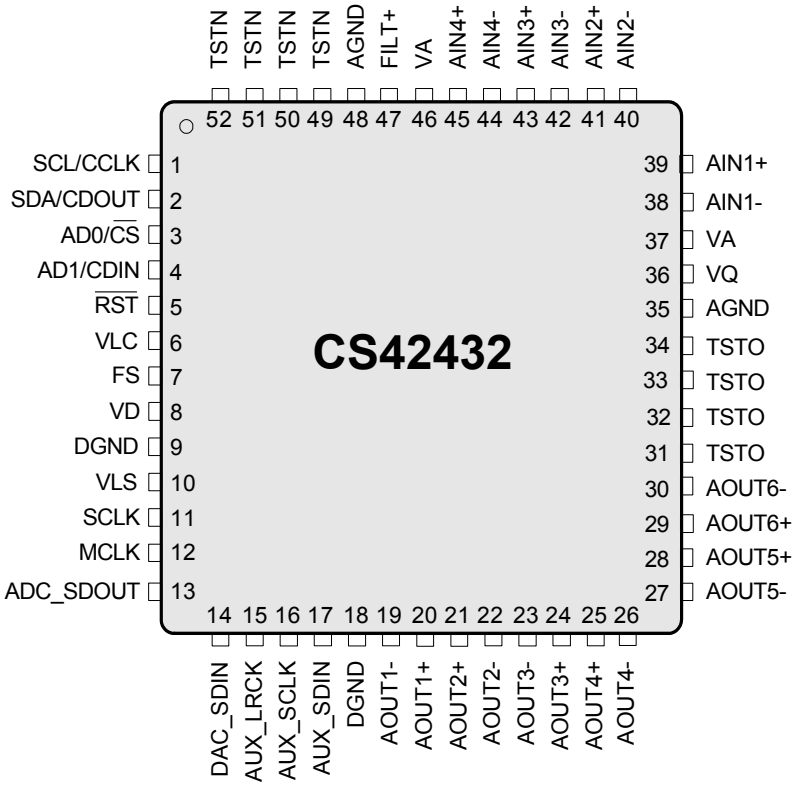


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. PIN DESCRIPTIONS - SOFTWARE MODE



Pin Name	#	Pin Description
SCL/CCLK	1	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA/CDOUT	2	**Serial Control Data I/O** (*Input/Output*) - Input/Output for I²C data. Output for SPI data.
AD0/$\overline{CS}$	3	**Address Bit [0]/ Chip Select** (*Input*) - Chip address bit in I²C Mode. Control signal used to select the chip in SPI Mode.
AD1/CDIN	4	**Address Bit [1]/ SPI Data Input** (*Input*) - Chip address bit in I²C Mode. Input for SPI data.
$\overline{RST}$	5	**Reset** (*Input*) - The device enters a low-power mode and all internal registers are reset to their default settings when low.
VLC	6	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port interface. See "Digital I/O Pin Characteristics" on page 8.
FS	7	**Frame Sync** (*Input*) - Signals the start of a new TDM frame in the TDM digital interface format.
VD	8	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	9,18	**Digital Ground** (*Input*) - Ground reference for the digital section.
VLS	10	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial port interfaces. See "Digital I/O Pin Characteristics" on page 8.
SCLK	11	**Serial Clock** *(Input)* - Serial clock for the serial audio interface. Input frequency must be 256 x Fs.
MCLK	12	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators and digital filters.
ADC_SDOUT	13	**Serial Audio Data Output** *(Output)* - TDM output for two's complement serial audio data.
DAC_SDIN	14	**DAC Serial Audio Data Input** (*Input*) - TDM Input for two's complement serial audio data.
AUX_LRCK	15	**Auxiliary Left/Right Clock** (*Output*) - Determines which channel, Left or Right, is currently active on the Auxiliary serial audio data line.

AUX_SCLK	16	**Auxiliary Serial Clock** *(Output)* - Serial clock for the Auxiliary serial audio interface.
AUX_SDIN	17	**Auxiliary Serial Input** (*Input*) - The 42432 provides an additional serial input for two's complement serial audio data.
AOUT1 +,- AOUT2 +,- AOUT3 +,- AOUT4 +,- AOUT5 +,- AOUT6 +,-	20,19 21,22 24,23 25,26 28,27 29,30	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table. Each positive leg of the differential outputs may also be used single-ended.
TSTO	31,32 33,34	**Test Out** - These pins are outputs used for test purposes only. They must not be connected to any external trace or other connection.
TSTN	49,50 51,52	**Test In** - These pins are inputs used for test purposes only. They must be tied to ground for normal operation.
AGND	35,48	**Analog Ground** (*Input*) - Ground reference for the analog section.
VQ	36	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
VA	37,46	**Analog Power** (*Input*) - Positive power supply for the analog section.
AIN1 +,- AIN2 +,- AIN3 +,- AIN4 +,-	39,38 41,40 43,42 45,44	**Differential Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators. The full-scale input level is specified in the Analog Characteristics specification table.
FILT+	47	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.

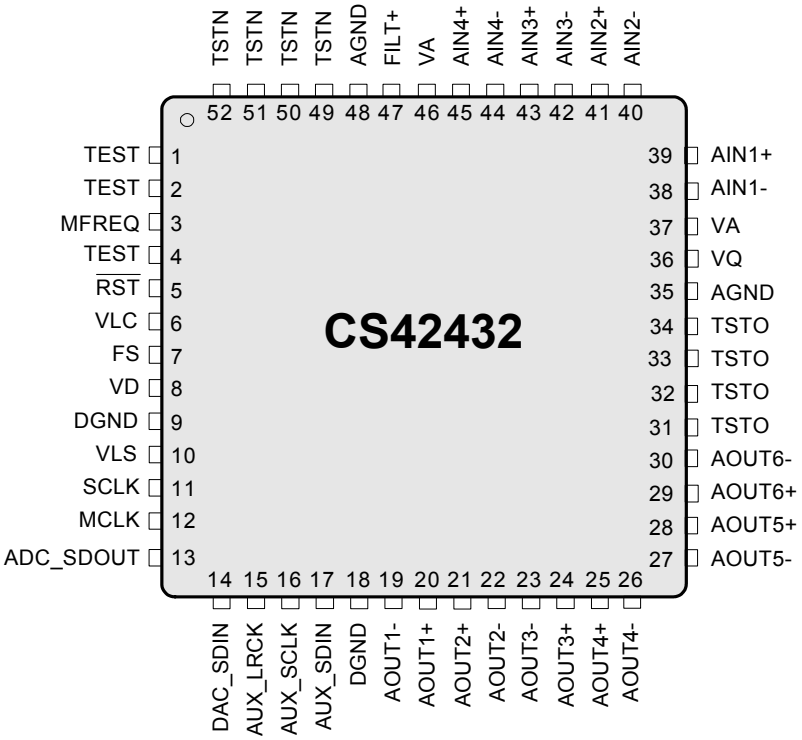
1.1 Digital I/O Pin Characteristics

Various pins on the CS42432 are powered from separate power supply rails. The logic level for each input should adhere to the corresponding power rail and should not exceed the maximum ratings.

Power Rail	Pin Name SW/(HW)	I/O	Driver	Receiver
VLC	$\overline{\text{RST}}$	Input	-	1.8 V - 5.0 V, CMOS
	SCL/CCLK (TEST)	Input	-	1.8 V - 5.0 V, CMOS, with Hysteresis
	SDA/CDOUT (TEST)	Input/ Output	1.8 V - 5.0 V, CMOS/Open Drain	1.8 V - 5.0 V, CMOS, with Hysteresis
	AD0/$\overline{\text{CS}}$ (MFREQ)	Input	-	1.8 V - 5.0 V, CMOS
	AD1/CDIN (TEST)	Input	-	1.8 V - 5.0 V, CMOS
VLS	MCLK	Input	-	1.8 V - 5.0 V, CMOS
	LRCK	Input	-	1.8 V - 5.0 V, CMOS
	SCLK	Input	-	1.8 V - 5.0 V, CMOS
	ADC_SDOUT2	Input/ Output	1.8 V - 5.0 V, CMOS	-
	DAC_SDIN	Input	-	1.8 V - 5.0 V, CMOS
	AUX_LRCK	Output	1.8 V - 5.0 V, CMOS	-
	AUX_SCLK	Output	1.8 V - 5.0 V, CMOS	-
	AUX_SDIN	Input	-	1.8 V - 5.0 V, CMOS

Table 1. I/O Power Rails

2. PIN DESCRIPTIONS - HARDWARE MODE



Pin Name	#	Pin Description
TEST	1,2,4	**Test** (*Input*) - Must be tied high or low. Do not leave unconnected.
MFREQ	3	**MCLK Frequency** (*Input*) - Sets the required frequency range of the input Master Clock. See section 5.4 for the appropriate settings.
RST	5	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
VLC	6	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port interface. See "Digital I/O Pin Characteristics" on page 8.
FS	7	**Frame Sync** (*Input*) - Signals the start of a new TDM frame in the TDM digital interface format.
VD	8	**Digital Power** (*Input*) - Positive power supply for the digital section.
VLS	10	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial port interfaces.
SCLK	11	**Serial Clock** *(Input)* - Serial clock for the serial audio interface. Input frequency must be 256xFs.
ADC_SDOUT	13	Serial Audio Data Output *(Output)* - TDM output for two's complement serial audio data.
DAC_SDIN	14	**DAC Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
AUX_LRCK	15	**Auxiliary Left/Right Clock** (*Output*) - Determines which channel, Left or Right, is currently active on the Auxiliary serial audio data line.
AUX_SCLK	16	**Auxiliary Serial Clock** *(Output)* - Serial clock for the Auxiliary serial audio interface.
AUX_SDIN	17	**Auxiliary Serial Input** (*Input*) - The 42432 provides an additional serial input for two's complement serial audio data.

AOUT1 +,- AOUT2 +,- AOUT3 +,- AOUT4 +,- AOUT5 +,- AOUT6 +,-	20,19 21,22 24,23 25,26 28,27 29,30	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table. Each positive leg of the differential outputs may also be used single-ended.
TSTN	49,50 51,52	**Test In** (*Input*) - This pin is an input used for test purposes. It must be tied to ground for normal operation.
TSTO	31,32 33,34	**Test Out** (*Output*) - This pin is an output used for test purposes only. It must not be connected to any external trace or other connection.
AGND	35,48	**Analog Ground** (*Input*) -
VQ	36	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
VA	37,46	**Analog Power** (*Input*) - Positive power supply for the analog section.
AIN1 +,- AIN2 +,- AIN3 +,- AIN4 +,-	39,38 41,40 43,42 45,44	**Differential Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators. The full-scale input level is specified in the Analog Characteristics specification table.
FILT+	47	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.

3. TYPICAL CONNECTION DIAGRAMS

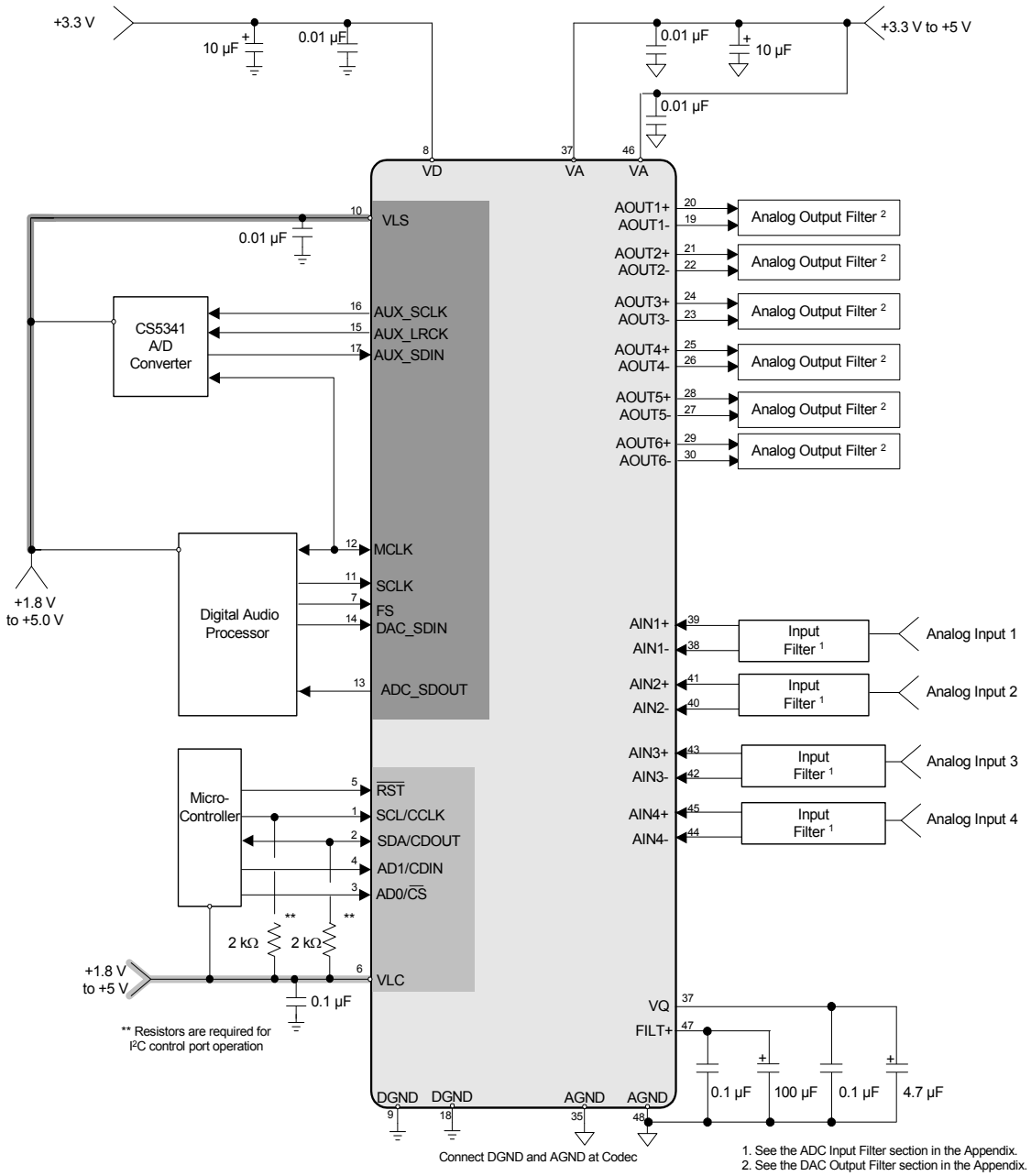


Figure 1. Typical Connection Diagram (Software Mode)

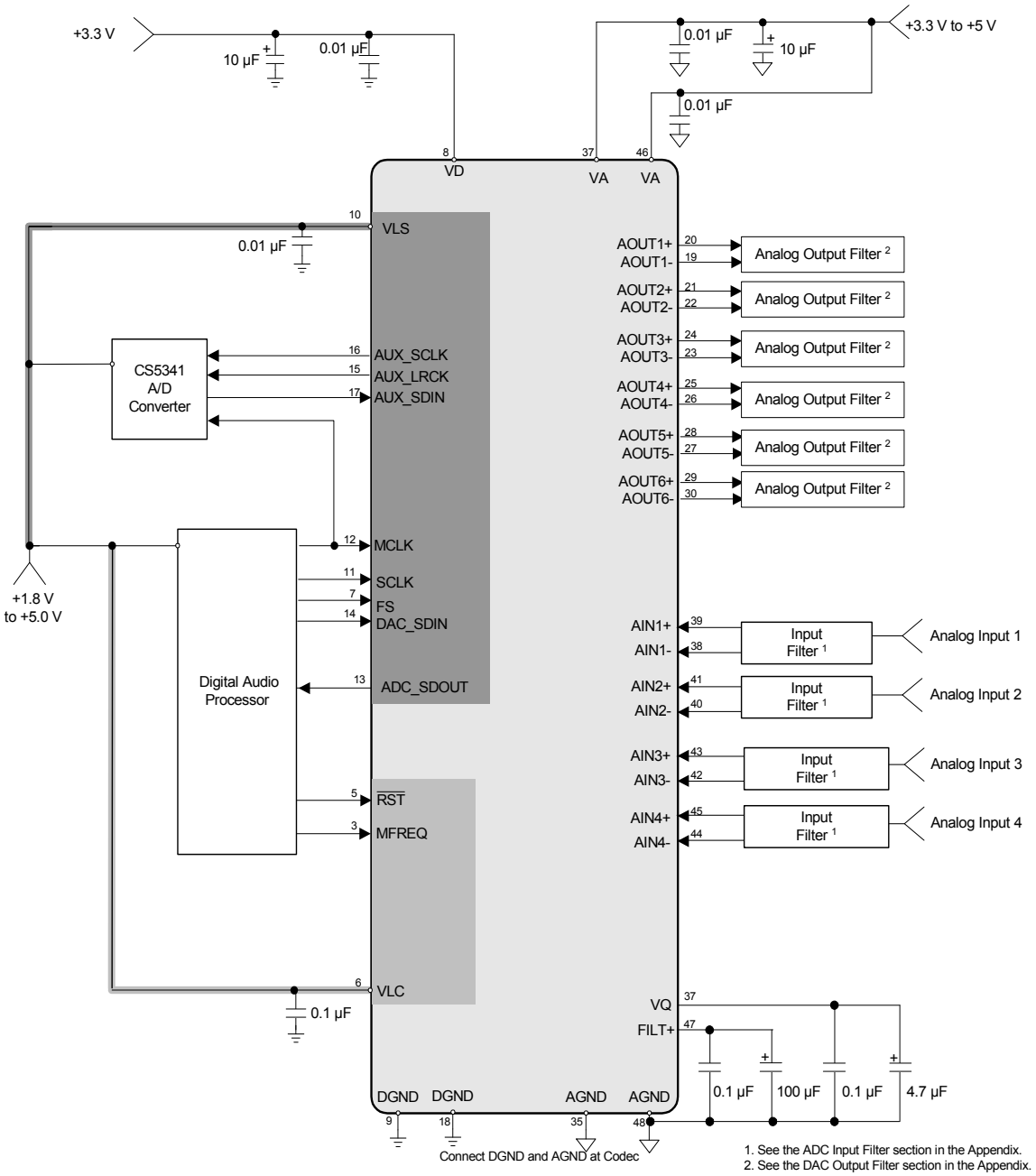


Figure 2. Typical Connection Diagram (Hardware Mode)

4. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Analog	(Note 1)	VA	3.14	5.25	V
Digital		VD	3.14	3.47	V
Serial Audio Interface	(Note 2)	VLS	1.71	5.25	V
Control Port Interface		VLC	1.71	5.25	V
Ambient Temperature					
Commercial Automotive	-CMZ -DMZ	T_A	-10 -40	+70 +105	°C °C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	Serial Port Interface	VLS	-0.3	6.0	V
	Control Port Interface	VLC	-0.3	6.0	V
Input Current	(Note 3)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 4)	V_{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage (Note 4)	Serial Port Interface	V_{IND-S}	-0.3	VLS+ 0.4	V
	Control Port Interface	V_{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)		T_A	-50	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. Typical Analog input/output performance will slightly degrade at VA = 3.3 V.
2. The ADC_SDOUT may not meet timing requirements in Double-Speed Mode.
3. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
4. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (COMMERCIAL)

(Test Conditions (unless otherwise specified): T_A = -10 to +70°C; VD = VLS = VLC = 3.3 V±5%, VA = 5 V±5% or 3.3 V±5%; Full-scale input sine wave: 1 kHz through the active input filter in Figure 19 on page 48 and Figure 20 on page 48; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential			Single-Ended			Unit
		Min	Typ	Max	Min	Typ	Max	
Fs=48 kHz, 96 kHz								
Dynamic Range	A-weighted	99	105	-	96	102	-	dB
	unweighted	96	102	-	93	99	-	dB
40 kHz bandwidth	unweighted	-	99	-		96	-	dB
Total Harmonic Distortion + Noise (Note 5)	-1 dB	-	-98	-92	-	-95	-89	dB
	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
40 kHz bandwidth	-1 dB	-	-90	-	-	-90	-	dB
ADC1-2 Interchannel Isolation		-	90	-	-	90	-	dB
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Analog Input								
Full-Scale Input Voltage		1.06*VA	1.12*VA	1.18*VA	0.53*VA	0.56*VA	0.59*VA	Vpp
Differential Input Impedance (Notes 7 & 9)		23	29	32	-	-	-	kΩ
Single-Ended Input Impedance (Notes 8 & 9)		-	-	-	23	29	32	kΩ
Common Mode Rejection Ratio (CMRR)		-	82	-	-	-	-	dB

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE)

(Test Conditions (unless otherwise specified): T_A = -40 to +85°C; VD = VLS = VLC = 3.3 V±5%, VA = 5 V±5% or 3.3 V±5%; Full-scale input sine wave: 1 kHz through the active input filter in Figure 19 on page 48 and Figure 20 on page 48; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter	Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs=48 kHz, 96 kHz							
Dynamic Range A-weighted	97	105	-	94	102	-	dB
unweighted	94	102	-	91	99	-	dB
40 kHz bandwidth unweighted	-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise (Note 5)						(Note 6)	
-1 dB	-	-98	-90	-	-95	-87/-79	dB
-20 dB	-	-82	-	-	-79	-	dB
-60 dB	-	-42	-	-	-39	-	dB
40 kHz bandwidth -1 dB	-	-87	-	-	-87	-	dB
ADC1-2 Interchannel Isolation	-	90	-	-	90	-	dB
DC Accuracy							
Interchannel Gain Mismatch	-	0.1	-	-	0.1	-	dB
Gain Drift	-	±100	-	-	±100	-	ppm/°C
Analog Input							
Full-Scale Input Voltage	1.04*VA	1.12*VA	1.20*VA	0.52*VA	0.56*VA	0.60*VA	Vpp
Differential Input Impedance (Notes 7 & 9)	23	29	32	-	-	-	kΩ
Single-Ended Input Impedance (Notes 8 & 9)	-	-	-	23	29	32	kΩ
Common Mode Rejection Ratio (CMRR)	-	82	-	-	-	-	dB

Notes:

5. Referred to the typical full-scale voltage.
6. Specification for VA = 5 V/specification for VA = 3.3 V.
7. Measured between AINx+ and AINx-.
8. Measured between AINxx and AGND.
9. The input impedance scales inversely proportionate to the sample rate of the ADC modulator.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Notes 10, 11)		Min	Typ	Max	Unit
Single-Speed Mode (Note 11)					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.08	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay		-	12/Fs	-	s
Double-Speed Mode (Note 11)					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.16	dB
Stopband		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay		-	9/Fs	-	s
High-Pass Filter Characteristics					
Frequency Response	-3.0 dB -0.13 dB	-	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time		-	10^5/Fs	0	s

Notes:

10. Filter response is guaranteed by design.
11. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 25 to 32) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL)

(Test Conditions (unless otherwise specified): T_A = -10 to +70°C; VD = VLS = VLC = 3.3 V±5%, VA = 5 V±5% or 3.3 V±5%; Full-scale 997 Hz output sine wave (see Note 14) into passive filter in Figure 25 on page 51 and active filter in Figure 25 on page 51; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs = 48 kHz, 96 kHz, 192 kHz								
Dynamic Range								
18 to 24-Bit	A-weighted	102	108	-	99	105	-	dB
	unweighted	99	105	-	96	102	-	dB
16-Bit	A-weighted	-	99	-	-	96	-	dB
	unweighted	-	96	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-98	-92	-	-95	-89	dB
	-20 dB	-	-85	-	-	-82	-	dB
	-60 dB	-	-45	-	-	-42	-	dB
16-Bit	0 dB	-	-93	-	-	-90	-	dB
	-20 dB	-	-76	-	-	-73	-	dB
	-60 dB	-	-36		-	-33	-	dB
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB
Analog Output								
Full-Scale Output		1.235•VA	1.300•VA	1.365•VA	0.618•VA	0.650•VA	0.683•VA	Vpp
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin	(Note 13)	-	-	10	-	-	10	µA
AC-Load Resistance (R_L)	(Note 15)	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)	(Note 15)	-	-	100	-	-	100	pF

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE)

(Test Conditions (unless otherwise specified): T_A = -40 to +85°C; VD = VLS = VLC = 3.3 V±5%, VA = 5 V±5% or 3.3 V±5%; Full-scale 997 Hz output sine wave (see Note 14) in Figure 25 on page 51 and Figure 25 on page 51; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs = 48 kHz, 96 kHz, 192 kHz								
Dynamic Range		(Note 12)			(Note 12)			
18 to 24-Bit	A-weighted	100/97	108	-	97/94	105	-	dB
	unweighted	97/94	105	-	94/91	102	-	dB
16-Bit	A-weighted	-	99	-	-	96	-	dB
	unweighted	-	96	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-98	-90	-	-95	-87	dB
	-20 dB	-	-85	-	-	-82	-	dB
	-60 dB	-	-45	-	-	-42	-	dB
16-Bit	0 dB	-	-93	-	-	-90	-	dB
	-20 dB	-	-76	-	-	-73	-	dB
	-60 dB	-	-36	-	-	-33	-	dB
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB
Analog Output								
Full-Scale Output		1.210•VA	1.300•VA	1.392•VA	0.605•VA	0.650•VA	0.696•VA	Vpp
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin (Note 13)		-	-	10	-	-	10	µA
AC-Load Resistance (R_L) (Note 15)		3	-	-	3	-	-	kΩ
Load Capacitance (C_L) (Note 15)		-	-	100	-	-	100	pF

Notes:

12. Specification for VA = 5 V/specification for VA = 3.3 V.
13. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC-blocking capacitors.
14. One LSB of triangular PDF dither is added to data.
15. Guaranteed by design. See 3. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the dominant pole of the two-pole amp in the output stage. Increasing this value beyond the recommended 100 pF can cause the internal op-amp to become unstable. See "External Filters" on page 48 for a recommended output filter.

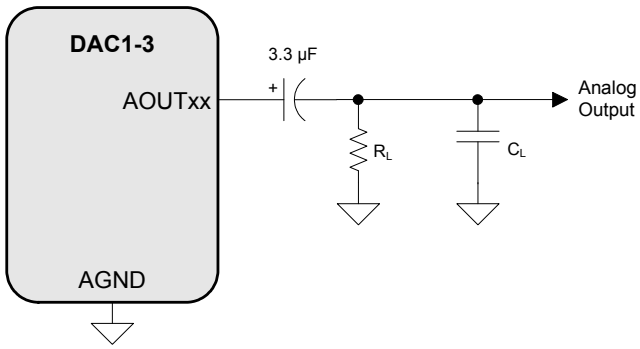


Figure 3. Output Test Load

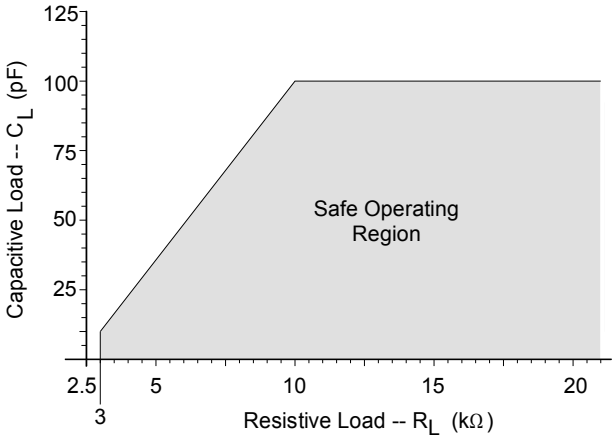


Figure 4. Maximum Loading

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Notes 10, 16)		Min	Typ	Max	Unit
Single-Speed Mode					
Passband (Frequency Response)	to -0.05 dB corner	0	-	0.4780	Fs
	to -3 dB corner	0	-	0.4996	Fs
Frequency Response 10 Hz to 20 kHz		-0.2	-	+0.08	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation	(Note 17)	50	-	-	dB
Group Delay		-	10/Fs	-	s
De-emphasis Error (Note 18)	Fs = 32 kHz	-	-	+1.5/+0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.25	dB
	Fs = 48 kHz	-	-	-0.2/-0.4	dB
Double-Speed Mode					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4650	Fs
	to -3 dB corner	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz		-0.2	-	+0.7	dB
StopBand		0.5770	-	-	Fs
StopBand Attenuation	(Note 17)	55	-	-	dB
Group Delay		-	5/Fs	-	s
Quad-Speed Mode					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.397	Fs
	to -3 dB corner	0	-	0.476	Fs
Frequency Response 10 Hz to 20 kHz		-0.2	-	+0.05	dB
StopBand		0.7	-	-	Fs
StopBand Attenuation	(Note 17)	51	-	-	dB
Group Delay		-	2.5/Fs	-	s

Notes:

16. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 33 to 44) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
17. Single- and Double-Speed Mode Measurement Bandwidth is from Stopband to 3 Fs.
    Quad-Speed Mode Measurement Bandwidth is from Stopband to 1.34 Fs.
18. De-emphasis is only available in Single-Speed Mode.

SWITCHING SPECIFICATIONS - ADC/DAC PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLS, ADC_SDOUT C_{LOAD} = 15 pF.)

Parameters		Symbol	Min	Max	Units
Slave Mode					
$\overline{\text{RST}}$ pin Low Pulse Width (Note 19)			1	-	ms
MCLK Frequency			0.512	50	MHz
MCLK Duty Cycle (Note 20)			45	55	%
Input Sample Rate (FS pin)	Single-Speed Mode	F_s	4	50	kHz
	Double-Speed Mode (Note 21)	F_s	50	100	kHz
	Quad-Speed Mode (Note 22)	F_s	100	200	kHz
SCLK Duty Cycle			45	55	%
SCLK High Time		t_{sckh}	8	-	ns
SCLK Low Time		t_{sckl}	8	-	ns
FS Rising Edge to SCLK Rising Edge		t_{fss}	5	-	ns
SCLK Rising Edge to FS Falling Edge		t_{fsh}	16	-	ns
DAC_SDIN Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
DAC_SDIN Hold Time After SCLK Rising Edge		t_{dh}	5	-	ns
DAC_SDIN Hold Time After SCLK Rising Edge		t_{dh1}	5	-	ns
ADC_SDOUT Hold Time After SCLK Rising Edge		t_{dh2}	10	-	ns
ADC_SDOUT Valid Before SCLK Rising Edge		t_{dval}	15	-	ns

Notes:

19. After powering up the CS42432, $\overline{\text{RST}}$ should be held low after the power supplies and clocks are settled.
20. See Table 5 on page 41 for suggested MCLK frequencies.
21. VLS is limited to nominal 2.5 V to 5.0 V operation only.
22. ADC does not meet timing specification for Quad-Speed Mode.

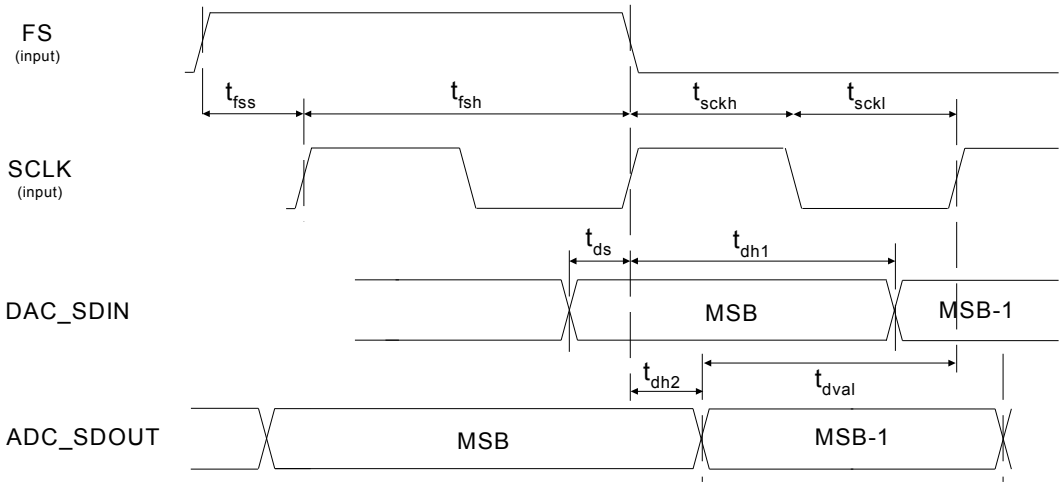


Figure 5. TDM Serial Audio Interface Timing

SWITCHING CHARACTERISTICS - AUX PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLS.)

Parameters		Symbol	Min	Max	Units
Master Mode					
Output Sample Rate (AUX_LRCK)	All Speed Modes	F_s	-	LRCK	kHz
AUX_SCLK Frequency			-	64•LRCK	kHz
AUX_SCLK Duty Cycle			45	55	%
AUX_LRCK Edge to SCLK Rising Edge		t_{lcks}	-	5	ns
AUX_SDIN Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
AUX_SDIN Hold Time After SCLK Rising Edge		t_{dh}	5	-	ns

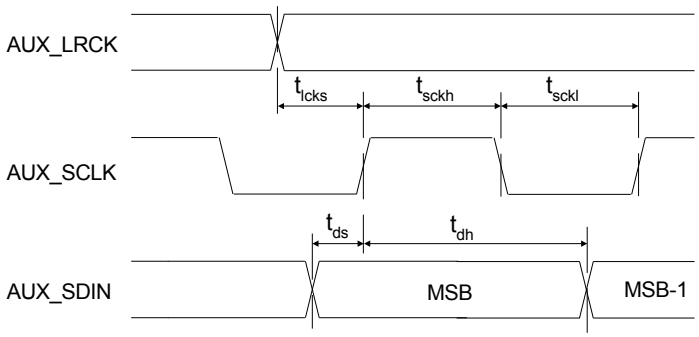


Figure 6. Serial Audio Interface Slave Mode Timing

SWITCHING SPECIFICATIONS - CONTROL PORT - I²C MODE

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, SDA C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SCL Clock Frequency		f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start		t_{irs}	500	-	ns
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling	(Note 23)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising		t_{sud}	250	-	ns
Rise Time of SCL and SDA	(Note 24)	t_{rc}	-	1	µs
Fall Time SCL and SDA	(Note 24)	t_{fc}	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling		t_{ack}	300	1000	ns

Notes:

23. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.
24. Guaranteed by design.

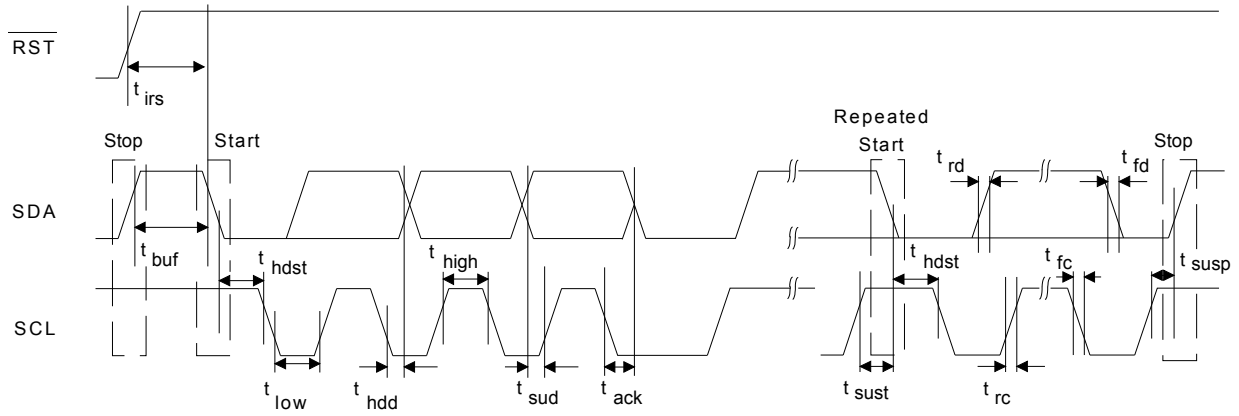


Figure 7. Control Port Timing - I²C Format

SWITCHING SPECIFICATIONS - CONTROL PORT - SPI FORMAT

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, CDOUT C_L = 30 pF)

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	20	-	ns
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 25)	t_{dh}	15	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	50	ns
Rise Time of CDOUT		t_{r1}	-	25	ns
Fall Time of CDOUT		t_{f1}	-	25	ns
Rise Time of CCLK and CDIN	(Note 26)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 26)	t_{f2}	-	100	ns

Notes:

25. Data must be held for sufficient time to bridge the transition time of CCLK.
26. For f_{sck} <1 MHz.

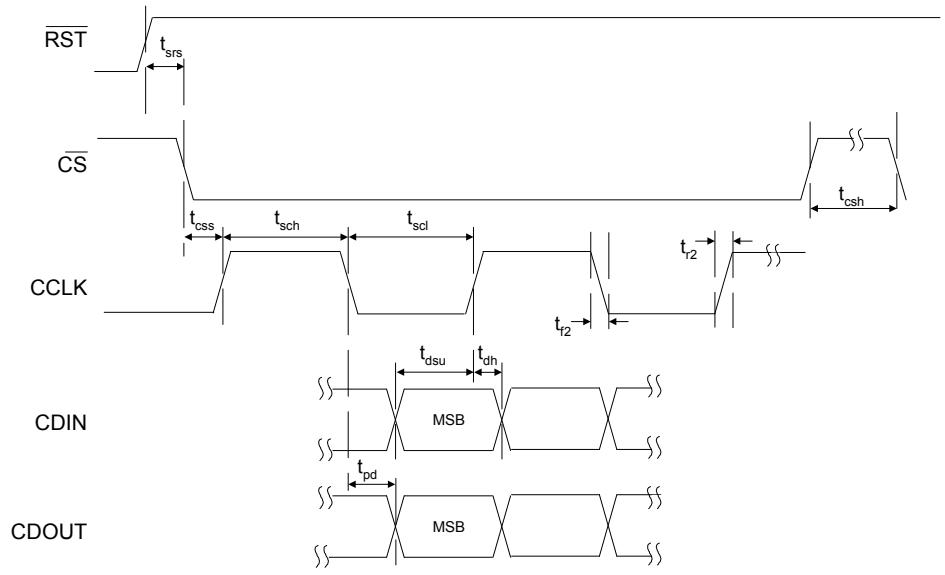


Figure 8. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 27)						
Power Supply Current	VA = 5.0 V	I_A	-	80	-	mA
	VLS = VLC = VD = 3.3 V					
	(Note 28)	I_{DT}	-	60.6	-	mA
Power Dissipation	VLS = VLC = VD = 3.3 V,5 V		-	600	850	mW
Power Supply Rejection Ratio	1 kHz	PSRR	-	60	-	dB
(Note 29)	60 Hz		-	40	-	dB
Power-Down Mode (Note 30)						
Power Dissipation	VLS = VLC = VD = 3.3 V,VA = 5 V		-	1.25	-	mW
VQ Characteristics						
Nominal Voltage			-	0.5•VA	-	V
Output Impedance			-	23	-	kΩ
DC Current Source/Sink (Note 31)			-	-	10	µA
FILT+ Nominal Voltage			-	VA	-	V

Notes:

27. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS input to the DAC and AUX port, and a 1 kHz, -1 dB analog input to the ADC port sampled at the highest F_s for each speed mode. DAC outputs are open, unless otherwise specified.
28. I_{DT} measured with no external loading on pin (SDA).
29. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.
30. Power-Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static and no analog input.
31. Guaranteed by design. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through the electrolytic de-coupling capacitors.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 32)		Symbol	Min	Typ	Max	Units
High-Level Output Voltage at I_o=2 mA	Serial Port		VLS-1.0	-	-	V
	Control Port	V_{OH}	VLC-1.0	-	-	V
Low-Level Output Voltage at I_o=2 mA	Serial Port		-	-	0.4	V
	Control Port	V_{OL}	-	-	0.4	V
High-Level Input Voltage	Serial Port		0.7xVLS	-	-	V
	Control Port	V_{IH}	0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port		-	-	0.2xVLS	V
	Control Port	V_{IL}	-	-	0.2xVLC	V
Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance (Note 24)			-	-	10	pF

Notes:

32. See "Digital I/O Pin Characteristics" on page 8 for serial and control port power rails.