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CS4244

4 In/4 Out Audio CODEC with PCM and TDM Interfaces

DAC Features

- Advanced multibit delta-sigma modulator
- 24-bit resolution
- Differential or single-ended outputs
- Dynamic range (A-weighted)
  - -109 dB differential
  - -105 dB single-ended
- THD+N
  - -90 dB differential
  - -88 dB single ended
- 2 Vrms full-scale output into 3-kΩ AC load
- Rail-to-rail operation

ADC Features

- Advanced multibit delta-sigma modulator
- 24-bit resolution
- Differential inputs
- -105 dB dynamic range (A-weighted)
- -88 dB THD+N
- 2 Vrms full-scale input

System Features

- TDM, left justified, and I²S serial inputs and outputs
- I²C host control port
- Supports logic levels between 5 and 1.8 V
- Supports sample rates up to 96 kHz

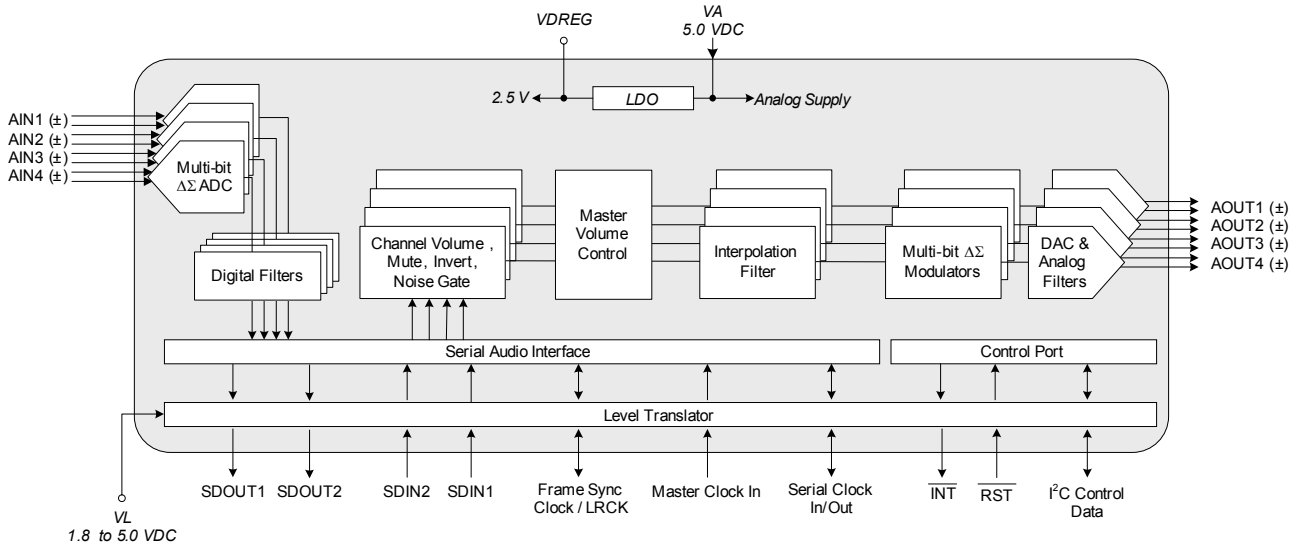
Common Applications

- Automotive audio systems
- AV, Blu-Ray® Disc, and DVD receivers
- Audio interfaces, mixing consoles, and effects processors

General Description

The CS4244 provides four multibit analog-to-digital and four multi-bit digital-to-analog Δ-Σ converters and is compatible with differential inputs and either differential or single-ended outputs. Digital volume control, noise gating, and muting is provided for each DAC path. A selectable high-pass filter is provided for the 4 ADC inputs. The CS4244 supports master and slave modes and TDM, left-justified, and I²S modes.

This product is available in a 40-pin QFN package in Automotive (-40°C to +85°C) and Commercial (0°C to +70°C) temperature grades. The CDB4244 Customer Demonstration Board is also available for device evaluation and implementation suggestions. See "Ordering Information" on page 64 for complete details.



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1. PIN DESCRIPTIONS

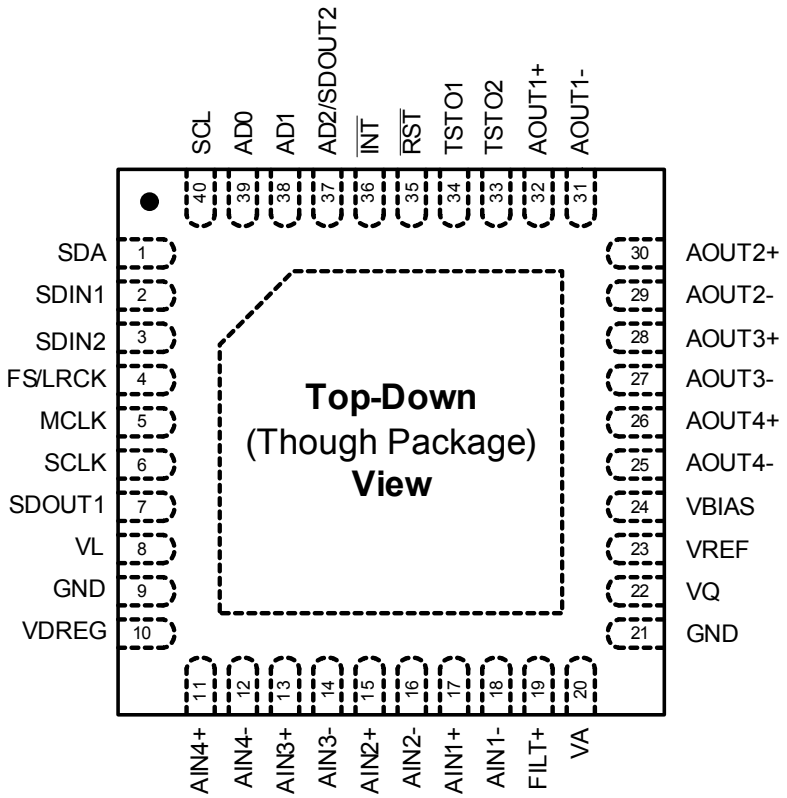


Figure 1. CS4244 Pinout

Pin Name	Pin #	Pin Description
SDA	1	**Serial Control Data** (*Input/Output*) - Bi-directional data I/O for the I²C control port.
SDINx	2,3	**Serial Data Input** (*Input*) - Input channels serial audio data.
FS/LRCK	4	**Frame Synchronization Clock/Left/Right Clock** (*Input/Output*) - Determines which channel or frame is currently active on the serial audio data line.
MCLK	5	**Master Clock** (*Input*) -Clock source for the internal logic, processing, and modulators.
SCLK	6	**Serial Clock** (*Input*/Output) -Serial Clock for the serial data port.
SDOUT1	7	**Serial Data Output 1** (*Output*) - ADC data output into a multi-slot TDM stream or AIN1 and AIN2 ADC data output in Left Justified and I²S modes.
VL	8	**Interface Power** (*Input*) - Positive power for the digital interface level shifters.
GND	9,21	**Ground** (*Input*) - Ground reference for the I/O and digital, analog sections.
VDREG	10	**Digital Power** (*Output*) - Internally generated positive power supply for digital section.
AINx+	11,13,15, 17	**Positive Analog Input** (*Input*) - Positive input signals to the internal analog to digital converters. The full scale analog input level is specified in the Analog Input Characteristics tables on pages 12 and 13.
AINx-	12,14,16, 18	**Negative Analog Input** (*Input*) - Negative input signals to the internal analog to digital converters. The full scale analog input level is specified in the Analog Input Characteristics tables on pages 12 and 13.
FILT+	19	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal ADCs.

VA	20	**Analog Power** (*Input*) - Positive power for the analog sections.
VQ	22	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
VREF	23	**Analog Power Reference** (*Input*) - Return pin for the VBIAS cap.
VBIAS	24	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal DACs.
AOUTx-	25,27,29, 31	**Negative Analog Output** *(Output)* - Negative output signals from the internal digital to analog converters. The full scale analog output level is specified in the Analog Output Characteristics tables on pages 16 and 17.
AOUTx+	26,28,30, 32	**Positive Analog Output** *(Output)* - Positive output signals from the internal digital to analog converters. The full scale analog output level is specified in the Analog Output Characteristics tables on pages 16 and 17.
TSTOx	33,34	**Test Outputs** *(Output)* - Test outputs. These pins should be left unconnected.
$\overline{\text{RST}}$	35	**Reset** (*Input*) - Applies reset to the internal circuitry when pulled low.
$\overline{\text{INT}}$	36	**Interrupt (Output)** - Sent to DSP to indicate an interrupt condition has occurred.
AD2/SDOUT2	37	**I²C Address Bit 2/Serial Data Output 2** (*Input/Output*) - Sets the I²C address bit 2 at reset. Functions as Serial Data Out 2 for AIN3 and AIN4 ADC data output in Left Justified and I²S modes. High impedance in TDM mode. See Section 4.3 I²C Control Port for more details concerning this mode of operation.
AD1	38	**I²C Address Bit 1** (*Input*) - Sets the I²C address bit 1.
AD0	39	**I²C Address Bit 0** (*Input*) - Sets the I²C address bit 0.
SCL	40	**Serial Control Port Clock** (*Input*) - Serial clock for the I²C control port.
GND	-	**Thermal Pad** - The thermal pad on the bottom of the device should be connected to the ground plane via an array of vias.

1.1 I/O Pin Characteristics

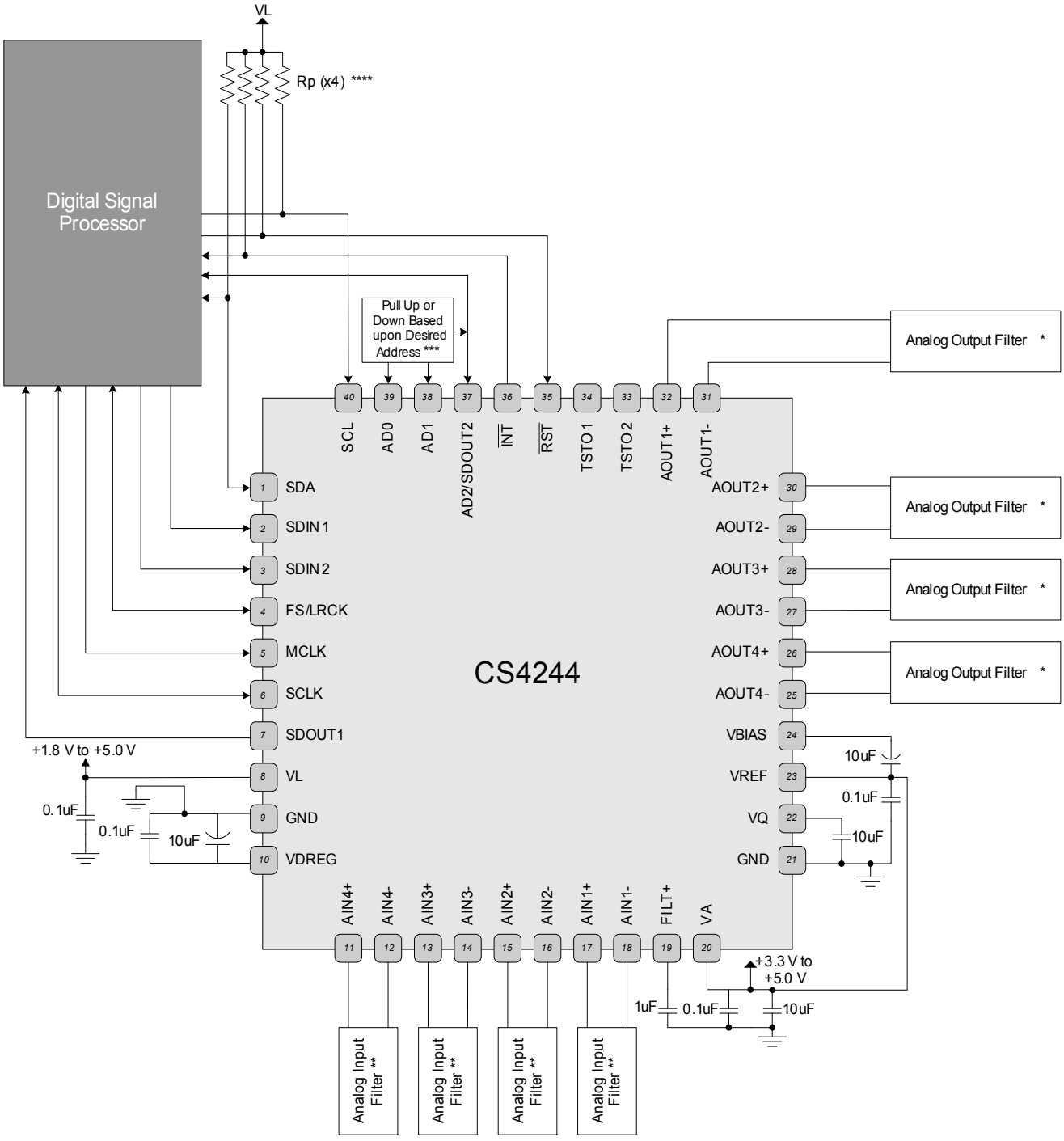
Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

Power Supply	Pin Name	I/O	Driver	Internal Connections (Note 1)	Receiver
VL	SCL	Input	-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	SDA	Input/Output	CMOS/Open Drain	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	$\overline{\text{INT}}$	Output	CMOS/Open Drain	(Note 2)	-
	$\overline{\text{RST}}$	Input	-	(Note 2)	5.0 V CMOS, with Hysteresis
	MCLK	Input	-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	FS/LRCK	Input/Output	5.0 V CMOS	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	SCLK	Input/Output	5.0 V CMOS	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	SDOUT1	Output	5.0 V CMOS	Weak Pull-down (~500kΩ)	
	SDINx	Input	-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	AD0,1	Input	-	(Note 2)	5.0 V CMOS
	AD2/SDOUT2	Input/Output	5.0 V CMOS	(Note 2)	5.0 V CMOS

Notes:

1. Internal connection valid when device is in reset.
2. This pin has no internal pull-up or pull-down resistors. External pull-up or pull-down resistors should be added in accordance with Figure 2.

2. TYPICAL CONNECTION DIAGRAM



* See Section 4.6.4
** See Section 4.6.2.2
*** See Section 4.3
**** See Switching Specifications - Control Port

Figure 2. Typical Connection Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = 0 V; all voltages with respect to ground. (Note 3)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply						
Analog Core		VA	3.135 4.75	3.3 5	3.465 5.25	V V
Level Translator		VL	1.71	-	5.25	V
Temperature						
Ambient Operating Temperature - Power Applied	Automotive Commercial	T_A	-40 0	- -	+85 +70	°C °C
Junction Temperature		T_J	-40	-	+150	°C

Notes: 3. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Analog Core		VA	-0.3	5.5	V
Level Translator		VL	-0.3	5.5	V
VDREG Current	(Note 4)	I_{VDREG}	-	10	µA
Inputs					
Input Current	(Note 5)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 6)	V_{INA}	- 0.3	VA + 0.4	V
Logic Level Input Voltage	(Note 6)	V_{IND}	-0.3	VL + 0.4	V
Temperature					
Ambient Operating Temperature - Power Applied		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: OPERATION BEYOND THESE LIMITS MAY RESULT IN PERMANENT DAMAGE TO THE DEVICE.

Notes: 4. No external loads should be connected to the VDREG pin. Any connection of a load to this point may result in errant operation or performance degradation in the device.

5. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

6. The maximum over/under voltage is limited by the input current.

DC ELECTRICAL CHARACTERISTICS

GND = 0 V; all voltages with respect to ground.

Parameters	Min	Typ	Max	Units
VDREG (Note 7)				
Nominal Voltage	-	2.5	-	V
Output Impedance	-	0.5	-	Ω
FILT+				
Nominal Voltage	-	VA	-	V
Output Impedance	-	23	-	kΩ
DC Current Source/Sink	-	-	1	µA
VQ				
Nominal Voltage	-	0.5•VA	-	V
Output Impedance	-	77	-	kΩ
DC Current Source/Sink	-	-	0	µA

Notes:

7. No external loads should be connected to the VDREG pin. Any connection of a load to this point may result in errant operation or performance degradation in the device.

TYPICAL CURRENT CONSUMPTION

This table represents the power consumption for individual circuit blocks within the CS4244. CS4244 is configured as shown in Figure 2 on page 8. VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC; F_S = 100 kHz; MCLK = 25.6 MHz; DAC load is 3 kΩ; All input signals are zero (digital zero for SDINx inputs and AC coupled to ground for AINx inputs) .

	Functional Block	**VA/VL**	**Typical Current [mA] (unless otherwise noted)** (Note 9), (Note 12)	
			i_{VA}	i_{VL}
1	Reset Overhead (All lines held static, $\overline{RST}$ line pulled low.)	5	0.030	0.001
		3.3	0.020	0.001
2	Power Down Overhead (All lines clocks and data lines active, $\overline{RST}$ line pulled high, All PDNx bits set high.)	5	5	0.101
		3.3	5	0.101
3	PLL (Note 10) (Current drawn resulting from PLL being active. PLL is active for 256x and 384x)	5	1	-
		3.3	1	-
4	DAC Overhead (Current drawn whenever any of the four DACs are powered up.)	5	50	-
		3.3	45	-
5	DAC Channel (Note 8) (Current drawn per each DAC powered up.)	5	5	-
		3.3	4	-
6	ADC Overhead (Current drawn whenever any of the four ADCs are powered up.)	5	11	-
		3.3	11	-
7	ADC Group (Current drawn due to an ADC “group” being powered up. See (Note 11))	5	2	-
		3.3	2	-
8	ADC Channel (Current drawn per each ADC powered up.)	5	2	0.109
		3.3	2	0.066

Notes:

8. Full-scale differential output signal.
9. Current consumption increases with increasing F_S and increasing MCLK. Values are based on F_S of 100 kHz and MCLK of 25.6 MHz. Current variance between speed modes is small.
10. PLL is activated by setting the MCLK RATE bit to either 000 (operating in 256x mode) or 001 (operating in 384kHz).
11. Internal to the CS4244, the analog to digital converters are grouped together in stereo pairs. ADC1 and ADC2 are grouped together as are ADC3 and ADC4. The ADC group current draw is the current that is drawn whenever one of these groups become active.
12. To calculate total current draw for an arbitrary amount of ADCs or DACs, the following equations apply:

Total Running Current Draw from VA Supply = *Power Down Overhead + PLL (If Applicable)+ DAC Current Draw + ADC Current Draw*
where
DAC Current Draw = DAC Overhead + (Number of DACs x DAC Channel)
ADC Current Draw = ADC Overhead + (Number of active ADC Groups x ADC Group) + (Number of active ADC Channels x ADC Channel)

and

Total Running Current Draw from VL Supply = *PDN Overhead + (Number of active ADC Channels x ADC Channel)*

ANALOG INPUT CHARACTERISTICS (COMMERCIAL GRADE)

Test Conditions (unless otherwise specified): Device configured as shown in Section 2. on page 8. Input sine wave: 1 kHz; VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = 25 °C; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Sample Rate = 48 kHz; all Power Down ADCx bits = 0.

Parameter	VA, VREF = 3.3 V			VA, VREF = 5.0 V			Unit
	Min	Typ	Max	Min	Typ	Max	
Dynamic Range							
A-weighted	95	101	-	99	105	-	dB
unweighted	92	98	-	96	102	-	dB
Total Harmonic Distortion + Noise							
-1 dBFS	-	-95	-89	-	-88	-82	dB
-60 dBFS	-	-38	-32	-	-42	-36	dB
Other Analog Characteristics							
Interchannel Gain Mismatch	-	0.2	-	-	0.2	-	dB
Gain Drift	-	±100	-	-	±100	-	ppm/°C
Offset Error (Note 13)							
High Pass Filter On	-	0.0001	-	-	0.0001	-	% Full Scale
High Pass Filter Off	-	0.25	-	-	0.25	-	% Full Scale
Interchannel Isolation	-	90	-	-	90	-	dB
Full-scale Input Voltage (Differential Inputs)	1.58•VA	1.66•VA	1.74•VA	1.58•VA	1.66•VA	1.74•VA	Vpp
Input Impedance	-	40	-	-	40	-	kΩ
Common Mode Rejection (Differential Inputs)	-	60	-	-	60	-	dB
PSRR (Note 14) 1 kHz	-	45	-	-	45	-	dB
60 Hz	-	20	-	-	20	-	dB

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE GRADE)

Test Conditions (unless otherwise specified): Device configured as shown in Section 2. on page 8. Input sine wave: 1 kHz; VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = -40 to +85 °C; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Sample Rate = 48 kHz; all Power Down ADCx bits = 0.

Parameter	VA, VREF = 3.3 V Min	Typ	Max	VA, VREF = 5.0 V Min	Typ	Max	Unit
Dynamic Range							
A-weighted	93	101	-	97	105	-	dB
unweighted	90	98	-	94	102	-	dB
Total Harmonic Distortion + Noise							
-1 dBFS	-	-95	-87	-	-88	-80	dB
-60 dBFS	-	-38	-30	-	-42	-34	dB
Other Analog Characteristics							
Interchannel Gain Mismatch	-	0.2	-	-	0.2	-	dB
Gain Drift	-	±100	-	-	±100	-	ppm/°C
Offset Error (Note 13)							
High Pass Filter On	-	0.0001	-	-	0.0001	-	% Full Scale
High Pass Filter Off	-	0.25	-	-	0.25	-	% Full Scale
Interchannel Isolation	-	90	-	-	90	-	dB
Full-scale Input Voltage (Differential Inputs)	1.58•VA	1.66•VA	1.74•VA	1.58•VA	1.66•VA	1.74•VA	Vpp
Input Impedance	-	40	-	-	40	-	kΩ
Common Mode Rejection (Differential Inputs)	-	60	-	-	60	-	dB
PSRR (Note 14) 1 kHz	-	45	-	-	45	-	dB
60 Hz	-	20	-	-	20	-	dB

Notes:

13. AINx+ connected to AINx-.
14. Valid with the recommended capacitor values on FILT+ and VQ. See Figure 4 for test configuration.

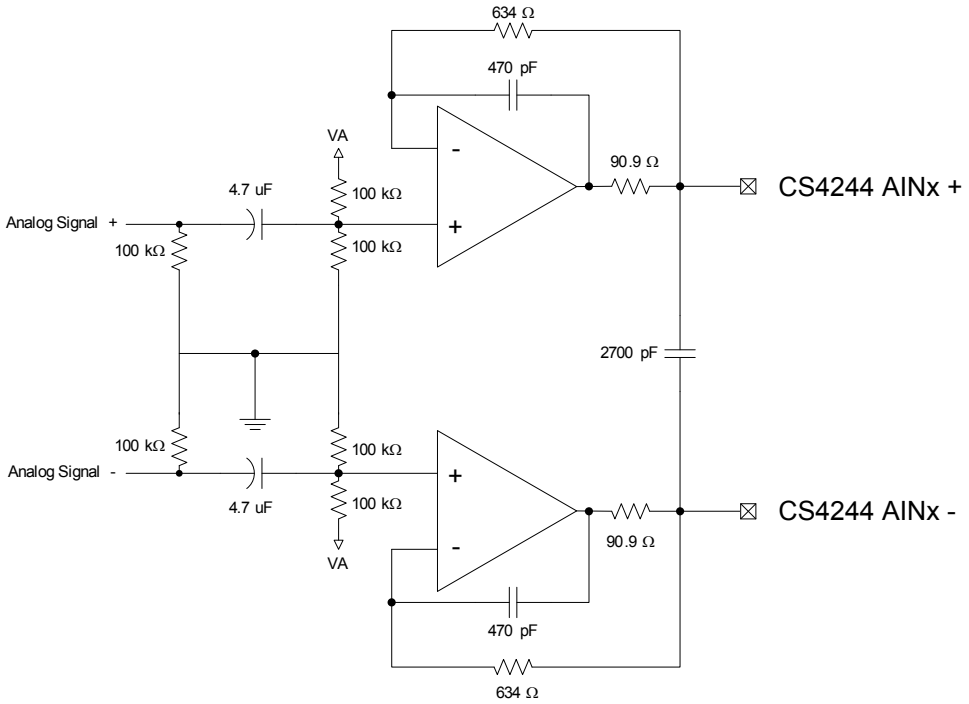


Figure 3. Test Circuit for ADC Performance Testing

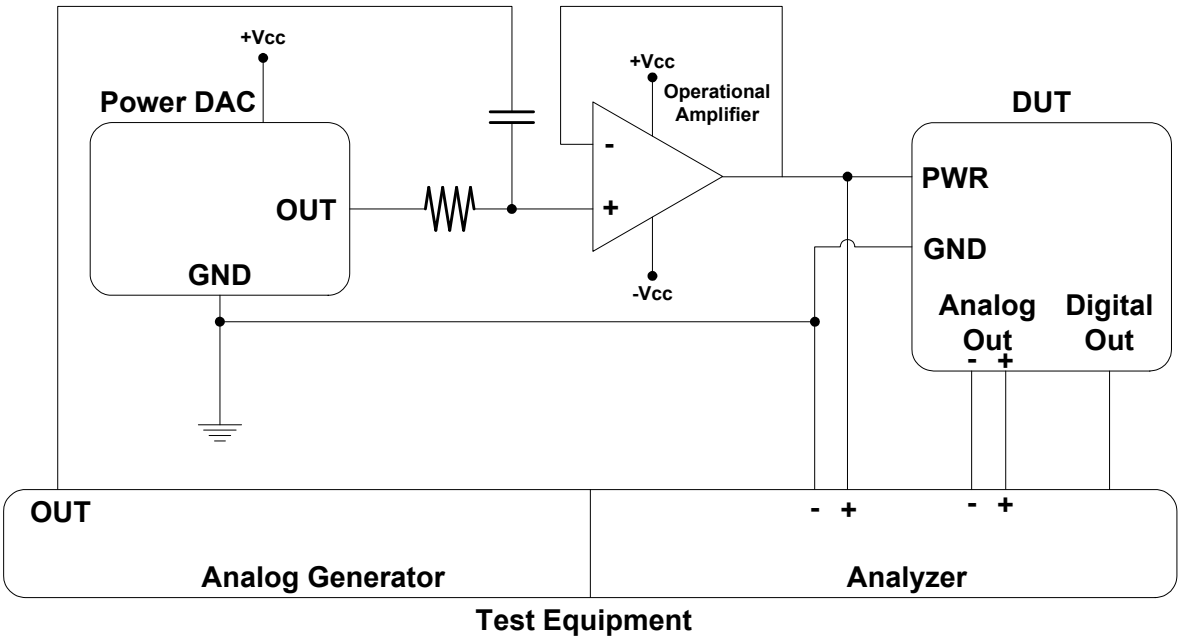


Figure 4. PSRR Test Configuration

ADC DIGITAL FILTER CHARACTERISTICS

Test Conditions (unless otherwise specified): Device configured as shown in Section 2. on page 8. Input sine wave: 1 kHz; VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified. See filter plots in Section 7. on page 60.

Parameter (Note 15)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4535	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		70	-	-	dB
Single-Speed Mode					
ADC Group Delay (Note 16)		-	9.5/Fs	-	s
High-Pass Filter Characteristics **(48 kHz Fs)**					
Frequency Response	-3.0 dB -0.13 dB	- -	2 11	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-0.09	-	0.17	dB
Filter Settling Time (Note 17)		-	25000/Fs	0	s
Double-Speed Mode					
ADC Group Delay (Note 16)		-	9.5/Fs	-	s
High-Pass Filter Characteristics **(96 kHz Fs)**					
Frequency Response	-3.0 dB -0.13 dB	- -	4 22	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-0.15	-	0.17	dB
Filter Settling Time (Note 17)		-	25000/Fs	0	s

Note:

15. Response is clock-dependent and will scale with Fs.
16. The ADC group delay is measured from the time the analog inputs are sampled on the AINx pins to the FS/LRCK transition (rising or falling) after the last bit of that (group of) sample(s) has been transmitted on SDOUTx.
17. The amount of time from input of half-full-scale step function until the filter output settles to 0.1% of full scale.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL GRADE)

Test Conditions (unless otherwise specified). Device configured as shown in Section 2. on page 8. VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = 25 °C; Full-scale 1 kHz input sine wave; Sample Rate = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Specifications apply to all channels unless otherwise indicated; all Power Down DACx bits = 0. See (Note 19) on page 17.

Parameter		VA, VREF= 3.3 V (Differential/Single-ended) Min	Typ	Max	VA, VREF= 5.0 V (Differential/Single-ended) Min	Typ	Max	Unit
Dynamic Performance								
Dynamic Range								
18 to 24-Bit	A-weighted	100/96	106/102	-	103/99	109/105	-	dB
	unweighted	97/93	103/99	-	100/96	106/102	-	dB
16-Bit	A-weighted	89	95	-	89	95	-	dB
	unweighted	86	92	-	86	92	-	dB
Total Harmonic Distortion + Noise		-	-90/-88	-84/-82	-	-90/-88	-84/-82	dB
Full-scale Output Voltage		1.48•VA/ 0.74•VA	1.56•VA/ 0.78•VA	1.64•VA/ 0.82•VA	1.48•VA/ 0.74•VA	1.56•VA/ 0.78•VA	1.64•VA/ 0.82•VA	Vpp
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)(Note 19)		3	-	-	3	-	-	kΩ
Load Capacitance (C_L)(Note 19)		-	-	100	-	-	100	pF
Parallel DC-Load Resistance(Note 20)		10	-	-	10	-	-	kΩ
Output Impedance		-	100	-	-	100	-	Ω
PSRR (Note 21)	1 kHz	-	60	-	-	60	-	dB
	60 Hz	-	60	-	-	60	-	dB

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE GRADE)

Test Conditions (unless otherwise specified): Device configured as shown in Section 2. on page 8. VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = -40 to +85 °C; Full-scale 1 kHz input sine wave; Sample Rate = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Specifications apply to all channels unless otherwise indicated; all Power Down DACx bits = 0. See (Note 19).

Parameter		VA, VREF= 3.3 V (Differential/Single-ended) Min	Typ	Max	VA, VREF= 5.0 V (Differential/Single-ended) Min	Typ	Max	Unit
Dynamic Performance								
Dynamic Range								
18 to 24-Bit	A-weighted	98/94	106/102	-	101/97	109/105	-	dB
	unweighted	95/91	103/99	-	98/94	106/102	-	dB
16-Bit	A-weighted	87	95	-	87	95	-	dB
	unweighted	84	92	-	84	92	-	dB
Total Harmonic Distortion + Noise		-	-90/-88	-82/-80	-	-90/-88	-82/-80	dB
Full-scale Output Voltage		1.48•VA/ 0.74•VA	1.56•VA/ 0.78•VA	1.64•VA/ 0.82•VA	1.48•VA/ 0.74•VA	1.56•VA/ 0.78•VA	1.64•VA/ 0.82•VA	Vpp
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)(Note 19)		3	-	-	3	-	-	kΩ
Load Capacitance (C_L)(Note 19)		-	-	100	-	-	100	pF
Parallel DC-Load Resistance(Note 20)		10	-	-	10	-	-	kΩ
Output Impedance		-	100	-	-	100	-	Ω
PSRR (Note 21)	1 kHz	-	60	-	-	60	-	dB
	60 Hz	-	60	-	-	60	-	dB

Notes:

18. One LSB of triangular PDF dither added to data.
19. Loading configuration is given in Figure 5 below.

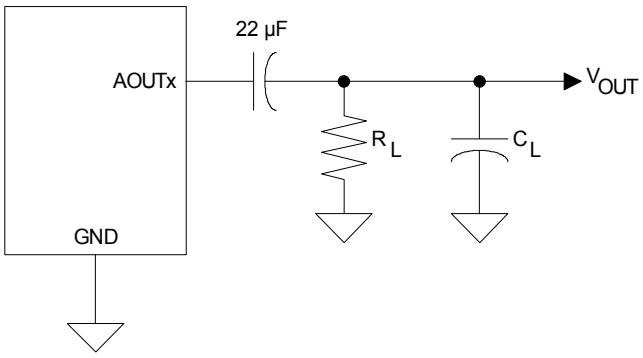


Figure 5. Equivalent Output Test Load

20. Parallel combination of all DAC DC loads. See Section 4.2.3.
21. Valid with the recommended capacitor values on FILT+ and VQ. See Figure 4 for test configuration.

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Test Conditions (unless otherwise specified): VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC. The filter characteristics have been normalized to the sample rate (F_S) and can be referenced to the desired sample rate by multiplying the given characteristic by F_S.

Parameter		Min	Typ	Max	Unit
Single-Speed Mode					
Passband (Note 22)	to -0.05 dB corner	0	-	0.4780	F_S
	to -3 dB corner	0	-	0.4996	F_S
Frequency Response 20 Hz to 20 kHz		-0.01	-	+0.12	dB
StopBand		0.5465	-	-	F_S
StopBand Attenuation	(Note 23)	102	-	-	dB
DAC1-4 Group Delay (Note 24)		-	11/Fs	-	s
Double-Speed Mode					
Passband (Note 22)	to -0.1 dB corner	0	-	0.4650	F_S
	to -3 dB corner	0	-	0.4982	F_S
Frequency Response 20 Hz to 20 kHz		-0.05	-	+0.2	dB
StopBand		0.5770	-	-	F_S
StopBand Attenuation	(Note 23)	80	-	-	dB
DAC1-4 Group Delay (Note 24)		-	7/Fs	-	s

Notes:

22. Response is clock-dependent and will scale with F_S.
23. For Single-Speed Mode, the measurement bandwidth is 0.5465 F_S to 3 F_S.
    For Double-Speed Mode, the measurement bandwidth is 0.577 F_S to 1.4 F_S.
24. The DAC group delay is measured from the FS/LRCK transition (rising or falling) before the first bit of a (group of) sample(s) is transmitted on the SDINx pins to the time it appears on the AOUTx pins.

DIGITAL I/O CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage (all input pins except $\overline{RST}$) (VL = 1.8 V)	(% of VL)	V_{IH}	75%	-	-	V
High-Level Input Voltage (all input pins except $\overline{RST}$) (VL = 2.5 V, 3.3 V, or 5 V)	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage (all input pins except $\overline{RST}$)	(% of VL)	V_{IL}	-	-	30%	V
High-Level Input Voltage ($\overline{RST}$ pin)		V_{IH}	1.2	-	-	V
Low-Level Input Voltage ($\overline{RST}$ pin)		V_{IL}	-	-	0.3	V
High-Level Output Voltage at I_o = 2 mA	(% of VL)	V_{OH}	80%	-	-	V
Low-Level Output Voltage at I_o = 2 mA	(% of VL)	V_{OL}	-	-	20%	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF

SWITCHING CHARACTERISTICS - SERIAL AUDIO INTERFACE

VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.

Parameters		Symbol	Min	Max	Units
$\overline{RST}$ pin Low Pulse Width	(Note 25)		1	-	ms
MCLK Frequency	(Note 26)		7.68	25.6	MHz
MCLK Duty Cycle			45	55	%
SCLK Duty Cycle			45	55	%
Input Sample Rate (FS/LRCK pin)	Single-Speed Mode	F_S	30	50	kHz
	Double-Speed Mode	F_S	60	100	kHz
SCLK Falling Edge to SDOUTx Valid (VL = 1.8 V)		t_{dh2}	-	31	ns
SCLK Falling Edge to SDOUTx Valid (VL = 2.5 V)		t_{dh2}	-	22	ns
SCLK Falling Edge to SDOUTx Valid (VL = 3.3 V or 5 V)		t_{dh2}	-	17	ns
TDM Slave Mode					
SCLK Frequency	(Note 27)		256x	512x	F_S
FS/LRCK High Time Pulse	(Note 28)	t_{lpw}	$1/f_{SCLK}$	$(n-1)/f_{SCLK}$ (Note 29)	ns
FS/LRCK Rising Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SDINx Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
SDINx Hold Time After SCLK Rising Edge		t_{dh1}	5	-	ns
PCM Slave Mode					
SCLK Frequency			32x	64x	F_S
FS/LRCK Duty Cycle			45	55	%
FS/LRCK Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SDINx Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
SDINx Hold Time After SCLK Rising Edge		t_{dh1}	5	-	ns
PCM Master Mode					
SCLK Frequency			64x	64x	F_S
FS/LRCK Duty Cycle			45	55	%
FS/LRCK Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SDINx Setup Time Before SCLK Rising Edge		t_{ds}	5	-	ns
SDINx Hold Time After SCLK Rising Edge (VL = 1.8 V)		t_{dh1}	11	-	ns
SDINx Hold Time After SCLK Rising Edge (VL = 2.5 V, 3.3 V, or 5 V)		t_{dh1}	10	-	ns

Notes:

25. After applying power to the CS4244, $\overline{RST}$ should be held low until after the power supplies and MCLK are stable.
26. MCLK must be synchronous to and scale with F_S.
27. The SCLK frequency must remain less than or equal to the MCLK frequency. For this reason, SCLK may range from 256x to 512x only in single speed mode. In double speed mode, 256x is the only ratio supported.
28. The MSB of CH1 is always aligned with the second SCLK rising edge following FS/LRCK rising edge.
29. Where “n” is equal to the MCLK to LRCK ratio (set by the Master Clock Rate register bits), i.e. in 256x mode, n = 256, in 512x mode, n = 512, etc.

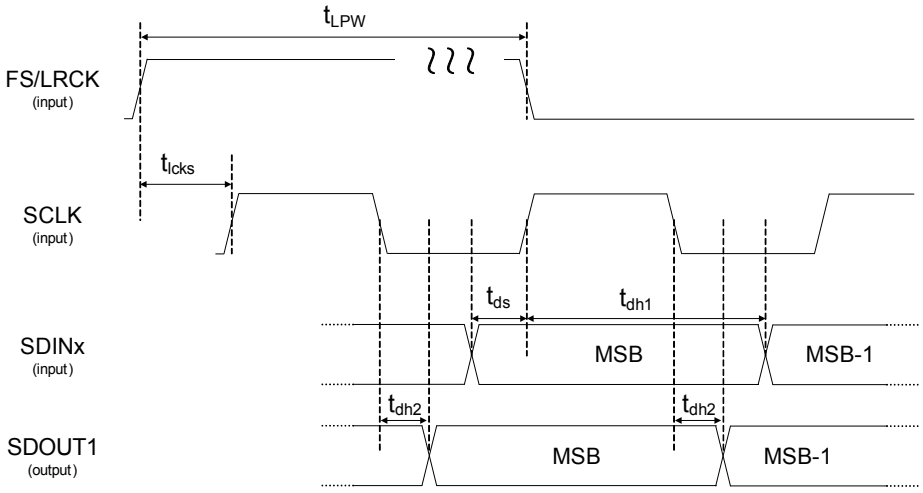


Figure 6. TDM Serial Audio Interface Timing

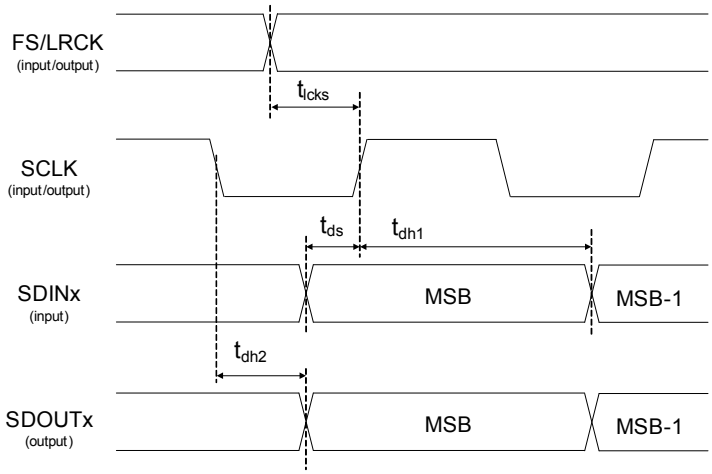


Figure 7. PCM Serial Audio Interface Timing

SWITCHING SPECIFICATIONS - CONTROL PORT

Test conditions (unless otherwise specified): Inputs: Logic 0 = GND = 0 V, Logic 1 = VL; SDA load capacitance equal to maximum value of C_b specified below (Note 30).

Parameters	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	550	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	(Note 31)	-	ns
Bus Free Time Between Transmissions	t_{buf}	1.3	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	0.6	-	µs
Clock Low time	t_{low}	1.3	-	µs
Clock High Time	t_{high}	0.6	-	µs
Setup Time for Repeated Start Condition	t_{sust}	0.6	-	µs
SDA Input Hold Time from SCL Falling (Note 32)	t_{hddi}	0	0.9	µs
SDA Output Hold Time from SCL Falling	t_{hddo}	0.2	0.9	µs
SDA Setup time to SCL Rising	t_{sud}	100	-	ns
Rise Time of SCL and SDA	t_r	-	300	ns
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	0.6	-	µs
SDA Bus Load Capacitance	C_b	-	400	pF
SDA Pull-Up Resistance	R_p	500	-	Ω

Notes:

30. All specifications are valid for the signals at the pins of the CS4244 with the specified load capacitance.
31. 2 ms + (3000/MCLK). See Section 4.2.1.
32. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

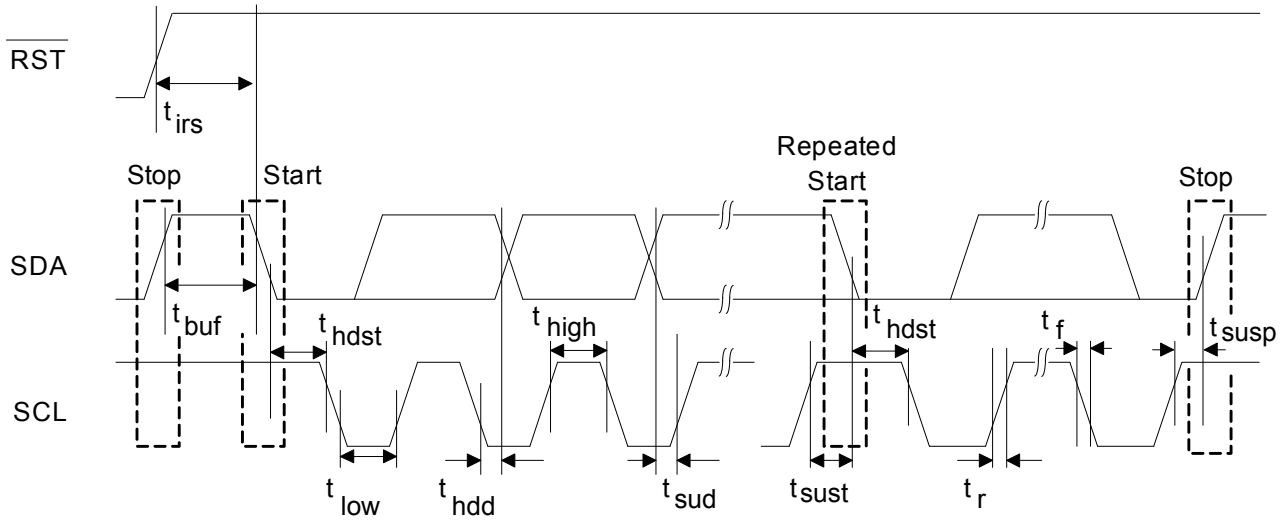


Figure 8. I²C Control Port Timing

4. APPLICATIONS

4.1 Power Supply Decoupling, Grounding, and PCB Layout

As with any high-resolution converter, the CS4244 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 2 shows the recommended power arrangements, with VA connected to clean supplies. VDREG, which powers the digital circuitry, is generated internally from an on-chip regulator from the VA supply. The VDREG pin provides a connection point for the decoupling capacitors, as shown in Figure 2.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as near to the pins of the CS4244 as possible. The low value ceramic capacitor should be the nearest to the pin and should be mounted on the same side of the board as the CS4244 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+, VBIAS, and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+, VBIAS, and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from their respective pins and GND.VA_SEL

For optimal heat dissipation from the package, it is recommended that the area directly under the device be filled with copper and tied to the ground plane. The use of vias connecting the topside ground to the backside ground is also recommended.

4.2 Recommended Power-up & Power-down Sequence

The initialization and Power-Up/Down sequence flow chart is shown in Figure 9. For the CS4244 Reset is defined as all lines held static, $\overline{\text{RST}}$ line is pulled low. Power Down is defined as all lines (excluding MCLK) held static, $\overline{\text{RST}}$ line is high, all PDNx bits are ‘1’. Running is defined as $\overline{\text{RST}}$ line high, all PDNx bits are ‘0’.

4.2.1 Power-up

The CS4244 enters a reset state upon the initial application of VA and VL. When these power supplies are initially applied to the device, the audio outputs, AOUTxx, are clamped to VQ which is initially low. Additionally, the interpolation and decimation filters, delta-sigma modulators and control port registers are all reset and the internal voltage reference, multi-bit digital-to-analog and analog-to-digital converters and low-pass filters are powered down. The device remains in the reset state until the $\overline{\text{RST}}$ pin is brought high.

Once $\overline{\text{RST}}$ is brought high, the control port address is latched after 2 ms + (3000/MCLK). Until this latching transition is complete, the device will not respond to I²C reads or writes, but the I²C bus may still be used during this time. Once the latching transition is complete, the address is latched and the control port is accessible. At this point and the desired register settings can be loaded per the interface descriptions detailed in the Section 4.3 I²C Control Port. To ensure specified performance and timing, the VA_SEL must be set to “0” for VA = 3.3 VDC and “1” for VA = 5.0 VDC before audio output begins.

After the $\overline{\text{RST}}$ pin is brought high and MCLK is applied, the outputs begin to ramp with VQ towards the nominal quiescent voltage. VQ will charge to VA/2 upon initial power up. The time that it takes to charge up to VA/2 is governed by the size of the capacitor attached to the VQ pin. With the capacitor value shown in the typical connection diagram, the charge time will be approximately 250 ms. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ, effectively blocking the quiescent DC voltage. Once FS/LRCK is valid, MCLK occurrences are counted over one F_S period to determine the MCLK/F_S ratio. With MCLK valid and any of the PDNx bits cleared, the internal voltage references will transition to their nominal voltage. Power is applied to the D/A converters and filters, and the analog outputs are un-clamped from the quiescent voltage, VQ. Afterwards, normal operation begins.

4.2.2 Power-down

To prevent audio transients at power-down, the DC-blocking capacitors must fully discharge before turning off the power. In order to do this in a controlled manner, it is recommended that all the converters be muted to start the sequence. Next, set PDNx for all converters to 1 to power them down internally. Then, FS/LRCK and SCLK can be removed if desired. Finally, the "VQ RAMP" bit in the "DAC Control 4" register must be set to '1' for a period of 50 ms before applying reset or removing power or MCLK. During this time, voltage on VQ and the audio outputs discharge gradually to GND. If power is removed before this 50 ms time period has passed, a transient will occur and a slight click or pop may be heard. There is no minimum time for a power cycle. Power may be re-applied at any time.

It is important to note that all clocks should be applied and removed in the order specified in Figure 9. If MCLK is removed or applied before $\overline{\text{RST}}$ has been pulled low, audible pops, clicks and/or distortion can result. If either SCLK or FS/LRCK is removed or applied before all PDNx bits are set to 1, audible pops, clicks and/or distortion can result.

Note: Timings are approximate and based upon the nominal value of the passive components specified in the "Typical Connection Diagram" on page 8. See Section 4.6.5.2 for volume ramp behavior.

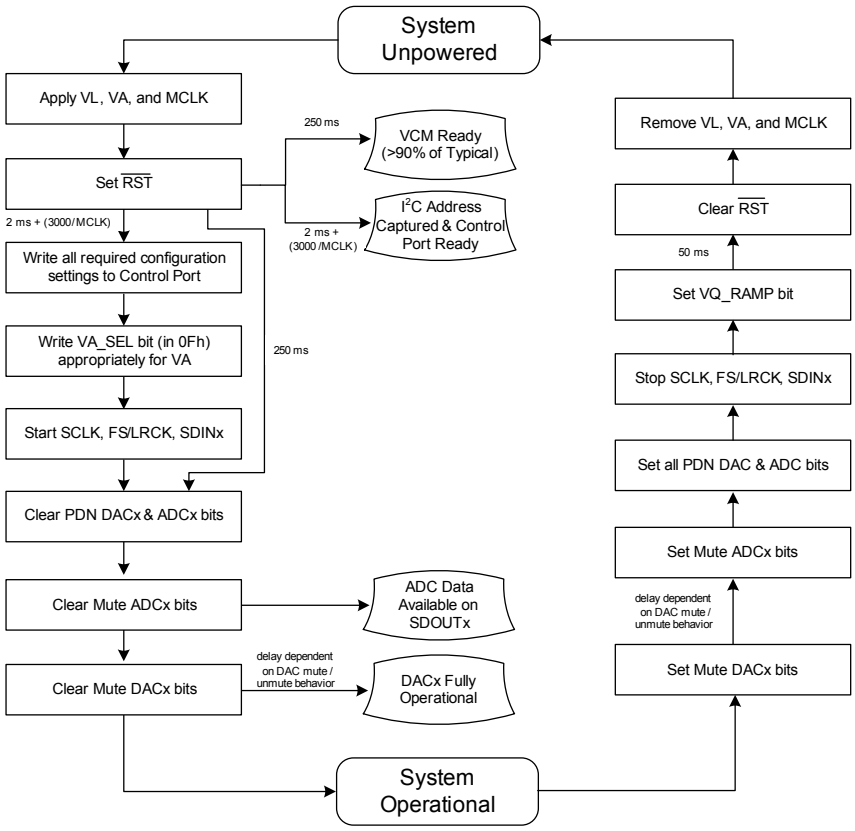


Figure 9. System Level Initialization and Power-Up/Down Sequence

4.2.3 DAC DC Loading

Figure 10 shows the analog output configuration during power-up, with the AOUTx± pins clamped to VQ to prevent pops and clicks. Thus any DC loads (RL_x) on the output pins will be in parallel when the switches are closed. These DC loads will pull the VQ voltage down towards ground. If the parallel combination of all DC loads exceeds the specification shown in the Analog Output Characteristics tables on pages 16

and 17, the VQ voltage will never rise to its minimum operating voltage. If the VQ voltage never rises above this minimum operating voltage, the device will not finish the power-up sequence and normal operation will not begin.

Also note that any AOUTx± pin(s) with a DC load must remain powered up (PDN DACx = 0) to keep the VQ net at its nominal voltage during normal operation, otherwise clipping may occur on the outputs.

Note that the load capacitors (CL_x) are also in parallel during power-up. The amount of total capacitance on the VQ net during power-up will affect the amount of time it takes for the VQ voltage to rise to its nominal operating voltage after VA power is applied. The time period can be calculated using the time constant given by the internal series resistor and the load capacitors.

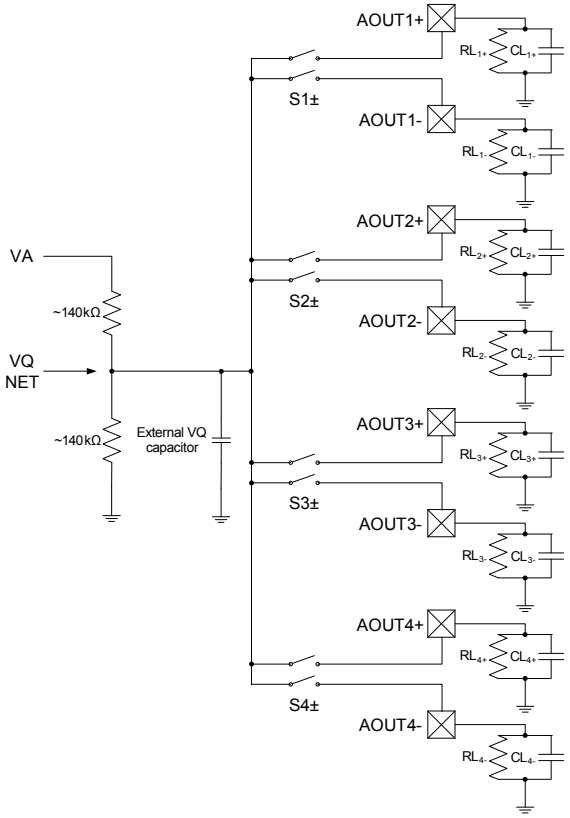


Figure 10. DAC DC Loading

4.3 I²C Control Port

All device configuration is achieved via the I²C control port registers as described in the Switching Specifications - Control Port table. The operation via the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the I²C pins should remain static if no operation is required. The CS4244 acts as an I²C slave device.

SDA is a bidirectional data line. Data is clocked into and out of the device by the clock, SCL. The AD0 and AD1 pins form the two least significant bits of the chip address and should be connected through a resistor to VL or GND as desired. The SDOUT2 pin is used to set the AD2 bit by connecting a resistor from the SDOUT2 pin to VL or to GND. The state of these pins are sensed after the CS4244 is released from reset.

The signal timings for a read and write cycle are shown in Figure 11 and Figure 12. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS4244 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 4 bits of the 7-bit address field are fixed at 0010. To communicate with a CS4244, the chip address field, which is the first byte sent to the CS4244, should match 0010 followed by the settings of the ADx pins. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS4244 after each input byte is read, and is input to the CS4244 from the microcontroller after each transmitted byte.

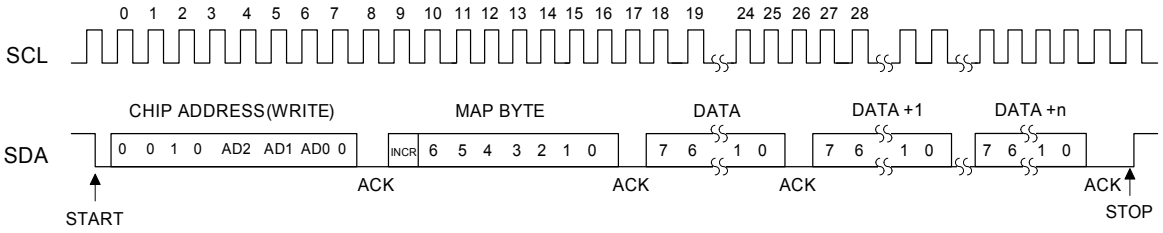


Figure 11. Timing, I²C Write

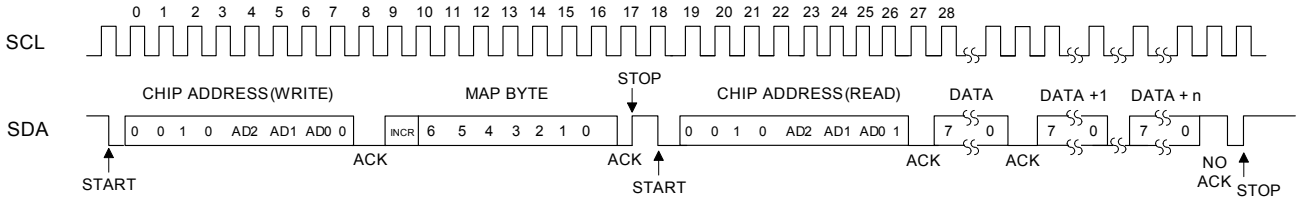


Figure 12. Timing, I²C Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 12, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.
Send 0010xxx0 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 0010xxx1 (chip address & read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.