Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CS4245

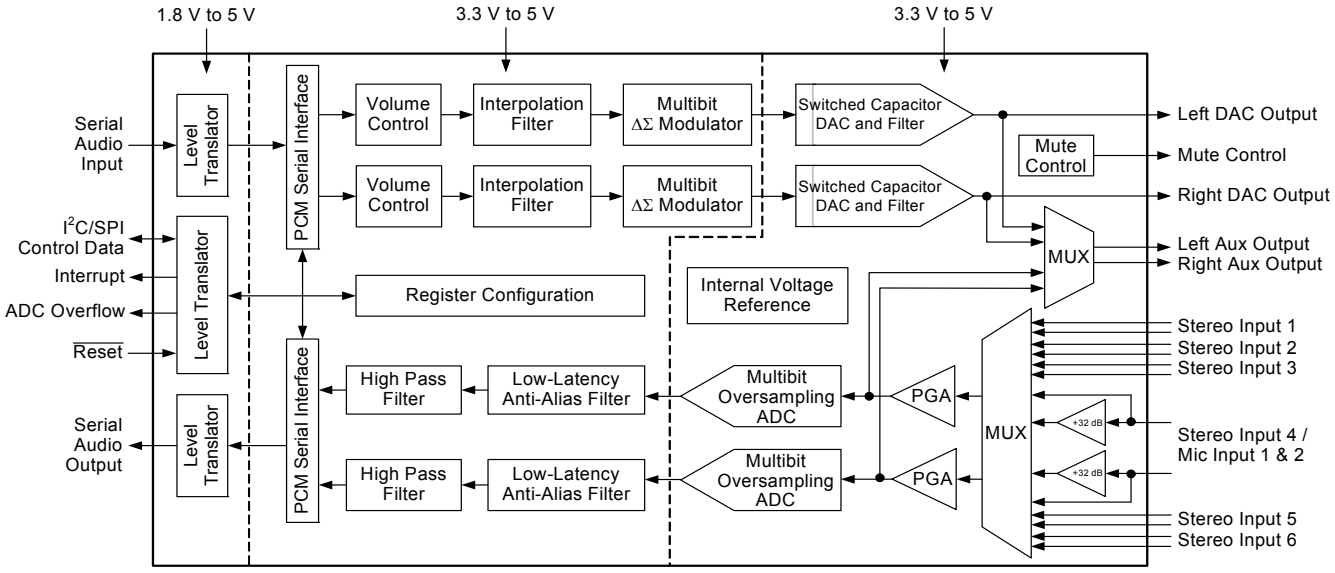
104 dB, 24-Bit, 192 kHz Stereo Audio CODEC

D/A Features

- Multi-bit Delta Sigma Modulator
- 104 dB Dynamic Range
- -90 dB THD+N
- Up to 192 kHz Sampling Rates
- Single-Ended Analog Architecture
- Volume Control with Soft Ramp
  - 0.5 dB Step Size
  - Zero Crossing, Click-Free Transitions
- Popguard® Technology
  - Minimizes the Effects of Output Transients
- Filtered Line-Level Outputs
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I²S up to 24-bit
  - Right-Justified 16-, 18-, 20-, and 24-bit
- Selectable 50/15 µs De-Emphasis
- Control Output for External Muting

A/D Features

- Multi-bit Delta Sigma Modulator
- 104 dB Dynamic Range
- -95 dB THD+N
- Stereo 6:1 Input Multiplexer
- Programmable Gain Amplifier (PGA)
  - ± 12 dB Gain, 0.5 dB Step Size
  - Zero Crossing, Click-Free Transitions
- Stereo Microphone Inputs
  - +32 dB Gain Stage
  - Low-Noise Bias Supply
- Up to 192 kHz Sampling Rates
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I²S up to 24-bit
- High-Pass Filter or DC Offset Calibration



System Features

- Direct Interface with 1.8 V to 5 V Logic Levels
- Optional Asynchronous Serial Port Operation
  - Each Serial Port Supports Master or Slave Operation
- Selectable Auxiliary Analog Output
  - Allows Analog Monitoring of Either the ADC Input Signal after PGA or DAC Output Signal
- Internal Digital Loopback
- Power-Down Mode
  - Available for A/D, D/A, CODEC, Mic Preamplifier
- +3.3 V to +5 V Analog Power Supply
- +3.3 V to +5 V Digital Power Supply
- Supports I²C® and SPI™ Control Port Interfaces
- Pin-Compatible with CS5345

General Description

The CS4245 is a highly integrated stereo audio CODEC. The CS4245 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 192 kHz.

A 6:1 stereo input multiplexer is included for selecting between line-level or microphone-level inputs. The microphone input path includes a +32 dB gain stage and a low-noise bias voltage supply. The PGA is available for line or microphone inputs and provides gain/attenuation of ±12 dB in 0.5 dB steps.

The output of the PGA is followed by an advanced 5th-order, multi-bit delta sigma modulator and digital filtering/decimation. Sampled data is transmitted by the serial audio interface at rates from 4 kHz to 192 kHz in either Slave or Master Mode.

The D/A converter is based on a 4th-order multi-bit delta sigma modulator with an ultra-linear low-pass filter and offers a volume control that operates with a 0.5 dB step size. It incorporates selectable soft ramp and zero crossing transition functions to eliminate clicks and pops.

Standard 50/15 µs de-emphasis is available for a 44.1 kHz sample rate for compatibility with digital audio programs mastered using the 50/15 µs pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4245 and other devices operating over a wide range of logic levels.

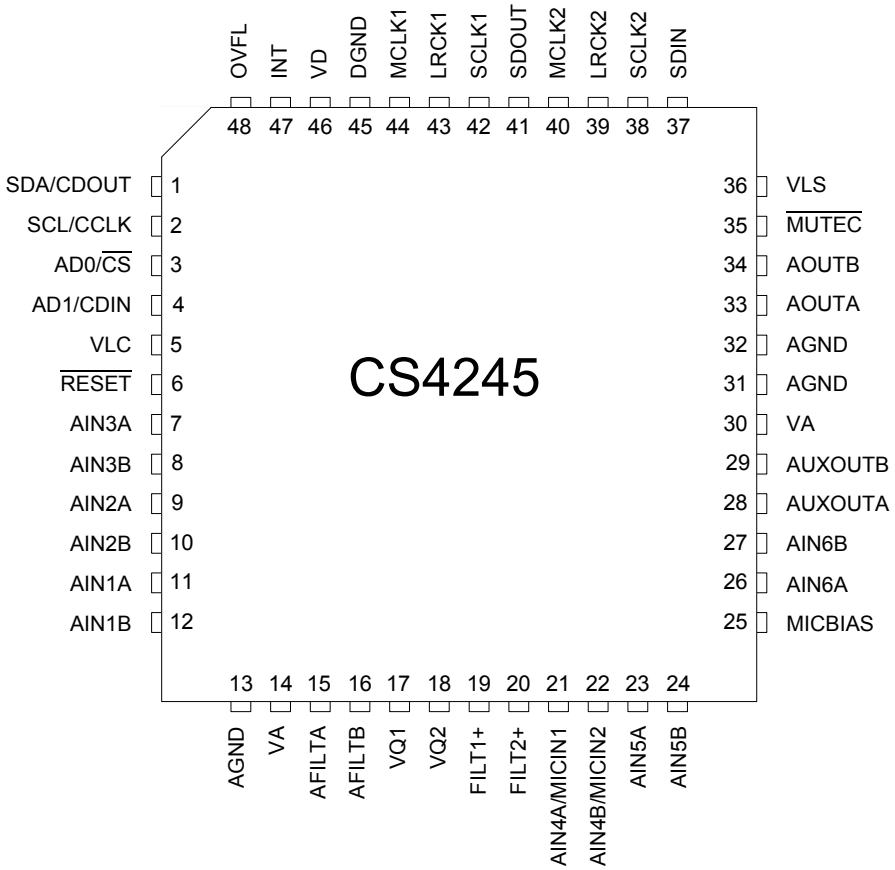
The CS4245 is available in a 48-pin LQFP package in both Commercial (-10° to +70° C) and Automotive (-40° to +105° C) grade. The CDB4245 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 58 for complete details.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDA/CDOUT	1	**Serial Control Data** (*Input/Output*) - SDA is a data I/O in I²C Mode. CDOUT is the output data line for the control port interface in SPI Mode.
SCL/CCLK	2	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
AD0/$\overline{CS}$	3	**Address Bit 0 (I²C)** / **Control Port Chip Select (SPI)** *(Input)* - AD0 is a chip address pin in I²C Mode; $\overline{CS}$ is the chip-select signal for SPI format.
AD1/CDIN	4	**Address Bit 1 (I²C)** / **Serial Control Data Input (SPI)** *(Input)* - AD1 is a chip address pin in I²C Mode; CDIN is the input data line for the control port interface in SPI Mode.
VLC	5	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port interface. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{RESET}$	6	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
AIN3A AIN3B	7, 8	**Stereo Analog Input 3** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN2A AIN2B	9, 10	**Stereo Analog Input 2** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN1A AIN1B	11, 12	**Stereo Analog Input 1** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.

AGND	13	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
VA	14	**Analog Power** *(Input)* - Positive power for the internal analog section.
AFILTA	15	**Antialias Filter Connection** (*Output*) - Antialias filter connection for the channel A ADC input.
AFILTB	16	**Antialias Filter Connection** (*Output*) - Antialias filter connection for the channel B ADC input.
VQ1	17	**Quiescent Voltage 1** (*Output*) - Filter connection for the internal quiescent reference voltage.
VQ2	18	**Quiescent Voltage 2** (*Output*) - Filter connection for the internal quiescent reference voltage.
FILT1+	19	**Positive Voltage Reference 1** (*Output*) - Positive reference voltage for the internal sampling circuits.
FILT2+	20	**Positive Voltage Reference 2** (*Output*) - Positive reference voltage for the internal sampling circuits.
AIN4A/MICIN1 AIN4B/MICIN2	21, 22	**Stereo Analog Input 4** / **Microphone Input 1 & 2** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN5A AIN5B	23, 24	**Stereo Analog Input 5** (*Input*) **-** The full-scale level is specified in the ADC Analog Characteristics specification table.
MICBIAS	25	**Microphone Bias Supply** (*Output*) **-** Low-noise bias supply for external microphone. Electrical characteristics are specified in the DC Electrical Characteristics specification table.
AIN6A AIN6B	26, 27	**Stereo Analog Input 6** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AUXOUTA AUXOUTB	28, 29	**Auxiliary Analog Audio Output** (*Output*) - Analog output from either the DAC, the PGA block, or high impedance. See "Auxiliary Output Source Select (Bits 6:5)" on page 46.
VA	30	**Analog Power** *(Input)* - Positive power for the internal analog section.
AGND	31, 32	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
AOUTA AOUTB	33, 34	**DAC Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.
$\overline{\text{MUTEC}}$	35	**Mute Control** *(Output)* - This pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
VLS	36	**Serial Audio Interface Power** (*Input*) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
SDIN	37	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK2	38	**Serial Port 2 Serial Bit Clock** *(Input/Output)* - Serial bit clock for serial audio interface 2.
LRCK2	39	**Serial Port 2 Left Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio input data line.
MCLK2	40	**Master Clock 2** (*Input*) - Optional asynchronous clock source for the DAC's delta-sigma modulators.
SDOUT	41	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
SCLK1	42	**Serial Port 1 Serial Bit Clock** *(Input/Output)* **-** Serial bit clock for serial audio interface 1.
LRCK1	43	**Serial Port 1 Left Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio output data line.
MCLK1	44	**Master Clock 1** (*Input*) - Clock source for the ADC's delta-sigma modulators. By default, this signal also clocks the DAC's delta-sigma modulators.
DGND	45	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VD	46	**Digital Power** (*Input*) - Positive power for the internal digital section.
INT	47	**Interrupt** (*Output*) - Indicates an interrupt condition has occurred.
OVFL	48	**ADC Overflow** (*Output*) - Indicates an ADC overflow condition is present.

2. CHARACTERISTICS AND SPECIFICATIONS

SPECIFIED OPERATING CONDITIONS

AGND = DGND = 0 V; All voltages with respect to ground.

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Analog	VA	3.13	5.0	5.25	V
	Digital	VD	3.13	3.3	(Note 1)	V
	Logic - Serial Port	VLS	1.71	3.3	5.25	V
	Logic - Control Port	VLC	1.71	3.3	5.25	V
Ambient Operating Temperature (Power Applied)		T_A	-10	-	+70	°C

Notes: 1. Maximum of VA+0.25 V or 5.25 V, whichever is less.

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V All voltages with respect to ground. (Note 2)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	VA	-0.3	+6.0	V
	Digital	VD	-0.3	+6.0	V
	Logic - Serial Port	VLS	-0.3	+6.0	V
	Logic - Control Port	VLC	-0.3	+6.0	V
Input Current	(Note 3)	I_{in}	-	±10	mA
Analog Input Voltage		V_{INA}	AGND-0.3	VA+0.3	V
Digital Input Voltage	Logic - Serial Port	V_{IND-S}	-0.3	VLS+0.3	V
	Logic - Control Port	V_{IND-C}	-0.3	VLC+0.3	V
Ambient Operating Temperature (Power Applied)		T_A	-50	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

2. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
3. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

DAC ANALOG CHARACTERISTICS

Test Conditions (unless otherwise specified): AGND = DGND = 0 V; VA = 3.13 V to 5.25 V; VD = 3.13 V to 5.25 V or VA + 0.25 V, whichever is less; VLS = VLC = 1.71 V to 5.25 V; T_A = -10° to +70° C for Commercial or -40° to +85° C for Automotive; Output test signal: 997 Hz full-scale sine wave; Test load R_L = 3 kΩ, C_L = 10 pF (see Figure 1), Fs = 48/96/192 kHz. Measurement Bandwidth 10 Hz to 20 kHz Synchronous mode; All Connections as shown in Figure 12 on page 29.

Parameter			Symbol	Commercial Grade			Automotive Grade			Unit
				Min	Typ	Max	Min	Typ	Max	
Dynamic Performance for VA = 4.75 V to 5.25 V										
Dynamic Range		(Note 4)								
	18 to 24-Bit	A-Weighted		98	104	-	96	104	-	dB
		unweighted		95	101	-	93	101	-	dB
	16-Bit	A-Weighted		90	96	-	88	96	-	dB
		unweighted		87	93	-	85	93	-	dB
Total Harmonic Distortion + Noise		(Note 4)								
	18 to 24-Bit	0 dB		-	-90	-84	-	-90	-82	dB
		-20 dB		-	-81	-	-	-81	-	dB
		-60 dB	THD+N	-	-41	-	-	-41	-	dB
	16-Bit	0 dB		-	-93	-87	-	-93	-85	dB
		-20 dB		-	-73	-	-	-73	-	dB
		-60 dB		-	-33	-	-	-33	-	dB
Dynamic Performance for VA = 3.13 V to 3.46 V										
Dynamic Range		(Note 4)								
	18 to 24-Bit	A-Weighted		95	101	-	93	101	-	dB
		unweighted		92	98	-	90	98	-	dB
	16-Bit	A-Weighted		88	93	-	86	93	-	dB
		unweighted		85	90	-	83	90	-	dB
Total Harmonic Distortion + Noise		(Note 4)								
	18 to 24-Bit	0 dB		-	-87	-79	-	-87	-77	dB
		-20 dB		-	-78	-	-	-78	-	dB
		-60 dB	THD+N	-	-38	-	-	-38	-	dB
	16-Bit	0 dB		-	-90	-82	-	-90	-80	dB
		-20 dB		-	-70	-	-	-70	-	dB
		-60 dB		-	-30	-	-	-30	-	dB
Interchannel Isolation		(1 kHz)		-	100	-	-	100	-	dB
DC Accuracy										
Interchannel Gain Mismatch				-	0.1	0.25	-	0.1	0.25	dB
Gain Drift				-	100	-	-	100	-	ppm/°C
Analog Output										
Full Scale Output Voltage				0.60*VA	0.65*VA	0.70*VA	0.60*VA	0.65*VA	0.70*VA	V_{pp}
DC Current draw from an AOUT pin		(Note 5)	I_{OUT}	-	-	10	-	-	10	µA
AC-Load Resistance		(Note 6)	R_L	3	-	-	3	-	-	kΩ
Load Capacitance		(Note 6)	C_L	-	-	100	-	-	100	pF
Output Impedance			Z_{OUT}	-	150	-	-	150	-	Ω

4. One-half LSB of triangular PDF dither added to data.
5. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC blocking capacitors.

6. Guaranteed by design. See Figure 2. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability. C_L affects the dominant pole of the internal output amp; increasing C_L beyond 100 pF can cause the internal op-amp to become unstable.

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 7,10)		Symbol	Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter Response			***Single-Speed Mode***			
Passband (Note 7)	to -0.1 dB corner to -3 dB corner		0 0	- -	0.35 0.4992	Fs Fs
Frequency Response 10 Hz to 20 kHz			-0.175	-	+0.01	dB
StopBand			0.5465	-	-	Fs
StopBand Attenuation	(Note 8)		50	-	-	dB
Group Delay		tgd	-	10/Fs	-	s
De-emphasis Error (Note 9)	Fs = 44.1 kHz		-	-	+0.05/-0.25	dB
Combined Digital and On-chip Analog Filter Response			***Double-Speed Mode***			
Passband (Note 7)	to -0.1 dB corner to -3 dB corner		0 0	- -	0.22 0.501	Fs Fs
Frequency Response 10 Hz to 20 kHz			-0.15	-	+0.15	dB
StopBand			0.5770	-	-	Fs
StopBand Attenuation	(Note 8)		55	-	-	dB
Group Delay		tgd	-	5/Fs	-	s
Combined Digital and On-chip Analog Filter Response			***Quad-Speed Mode***			
Passband (Note 7)	to -0.1 dB corner to -3 dB corner		0 0	- -	0.110 0.469	Fs Fs
Frequency Response 10 Hz to 20 kHz			-0.12	-	0	dB
StopBand			0.7	-	-	Fs
StopBand Attenuation	(Note 8)		51	-	-	dB
Group Delay		tgd	-	2.5/Fs	-	s

7. Filter response is guaranteed by design.
8. For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
   For Double-Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
   For Quad-Speed Mode, the Measurement Bandwidth is 0.7 Fs to 1 Fs.
9. De-emphasis is available only in Single-Speed Mode.
10. Response is clock dependent and will scale with Fs. Note that the amplitude vs. frequency plots of this data (Figures 21 to 30) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

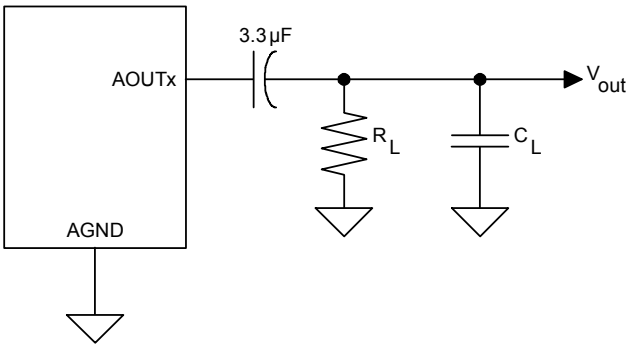


Figure 1. DAC Output Test Load

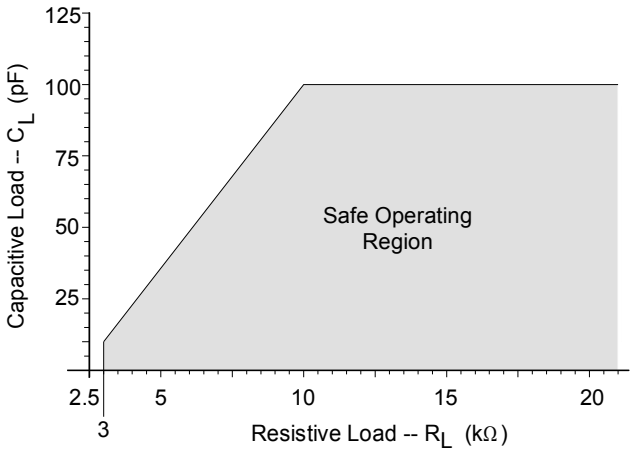


Figure 2. Maximum DAC Loading

ADC ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VA = 3.13 V to 5.25 V; VD = 3.13 V to 5.25 V or VA + 0.25 V, whichever is less; VLS = VLC = 1.71 V to 5.25 V; T_A = -10° to +70° C for Commercial or -40° to +85° C for Automotive; Input test signal: 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Fs = 48/96/192 kHz. Synchronous mode; All connections as shown in Figure 12 on page 29.

Line-Level Inputs					
Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance for VA = 4.75 V to 5.25 V					
Dynamic Range					
PGA Setting: -12 dB to +6 dB					
A-weighted		98	104	-	dB
unweighted		95	101	-	dB
(Note 13) 40 kHz bandwidth unweighted		-	98	-	dB
PGA Setting: +12 dB Gain					
A-weighted		92	98	-	dB
unweighted		89	95	-	dB
(Note 13) 40 kHz bandwidth unweighted		-	92	-	dB
Total Harmonic Distortion + Noise (Note 12)					
PGA Setting: -12 dB to +6 dB					
-1 dB		-	-95	-89	dB
-20 dB		-	-81	-	dB
-60 dB		-	-41	-	dB
(Note 13) 40 kHz bandwidth -1 dB	THD+N	-	-92	-	dB
PGA Setting: +12 dB Gain					
-1 dB		-	-92	-86	dB
-20 dB		-	-75	-	dB
-60 dB		-	-35	-	dB
(Note 13) 40 kHz bandwidth -1 dB		-	-89	-	dB
Dynamic Performance for VA = 3.13 V to 3.46 V					
Dynamic Range					
PGA Setting: -12 dB to +6 dB					
A-weighted		93	101	-	dB
unweighted		90	98	-	dB
(Note 13) 40 kHz bandwidth unweighted		-	95	-	dB
PGA Setting: +12 dB Gain					
A-weighted		89	95	-	dB
unweighted		86	92	-	dB
(Note 13) 40 kHz bandwidth unweighted		-	89	-	dB
Total Harmonic Distortion + Noise (Note 12)					
PGA Setting: -12 dB to +6 dB					
-1 dB		-	-92	-86	dB
-20 dB		-	-78	-	dB
-60 dB		-	-38	-	dB
(Note 13) 40 kHz bandwidth -1 dB	THD+N	-	-84	-	dB
PGA Setting: +12 dB Gain					
-1 dB		-	-89	-83	dB
-20 dB		-	-72	-	dB
-60 dB		-	-32	-	dB
(Note 13) 40 kHz bandwidth -1 dB		-	-81	-	dB

Line-Level Inputs					
		Commercial Grade			
Parameter	Symbol	Min	Typ	Max	Unit
Interchannel Isolation		-	90	-	dB

DC Accuracy					
Gain Error		-	-	±10	%
Gain Drift		-	±100	-	ppm/°C
Line-Level Input Characteristics					
Full-scale Input Voltage		0.51*VA	0.57*VA	0.63*VA	V_{pp}
Input Impedance (Note 11)		6.12	6.8	7.48	kΩ
Maximum Interchannel Input Impedance Mismatch		-	5	-	%

Line-Level and Microphone-Level Inputs

Parameter	Symbol	Commercial Grade			Unit
		Min	Typ	Max	
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Programmable Gain Characteristics					
Gain Step Size		-	0.5	-	dB
Absolute Gain Step Error		-	-	0.4	dB

11. Valid for the selected input pair.

ADC ANALOG CHARACTERISTICS

(Continued)

Microphone-Level Inputs					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Performance for VA = 4.75 V to 5.25 V					
Dynamic Range					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 12)					
PGA Setting: -12 dB to 0 dB					
-1 dB	THD+N	-	-80	-74	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB
Dynamic Performance for VA = 3.13 V to 3.46 V					
Dynamic Range					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 12)					
PGA Setting: -12 dB to 0 dB					
-1 dB	THD+N	-	-80	-74	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB
Interchannel Isolation		-	80	-	dB
DC Accuracy					
Gain Error		-	±5	-	%
Gain Drift		-	±300	-	ppm/°C
Microphone-Level Input Characteristics					
Full-scale Input Voltage		0.013*VA	0.017*VA	0.021*VA	V_{pp}
Input Impedance (Note 14)		-	60	-	kΩ

12. Referred to the typical line-level full-scale input voltage
13. Valid for Double- and Quad-Speed Modes only.
14. Valid when the microphone-level inputs are selected.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Notes 15, 17)			Symbol	Min	Typ	Max	Unit
Single-Speed Mode							
Passband	(-0.1 dB)			0	-	0.4896	Fs
Passband Ripple				-	-	0.035	dB
Stopband				0.5688	-	-	Fs
Stopband Attenuation				70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	12/Fs	-	s
Double-Speed Mode							
Passband	(-0.1 dB)			0	-	0.4896	Fs
Passband Ripple				-	-	0.025	dB
Stopband				0.5604	-	-	Fs
Stopband Attenuation				69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	9/Fs	-	s
Quad-Speed Mode							
Passband	(-0.1 dB)			0	-	0.2604	Fs
Passband Ripple				-	-	0.025	dB
Stopband				0.5000	-	-	Fs
Stopband Attenuation				60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	5/Fs	-	s
High-Pass Filter Characteristics							
Frequency Response	-3.0 dB			-	1	-	Hz
	-0.13 dB	(Note 16)			20	-	Hz
Phase Deviation	@ 20 Hz	(Note 16)		-	10	-	Deg
Passband Ripple				-	-	0	dB
Filter Settling Time					10^5/Fs		s

15. Filter response is guaranteed by design.
16. Response shown is for Fs = 48 kHz.
17. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 33 to 44) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

AUXILIARY OUTPUT ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VA = 3.13 V to 5.25 V; VD = 3.13 V to 5.25 V or VA + 0.25 V, whichever is less; VLS = VLC = 1.71 V to 5.25 V; T_A = -10° to +70° C for Commercial or -40° to +85° C for Automotive; Input test signal: 1 kHz sine wave; Measurement bandwidth: 10 Hz to 20 kHz; Fs = 48/96/192 kHz; Synchronous mode; All connections as shown in Figure 12 on page 29.

VA = 4.75 V to 5.25 V								
		Commercial Grade			Automotive Grade			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Dynamic Performance with PGA Output Selected, Line Level Input								
Dynamic Range								
PGA Setting: -12 dB to +6 dB								
A-weighted		98	104	-	96	104	-	dB
unweighted		95	101	-	93	101	-	dB
PGA Setting: +12 dB Gain								
A-weighted		92	98	-	90	98	-	dB
unweighted		89	95	-	87	95	-	dB
Total Harmonic Distortion + Noise (Note 19)								
PGA Setting: -12 dB to +6 dB								
-1 dB		-	-80	-74	-	-80	-72	dB
-20 dB		-	-81	-	-	-81	-	dB
-60 dB	THD+N	-	-41	-	-	-41	-	dB
PGA Setting: +12 dB Gain								
-1 dB		-	-80	-74	-	-80	-72	dB
-20 dB		-	-75	-	-	-75	-	dB
-60 dB		-	-35	-	-	-35	-	dB
Dynamic Performance with PGA Output Selected, Mic Level Input								
Dynamic Range								
PGA Setting: -12 dB to 0 dB								
A-weighted		77	83	-	75	83	-	dB
unweighted		74	80	-	72	80	-	dB
PGA Setting: +12 dB								
A-weighted		65	71	-	63	71	-	dB
unweighted		62	68	-	60	68	-	dB
Total Harmonic Distortion + Noise (Note 19)								
PGA Setting: -12 dB to 0 dB								
-1 dB		-	-74	-68	-	-74	-66	dB
-20 dB	THD+N	-	-60	-	-	-60	-	dB
-60 dB		-	-20	-	-	-20	-	dB
PGA Setting: +12 dB								
-1 dB		-	-68	-	-	-68	-	dB
Dynamic Performance with DAC Output Selected								
Dynamic Range (Notes 18)								
18 to 24-Bit A-weighted		98	104	-	96	104	-	dB
unweighted		95	101	-	93	101	-	dB
16-Bit A-Weighted		90	96	-	88	96	-	dB
unweighted		87	93	-	85	93	-	dB
Total Harmonic Distortion + Noise (Notes 18, 20)								
18 to 24-Bit 0 dB		-	-80	-74	-	-80	-72	dB
-20 dB		-	-81	-	-	-81	-	dB
-60 dB	THD+N	-	-41	-	-	-41	-	dB
16-Bit 0 dB		-	-80	-74	-	-80	-72	dB
-20 dB		-	-73	-	-	-73	-	dB
-60 dB		-	-33	-	-	-33	-	dB

AUXILIARY OUTPUT ANALOG CHARACTERISTICS

(Continued)

VA = 3.13 V to 3.46 V								
		Commercial Grade			Automotive Grade			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Dynamic Performance with PGA Output Selected, Line Level Input								
Dynamic Range								
PGA Setting: -12 dB to +6 dB								
A-weighted		93	101	-	91	101	-	dB
unweighted		90	98	-	88	98	-	dB
PGA Setting: +12 dB Gain								
A-weighted		89	95	-	87	95	-	dB
unweighted		86	92	-	84	92	-	dB
Total Harmonic Distortion + Noise (Note 19)								
PGA Setting: -12 dB to +6 dB								
-1 dB		-	-80	-74	-	-80	-72	dB
-20 dB		-	-78	-	-	-78	-	dB
-60 dB	THD+N	-	-38	-	-	-38	-	dB
PGA Setting: +12 dB Gain								
-1 dB		-	-80	-74	-	-80	-72	dB
-20 dB		-	-72	-	-	-72	-	dB
-60 dB		-	-32	-	-	-32	-	dB
Dynamic Performance with PGA Output Selected, Mic Level Input								
Dynamic Range								
PGA Setting: -12 dB to 0 dB								
A-weighted		77	83	-	75	83	-	dB
unweighted		74	80	-	72	80	-	dB
PGA Setting: +12 dB								
A-weighted		65	71	-	63	71	-	dB
unweighted		62	68	-	60	68	-	dB
Total Harmonic Distortion + Noise (Note 19)								
PGA Setting: -12 dB to 0 dB								
-1 dB		-	-74	-68	-	-74	-66	dB
-20 dB	THD+N	-	-60	-	-	-60	-	dB
-60 dB		-	-20	-	-	-20	-	dB
PGA Setting: +12 dB								
-1 dB		-	-68	-	-	-68	-	dB
Dynamic Performance with DAC Output Selected								
Dynamic Range (Notes 18)								
18 to 24-Bit A-Weighted		95	101	-	93	101	-	dB
unweighted		92	98	-	90	98	-	dB
16-Bit A-Weighted		88	93	-	86	93	-	dB
unweighted		85	90	-	83	90	-	dB
Total Harmonic Distortion + Noise (Notes 18, 20)								
18 to 24-Bit 0 dB		-	-80	-74	-	-80	-72	dB
-20 dB		-	-78	-	-	-78	-	dB
-60 dB	THD+N	-	-38	-	-	-38	-	dB
16-Bit 0 dB		-	-80	-74	-	-80	-72	dB
-20 dB		-	-70	-	-	-70	-	dB
-60 dB		-	-30	-	-	-30	-	dB

18. One-half LSB of triangular PDF dither added to data.
19. Referred to the typical Line-Level Full-Scale Input Voltage.

20. Referred to the typical DAC Full-Scale Output Voltage.

AUXILIARY OUTPUT ANALOG CHARACTERISTICS

(Continued)

VA = 3.13 V to 5.25 V								
		Commercial Grade			Automotive Grade			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
DC Accuracy with PGA Output Selected, Line Level Input								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Error		-	±5	-	-	±5	-	%
Gain Drift		-	±100	-	-	±100	-	ppm/°C
DC Accuracy with PGA Output Selected, Mic Level Input								
Interchannel Gain Mismatch		-	0.3	-	-	0.3	-	dB
Gain Error		-	±5	-	-	±5	-	%
Gain Drift		-	±300	-	-	±300	-	ppm/°C
DC Accuracy with DAC Output Selected								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Analog Output								
Frequency Response 10 Hz to 20 kHz (Note 22)		-0.1dB	-	+0.1dB	-0.1dB	-	+0.1dB	dB
Analog In to Analog Out Phase Shift (Note 21)		-	180	-	-	180	-	deg
DC Current draw from an AUXOUT pin	I_{OUT}	-	-	1	-	-	1	µA
AC-Load Resistance	R_L	100	-	-	100	-	-	kΩ
Load Capacitance	C_L	-	-	20	-	-	20	pF

21. Valid only when PGA output is selected.
22. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS

AGND = DGND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Fs=48 kHz; Master Mode.

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA = 5 V	I_A	-	41	50	mA
(Normal Operation)	VA = 3.3 V	I_A	-	37	45	mA
	VD, VLS, VLC = 5 V	I_D	-	39	47	mA
	VD, VLS, VLC = 3.3 V	I_D	-	23	28	mA
Power Supply Current	VA = 5 V	I_A	-	0.50	-	mA
(Power-Down Mode) (Note 23)	VLS, VLC, VD=5 V	I_D	-	0.54	-	mA
Power Consumption						
(Normal Operation)	VA, VD, VLS, VLC = 5 V	-	-	400	485	mW
	VA, VD, VLS, VLC = 3.3 V	-	-	198	241	mW
(Power-Down Mode)	VA, VD, VLS, VLC = 5 V	-	-	4.2	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 24)	PSRR	-	55	-	dB
VQ Characteristics						
Quiescent Voltage 1		VQ1	-	0.5 x VA	-	VDC
DC Current from VQ1	(Note 25)	I_{Q1}	-	-	1	µA
VQ1 Output Impedance		Z_{Q1}	-	23	-	kΩ
Quiescent Voltage 2		VQ2	-	0.5 x VA	-	VDC
DC Current from VQ2	(Note 25)	I_{Q2}	-	-	1	µA
VQ2 Output Impedance		Z_{Q2}	-	4.5	-	kΩ
FILT1+ Nominal Voltage		FILT1+	-	VA	-	VDC
FILT2+ Nominal Voltage		FILT2+	-	VA	-	VDC
Microphone Bias Voltage		MICBIAS	-	0.8 x VA	-	VDC
Current from MICBIAS		I_{MB}	-	-	2	mA

23. Power-Down Mode is defines as $\overline{\text{RESET}}$ = Low with all clock and data lines held static and no analog input.
24. Valid with the recommended capacitor values on FILT1+, FILT2+, VQ1 and VQ2 as shown in the Typical Connection Diagram.
25. Guaranteed by design. The DC current draw represents the allowed current draw due to typical leakage through the electrolytic de-coupling capacitors.

DIGITAL INTERFACE CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VLS = VLC = 1.71 V to 5.25 V.

Parameters (Note 26)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage						
VL = 1.71 V	Serial Port	V_{IH}	0.8xVLS	-	-	V
	Control Port	V_{IH}	0.8xVLC	-	-	V
VL > 2.0 V	Serial Port	V_{IH}	0.7xVLS	-	-	V
	Control Port	V_{IH}	0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.2xVLS	V
	Control Port	V_{IL}	-	-	0.2xVLC	V
High-Level Output Voltage at I_o = 2 mA	Serial Port	V_{OH}	VLS-1.0	-	-	V
	Control Port	V_{OH}	VLC-1.0	-	-	V
	MUTEC	V_{OH}	VA-1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA	Serial Port	V_{OL}	-	-	0.4	V
	Control Port	V_{OL}	-	-	0.4	V
	MUTEC	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance	(Note 27)		-	-	1	pF
Maximum MUTEC Drive Current			-	3	-	mA
Minimum OVFL Active Time			$\frac{10^6}{LRCK1}$	-	-	µs

26. Serial Port signals include: MCLK1, MCLK2, SCLK1, SCLK2, LRCK1, LRCK2, SDIN, SDOUT. Control Port signals include: SCL/CCLK, SDA/CDOUT, AD0/CS, AD1/CDIN, RESET, INT, OVFL.
27. Guaranteed by design.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT 1

Logic '0' = DGND = AGND = 0 V; Logic '1' = VL, C_L = 20 pF. (Note 28)

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rate	Single Speed Mode	Fs	4	-	50	kHz
	Double Speed Mode	Fs	50	-	100	kHz
	Quad Speed Mode	Fs	100	-	200	kHz
MCLK Specifications						
MCLK1 Input Frequency		fmclk	1.024	-	51.200	MHz
MCLK1 Input Pulse Width High/Low		tclkhl	8	-	-	ns
Master Mode						
LRCK1 Duty Cycle			-	50	-	%
SCLK1 Duty Cycle			-	50	-	%
SCLK1 falling to LRCK1 edge		t_{slr}	-10	-	10	ns
SCLK1 falling to SDOUT valid		t_{sdo}	0	-	36	ns
Slave Mode						
LRCK1 Duty Cycle			40	50	60	%
SCLK1 Period						
	Single-Speed Mode	t_{sclkw}	$\frac{10^9}{(128)Fs}$	-	-	ns
	Double-Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
	Quad-Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
SCLK1 Pulse Width High		t_{sclkh}	30	-	-	ns
SCLK1 Pulse Width Low		t_{sclkl}	48	-	-	ns
SCLK1 falling to LRCK1 edge		t_{slr}	-10	-	10	ns
SCLK1 falling to SDOUT valid		t_{sdo}	0	-	36	ns

28. See Figure 3 and Figure 4 on page 23.

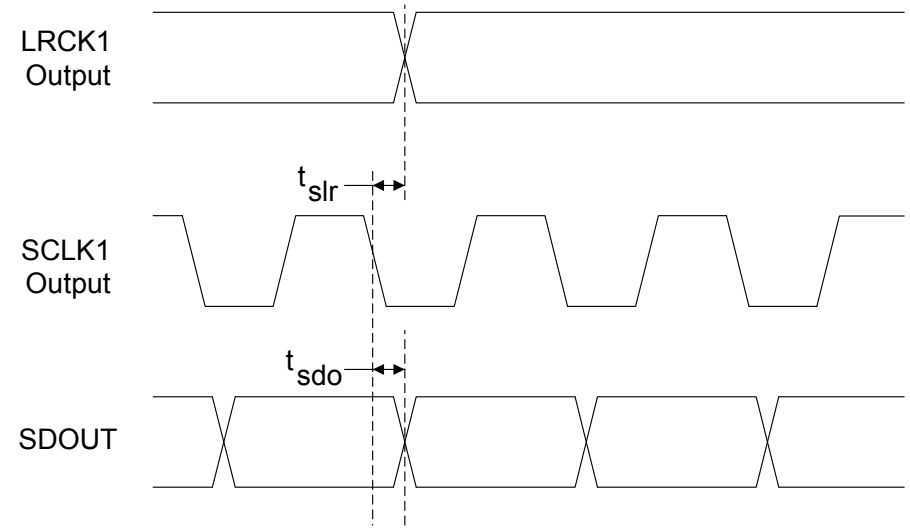


Figure 3. Master Mode Timing - Serial Audio Port 1

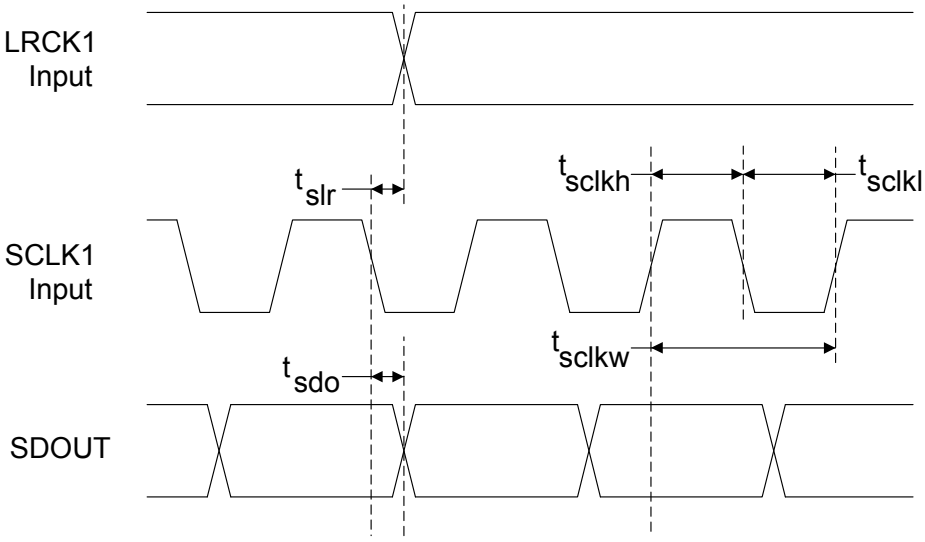


Figure 4. Slave Mode Timing - Serial Audio Port 1

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT 2

Logic '0' = DGND = AGND = 0 V; Logic '1' = VL, C_L = 20 pF. (Note 29)

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rate	Single Speed Mode	Fs	4	-	50	kHz
	Double Speed Mode	Fs	50	-	100	kHz
	Quad Speed Mode	Fs	100	-	200	kHz
MCLK Specifications						
MCLK2 Input Frequency		fmclk	1.024	-	51.200	MHz
MCLK2 Input Pulse Width High/Low		tclkhl	8	-	-	ns
Master Mode						
LRCK2 Duty Cycle			-	50	-	%
SCLK2 Duty Cycle			-	50	-	%
SCLK2 falling to LRCK edge		t_{slr}	-10	-	10	ns
SDIN valid to SCLK2 rising setup time		t_{sdis}	16	-	-	ns
SCLK2 rising to SDIN hold time		t_{sdih}	20	-	-	ns
Slave Mode						
LRCK2 Duty Cycle			40	50	60	%
SCLK2 Period						
	Single-Speed Mode	t_{sclkw}	$\frac{10^9}{(128)Fs}$	-	-	ns
	Double-Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
	Quad-Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
SCLK2 Pulse Width High		t_{sclkh}	30	-	-	ns
SCLK2 Pulse Width Low		t_{sclkl}	48	-	-	ns
SCLK2 falling to LRCK2 edge		t_{slr}	-10	-	10	ns
SDIN valid to SCLK2 rising setup time		t_{sdis}	16	-	-	ns
SCLK2 rising to SDIN hold time		t_{sdih}	20	-	-	ns

29. See Figure 5 and Figure 6 on page 25.

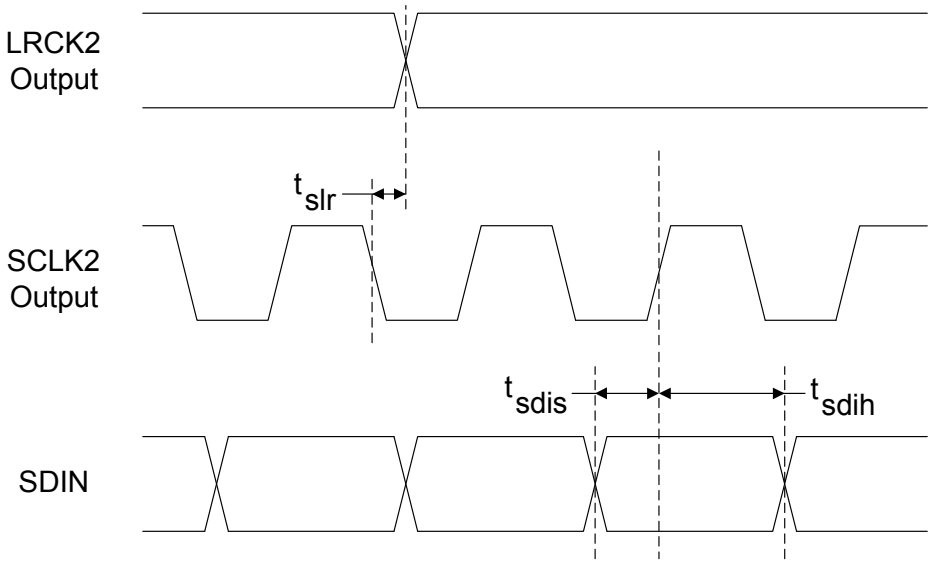


Figure 5. Master Mode Timing - Serial Audio Port 2

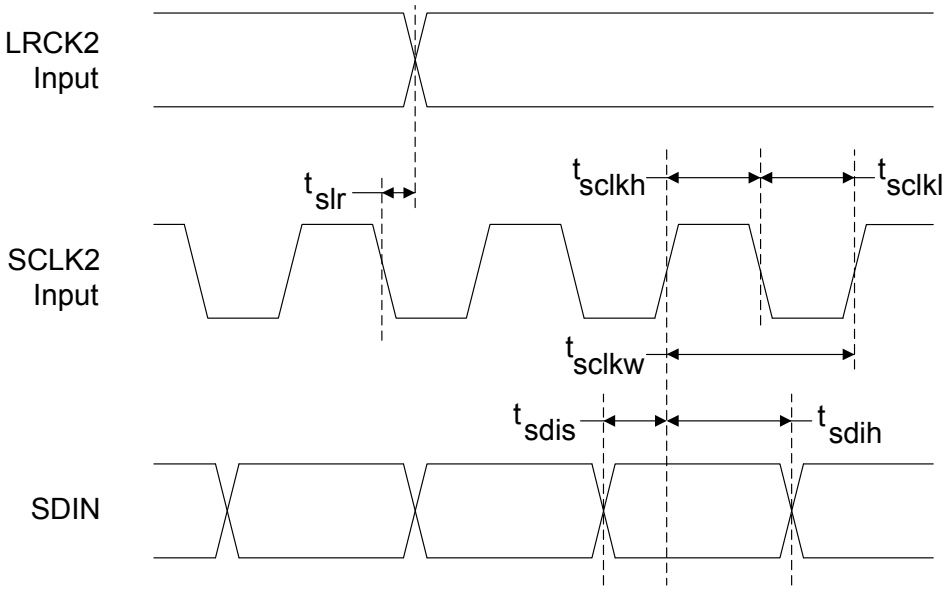


Figure 6. Slave Mode Timing - Serial Audio Port 2