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CS4265

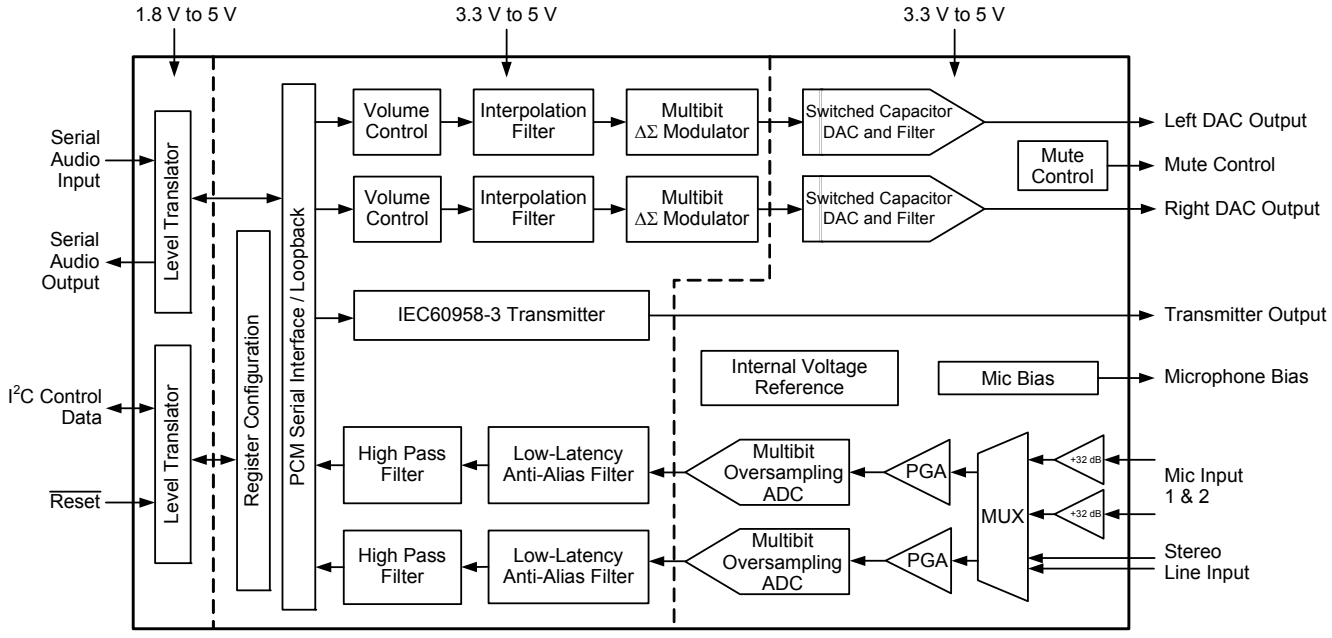
# 104 dB, 24-Bit, 192 kHz Stereo Audio CODEC

## D/A Features

- Multi-Bit Delta Sigma Modulator
- 104 dB Dynamic Range
- -90 dB THD+N
- Up to 192 kHz Sampling Rates
- Single-Ended Analog Architecture
- Volume Control with Soft Ramp
  - 0.5 dB Step Size
  - Zero Crossing, Click-Free Transitions
- Popguard® Technology
  - Minimizes the Effects of Output Transients
- Filtered Line-Level Outputs
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I²S up to 24-bit
  - Right-Justified 16-, 18-, 20-, and 24-bit
- Selectable 50/15 µs De-Emphasis

## A/D Features

- Multi-Bit Delta Sigma Modulator
- 104 dB Dynamic Range
- -95 dB THD+N
- Stereo 2:1 Input Multiplexer
- Programmable Gain Amplifier (PGA)
  - ± 12 dB Gain, 0.5 dB Step Size
  - Zero Crossing, Click-Free Transitions
- Pseudo-Differential Stereo Line Inputs
- Stereo Microphone Inputs
  - +32 dB Gain Stage
  - Low-Noise Bias Supply
- Up to 192 kHz Sampling Rates
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I²S up to 24-bit
- High-Pass Filter or DC Offset Calibration



## System Features

- Synchronous IEC60958-3 Transmitter
  - Up to 192 kHz Sampling Rates
  - 75 Ω Drive Capability
- Serial Audio Data Input Multiplexer
- Internal Digital Loopback
- Supports Master or Slave Operation
- Mute Output Control
- Power-Down Mode
  - Available for A/D, D/A, CODEC, Mic Preamplifier
- +3.3 V to +5 V Analog Power Supply
- +3.3 V to +5 V Digital Power Supply
- Direct Interface with 1.8 V to 5 V Logic Levels
- Supports I²C® Control Port Interface

## General Description

The CS4265 is a highly integrated stereo audio CODEC. The CS4265 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 192 kHz.

A 2:1 stereo input multiplexer is included for selecting between line-level or microphone-level inputs. The microphone input path includes a +32 dB gain stage and a low noise bias voltage supply. The PGA is available for line or microphone inputs and provides gain or attenuation of ±12 dB in 0.5 dB steps.

The output of the PGA is followed by an advanced 5th-order, multi-bit delta sigma modulator and digital filtering/decimation. Sampled data is transmitted by the serial audio interface at rates from 4 kHz to 192 kHz in either Slave or Master Mode.

The D/A converter is based on a 4th-order multi-bit delta sigma modulator with an ultra-linear low-pass filter and offers a volume control that operates with a 0.5 dB step size. It incorporates selectable soft ramp and zero crossing transition functions to eliminate clicks and pops.

Standard 50/15 µs de-emphasis is available for a 44.1 kHz sample rate for compatibility with digital audio programs mastered using the 50/15 µs pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4265 and other devices operating over a wide range of logic levels.

The CS4265 is available in a 32-pin QFN package for both Commercial (-10° to +70° C) and Automotive (-40° to +105° C) grade. The CDB4265 is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 57 for complete details.

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## LIST OF FIGURES

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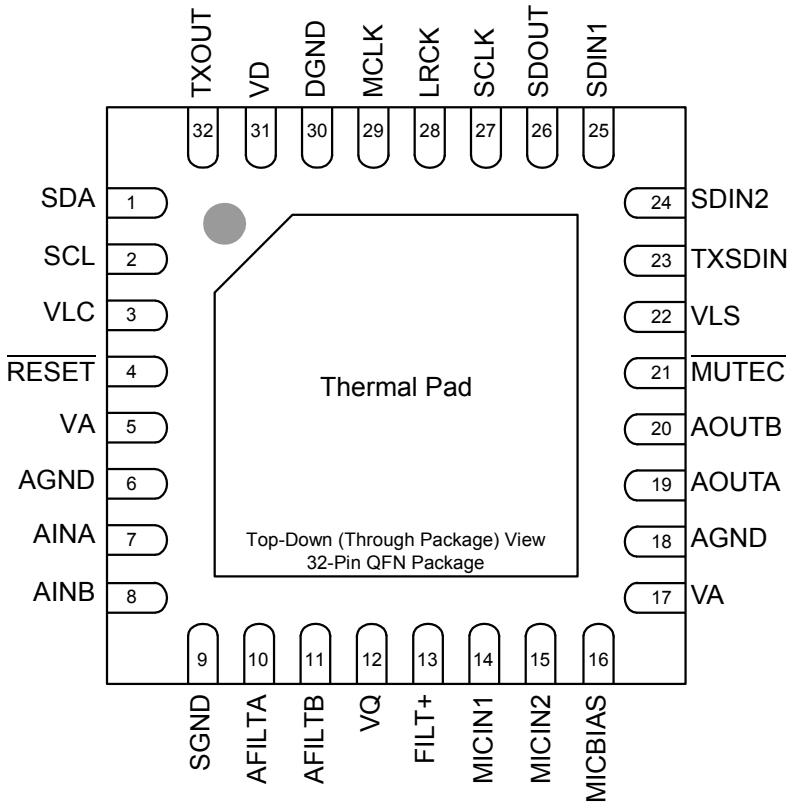
# 1. PIN DESCRIPTIONS




| Pin Name | # | Pin Description |
|---|---|---|
| SDA | 1 | **Serial Control Data** (*Input*/*Output*) - Bidirectional data line for the I²C control port. |
| SCL | 2 | **Serial Control Port Clock** (*Input*) - Serial clock for the I²C control port. |
| VLC | 3 | **Control Port Power** (*Input*) - Determines the required signal level for the control port interface. Refer to the Recommended Operating Conditions for appropriate voltages. |
| $\overline{\text{RESET}}$ | 4 | **Reset** (*Input*) - The device enters a low-power mode when this pin is driven low. |
| VA | 5 | **Analog Power** *(Input)* - Positive power for the internal analog section. |
| AGND | 6 | **Analog Ground** (*Input*) - Ground reference for the internal analog section. |
| AINA<br>AINB | 7,<br>8 | **Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table. |
| SGND | 9 | **Signal Ground** (*Input*) - Ground reference for the analog line inputs. |
| AFILTA<br>AFILTB | 10,<br>11 | **Antialias Filter Connection** (*Output*) - Antialias filter connection for the ADC inputs. |
| VQ | 12 | **Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. |
| FILT+ | 13 | **Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits. |
| MICIN1<br>MICIN2 | 14,<br>15 | **Microphone Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table. |
| MICBIAS | 16 | **Microphone Bias** (*Output*) - Low noise bias supply for external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table. |

| | | |
|---|---|---|
| VA | 17 | **Analog Power** *(Input)* - Positive power for the internal analog section. |
| AGND | 18 | **Analog Ground** (*Input*) - Ground reference for the internal analog section. |
| AOUTA<br>AOUTB | 19, 20 | **Analog Audio Output** (*Output*) - The full scale output level is specified in the DAC Analog Characteristics specification table. |
| $\overline{\text{MUTEC}}$ | 21 | **Mute Control** (*Output)* - This pin is active during power-up initialization, reset, muting, when master clock left/right clock frequency ratio is incorrect, or power-down. |
| VLS | 22 | **Serial Audio Interface Power** (*Input*) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages. |
| TXSDIN | 23 | **Transmitter Serial Audio Data Input** (*Input)* - Input for two's complement serial audio data. |
| SDIN2 | 24 | **Serial Audio Data Input 2** (*Input*) - Input for two's complement serial audio data. |
| SDIN1 | 25 | **Serial Audio Data Input 1** (*Input*) - Input for two's complement serial audio data. |
| SDOUT | 26 | **Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data. |
| SCLK | 27 | **Serial Clock** *(Input/Output*) - Serial clock for the serial audio interface. |
| LRCK | 28 | **Left Right Clock** *(Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line. |
| MCLK | 29 | **Master Clock** (*Input*) - Clock source for the delta-sigma modulators. |
| DGND | 30 | **Digital Ground** (*Input*) - Ground reference for the internal digital section. |
| VD | 31 | **Digital Power** (*Input*) - Positive power for the internal digital section. |
| TXOUT | 32 | **Transmitter Line Driver Output** (*Output)* - IEC60958-3 driver output. |
| Thermal Pad | - | **Thermal Pad** - Thermal relief pad for optimized heat dissipation. |

# 2. CHARACTERISTICS AND SPECIFICATIONS

## SPECIFIED OPERATING CONDITIONS

AGND = DGND = 0 V; All voltages with respect to ground.

| Parameters | | Symbol | Min | Nom | Max | Units |
|---|---|---|---|---|---|---|
| DC Power Supplies: | Analog | VA | 3.13 | 5.0 | 5.25 | V |
| | Digital | VD | 3.13 | 3.3 | (Note 1) | V |
| | Logic - Serial Port | VLS | 1.71 | 3.3 | 5.25 | V |
| | Logic - Control Port | VLC | 1.71 | 3.3 | 5.25 | V |
| Ambient Operating Temperature (Power Applied) | | $T_A$ | -10 | - | +70 | °C |

**Notes:** 1. Maximum of VA+0.25 V or 5.25 V, whichever is less.

## ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V All voltages with respect to ground. (Note 2)

| Parameter | | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| DC Power Supplies: | Analog | VA | -0.3 | +6.0 | V |
| | Digital | VD | -0.3 | +6.0 | V |
| | Logic - Serial Port | VLS | -0.3 | +6.0 | V |
| | Logic - Control Port | VLC | -0.3 | +6.0 | V |
| Input Current | (Note 3) | $I_{in}$ | - | ±10 | mA |
| Analog Input Voltage | | $V_{INA}$ | AGND-0.3 | VA+0.3 | V |
| Digital Input Voltage | Logic - Serial Port | $V_{IND-S}$ | -0.3 | VLS+0.3 | V |
| | Logic - Control Port | $V_{IND-C}$ | -0.3 | VLC+0.3 | V |
| Ambient Operating Temperature (Power Applied) | | $T_A$ | -50 | +125 | °C |
| Storage Temperature | | $T_{stg}$ | -65 | +150 | °C |

2. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
3. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

## DAC ANALOG CHARACTERISTICS

Test Conditions (unless otherwise specified): AGND = DGND = 0 V; VA = 3.13 V to 5.25 V; VD = 3.13 V to 5.25 V or VA + 0.25 V, whichever is less; VLS = VLC = 1.71 V to 5.25 V; $T_A$ = -10° to +70° C for Commercial or -40° to +85° C for Automotive; Output test signal: 997 Hz full-scale sine wave; Test load $R_L$ = 3 kΩ, $C_L$ = 10 pF (see Figure 1), Fs = 48/96/192 kHz. Measurement Bandwidth 10 Hz to 20 kHz; All Connections as shown in Figure 9 on page 23.

| Parameter | | | Symbol | Commercial Grade | | | Automotive Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| ***Dynamic Performance for VA = 4.75 V to 5.25 V*** | | | | | | | | | | |
| Dynamic Range | | (Note 4) | | | | | | | | |
| | 18 to 24-Bit | A-Weighted | | 98 | 104 | - | 96 | 104 | - | dB |
| | | unweighted | | 95 | 101 | - | 93 | 101 | - | dB |
| | 16-Bit | A-Weighted | | 90 | 96 | - | 88 | 96 | - | dB |
| | | unweighted | | 87 | 93 | - | 85 | 93 | - | dB |
| Total Harmonic Distortion + Noise | | (Note 4) | | | | | | | | |
| | 18 to 24-Bit | 0 dB | | - | -90 | -84 | - | -90 | -82 | dB |
| | | -20 dB | | - | -81 | - | - | -81 | - | dB |
| | | -60 dB | THD+N | - | -41 | - | - | -41 | - | dB |
| | 16-Bit | 0 dB | | - | -93 | -87 | - | -93 | -85 | dB |
| | | -20 dB | | - | -73 | - | - | -73 | - | dB |
| | | -60 dB | | - | -33 | - | - | -33 | - | dB |
| ***Dynamic Performance for VA = 3.13 V to 3.46 V*** | | | | | | | | | | |
| Dynamic Range | | (Note 4) | | | | | | | | |
| | 18 to 24-Bit | A-Weighted | | 95 | 101 | - | 93 | 101 | - | dB |
| | | unweighted | | 92 | 98 | - | 90 | 98 | - | dB |
| | 16-Bit | A-Weighted | | 88 | 93 | - | 86 | 93 | - | dB |
| | | unweighted | | 85 | 90 | - | 83 | 90 | - | dB |
| Total Harmonic Distortion + Noise | | (Note 4) | | | | | | | | |
| | 18 to 24-Bit | 0 dB | | - | -87 | -79 | - | -87 | -77 | dB |
| | | -20 dB | | - | -78 | - | - | -78 | - | dB |
| | | -60 dB | THD+N | - | -38 | - | - | -38 | - | dB |
| | 16-Bit | 0 dB | | - | -90 | -82 | - | -90 | -80 | dB |
| | | -20 dB | | - | -70 | - | - | -70 | - | dB |
| | | -60 dB | | - | -30 | - | - | -30 | - | dB |
| Interchannel Isolation | | (1 kHz) | | - | 100 | - | - | 100 | - | dB |
| ***DC Accuracy*** | | | | | | | | | | |
| Interchannel Gain Mismatch | | | | - | 0.1 | 0.25 | - | 0.1 | 0.25 | dB |
| Gain Drift | | | | - | 100 | - | - | 100 | - | ppm/°C |
| ***Analog Output*** | | | | | | | | | | |
| Full Scale Output Voltage | | | | 0.60*VA | 0.65*VA | 0.70*VA | 0.60*VA | 0.65*VA | 0.70*VA | $V_{pp}$ |
| DC Current draw from an AOUT pin | | (Note 5) | $I_{OUT}$ | - | - | 10 | - | - | 10 | µA |
| AC-Load Resistance | | (Note 6) | $R_L$ | 3 | - | - | 3 | - | - | kΩ |
| Load Capacitance | | (Note 6) | $C_L$ | - | - | 100 | - | - | 100 | pF |
| Output Impedance | | | $Z_{OUT}$ | - | 150 | - | - | 150 | - | Ω |

4. One-half LSB of triangular PDF dither added to data.
5. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC blocking capacitors.

6. Guaranteed by design. See Figure 2. $R_L$ and $C_L$ reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability. $C_L$ affects the dominant pole of the internal output amp; increasing $C_L$ beyond 100 pF can cause the internal op-amp to become unstable.

## DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

| Parameter (Note 7,10) | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ***Combined Digital and On-chip Analog Filter Response*** | | | ***Single-Speed Mode*** | | | |
| Passband (Note 7) | to -0.1 dB corner<br>to -3 dB corner | | 0<br>0 | -<br>- | 0.35<br>0.4992 | Fs<br>Fs |
| Frequency Response 10 Hz to 20 kHz | | | -0.175 | - | +0.01 | dB |
| StopBand | | | 0.5465 | - | - | Fs |
| StopBand Attenuation | (Note 8) | | 50 | - | - | dB |
| Group Delay | | tgd | - | 10/Fs | - | s |
| De-emphasis Error (Note 9) | Fs = 44.1 kHz | | - | - | +0.05/-0.25 | dB |
| ***Combined Digital and On-chip Analog Filter Response*** | | | ***Double-Speed Mode*** | | | |
| Passband (Note 7) | to -0.1 dB corner<br>to -3 dB corner | | 0<br>0 | -<br>- | 0.22<br>0.501 | Fs<br>Fs |
| Frequency Response 10 Hz to 20 kHz | | | -0.15 | - | +0.15 | dB |
| StopBand | | | 0.5770 | - | - | Fs |
| StopBand Attenuation | (Note 8) | | 55 | - | - | dB |
| Group Delay | | tgd | - | 5/Fs | - | s |
| ***Combined Digital and On-chip Analog Filter Response*** | | | ***Quad-Speed Mode*** | | | |
| Passband (Note 7) | to -0.1 dB corner<br>to -3 dB corner | | 0<br>0 | -<br>- | 0.110<br>0.469 | Fs<br>Fs |
| Frequency Response 10 Hz to 20 kHz | | | -0.12 | - | 0 | dB |
| StopBand | | | 0.7 | - | - | Fs |
| StopBand Attenuation | (Note 8) | | 51 | - | - | dB |
| Group Delay | | tgd | - | 2.5/Fs | - | s |

7. Filter response is guaranteed by design.
8. For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
   For Double-Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
   For Quad-Speed Mode, the Measurement Bandwidth is 0.7 Fs to 1 Fs.
9. De-emphasis is available only in Single-Speed Mode.
10. Response is clock dependent and will scale with Fs. Note that the amplitude vs. frequency plots of this data (Figures 18 to 27) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

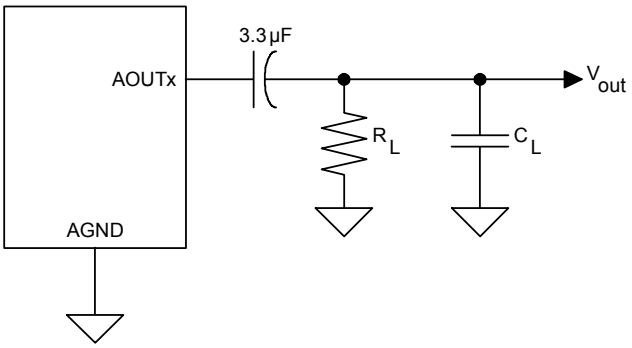



**Figure 1. DAC Output Test Load**

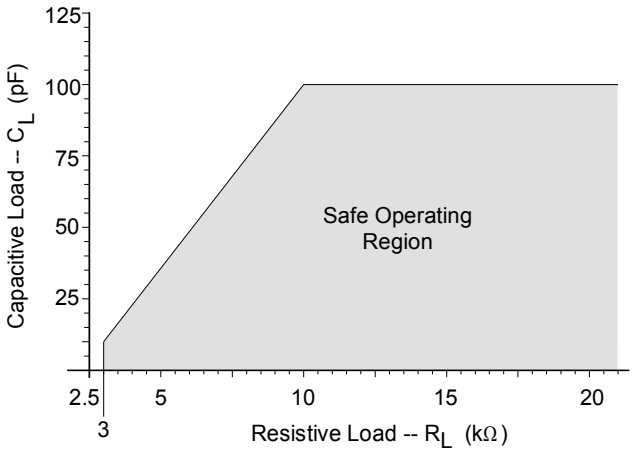



**Figure 2. Maximum DAC Loading**

## ADC ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VA = 3.13 V to 5.25 V; VD = 3.13 V to 5.25 V or VA + 0.25 V, whichever is less; VLS = VLC = 1.71 V to 5.25 V; $T_A$ = -10° to +70° C for Commercial or -40° to +85° C for Automotive; Input test signal: 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Fs = 48/96/192 kHz.; All connections as shown in Figure 9 on page 23.

| Line-Level Inputs | | | | | |
|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typ | Max | Unit |
| ***Dynamic Performance for VA = 4.75 V to 5.25 V*** | | | | | |
| Dynamic Range | | | | | |
| PGA Setting: -12 dB to +6 dB | | | | | |
| A-weighted | | 98 | 104 | - | dB |
| unweighted | | 95 | 101 | - | dB |
| (Note 13) 40 kHz bandwidth unweighted | | - | 98 | - | dB |
| PGA Setting: +12 dB Gain | | | | | |
| A-weighted | | 92 | 98 | - | dB |
| unweighted | | 89 | 95 | - | dB |
| (Note 13) 40 kHz bandwidth unweighted | | - | 92 | - | dB |
| Total Harmonic Distortion + Noise (Note 12) | | | | | |
| PGA Setting: -12 dB to +6 dB | | | | | |
| -1 dB | | - | -95 | -89 | dB |
| -20 dB | | - | -81 | - | dB |
| -60 dB | | - | -41 | - | dB |
| (Note 13) 40 kHz bandwidth -1 dB | THD+N | - | -92 | - | dB |
| PGA Setting: +12 dB Gain | | | | | |
| -1 dB | | - | -92 | -86 | dB |
| -20 dB | | - | -75 | - | dB |
| -60 dB | | - | -35 | - | dB |
| (Note 13) 40 kHz bandwidth -1 dB | | - | -89 | - | dB |
| ***Dynamic Performance for VA = 3.13 V to 3.46 V*** | | | | | |
| Dynamic Range | | | | | |
| PGA Setting: -12 dB to +6 dB | | | | | |
| A-weighted | | 93 | 101 | - | dB |
| unweighted | | 90 | 98 | - | dB |
| (Note 13) 40 kHz bandwidth unweighted | | - | 95 | - | dB |
| PGA Setting: +12 dB Gain | | | | | |
| A-weighted | | 89 | 95 | - | dB |
| unweighted | | 86 | 92 | - | dB |
| (Note 13) 40 kHz bandwidth unweighted | | - | 89 | - | dB |
| Total Harmonic Distortion + Noise (Note 12) | | | | | |
| PGA Setting: -12 dB to +6 dB | | | | | |
| -1 dB | | - | -92 | -86 | dB |
| -20 dB | | - | -78 | - | dB |
| -60 dB | | - | -38 | - | dB |
| (Note 13) 40 kHz bandwidth -1 dB | THD+N | - | -84 | - | dB |
| PGA Setting: +12 dB Gain | | | | | |
| -1 dB | | - | -89 | -83 | dB |
| -20 dB | | - | -72 | - | dB |
| -60 dB | | - | -32 | - | dB |
| (Note 13) 40 kHz bandwidth -1 dB | | - | -81 | - | dB |

| Line-Level Inputs | | | | | |
|---|---|---|---|---|---|
| | | Commercial Grade | | | |
| Parameter | Symbol | Min | Typ | Max | Unit |
| Interchannel Isolation | | - | 90 | - | dB |

| | | | | | |
|---|---|---|---|---|---|
| ***DC Accuracy*** | | | | | |
| Gain Error | | - | - | ±10 | % |
| Gain Drift | | - | ±100 | - | ppm/°C |
| ***Line-Level Input Characteristics*** | | | | | |
| Full-scale Input Voltage | | 0.51*VA | 0.57*VA | 0.63*VA | $V_{pp}$ |
| Input Impedance (Note 11) | | 6.12 | 6.8 | 7.48 | kΩ |
| Maximum Interchannel Input Impedance Mismatch | | - | 5 | - | % |

**Line-Level and Microphone-Level Inputs**

| Parameter | Symbol | Commercial Grade | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| ***DC Accuracy*** | | | | | |
| Interchannel Gain Mismatch | | - | 0.1 | - | dB |
| ***Programmable Gain Characteristics*** | | | | | |
| Gain Step Size | | - | 0.5 | - | dB |
| Absolute Gain Step Error | | - | - | 0.4 | dB |

11. Valid when the line-level inputs are selected.

## ADC ANALOG CHARACTERISTICS

(Continued)

| Microphone-Level Inputs | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| ***Dynamic Performance for VA = 4.75 V to 5.25 V*** | | | | | |
| Dynamic Range | | | | | |
| PGA Setting: -12 dB to 0 dB | | | | | |
| A-weighted | | 77 | 83 | - | dB |
| unweighted | | 74 | 80 | - | dB |
| PGA Setting: +12 dB | | | | | |
| A-weighted | | 65 | 71 | - | dB |
| unweighted | | 62 | 68 | - | dB |
| Total Harmonic Distortion + Noise (Note 12) | | | | | |
| PGA Setting: -12 dB to 0 dB | | | | | |
| -1 dB | THD+N | - | -80 | -74 | dB |
| -20 dB | | - | -60 | - | dB |
| -60 dB | | - | -20 | - | dB |
| PGA Setting: +12 dB | | | | | |
| -1 dB | | - | -68 | - | dB |
| ***Dynamic Performance for VA = 3.13 V to 3.46 V*** | | | | | |
| Dynamic Range | | | | | |
| PGA Setting: -12 dB to 0 dB | | | | | |
| A-weighted | | 77 | 83 | - | dB |
| unweighted | | 74 | 80 | - | dB |
| PGA Setting: +12 dB | | | | | |
| A-weighted | | 65 | 71 | - | dB |
| unweighted | | 62 | 68 | - | dB |
| Total Harmonic Distortion + Noise (Note 12) | | | | | |
| PGA Setting: -12 dB to 0 dB | | | | | |
| -1 dB | THD+N | - | -80 | -74 | dB |
| -20 dB | | - | -60 | - | dB |
| -60 dB | | - | -20 | - | dB |
| PGA Setting: +12 dB | | | | | |
| -1 dB | | - | -68 | - | dB |
| Interchannel Isolation | | - | 80 | - | dB |
| ***DC Accuracy*** | | | | | |
| Gain Error | | - | ±5 | - | % |
| Gain Drift | | - | ±300 | - | ppm/°C |
| ***Microphone-Level Input Characteristics*** | | | | | |
| Full-scale Input Voltage | | 0.013*VA | 0.017*VA | 0.021*VA | $V_{pp}$ |
| Input Impedance (Note 14) | | - | 60 | - | kΩ |

12. Referred to the typical line-level full-scale input voltage
13. Valid for Double- and Quad-Speed Modes only.
14. Valid when the microphone-level inputs are selected.

## ADC DIGITAL FILTER CHARACTERISTICS

| Parameter (Notes 15, 17) | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ***Single-Speed Mode*** | | | | | | | |
| Passband | (-0.1 dB) | | | 0 | - | 0.4896 | Fs |
| Passband Ripple | | | | - | - | 0.035 | dB |
| Stopband | | | | 0.5688 | - | - | Fs |
| Stopband Attenuation | | | | 70 | - | - | dB |
| Total Group Delay (Fs = Output Sample Rate) | | | $t_{gd}$ | - | 12/Fs | - | s |
| ***Double-Speed Mode*** | | | | | | | |
| Passband | (-0.1 dB) | | | 0 | - | 0.4896 | Fs |
| Passband Ripple | | | | - | - | 0.025 | dB |
| Stopband | | | | 0.5604 | - | - | Fs |
| Stopband Attenuation | | | | 69 | - | - | dB |
| Total Group Delay (Fs = Output Sample Rate) | | | $t_{gd}$ | - | 9/Fs | - | s |
| ***Quad-Speed Mode*** | | | | | | | |
| Passband | (-0.1 dB) | | | 0 | - | 0.2604 | Fs |
| Passband Ripple | | | | - | - | 0.025 | dB |
| Stopband | | | | 0.5000 | - | - | Fs |
| Stopband Attenuation | | | | 60 | - | - | dB |
| Total Group Delay (Fs = Output Sample Rate) | | | $t_{gd}$ | - | 5/Fs | - | s |
| ***High-Pass Filter Characteristics*** | | | | | | | |
| Frequency Response | -3.0 dB | | | - | 1 | - | Hz |
| | -0.13 dB | (Note 16) | | | 20 | - | Hz |
| Phase Deviation | @ 20 Hz | (Note 16) | | - | 10 | - | Deg |
| Passband Ripple | | | | - | - | 0 | dB |
| Filter Settling Time | | | | | $10^5$/Fs | | s |

15. Filter response is guaranteed by design.
16. Response shown is for Fs = 48 kHz.
17. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 30 to 41) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

## DC ELECTRICAL CHARACTERISTICS

AGND = DGND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Fs=48 kHz; Master Mode.

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply Current | VA = 5 V | $I_A$ | - | 41 | 50 | mA |
| (Normal Operation) | VA = 3.3 V | $I_A$ | - | 37 | 45 | mA |
| | VD, VLS, VLC = 5 V | $I_D$ | - | 39 | 47 | mA |
| | VD, VLS, VLC = 3.3 V | $I_D$ | - | 23 | 28 | mA |
| Power Supply Current | VA = 5 V | $I_A$ | - | 0.50 | - | mA |
| (Power-Down Mode) (Note 18) | VLS, VLC, VD=5 V | $I_D$ | - | 0.54 | - | mA |
| Power Consumption | | | | | | |
| (Normal Operation) | VA, VD, VLS, VLC = 5 V | - | - | 400 | 485 | mW |
| | VA, VD, VLS, VLC = 3.3 V | - | - | 198 | 241 | mW |
| (Power-Down Mode) | VA, VD, VLS, VLC = 5 V | - | - | 4.2 | - | mW |
| Power Supply Rejection Ratio (1 kHz) | (Note 19) | PSRR | - | 55 | - | dB |
| ***VQ Characteristics*** | | | | | | |
| Quiescent Voltage | | VQ | - | 0.5 x VA | - | VDC |
| DC Current from VQ | (Note 20) | $I_Q$ | - | - | 1 | µA |
| VQ Output Impedance | | $Z_Q$ | - | 4.5 | - | kΩ |
| FILT+ Nominal Voltage | | FILT+ | - | VA | - | VDC |
| Microphone Bias Voltage | | MICBIAS | - | 0.8 x VA | - | VDC |
| Current from MICBIAS | | $I_{MB}$ | - | - | 2 | mA |

18. Power-Down Mode is defines as $\overline{\text{RESET}}$ = Low with all clock and data lines held static and no analog input.
19. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.
20. Guaranteed by design. The DC current draw represents the allowed current draw due to typical leakage through the electrolytic de-coupling capacitors.

## DIGITAL INTERFACE CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VLS = VLC = 1.71 V to 5.25 V.

| Parameters (Note 21) | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| High-Level Input Voltage | | | | | | |
| VL = 1.71 V | Serial Port | $V_{IH}$ | 0.8xVLS | - | - | V |
| | Control Port | $V_{IH}$ | 0.8xVLC | - | - | V |
| VL > 2.0 V | Serial Port | $V_{IH}$ | 0.7xVLS | - | - | V |
| | Control Port | $V_{IH}$ | 0.7xVLC | - | - | V |
| Low-Level Input Voltage | Serial Port | $V_{IL}$ | - | - | 0.2xVLS | V |
| | Control Port | $V_{IL}$ | - | - | 0.2xVLC | V |
| High-Level Output Voltage at $I_o$ = 2 mA | Serial Port | $V_{OH}$ | VLS-1.0 | - | - | V |
| | Control Port | $V_{OH}$ | VLC-1.0 | - | - | V |
| | MUTEC | $V_{OH}$ | VA-1.0 | - | - | V |
| | TXOUT | $V_{OH}$ | VD-1.0 | - | - | V |
| Low-Level Output Voltage at $I_o$ = 2 mA | Serial Port | $V_{OL}$ | - | - | 0.4 | V |
| | Control Port | $V_{OL}$ | - | - | 0.4 | V |
| | MUTEC | $V_{OL}$ | - | - | 0.4 | V |
| | TXOUT | $V_{OL}$ | - | - | 0.4 | V |
| Input Leakage Current | | $I_{in}$ | - | - | ±10 | µA |
| Input Capacitance | (Note 22) | | - | - | 1 | pF |
| Maximum MUTEC Drive Current | | | - | 3 | - | mA |

21. Serial Port signals include: MCLK, SCLK, LRCK, SDIN1, SDIN2, TXSDIN, SDOUT. Control Port signals include: SCL, SDA, RESET.
22. Guaranteed by design.

## SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

Logic '0' = DGND = AGND = 0 V; Logic '1' = VL, $C_L$ = 20 pF. (Note 23)

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Sample Rate | Single-Speed Mode | Fs | 4 | - | 50 | kHz |
| | Double-Speed Mode | Fs | 50 | - | 100 | kHz |
| | Quad-Speed Mode | Fs | 100 | - | 200 | kHz |
| ***MCLK Specifications*** | | | | | | |
| MCLK Frequency | | fmclk | 1.024 | - | 51.200 | MHz |
| MCLK Input Pulse Width High/Low | | tclkhl | 8 | - | - | ns |
| MCLK Output Duty Cycle | | | 45 | 50 | 55 | % |
| ***Master Mode*** | | | | | | |
| LRCK Duty Cycle | | | - | 50 | - | % |
| SCLK Duty Cycle | | | - | 50 | - | % |
| SCLK falling to LRCK edge | | $t_{slr}$ | -10 | - | 10 | ns |
| SCLK falling to SDOUT valid | | $t_{sdo}$ | 0 | - | 36 | ns |
| SDIN valid to SCLK rising setup time | | $t_{sdis}$ | 16 | - | - | ns |
| SCLK rising to SDIN hold time | | $t_{sdih}$ | 20 | - | - | ns |
| ***Slave Mode*** | | | | | | |
| LRCK Duty Cycle | | | 40 | 50 | 60 | % |
| SCLK Period | | | | | | |
| | Single-Speed Mode | $t_{sclkw}$ | $\frac{10^9}{(128)Fs}$ | - | - | ns |
| | Double-Speed Mode | $t_{sclkw}$ | $\frac{10^9}{(64)Fs}$ | - | - | ns |
| | Quad-Speed Mode | $t_{sclkw}$ | $\frac{10^9}{(64)Fs}$ | - | - | ns |
| SCLK Pulse Width High | | $t_{sclkh}$ | 30 | - | - | ns |
| SCLK Pulse Width Low | | $t_{sclkl}$ | 48 | - | - | ns |
| SCLK falling to LRCK edge | | $t_{slr}$ | -10 | - | 10 | ns |
| SCLK falling to SDOUT valid | | $t_{sdo}$ | 0 | - | 36 | ns |
| SDIN valid to SCLK rising setup time | | $t_{sdis}$ | 16 | - | - | ns |
| SCLK rising to SDIN hold time | | $t_{sdih}$ | 20 | - | - | ns |

23. See Figures 3 and 4 on page 20.

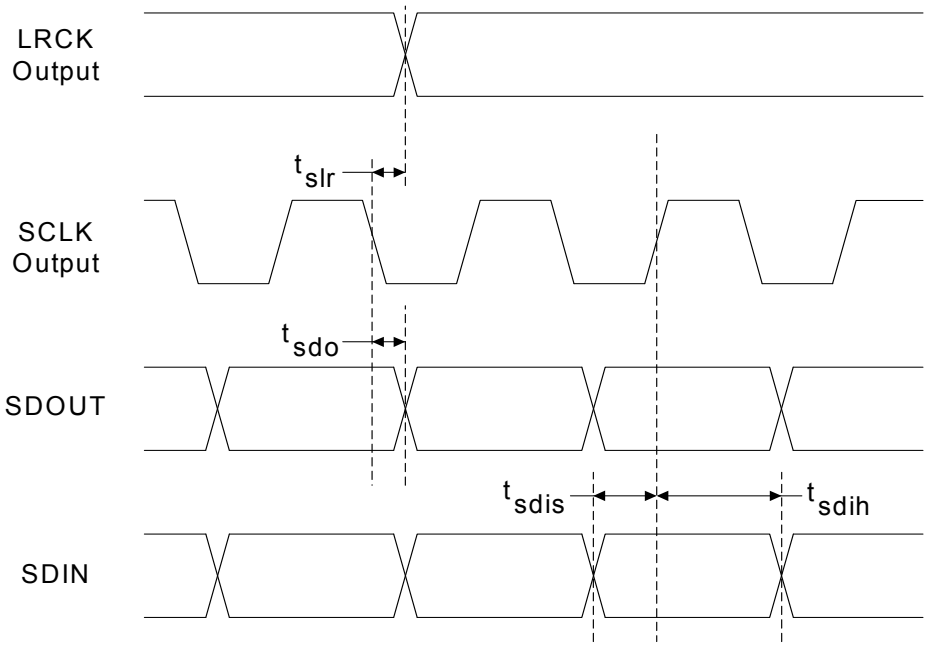



**Figure 3. Master Mode Serial Audio Port Timing**

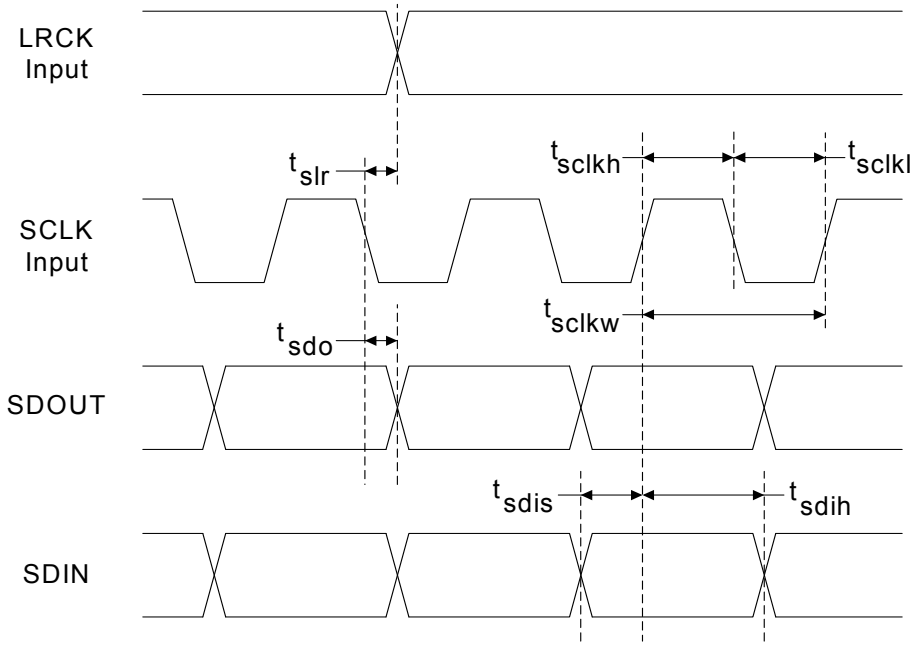



**Figure 4. Slave Mode Serial Audio Port Timing**

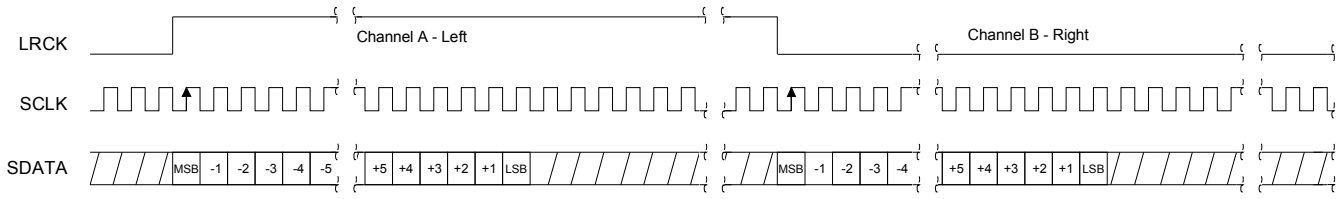



**Figure 5. Format 0, Left-Justified up to 24-Bit Data**

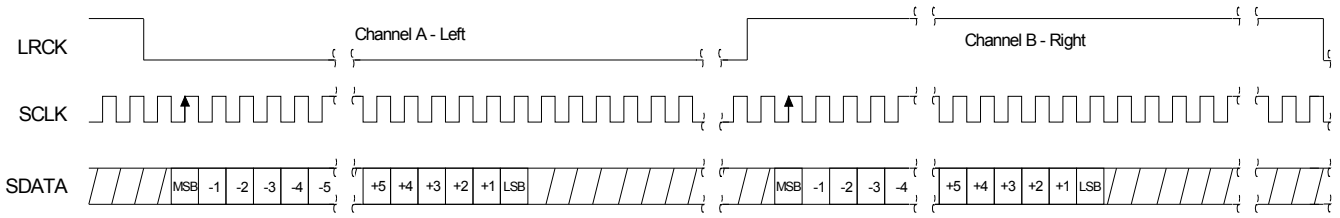



**Figure 6. Format 1, I²S up to 24-Bit Data**

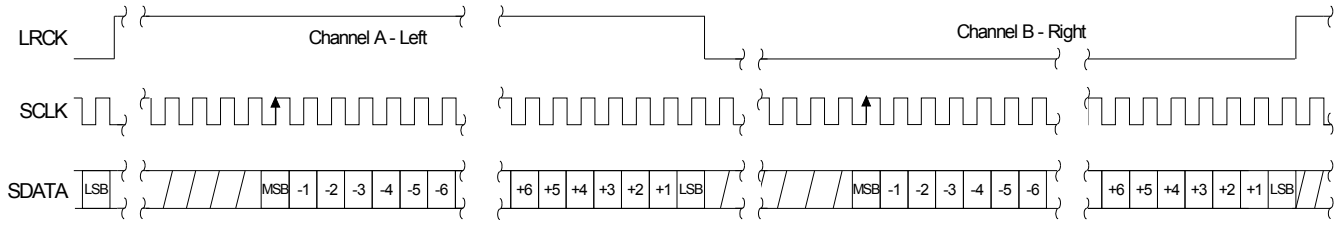



**Figure 7. Format 2, Right-Justified 16-Bit Data.**
**Format 3, Right-Justified 24-Bit Data.**

## SWITCHING CHARACTERISTICS - I²C CONTROL PORT

Inputs: Logic 0 = DGND = AGND = 0 V, Logic 1 = VLC, $C_L$ = 30 pF.

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SCL Clock Frequency | | $f_{scl}$ | - | 100 | kHz |
| $\overline{\text{RESET}}$ Rising Edge to Start | | $t_{irs}$ | 500 | - | ns |
| Bus Free Time Between Transmissions | | $t_{buf}$ | 4.7 | - | µs |
| Start Condition Hold Time (prior to first clock pulse) | | $t_{hdst}$ | 4.0 | - | µs |
| Clock Low time | | $t_{low}$ | 4.7 | - | µs |
| Clock High Time | | $t_{high}$ | 4.0 | - | µs |
| Setup Time for Repeated Start Condition | | $t_{sust}$ | 4.7 | - | µs |
| SDA Hold Time from SCL Falling | (Note 24) | $t_{hdd}$ | 0 | - | µs |
| SDA Setup time to SCL Rising | | $t_{sud}$ | 250 | - | ns |
| Rise Time of SCL and SDA | (Note 25) | $t_{rc}$, $t_{rd}$ | - | 1 | µs |
| Fall Time SCL and SDA | (Note 25) | $t_{fc}$, $t_{fd}$ | - | 300 | ns |
| Setup Time for Stop Condition | | $t_{susp}$ | 4.7 | - | µs |
| Acknowledge Delay from SCL Falling | | $t_{ack}$ | 300 | 1000 | ns |

24. Data must be held for sufficient time to bridge the transition time, $t_{fc}$, of SCL.
25. Guaranteed by design.

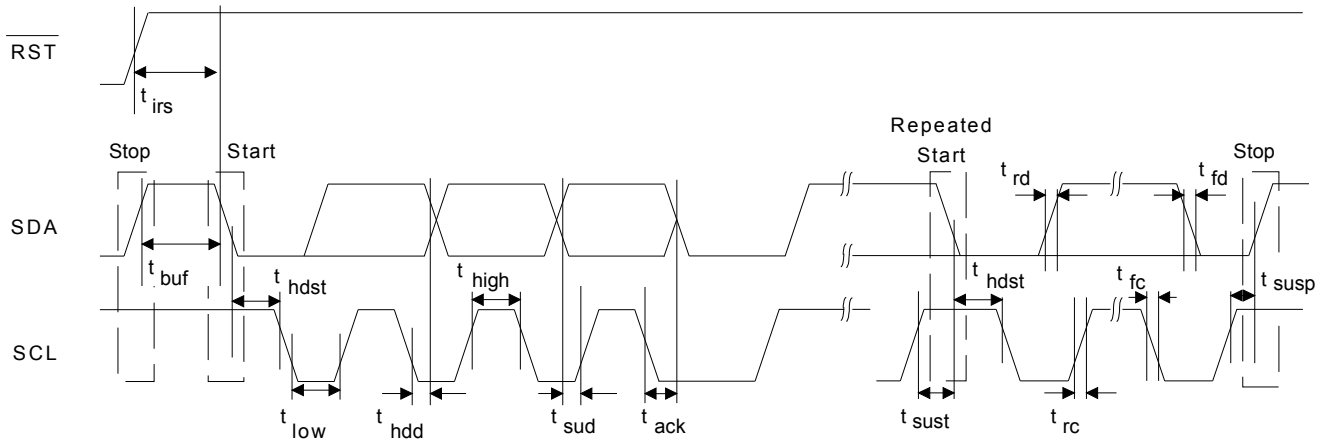



**Figure 8. Control Port Timing - I²C Format**

# 3. TYPICAL CONNECTION DIAGRAM

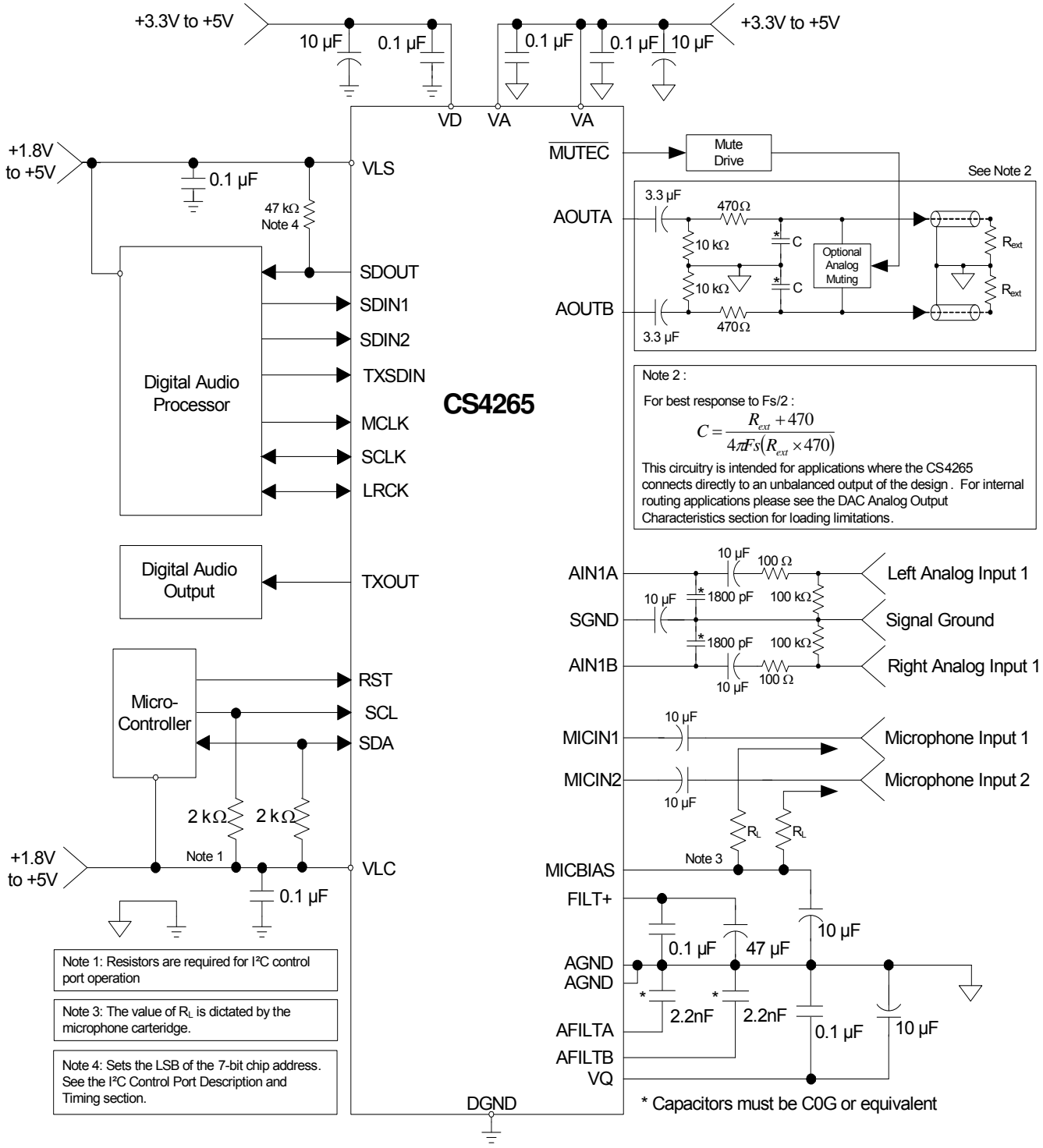



**Figure 9. Typical Connection Diagram**

# 4. APPLICATIONS

## 4.1 Recommended Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supply, MCLK, and LRCK are stable. In this state, the Control Port is reset to its default settings.
2. Bring $\overline{\text{RESET}}$ high. The device will remain in a low power state with the PDN bit set by default. The control port will be accessible.
3. The desired register settings can be loaded while the PDN bit remains set.
4. Clear the PDN bit to initiate the power-up sequence.

## 4.2 System Clocking

The CS4265 will operate at sampling frequencies from 4 kHz to 200 kHz. This range is divided into three speed modes as shown in Table 1.

| Mode | Sampling Frequency |
|---|---|
| ***Single-Speed*** | 4-50 kHz |
| ***Double-Speed*** | 50-100 kHz |
| ***Quad-Speed*** | 100-200 kHz |

**Table 1. Speed Modes**

### *4.2.1 Master Clock*

MCLK/LRCK must maintain an integer ratio as shown in Table 2. The LRCK frequency is equal to Fs, the frequency at which audio samples for each channel are clocked into or out of the device. The FM bits (See "Functional Mode (Bits 7:6)" on page 38.) and the MCLK Freq bits (See "MCLK Frequency - Address 05h" on page 39.) configure the device to generate the proper clocks in Master Mode, and receive the proper clocks in Slave Mode. Table 2 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies.

| LRCK (kHz) | MCLK (MHz) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 64x | 96x | 128x | 192x | 256x | 384x | 512x | 768x | 1024x |
| 32 | - | - | - | - | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.7680 |
| 44.1 | - | - | - | - | 11.2896 | 16.9344 | 22.5792 | 33.8680 | 45.1584 |
| 48 | - | - | - | - | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 49.1520 |
| 64 | - | - | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.7680 | - | - |
| 88.2 | - | - | 11.2896 | 16.9344 | 22.5792 | 33.8680 | 45.1584 | - | - |
| 96 | - | - | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 49.1520 | - | - |
| 128 | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.7680 | - | - | - | - |
| 176.4 | 11.2896 | 16.9344 | 22.5792 | 33.8680 | 45.1584 | - | - | - | - |
| 192 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 49.1520 | - | - | - | - |
| **Mode** | **QSM** | | | | | **DSM** | | **SSM** | |

**Table 2. Common Clock Frequencies**

In both Master and Slave Modes, the external MCLK must be divided down based on the MCLK/LRCK ratio to achieve a post-divider MCLK/LRCK ratio of 256x for SSM, 128x for DSM, or 64x for QSM. Table 3 lists the appropriate dividers.

| MCLK/LRCK Ratio | MCLK Dividers | | |
|---|---|---|---|
| **64x** | - | - | ÷1 |
| **96x** | - | - | ÷1.5 |
| **128x** | - | ÷1 | ÷2 |
| **192x** | - | ÷1.5 | ÷3 |
| **256x** | ÷1 | ÷2 | ÷4 |
| **384x** | ÷1.5 | ÷3 | - |
| **512x** | ÷2 | ÷4 | - |
| **768x** | ÷3 | - | - |
| **1024x** | ÷4 | - | - |
| **Mode** | **SSM** | **DSM** | **QSM** |

**Table 3. MCLK Dividers**

### 4.2.2 Master Mode

As a clock master, LRCK and SCLK will operate as outputs. LRCK and SCLK are internally derived from MCLK with LRCK equal to Fs and SCLK equal to 64 x Fs as shown in Figure 10.

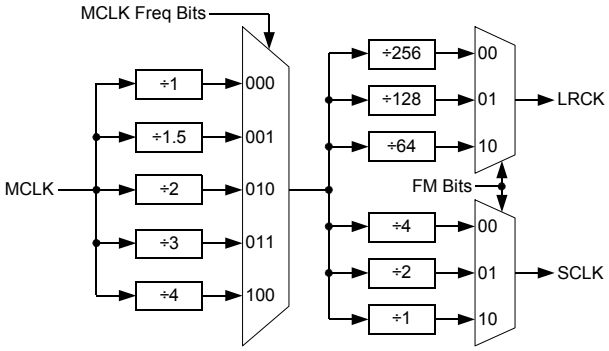



**Figure 10. Master Mode Clocking**

### 4.2.3 Slave Mode

In Slave Mode, SCLK and LRCK operate as inputs. The Left/Right clock signal must be equal to the sample rate, Fs, and must be synchronously derived from the supplied master clock, MCLK.

The serial bit clock, SCLK, must be synchronously derived from the master clock, MCLK, and be equal to 128x, 64x, 48x or 32x Fs, depending on the desired speed mode. Refer to Table 4 for required clock ratios.

| | Single-Speed | Double-Speed | Quad-Speed |
|---|---|---|---|
| SCLK/LRCK Ratio | 32x, 48x, 64x, 128x | 32x, 48x, 64x | 32x, 48x, 64x |

**Table 4. Slave Mode Serial Bit Clock Ratios**

## 4.3 High-Pass Filter and DC Offset Calibration

When using operational amplifiers in the input circuitry driving the CS4265, a small DC offset may be driven into the A/D converter. The CS4265 includes a high-pass filter after the decimator to remove any DC offset