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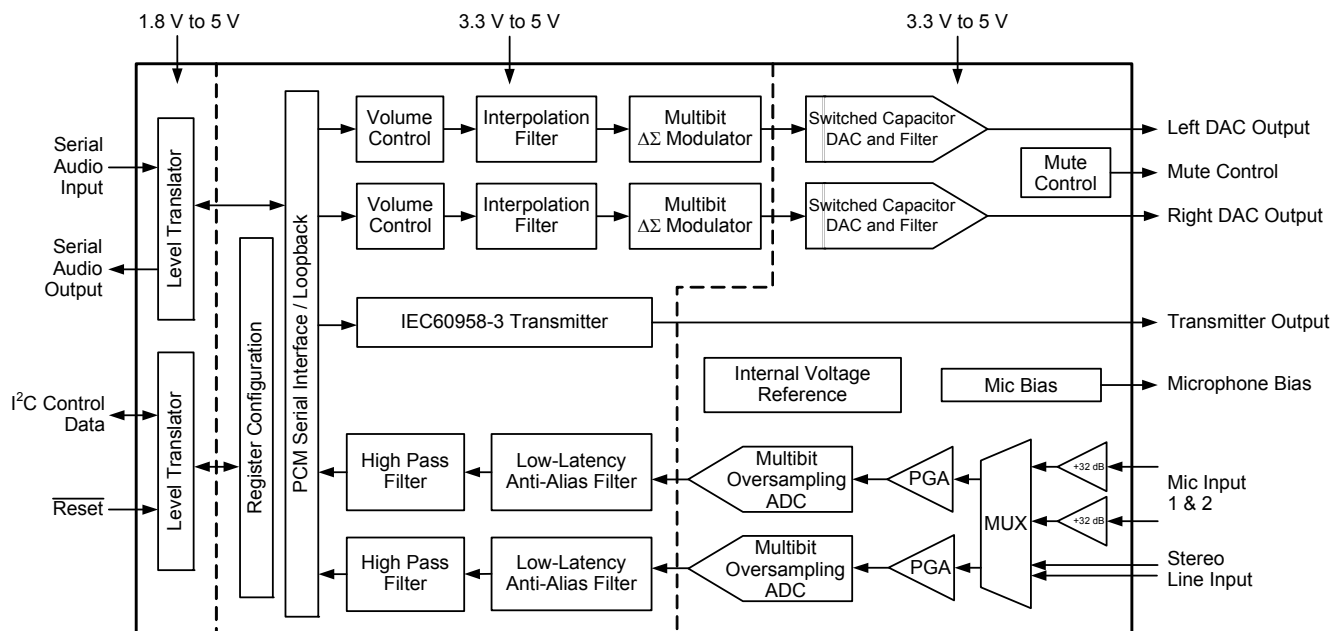
# 104 dB, 24-Bit, 192 kHz Stereo Audio CODEC

## D/A Features

- ◆ Multi-Bit Delta Sigma Modulator
- ◆ 104 dB Dynamic Range
- ◆ -90 dB THD+N
- ◆ Up to 192 kHz Sampling Rates
- ◆ Single-Ended Analog Architecture
- ◆ Volume Control with Soft Ramp
  - 0.5 dB Step Size
  - Zero Crossing, Click-Free Transitions
- ◆ Popguard® Technology
  - Minimizes the Effects of Output Transients
- ◆ Filtered Line-Level Outputs
- ◆ Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I<sup>2</sup>S up to 24-bit
  - Right-Justified 16-, 18-, 20-, and 24-bit
- ◆ Selectable 50/15 μs De-Emphasis

## A/D Features

- ◆ Multi-Bit Delta Sigma Modulator
- ◆ 104 dB Dynamic Range
- ◆ -95 dB THD+N
- ◆ Stereo 2:1 Input Multiplexer
- ◆ Programmable Gain Amplifier (PGA)
  - ± 12 dB Gain, 0.5 dB Step Size
  - Zero Crossing, Click-Free Transitions
- ◆ Pseudo-Differential Stereo Line Inputs
- ◆ Stereo Microphone Inputs
  - +32 dB Gain Stage
  - Low-Noise Bias Supply
- ◆ Up to 192 kHz Sampling Rates
- ◆ Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I<sup>2</sup>S up to 24-bit
- ◆ High-Pass Filter or DC Offset Calibration



## System Features

- ◆ Synchronous IEC60958-3 Transmitter
  - Up to 192 kHz Sampling Rates
  - 75  $\Omega$  Drive Capability
- ◆ Serial Audio Data Input Multiplexer
- ◆ Internal Digital Loopback
- ◆ Supports Master or Slave Operation
- ◆ Mute Output Control
- ◆ Power-Down Mode
  - Available for A/D, D/A, CODEC, Mic Preamplifier
- ◆ +3.3 V to +5 V Analog Power Supply
- ◆ +3.3 V to +5 V Digital Power Supply
- ◆ Direct Interface with 1.8 V to 5 V Logic Levels
- ◆ Supports I<sup>2</sup>C® Control Port Interface

## General Description

The CS4265 is a highly integrated stereo audio CO-DEC. The CS4265 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 192 kHz.

A 2:1 stereo input multiplexer is included for selecting between line-level or microphone-level inputs. The microphone input path includes a +32 dB gain stage and a low noise bias voltage supply. The PGA is available for line or microphone inputs and provides gain or attenuation of  $\pm 12$  dB in 0.5 dB steps.

The output of the PGA is followed by an advanced 5th-order, multi-bit delta sigma modulator and digital filtering/decimation. Sampled data is transmitted by the serial audio interface at rates from 4 kHz to 192 kHz in either Slave or Master Mode.

The D/A converter is based on a 4th-order multi-bit delta sigma modulator with an ultra-linear low-pass filter and offers a volume control that operates with a 0.5 dB step size. It incorporates selectable soft ramp and zero crossing transition functions to eliminate clicks and pops.

Standard 50/15  $\mu$ s de-emphasis is available for a 44.1 kHz sample rate for compatibility with digital audio programs mastered using the 50/15  $\mu$ s pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4265 and other devices operating over a wide range of logic levels.

The CS4265 is available in a 32-pin QFN package for both Commercial ( $-10^{\circ}$  to  $+70^{\circ}$  C) and Automotive ( $-40^{\circ}$  to  $+105^{\circ}$  C) grade. The CDB4265 is also available for device evaluation and implementation suggestions. Please refer to [“Ordering Information” on page 57](#) for complete details.

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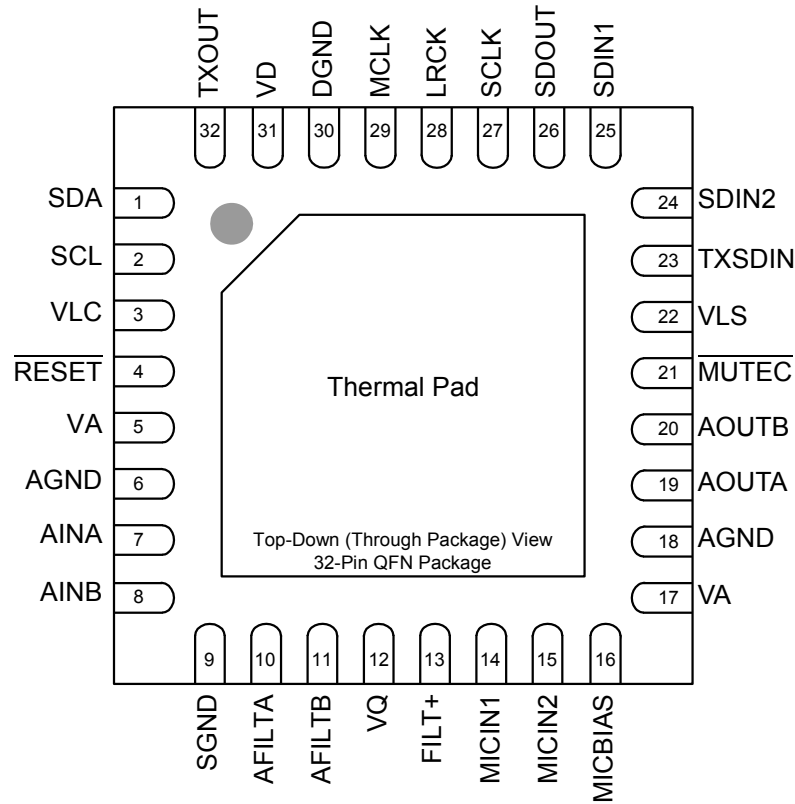
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## 1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDA	1	<b>Serial Control Data</b> ( <i>Input/Output</i> ) - Bidirectional data line for the I <sup>2</sup> C control port.
SCL	2	<b>Serial Control Port Clock</b> ( <i>Input</i> ) - Serial clock for the I <sup>2</sup> C control port.
VLC	3	<b>Control Port Power</b> ( <i>Input</i> ) - Determines the required signal level for the control port interface. Refer to the Recommended Operating Conditions for appropriate voltages.
RESET	4	<b>Reset</b> ( <i>Input</i> ) - The device enters a low-power mode when this pin is driven low.
VA	5	<b>Analog Power</b> ( <i>Input</i> ) - Positive power for the internal analog section.
AGND	6	<b>Analog Ground</b> ( <i>Input</i> ) - Ground reference for the internal analog section.
AINA AINB	7, 8	<b>Analog Input</b> ( <i>Input</i> ) - The full-scale level is specified in the ADC Analog Characteristics specification table.
SGND	9	<b>Signal Ground</b> ( <i>Input</i> ) - Ground reference for the analog line inputs.
AFILTA AFILTB	10, 11	<b>Antialias Filter Connection</b> ( <i>Output</i> ) - Antialias filter connection for the ADC inputs.
VQ	12	<b>Quiescent Voltage</b> ( <i>Output</i> ) - Filter connection for internal quiescent voltage.
FILT+	13	<b>Positive Voltage Reference</b> ( <i>Output</i> ) - Positive reference voltage for the internal sampling circuits.
MICIN1 MICIN2	14, 15	<b>Microphone Input</b> ( <i>Input</i> ) - The full-scale level is specified in the ADC Analog Characteristics specification table.
MICBIAS	16	<b>Microphone Bias</b> ( <i>Output</i> ) - Low noise bias supply for external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.



VA	17	<b>Analog Power</b> ( <i>Input</i> ) - Positive power for the internal analog section.
AGND	18	<b>Analog Ground</b> ( <i>Input</i> ) - Ground reference for the internal analog section.
AOUTA AOUTB	19, 20	<b>Analog Audio Output</b> ( <i>Output</i> ) - The full scale output level is specified in the DAC Analog Characteristics specification table.
$\overline{\text{MUTE}}\text{C}$	21	<b>Mute Control</b> ( <i>Output</i> ) - This pin is active during power-up initialization, reset, muting, when master clock left/right clock frequency ratio is incorrect, or power-down.
VLS	22	<b>Serial Audio Interface Power</b> ( <i>Input</i> ) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
TXSDIN	23	<b>Transmitter Serial Audio Data Input</b> ( <i>Input</i> ) - Input for two's complement serial audio data.
SDIN2	24	<b>Serial Audio Data Input 2</b> ( <i>Input</i> ) - Input for two's complement serial audio data.
SDIN1	25	<b>Serial Audio Data Input 1</b> ( <i>Input</i> ) - Input for two's complement serial audio data.
SDOUT	26	<b>Serial Audio Data Output</b> ( <i>Output</i> ) - Output for two's complement serial audio data.
SCLK	27	<b>Serial Clock</b> ( <i>Input/Output</i> ) - Serial clock for the serial audio interface.
LRCK	28	<b>Left Right Clock</b> ( <i>Input/Output</i> ) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	29	<b>Master Clock</b> ( <i>Input</i> ) - Clock source for the delta-sigma modulators.
DGND	30	<b>Digital Ground</b> ( <i>Input</i> ) - Ground reference for the internal digital section.
VD	31	<b>Digital Power</b> ( <i>Input</i> ) - Positive power for the internal digital section.
TXOUT	32	<b>Transmitter Line Driver Output</b> ( <i>Output</i> ) - IEC60958-3 driver output.
Thermal Pad	-	<b>Thermal Pad</b> - Thermal relief pad for optimized heat dissipation.

## 2. CHARACTERISTICS AND SPECIFICATIONS

### SPECIFIED OPERATING CONDITIONS

AGND = DGND = 0 V; All voltages with respect to ground.

Parameters	Symbol	Min	Nom	Max	Units	
DC Power Supplies:	Analog	VA	3.13	5.0	5.25	V
	Digital	VD	3.13	3.3	(Note 1)	V
	Logic - Serial Port	VLS	1.71	3.3	5.25	V
	Logic - Control Port	VLC	1.71	3.3	5.25	V
Ambient Operating Temperature (Power Applied)	T <sub>A</sub>	-10	-	+70	°C	

**Notes:** 1. Maximum of VA+0.25 V or 5.25 V, whichever is less.

### ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V All voltages with respect to ground. (Note 2)

Parameter	Symbol	Min	Max	Units	
DC Power Supplies:	Analog	VA	-0.3	+6.0	V
	Digital	VD	-0.3	+6.0	V
	Logic - Serial Port	VLS	-0.3	+6.0	V
	Logic - Control Port	VLC	-0.3	+6.0	V
Input Current (Note 3)	I <sub>in</sub>	-	±10	mA	
Analog Input Voltage	V <sub>INA</sub>	AGND-0.3	VA+0.3	V	
Digital Input Voltage	Logic - Serial Port	V <sub>IND-S</sub>	-0.3	VLS+0.3	V
	Logic - Control Port	V <sub>IND-C</sub>	-0.3	VLC+0.3	V
Ambient Operating Temperature (Power Applied)	T <sub>A</sub>	-50	+125	°C	
Storage Temperature	T <sub>stg</sub>	-65	+150	°C	

- Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
- Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

## DAC ANALOG CHARACTERISTICS

Test Conditions (unless otherwise specified): AGND = DGND = 0 V; VA = 3.13 V to 5.25 V; VD = 3.13 V to 5.25 V or VA + 0.25 V, whichever is less; VLS = VLC = 1.71 V to 5.25 V; T<sub>A</sub> = -10° to +70° C for Commercial or -40° to +85° C for Automotive; Output test signal: 997 Hz full-scale sine wave; Test load R<sub>L</sub> = 3 kΩ, C<sub>L</sub> = 10 pF (see Figure 1), F<sub>s</sub> = 48/96/192 kHz. Measurement Bandwidth 10 Hz to 20 kHz; All Connections as shown in Figure 9 on page 23.

Parameter	Symbol	Commercial Grade			Automotive Grade			Unit	
		Min	Typ	Max	Min	Typ	Max		
<b>Dynamic Performance for VA = 4.75 V to 5.25 V</b>									
Dynamic Range	(Note 4)								
18 to 24-Bit	A-Weighted	98	104	-	96	104	-	dB	
	unweighted	95	101	-	93	101	-	dB	
16-Bit	A-Weighted	90	96	-	88	96	-	dB	
	unweighted	87	93	-	85	93	-	dB	
Total Harmonic Distortion + Noise	(Note 4)								
18 to 24-Bit	0 dB	-	-90	-84	-	-90	-82	dB	
	-20 dB	-	-81	-	-	-81	-	dB	
	-60 dB	-	-41	-	-	-41	-	dB	
16-Bit	0 dB	-	-93	-87	-	-93	-85	dB	
	-20 dB	-	-73	-	-	-73	-	dB	
	-60 dB	-	-33	-	-	-33	-	dB	
<b>Dynamic Performance for VA = 3.13 V to 3.46 V</b>									
Dynamic Range	(Note 4)								
18 to 24-Bit	A-Weighted	95	101	-	93	101	-	dB	
	unweighted	92	98	-	90	98	-	dB	
16-Bit	A-Weighted	88	93	-	86	93	-	dB	
	unweighted	85	90	-	83	90	-	dB	
Total Harmonic Distortion + Noise	(Note 4)								
18 to 24-Bit	0 dB	-	-87	-79	-	-87	-77	dB	
	-20 dB	-	-78	-	-	-78	-	dB	
	-60 dB	-	-38	-	-	-38	-	dB	
16-Bit	0 dB	-	-90	-82	-	-90	-80	dB	
	-20 dB	-	-70	-	-	-70	-	dB	
	-60 dB	-	-30	-	-	-30	-	dB	
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB	
<b>DC Accuracy</b>									
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB	
Gain Drift		-	100	-	-	100	-	ppm/°C	
<b>Analog Output</b>									
Full Scale Output Voltage		0.60*VA	0.65*VA	0.70*VA	0.60*VA	0.65*VA	0.70*VA	V <sub>pp</sub>	
DC Current draw from an AOUT pin	(Note 5)	I <sub>OUT</sub>	-	-	10	-	-	10	μA
AC-Load Resistance	(Note 6)	R <sub>L</sub>	3	-	-	3	-	-	kΩ
Load Capacitance	(Note 6)	C <sub>L</sub>	-	-	100	-	-	100	pF
Output Impedance		Z <sub>OUT</sub>	-	150	-	-	150	-	Ω

4. One-half LSB of triangular PDF dither added to data.
5. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC blocking capacitors.

6. Guaranteed by design. See [Figure 2](#).  $R_L$  and  $C_L$  reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability.  $C_L$  affects the dominant pole of the internal output amp; increasing  $C_L$  beyond 100 pF can cause the internal op-amp to become unstable.

## DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 7,10)	Symbol	Min	Typ	Max	Unit
<b>Combined Digital and On-chip Analog Filter Response</b>		<b>Single-Speed Mode</b>			
Passband (Note 7)	to -0.1 dB corner to -3 dB corner	0	-	0.35	Fs
		0	-	0.4992	Fs
Frequency Response 10 Hz to 20 kHz		-0.175	-	+0.01	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation	(Note 8)	50	-	-	dB
Group Delay	tgd	-	10/Fs	-	s
De-emphasis Error (Note 9)	Fs = 44.1 kHz	-	-	+0.05/-0.25	dB
<b>Combined Digital and On-chip Analog Filter Response</b>		<b>Double-Speed Mode</b>			
Passband (Note 7)	to -0.1 dB corner to -3 dB corner	0	-	0.22	Fs
		0	-	0.501	Fs
Frequency Response 10 Hz to 20 kHz		-0.15	-	+0.15	dB
StopBand		0.5770	-	-	Fs
StopBand Attenuation	(Note 8)	55	-	-	dB
Group Delay	tgd	-	5/Fs	-	s
<b>Combined Digital and On-chip Analog Filter Response</b>		<b>Quad-Speed Mode</b>			
Passband (Note 7)	to -0.1 dB corner to -3 dB corner	0	-	0.110	Fs
		0	-	0.469	Fs
Frequency Response 10 Hz to 20 kHz		-0.12	-	0	dB
StopBand		0.7	-	-	Fs
StopBand Attenuation	(Note 8)	51	-	-	dB
Group Delay	tgd	-	2.5/Fs	-	s

7. Filter response is guaranteed by design.
8. For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.  
For Double-Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.  
For Quad-Speed Mode, the Measurement Bandwidth is 0.7 Fs to 1 Fs.
9. De-emphasis is available only in Single-Speed Mode.
10. Response is clock dependent and will scale with Fs. Note that the amplitude vs. frequency plots of this data ([Figures 18 to 27](#)) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

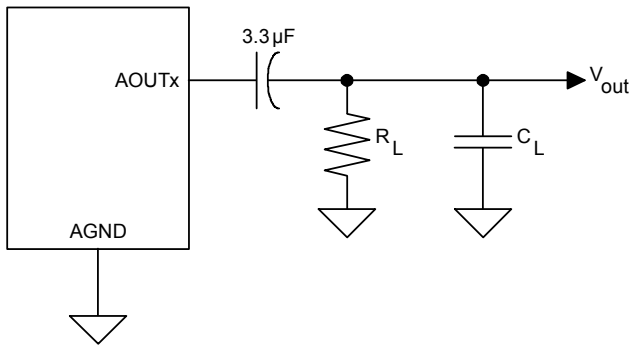


Figure 1. DAC Output Test Load

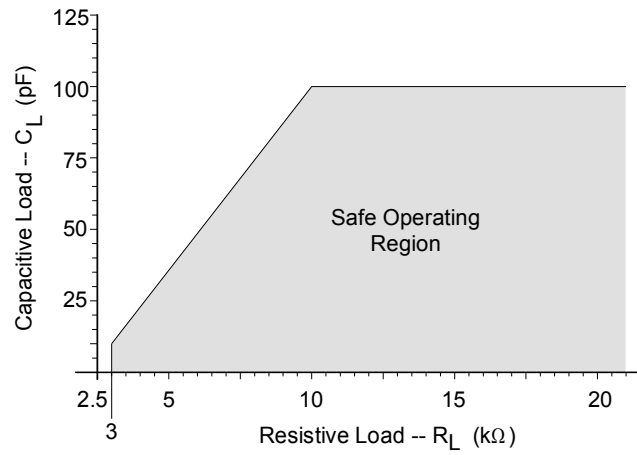


Figure 2. Maximum DAC Loading

## ADC ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VA = 3.13 V to 5.25 V; VD = 3.13 V to 5.25 V or VA + 0.25 V, whichever is less; VLS = VLC = 1.71 V to 5.25 V; T<sub>A</sub> = -10° to +70° C for Commercial or -40° to +85° C for Automotive; Input test signal: 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Fs = 48/96/192 kHz.; All connections as shown in [Figure 9 on page 23](#).

Line-Level Inputs						
Parameter	Symbol	Min	Typ	Max	Unit	
<b>Dynamic Performance for VA = 4.75 V to 5.25 V</b>						
Dynamic Range	PGA Setting: -12 dB to +6 dB					
	A-weighted	98	104	-		dB
	unweighted	95	101	-		dB
(Note 13)	40 kHz bandwidth unweighted	-	98	-		dB
(Note 13)	PGA Setting: +12 dB Gain					
	A-weighted	92	98	-		dB
	unweighted	89	95	-		dB
(Note 13)	40 kHz bandwidth unweighted	-	92	-		dB
<b>Total Harmonic Distortion + Noise (Note 12)</b>						
(Note 13)	PGA Setting: -12 dB to +6 dB					
	-1 dB	-	-95	-89		dB
	-20 dB	-	-81	-		dB
(Note 13)	40 kHz bandwidth -60 dB	-	-41	-		dB
(Note 13)	PGA Setting: +12 dB Gain					
	-1 dB	-	-92	-86		dB
	-20 dB	-	-75	-		dB
(Note 13)	40 kHz bandwidth -60 dB	-	-35	-		dB
(Note 13)	40 kHz bandwidth -1 dB	-	-89	-		dB
<b>Dynamic Performance for VA = 3.13 V to 3.46 V</b>						
Dynamic Range	PGA Setting: -12 dB to +6 dB					
	A-weighted	93	101	-		dB
	unweighted	90	98	-		dB
(Note 13)	40 kHz bandwidth unweighted	-	95	-		dB
(Note 13)	PGA Setting: +12 dB Gain					
	A-weighted	89	95	-		dB
	unweighted	86	92	-		dB
(Note 13)	40 kHz bandwidth unweighted	-	89	-		dB
<b>Total Harmonic Distortion + Noise (Note 12)</b>						
(Note 13)	PGA Setting: -12 dB to +6 dB					
	-1 dB	-	-92	-86		dB
	-20 dB	-	-78	-		dB
(Note 13)	40 kHz bandwidth -60 dB	-	-38	-		dB
(Note 13)	PGA Setting: +12 dB Gain					
	-1 dB	-	-89	-83		dB
	-20 dB	-	-72	-		dB
(Note 13)	40 kHz bandwidth -60 dB	-	-32	-		dB
(Note 13)	40 kHz bandwidth -1 dB	-	-81	-		dB

### Line-Level Inputs

Parameter	Symbol	Commercial Grade			Unit
		Min	Typ	Max	
Interchannel Isolation		-	90	-	dB

<b>DC Accuracy</b>					
Gain Error		-	-	±10	%
Gain Drift		-	±100	-	ppm/°C
<b>Line-Level Input Characteristics</b>					
Full-scale Input Voltage		0.51*VA	0.57*VA	0.63*VA	V <sub>pp</sub>
Input Impedance	(Note 11)	6.12	6.8	7.48	kΩ
Maximum Interchannel Input Impedance Mismatch		-	5	-	%

**Line-Level and Microphone-Level Inputs**

Parameter	Symbol	Commercial Grade			Unit
		Min	Typ	Max	
<b>DC Accuracy</b>					
Interchannel Gain Mismatch		-	0.1	-	dB
<b>Programmable Gain Characteristics</b>					
Gain Step Size		-	0.5	-	dB
Absolute Gain Step Error		-	-	0.4	dB

11. Valid when the line-level inputs are selected.

**ADC ANALOG CHARACTERISTICS**

(Continued)

Microphone-Level Inputs										
Parameter	Symbol	Min	Typ	Max	Unit					
<b>Dynamic Performance for VA = 4.75 V to 5.25 V</b>										
Dynamic Range	PGA Setting: -12 dB to 0 dB									
						A-weighted	77	83	-	dB
						unweighted	74	80	-	dB
PGA Setting: +12 dB										
						A-weighted	65	71	-	dB
						unweighted	62	68	-	dB
Total Harmonic Distortion + Noise (Note 12)	PGA Setting: -12 dB to 0 dB	THD+N								
						-1 dB	-	-80	-74	dB
						-20 dB	-	-60	-	dB
						-60 dB	-	-20	-	dB
						PGA Setting: +12 dB				
						-1 dB	-	-68	-	dB
<b>Dynamic Performance for VA = 3.13 V to 3.46 V</b>										
Dynamic Range	PGA Setting: -12 dB to 0 dB									
						A-weighted	77	83	-	dB
						unweighted	74	80	-	dB
PGA Setting: +12 dB										
						A-weighted	65	71	-	dB
						unweighted	62	68	-	dB
Total Harmonic Distortion + Noise (Note 12)	PGA Setting: -12 dB to 0 dB	THD+N								
						-1 dB	-	-80	-74	dB
						-20 dB	-	-60	-	dB
						-60 dB	-	-20	-	dB
						PGA Setting: +12 dB				
						-1 dB	-	-68	-	dB
Interchannel Isolation		-	80	-	dB					
<b>DC Accuracy</b>										
Gain Error		-	±5	-	%					
Gain Drift		-	±300	-	ppm/°C					
<b>Microphone-Level Input Characteristics</b>										
Full-scale Input Voltage		0.013*VA	0.017*VA	0.021*VA	V <sub>pp</sub>					
Input Impedance (Note 14)		-	60	-	kΩ					

12. Referred to the typical line-level full-scale input voltage

13. Valid for Double- and Quad-Speed Modes only.

14. Valid when the microphone-level inputs are selected.



**ADC DIGITAL FILTER CHARACTERISTICS**

Parameter (Notes 15, 17)	Symbol	Min	Typ	Max	Unit
<b>Single-Speed Mode</b>					
Passband (-0.1 dB)		0	-	0.4896	Fs
Passband Ripple		-	-	0.035	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	$t_{gd}$	-	12/Fs	-	s
<b>Double-Speed Mode</b>					
Passband (-0.1 dB)		0	-	0.4896	Fs
Passband Ripple		-	-	0.025	dB
Stopband		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	$t_{gd}$	-	9/Fs	-	s
<b>Quad-Speed Mode</b>					
Passband (-0.1 dB)		0	-	0.2604	Fs
Passband Ripple		-	-	0.025	dB
Stopband		0.5000	-	-	Fs
Stopband Attenuation		60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	$t_{gd}$	-	5/Fs	-	s
<b>High-Pass Filter Characteristics</b>					
Frequency Response	-3.0 dB		-	1	Hz
	-0.13 dB	(Note 16)		20	Hz
Phase Deviation	@ 20 Hz	(Note 16)		10	Deg
Passband Ripple				0	dB
Filter Settling Time				$10^5/Fs$	s

15. Filter response is guaranteed by design.

16. Response shown is for Fs = 48 kHz.

17. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 30 to 41) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

## DC ELECTRICAL CHARACTERISTICS

AGND = DGND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Fs=48 kHz; Master Mode.

Parameter	Symbol	Min	Typ	Max	Unit	
Power Supply Current (Normal Operation)	VA = 5 V	IA	-	41	50	mA
	VA = 3.3 V	IA	-	37	45	mA
	VD, VLS, VLC = 5 V	ID	-	39	47	mA
	VD, VLS, VLC = 3.3 V	ID	-	23	28	mA
Power Supply Current (Power-Down Mode) (Note 18)	VA = 5 V	IA	-	0.50	-	mA
	VLS, VLC, VD=5 V	ID	-	0.54	-	mA
Power Consumption (Normal Operation)	VA, VD, VLS, VLC = 5 V	-	-	400	485	mW
	VA, VD, VLS, VLC = 3.3 V	-	-	198	241	mW
	(Power-Down Mode)	VA, VD, VLS, VLC = 5 V	-	4.2	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 19)	PSRR	-	55	-	dB
<b>VQ Characteristics</b>						
Quiescent Voltage	(Note 20)	VQ	-	0.5 x VA	-	VDC
DC Current from VQ	(Note 20)	IQ	-	-	1	μA
VQ Output Impedance		ZQ	-	4.5	-	kΩ
FILT+ Nominal Voltage		FILT+	-	VA	-	VDC
Microphone Bias Voltage		MICBIAS	-	0.8 x VA	-	VDC
Current from MICBIAS		IMB	-	-	2	mA

18. Power-Down Mode is defines as  $\overline{\text{RESET}} = \text{Low}$  with all clock and data lines held static and no analog input.
19. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.
20. Guaranteed by design. The DC current draw represents the allowed current draw due to typical leakage through the electrolytic de-coupling capacitors.

**DIGITAL INTERFACE CHARACTERISTICS**

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VLS = VLC = 1.71 V to 5.25 V.

Parameters (Note 21)	Symbol	Min	Typ	Max	Units
High-Level Input Voltage VL = 1.71 V Serial Port Control Port VL > 2.0 V Serial Port Control Port	V <sub>IH</sub>	0.8xVLS	-	-	V
	V <sub>IH</sub>	0.8xVLC	-	-	V
	V <sub>IH</sub>	0.7xVLS	-	-	V
	V <sub>IH</sub>	0.7xVLC	-	-	V
Low-Level Input Voltage Serial Port Control Port	V <sub>IL</sub>	-	-	0.2xVLS	V
	V <sub>IL</sub>	-	-	0.2xVLC	V
High-Level Output Voltage at I <sub>o</sub> = 2 mA Serial Port Control Port MUTEC TXOUT	V <sub>OH</sub>	VLS-1.0	-	-	V
	V <sub>OH</sub>	VLC-1.0	-	-	V
	V <sub>OH</sub>	VA-1.0	-	-	V
	V <sub>OH</sub>	VD-1.0	-	-	V
Low-Level Output Voltage at I <sub>o</sub> = 2 mA Serial Port Control Port MUTEC TXOUT	V <sub>OL</sub>	-	-	0.4	V
	V <sub>OL</sub>	-	-	0.4	V
	V <sub>OL</sub>	-	-	0.4	V
	V <sub>OL</sub>	-	-	0.4	V
Input Leakage Current	I <sub>in</sub>	-	-	±10	μA
Input Capacitance	(Note 22)	-	-	1	pF
Maximum MUTEC Drive Current		-	3	-	mA

21. Serial Port signals include: MCLK, SCLK, LRCK, SDIN1, SDIN2, TXSDIN, SDOOUT.  
Control Port signals include: SCL, SDA, RESET.

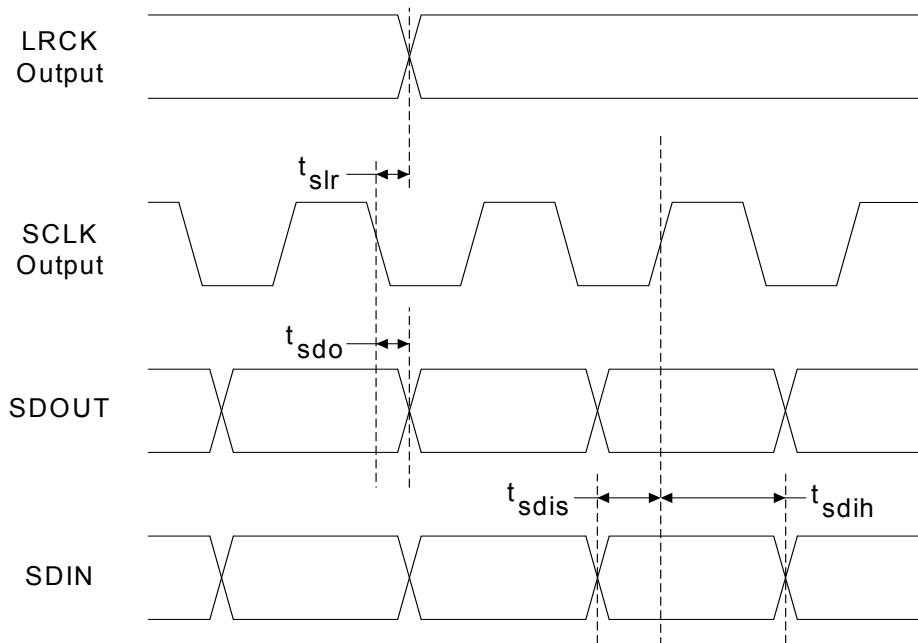
22. Guaranteed by design.

## SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

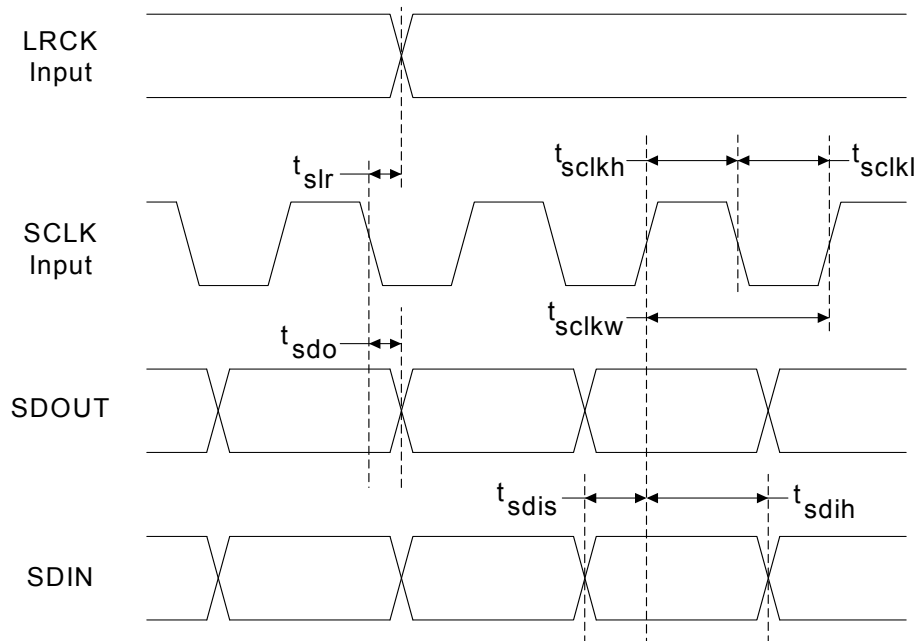
Logic '0' = DGND = AGND = 0 V; Logic '1' = VL, C<sub>L</sub> = 20 pF. (Note 23)

Parameter	Symbol	Min	Typ	Max	Unit	
Sample Rate	Single-Speed Mode	F <sub>s</sub>	4	-	50	kHz
	Double-Speed Mode	F <sub>s</sub>	50	-	100	kHz
	Quad-Speed Mode	F <sub>s</sub>	100	-	200	kHz
<b>MCLK Specifications</b>						
MCLK Frequency	fmclk	1.024	-	51.200	MHz	
MCLK Input Pulse Width High/Low	tclkhl	8	-	-	ns	
MCLK Output Duty Cycle		45	50	55	%	
<b>Master Mode</b>						
LRCK Duty Cycle		-	50	-	%	
SCLK Duty Cycle		-	50	-	%	
SCLK falling to LRCK edge	t <sub>slr</sub>	-10	-	10	ns	
SCLK falling to SDOUT valid	t <sub>sdo</sub>	0	-	36	ns	
SDIN valid to SCLK rising setup time	t <sub>sdis</sub>	16	-	-	ns	
SCLK rising to SDIN hold time	t <sub>sdih</sub>	20	-	-	ns	
<b>Slave Mode</b>						
LRCK Duty Cycle		40	50	60	%	
SCLK Period	Single-Speed Mode	t <sub>sclkw</sub>	$\frac{10^9}{(128)F_s}$	-	-	ns
	Double-Speed Mode	t <sub>sclkw</sub>	$\frac{10^9}{(64)F_s}$	-	-	ns
	Quad-Speed Mode	t <sub>sclkw</sub>	$\frac{10^9}{(64)F_s}$	-	-	ns
SCLK Pulse Width High	t <sub>sclkh</sub>	30	-	-	ns	
SCLK Pulse Width Low	t <sub>sckl</sub>	48	-	-	ns	
SCLK falling to LRCK edge	t <sub>slr</sub>	-10	-	10	ns	
SCLK falling to SDOUT valid	t <sub>sdo</sub>	0	-	36	ns	
SDIN valid to SCLK rising setup time	t <sub>sdis</sub>	16	-	-	ns	
SCLK rising to SDIN hold time	t <sub>sdih</sub>	20	-	-	ns	

23. See Figures 3 and 4 on page 20.



**Figure 3. Master Mode Serial Audio Port Timing**



**Figure 4. Slave Mode Serial Audio Port Timing**



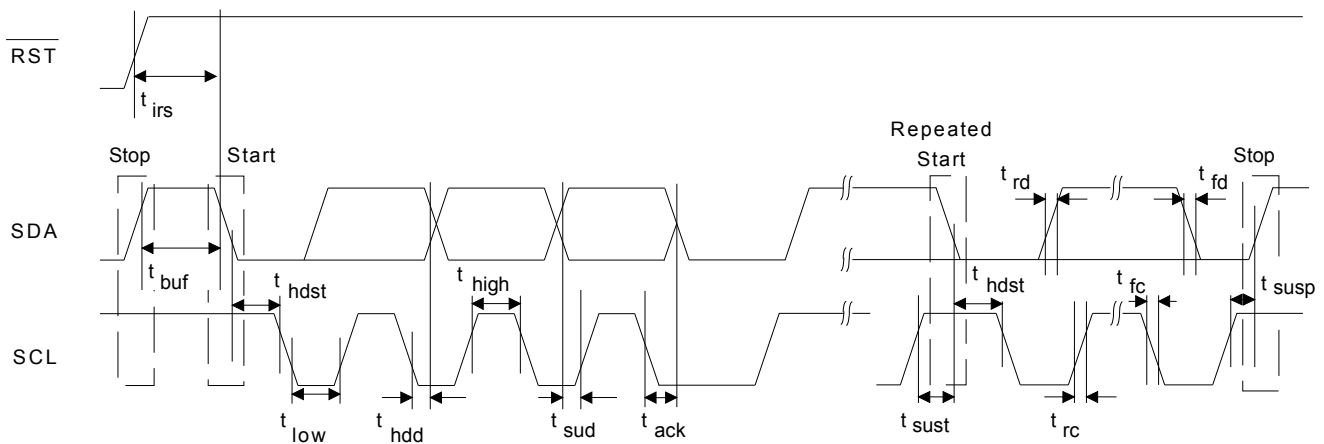
## SWITCHING CHARACTERISTICS - I<sup>2</sup>C CONTROL PORT

Inputs: Logic 0 = DGND = AGND = 0 V, Logic 1 = VLC, C<sub>L</sub> = 30 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f <sub>scl</sub>	-	100	kHz
RESET Rising Edge to Start	t <sub>irs</sub>	500	-	ns
Bus Free Time Between Transmissions	t <sub>buf</sub>	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t <sub>hdst</sub>	4.0	-	μs
Clock Low time	t <sub>low</sub>	4.7	-	μs
Clock High Time	t <sub>high</sub>	4.0	-	μs
Setup Time for Repeated Start Condition	t <sub>sust</sub>	4.7	-	μs
SDA Hold Time from SCL Falling (Note 24)	t <sub>hdd</sub>	0	-	μs
SDA Setup time to SCL Rising	t <sub>sud</sub>	250	-	ns
Rise Time of SCL and SDA (Note 25)	t <sub>rc</sub> , t <sub>rd</sub>	-	1	μs
Fall Time SCL and SDA (Note 25)	t <sub>fc</sub> , t <sub>fd</sub>	-	300	ns
Setup Time for Stop Condition	t <sub>susp</sub>	4.7	-	μs
Acknowledge Delay from SCL Falling	t <sub>ack</sub>	300	1000	ns

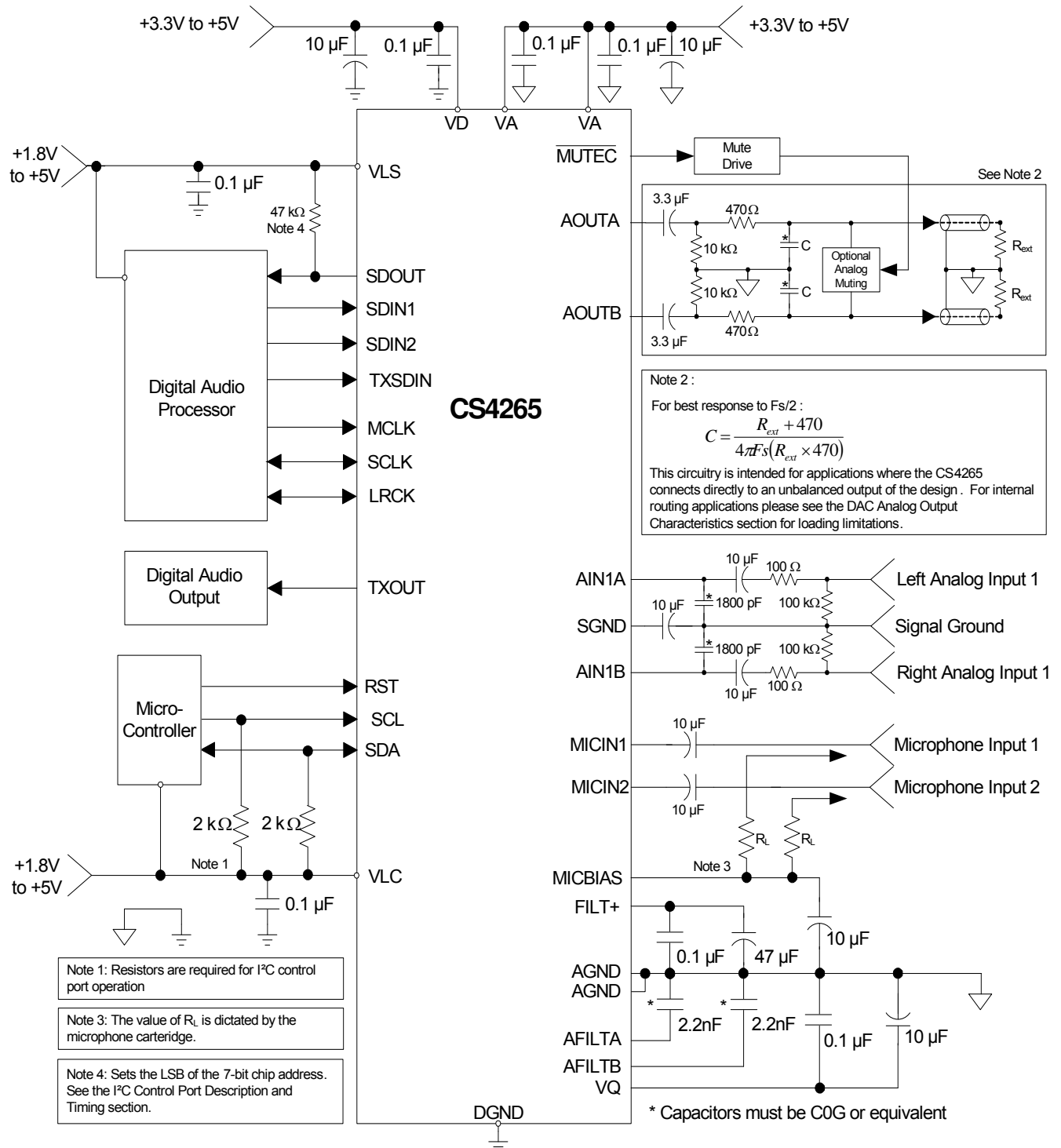
24. Data must be held for sufficient time to bridge the transition time, t<sub>fc</sub>, of SCL.

25. Guaranteed by design.



**Figure 8. Control Port Timing - I<sup>2</sup>C Format**

### 3. TYPICAL CONNECTION DIAGRAM



**Figure 9. Typical Connection Diagram**



## 4. APPLICATIONS

### 4.1 Recommended Power-Up Sequence

1. Hold  $\overline{\text{RESET}}$  low until the power supply, MCLK, and LRCK are stable. In this state, the Control Port is reset to its default settings.
2. Bring  $\overline{\text{RESET}}$  high. The device will remain in a low power state with the PDN bit set by default. The control port will be accessible.
3. The desired register settings can be loaded while the PDN bit remains set.
4. Clear the PDN bit to initiate the power-up sequence.

### 4.2 System Clocking

The CS4265 will operate at sampling frequencies from 4 kHz to 200 kHz. This range is divided into three speed modes as shown in [Table 1](#).

Mode	Sampling Frequency
<i>Single-Speed</i>	4-50 kHz
<i>Double-Speed</i>	50-100 kHz
<i>Quad-Speed</i>	100-200 kHz

Table 1. Speed Modes

#### 4.2.1 Master Clock

MCLK/LRCK must maintain an integer ratio as shown in [Table 2](#). The LRCK frequency is equal to  $F_s$ , the frequency at which audio samples for each channel are clocked into or out of the device. The FM bits (See “[Functional Mode \(Bits 7:6\)](#)” on page 38.) and the MCLK Freq bits (See “[MCLK Frequency - Address 05h](#)” on page 39.) configure the device to generate the proper clocks in Master Mode, and receive the proper clocks in Slave Mode. [Table 2](#) illustrates several standard audio sample rates and the required MCLK and LRCK frequencies.

LRCK (kHz)	MCLK (MHz)								
	64x	96x	128x	192x	256x	384x	512x	768x	1024x
32	-	-	-	-	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1584
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520
64	-	-	8.1920	12.2880	16.3840	24.5760	32.7680	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	45.1584	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-	-
128	8.1920	12.2880	16.3840	24.5760	32.7680	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	45.1584	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	49.1520	-	-	-	-
Mode	QSM				DSM			SSM	

Table 2. Common Clock Frequencies

In both Master and Slave Modes, the external MCLK must be divided down based on the MCLK/LRCK ratio to achieve a post-divider MCLK/LRCK ratio of 256x for SSM, 128x for DSM, or 64x for QSM. Table 3 lists the appropriate dividers.

MCLK/LRCK Ratio	MCLK Dividers		
<b>64x</b>	-	-	÷1
<b>96x</b>	-	-	÷1.5
<b>128x</b>	-	÷1	÷2
<b>192x</b>	-	÷1.5	÷3
<b>256x</b>	÷1	÷2	÷4
<b>384x</b>	÷1.5	÷3	-
<b>512x</b>	÷2	÷4	-
<b>768x</b>	÷3	-	-
<b>1024x</b>	÷4	-	-
<b>Mode</b>	<b>SSM</b>	<b>DSM</b>	<b>QSM</b>

Table 3. MCLK Dividers

### 4.2.2 Master Mode

As a clock master, LRCK and SCLK will operate as outputs. LRCK and SCLK are internally derived from MCLK with LRCK equal to  $F_s$  and SCLK equal to  $64 \times F_s$  as shown in Figure 10.

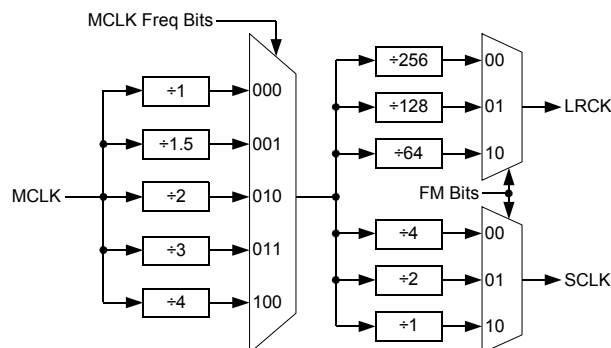


Figure 10. Master Mode Clocking

### 4.2.3 Slave Mode

In Slave Mode, SCLK and LRCK operate as inputs. The Left/Right clock signal must be equal to the sample rate,  $F_s$ , and must be synchronously derived from the supplied master clock, MCLK.

The serial bit clock, SCLK, must be synchronously derived from the master clock, MCLK, and be equal to 128x, 64x, 48x or 32x  $F_s$ , depending on the desired speed mode. Refer to Table 4 for required clock ratios.

	Single-Speed	Double-Speed	Quad-Speed
SCLK/LRCK Ratio	32x, 48x, 64x, 128x	32x, 48x, 64x	32x, 48x, 64x

Table 4. Slave Mode Serial Bit Clock Ratios

## 4.3 High-Pass Filter and DC Offset Calibration

When using operational amplifiers in the input circuitry driving the CS4265, a small DC offset may be driven into the A/D converter. The CS4265 includes a high-pass filter after the decimator to remove any DC offset