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24-Bit, 192 kHz Stereo Audio CODEC

D/A Features
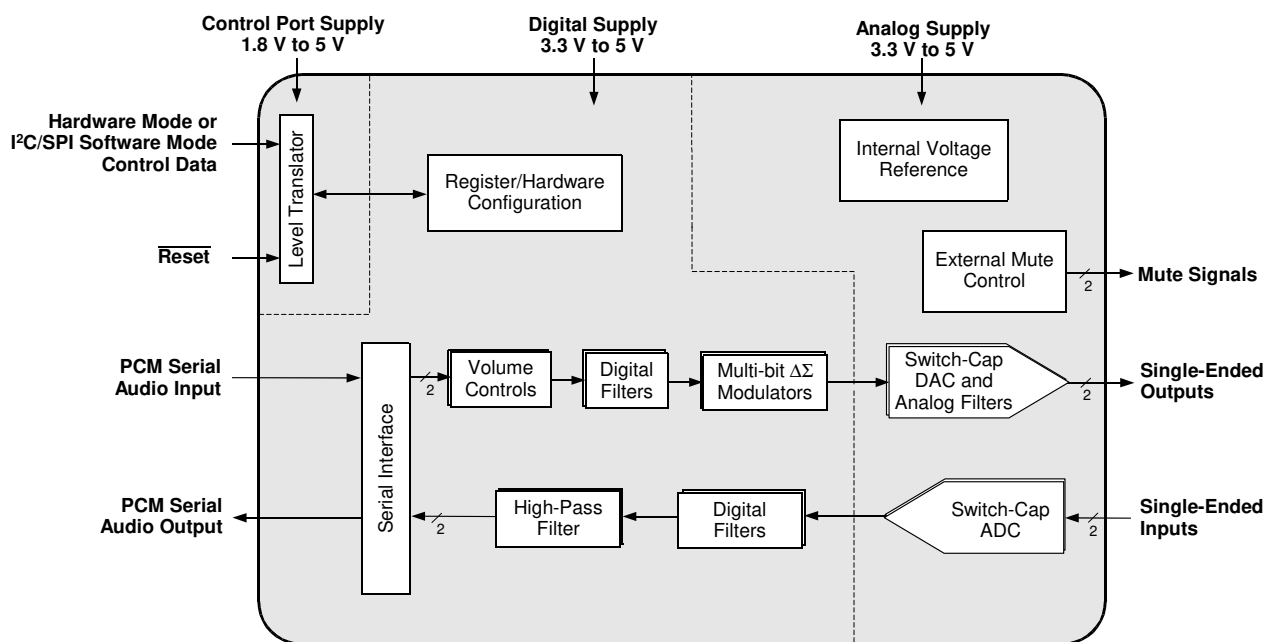
♦ High Performance
  – 105 dB Dynamic Range
  – -95 dB THD+N

♦ Selectable Serial Audio Interface Formats
  – Left-Justified up to 24-bit
  – I²S up to 24-bit
  – Right-Justified 16-, and 24-Bit

♦ Control Output for External Muting

♦ On-Chip Digital De-Emphasis

♦ Popguard® Technology

♦ Multi-bit $\Delta\Sigma$ Conversion

♦ Digital Volume Control

♦ Single-Ended Output

A/D Features

♦ High Performance
  – 105 dB Dynamic Range
  – -95 dB THD+N

♦ Multi-bit $\Delta\Sigma$ Conversion

♦ High-Pass Filter to Remove DC Offsets

♦ Selectable Serial Audio Interface Formats
  – Left-Justified up to 24-bit
  – I²S up to 24-bit

♦ Single-Ended Input

System Features

♦ Direct Interface with Logic Levels 1.8 V to 5 V

♦ Internal Digital Loopback

♦ Stand-Alone or Control Port Functionality

♦ Single-Ended Analog Architecture

♦ Supports all Audio Sample Rates from 4 kHz to 216 kHz

♦ 3.3 V or 5 V Core Supply

Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Stand-Alone Mode Feature Set

♦ System Features

  – Serial Audio Port Master or Slave Operation

  – Single-, Double-, or Quad-Speed Operation

♦ D/A Features

  – Auto-Mute on Static Samples

  – 44.1 kHz 50/15 μs De-emphasis Available

  – Selectable Serial Audio Interface Formats

    • Left-Justified up to 24-bit

    • I²S up to 24-bit

♦ A/D Features

  – High-Pass Filter

  – Selectable Serial Audio Interface Formats

    • Left-Justified up to 24-bit

    • I²S up to 24-bit

Software Mode Feature Set

♦ System Features

  – Serial Audio Port Master or Slave Operation

  – Internal Digital Loopback Available

♦ D/A Features

  – Selectable Auto-mute

  – 44.1-kHz De-emphasis Filters

  – Configurable Muting Controls

  – Volume Control

  – Selectable Serial Audio Interface Formats

    • Left-Justified up to 24-bit

    • I²S up to 24-bit

    • Right-Justified 16, and 24-bit

♦ A/D Features

  – Selectable High-Pass Filter or DC Offset Calibration

  – Selectable Serial Audio Interface Formats

    • Left-Justified up to 24-bit

    • I²S up to 24-bit

General Description

The CS4270 is a high-performance, integrated audio CODEC. The CS4270 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 216 kHz.

Standard 50/15 μs de-emphasis is available for sampling rates of 44.1 kHz for compatibility with digital audio programs mastered using the 50/15 μs pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4270 and other devices operating over a wide range of logic levels.

Independently addressable high-pass filters are available for the right and left channel of the A/D. This allows the A/D to be used in a wide variety of applications where one audio channel and one DC measurement channel is desired.

The CS4270 is available in a 24-pin TSSOP package in both Commercial (-10° to +70° C) and Automotive grades (-40° to +85° C). The CDB4270 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to for complete ordering information.

The CS4270's wide dynamic range, negligible distortion, and low noise make it ideal for applications such as DVD-recorders, digital televisions, set-top boxes, effects processors, and automotive audio systems.

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LIST OF TABLES

1. PIN DESCRIPTIONS - SOFTWARE MODE

```
            SDIN  ⊏ 1 ●        24 ⊐  MUTEB
            LRCK  ⊏ 2          23 ⊐  AOUTB
            MCLK  ⊏ 3          22 ⊐  AOUTA
            SCLK  ⊏ 4          21 ⊐  MUTEA
              VD  ⊏ 5          20 ⊐  AGND
            DGND  ⊏ 6          19 ⊐  VA
           SDOUT  ⊏ 7          18 ⊐  FILT+
             VLC  ⊏ 8          17 ⊐  VQ
       SDA/CDOUT  ⊏ 9          16 ⊐  AINB
        SCL/CCLK  ⊏ 10         15 ⊐  AINA
          AD0/CS  ⊏ 11         14 ⊐  RST
        AD1/CDIN  ⊏ 12         13 ⊐  AD2
```

Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
LRCK	2	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	3	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
SCLK	4	**Serial Clock** (*Input/Output*) - Serial clock for the serial audio interface.
VD	5	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	6	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
SDOUT	7	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
VLC	8	**Control Port Power** (*Input*) - Determines the signal level for the Control Port.
SDA/CDOUT	9	**Serial Control Data** (*Input/Output*) - SDA is a data I/O in I²C® Mode. CDOUT is the output data line for the Control Port interface in SPI® Mode.
SCL/CCLK	10	**Serial Control Port Clock** (*Input*) - Serial clock for the serial Control Port.
AD0/CS	11	**Address Bit 0 (I²C)** / **Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode. CS is the chip select signal for SPI format.
AD1/CDIN	12	**Address Bit 1 (I²C)** / **Serial Control Data** (*Input*) - AD1 is a chip address pin in I²C Mode. CDIN is the input data line for the Control Port interface in SPI Mode.
AD2	13	**Address Bit 2 (I²C)** (*Input*) - AD2 is a chip address pin in I²C Mode.
RST	14	**Reset** (*Input*) - The device enters a low power mode when low.
AINA AINB	15 16	**Analog Input** (*Input*) - The full-scale analog input level is specified in the ADC Analog Characteristics specification table.
VQ	17	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
VA	19	**Analog Power** (*Input*) - Positive power for the analog sections.
AGND	20	**Analog Ground** (*Input*) - Ground reference. Must be connected to analog ground.
MUTEA MUTEB	21 24	**Mute Control** (*Output*) - Each pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
AOUTA AOUTB	22 23	**Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.

2. PIN DESCRIPTIONS - STAND-ALONE MODE

```
        SDIN  ☐☐ 1 ●      24 ☐☐  MUTEB
        LRCK  ☐☐ 2        23 ☐☐  AOUTB
        MCLK  ☐☐ 3        22 ☐☐  AOUTA
        SCLK  ☐☐ 4        21 ☐☐  MUTEA
          VD  ☐☐ 5        20 ☐☐  AGND
        DGND  ☐☐ 6        19 ☐☐  VA
       SDOUT  ☐☐ 7        18 ☐☐  FILT+
         VLC  ☐☐ 8        17 ☐☐  VQ
          M1  ☐☐ 9        16 ☐☐  AINB
          M0  ☐☐ 10       15 ☐☐  AINA
      I²S/LJ  ☐☐ 11       14 ☐☐  RST
       MDIV1  ☐☐ 12       13 ☐☐  MDIV2
```

Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input (*Input*)** - Input for two's complement serial audio data.
LRCK	2	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	3	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
SCLK	4	**Serial Clock (*Input*/*Output*)** - Serial clock for the serial audio interface.
VD	5	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	6	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
SDOUT (M/S̄)	7	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data. This pin must be pulled-up or pulled-down to select Master or Slave Mode.
VLC	8	**Control Port Power** (*Input*) - Determines the signal level for the Control Port.
M1 M0	9 10	**Mode Selection** (*Input*) - Determines the operational mode of the device.
I²S/LJ̄	11	**Serial Audio Interface Select** *(Input)* - Selects either the Left-Justified or I²S format for the Serial Audio Interface.
MDIV1 MDIV2	12 13	**MCLK Divide** (*Input*) - Configures MCLK divider to divide by 1, 1.5, 2, or 4.
R̄S̄T̄	14	**Reset** (*Input*) - The device enters a low power mode when low.
AINA AINB	15 16	**Analog Input** (*Input*) - The full-scale analog input level is specified in the ADC Analog Characteristics specification table.
VQ	17	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
VA	19	**Analog Power (*Input*)** - Positive power for the analog sections.
AGND	20	**Analog Ground** (*Input*) - Ground reference. Must be connected to analog ground.
M̄ŪT̄ĒĀ M̄ŪT̄ĒB̄	21 24	**Mute Control** *(Output)* - Each pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
AOUTA AOUTB	22 23	**Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table.

3. TYPICAL CONNECTION DIAGRAM

Figure 1. CS4270 Typical Connection Diagram

1. If using separate supplies for VA and VD, 5.1 Ω resistor not needed. See "Grounding and Power Supply Decoupling."

2. Use a 47 kΩ pull-down to select Slave Mode or 47 kΩ pull-up to VD to select Master Mode. See "Master/Slave Mode Selection."

3. Use pull-up resistors in Software Mode. In Hardware Mode, use pull-up or pull-down. See "Mode Selection & De-Emphasis."

4. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Analog	VA	3.1	5.0	5.25	V
	Digital	VD	3.1	3.3	5.25	V
	Control Port Interface	VLC	1.7	3.3	5.25	V
Ambient Operating Temperature (Power Applied)	Commercial	T_A	-10	-	+70	°C
	Automotive		-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V, All voltages with respect to ground.) (Note 1)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Analog	VA	-0.3	-	+6.0	V
	Digital	VD	-0.3	-	+6.0	V
	Control Port Interface	VLC	-0.3	-	+6.0	V
Input Current	(Note 2)	I_{in}	-10	-	+10	mA
Analog Input Voltage		V_{IN}	AGND-0.7	-	VA+0.7	V
Digital Input Voltage	Control Port Interface	V_{IND-C}	-0.3	-	VLC+0.3	V
	Digital Interface	V_{IND-D}	-0.3		VD+0.3	V
Ambient Operating Temperature (Power Applied)		T_{AC}	-50	-	+95	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes:

1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SRC latch-up.

THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Allowable Junction Temperature			-	-	135	°C
Junction to Ambient Thermal Impedance (Note 3)	(Multi-layer PCB) TSSOP	θ_{JA-M}	-	70	-	°C/W
	(Single-layer PCB) TSSOP	θ_{JA-S}	-	105	-	°C/W

3. θ_{JA} is specified according to JEDEC specifications for multi-layer PCBs.

DAC ANALOG CHARACTERISTICS - COMMERCIAL GRADE

(Full-Scale Output Sine Wave, 997 Hz (Note 4), Fs = 48/96/192 kHz; Test load R_L = 3 kΩ, C_L = 10 pF
(see Figure 2). Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

Parameter			VA = 5 V			VA = 3.3 V			Unit
			Min	Typ	Max	Min	Typ	Max	
Dynamic Range	18 to 24-Bit	A-weighted	99	105	-	97	103	-	dB
		unweighted	96	102	-	94	100	-	dB
	16-Bit	A-weighted	90	96	-	90	96	-	dB
		unweighted	87	93	-	87	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-89	-83	-	-89	-83	dB
		-20 dB	-	-76	-70	-	-76	-70	dB
		-60 dB	-	-36	-30	-	-36	-30	dB
	16-Bit	0 dB	-	-87	-81	-	-87	-81	dB
		-20 dB	-	-67	-61	-	-67	-61	dB
		-60 dB	-	-27	-21	-	-27	-21	dB

DAC ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE

(Full-Scale Output Sine Wave, 997 Hz (Note 4), Fs = 48/96/192 kHz; Test load R_L = 3 kΩ, C_L = 10 pF
(see Figure 2). Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

Parameter			VA = 5 V			VA = 3.3 V			Unit
			Min	Typ	Max	Min	Typ	Max	
Dynamic Range	18 to 24-Bit	A-weighted	95	105	-	93	103	-	dB
		unweighted	92	102	-	90	100	-	dB
	16-Bit	A-weighted	86	96	-	86	96	-	dB
		unweighted	83	93	-	83	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-89	-79	-	-89	-79	dB
		-20 dB	-	-76	-66	-	-76	-66	dB
		-60 dB	-	-36	-26	-	-36	-26	dB
	16-Bit	0 dB	-	-87	-77	-	-87	-77	dB
		-20 dB	-	-67	-57	-	-67	-57	dB
		-60 dB	-	-27	-17	-	-27	-17	dB

4.   One-half LSB of triangular PDF dither added to data.

DAC ANALOG CHARACTERISTICS - ALL MODES

Parameter		Symbol	Min	Typ	Max	Unit
Interchannel Isolation	(1 kHz)		-	100	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	0.25	dB
Gain Drift			-100		+100	ppm/°C
Analog Output						
Full Scale Output Voltage			0.6•VA	0.65•VA	0.7•VA	Vpp
Max DC Current draw from AOUTA or AOUTB		I_{OUTmax}	-	10	-	μA
Max AC-Load Resistance (see Figure 3)		R_L	-	3	-	kΩ
Max Load Capacitance (see Figure 3)		C_L	-	100	-	pF
Output Impedance of AOUTA and AOUTB		Z_{OUT}	-	100	-	Ω
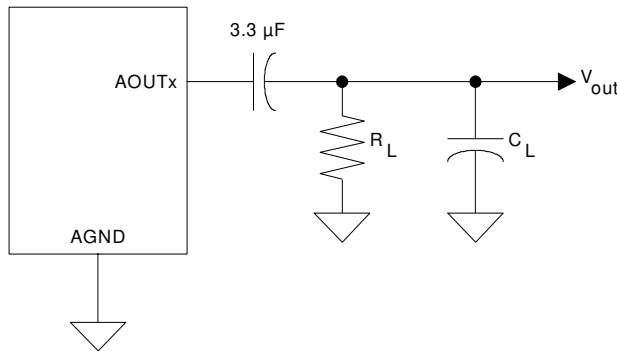
Figure 2. Output Test Load
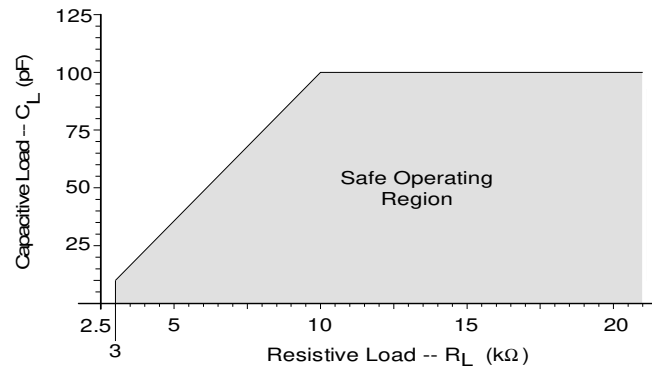
Figure 3. Maximum Loading

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.) (See Note 5)

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Passband (Note 6)	to -0.1 dB corner		0	-	.35	Fs
	to -3 dB corner		0	-	.4992	Fs
Frequency Response 10 Hz to 20 kHz			-.175	-	+.01	dB
StopBand			.5465	-	-	Fs
StopBand Attenuation	(Note 7)		50	-	-	dB
Group Delay		tgd	-	10/Fs	-	s
De-emphasis Error (Note 8)	Fs = 32 kHz		-	-	+1.5/+0	dB
	Fs = 44.1 kHz		-	-	+.05/-.25	dB
	Fs = 48 kHz		-	-	-.2/-.4	dB
Double-Speed Mode						
Passband (Note 6)	to -0.1 dB corner		0	-	.22	Fs
	to -3 dB corner		0	-	.501	Fs
Frequency Response 10 Hz to 20 kHz			-.15	-	+.15	dB
StopBand			.5770	-	-	Fs
StopBand Attenuation	(Note 7)		55	-	-	dB
Group Delay		tgd	-	5/Fs	-	s
Quad-Speed Mode						
Passband (Note 6)	to -0.1 dB corner		0	-	0.110	Fs
	to -3 dB corner		0	-	0.469	Fs
Frequency Response 10 Hz to 20 kHz			-.12	-	+0	dB
StopBand			0.7	-	-	Fs
StopBand Attenuation	(Note 7)		51	-	-	dB
Group Delay		tgd	-	2.5/Fs	-	s

5. Amplitude vs. Frequency plots of this data are available in Section 9. "Filter Plots" on page 41. See Figures 24 through 47.

6. Response is clock dependent and will scale with Fs.

7. For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
   For Double-Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
   For Quad-Speed Mode, the Measurement Bandwidth is 0.7 Fs to 1 Fs.

8. De-emphasis is available only in Single-Speed Mode.

ADC ANALOG CHARACTERISTICS - COMMERCIAL GRADE

Measurement bandwidth is 10 Hz to 20 kHz unless otherwise specified. Figure 18 input circuit, 1 kHz sine wave in.

Dynamic Performance for Commercial Grade			VA = 5 V			VA = 3.3 V			
Single-Speed Mode Fs = 48 kHz	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Range A-weighted unweighted		99 96	105 102	- -	96 93	102 99	- -	dB dB
Total Harmonic Distortion + Noise (Note 9) -1 dB -20 dB -60 dB	THD+N	- - -	-95 -82 -42	-90 - -	- - -	-92 -79 -39	-87 - -	dB dB dB
Double-Speed Mode Fs = 96 kHz								
Dynamic Range A-weighted unweighted 40 kHz bandwidth unweighted		99 96 -	105 102 99	- - -	96 93 -	102 99 96	- - -	dB dB dB
Total Harmonic Distortion + Noise (Note 9) -1 dB -20 dB -60 dB 40 kHz bandwidth -1 dB	THD+N	- - - -	-95 -82 -42 -95	-90 - - -	- - - -	-92 -79 -39 -87	-87 - - -	dB dB dB dB
Quad-Speed Mode Fs = 192 kHz								
Dynamic Range A-weighted unweighted 40 kHz bandwidth unweighted		99 96 -	105 102 99	- - -	96 93 -	102 99 96	- - -	dB dB dB
Total Harmonic Distortion + Noise (Note 9) -1 dB -20 dB -60 dB 40 kHz bandwidth -1 dB	THD+N	- - - -	-95 -82 -42 -95	-90 - - -	- - - -	-92 -79 -39 -87	-87 - - -	dB dB dB dB

Dynamic Performance for Commercial Grade - All Modes					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Interchannel Isolation		-	90	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error		-3	-	+3	%
Gain Drift		-	±100	-	ppm/°C
Analog Input Characteristics					
Full-Scale Input Voltage		0.53*VA	0.56*VA	0.58*VA	Vpp
Input Impedance		-	300	-	kΩ

9. Referred to the typical full-scale input voltage.

ADC ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE

Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Figure 18 input circuit, 1 kHz sine wave in.

Dynamic Performance for Automotive Grade			VA = 5 V			VA = 3.3 V			
Single-Speed Mode Fs = 48 kHz	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Range A-weighted		97	105	-	94	102	-	dB
unweighted		94	102	-	91	99	-	dB
Total Harmonic Distortion + Noise (Note 10)	THD+N							
-1 dB		-	-95	-90	-	-92	-87	dB
-20 dB		-	-82	-	-	-79	-	dB
-60 dB		-	-42	-	-	-39	-	dB
Double-Speed Mode Fs = 96 kHz								
Dynamic Range A-weighted		97	105	-	94	102	-	dB
unweighted		94	102	-	91	99	-	dB
40 kHz bandwidth unweighted		-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise (Note 10)	THD+N							
-1 dB		-	-95	-90	-	-92	-87	dB
-20 dB		-	-82	-	-	-79	-	dB
-60 dB		-	-42	-	-	-39	-	dB
40 kHz bandwidth -1 dB		-	-95	-	-	-87	-	dB
Quad-Speed Mode Fs = 192 kHz								
Dynamic Range A-weighted		97	105	-	94	102	-	dB
unweighted		94	102	-	91	99	-	dB
40 kHz bandwidth unweighted		-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise (Note 10)	THD+N							
-1 dB		-	-95	-90	-	-92	-87	dB
-20 dB		-	-82	-	-	-79	-	dB
-60 dB		-	-42	-	-	-39	-	dB
40 kHz bandwidth -1 dB		-	-95	-	-	-87	-	dB

Dynamic Performance for Automotive Grade - All Modes					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Interchannel Isolation		-	90	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error		-3	-	+3	%
Gain Drift		-	±100	-	ppm/°C
Analog Input Characteristics					
Full-Scale Input Voltage		0.53*VA	0.56*VA	0.58*VA	Vpp
Input Impedance		-	300	-	kΩ

10. Referred to the typical full-scale input voltage.

ADC DIGITAL FILTER CHARACTERISTICS

(Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified) (Note 11)

Parameter			Symbol	Min	Typ	Max	Unit
Single-Speed Mode							
Passband	(-0.1 dB)	(Note 12)		0	-	0.49	Fs
Passband Ripple				-	-	0.035	dB
Stopband		(Note 12)		0.57	-	-	Fs
Stopband Attenuation				70	-	-	dB
Group Delay			t_{gd}	-	12/Fs	-	s
Double-Speed Mode							
Passband	(-0.1 dB)	(Note 12)		0	-	0.49	Fs
Passband Ripple				-	-	0.05	dB
Stopband		(Note 12)		0.56	-	-	Fs
Stopband Attenuation				69	-	-	dB
Group Delay			t_{gd}	-	9/Fs	-	s
Quad-Speed Mode							
Passband	(-0.1 dB)	(Note 12)		0	-	0.26	Fs
Passband Ripple				-	-	0.05	dB
Stopband		(Note 12)		0.50	-	-	Fs
Stopband Attenuation				60	-	-	dB
Group Delay			t_{gd}	-	5/Fs	-	s
High-Pass Filter Characteristics							
Frequency Response	-3.0 dB			-	1	-	Hz
	-0.13 dB	(Note 13)			20	-	Hz
Phase Deviation	@ 20 Hz	(Note 13)		-	10	-	deg
Passband Ripple				-	-	0	dB

11. Plots of this data are contained in Section 9. "Filter Plots" on page 41. See Figures 24 through 47.

12. The filter frequency response scales precisely with Fs.

13. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

DC ELECTRICAL CHARACTERISTICS

(T_A = 25° C; AGND=DGND=0, all voltages with respect to ground; MLCK=12.288 MHz; Master Mode)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply					
Power Supply Current VA = 5 V	I_A	-	31	40	mA
(Normal Operation) VA = 3.3 V	I_A	-	27	35	mA
VD, VLC = 5 V	I_D	-	29	38	mA
VD, VLC = 3.3 V	I_D	-	20	29	mA
Power Supply Current VA = 5 V	I_A	-	1.51	-	mA
(Power-Down Mode) (Note 14) VD, VLC = 5 V	I_D	-	0.45	-	mA
Power Consumption					
VA = 5 V, VD = VLC= 3.3 V Normal Operation	-	-	221	296	mW
VA = 5 V, VD = VLC = 5 V Normal Operation	-	-	255	-	mW
Power-Down Mode (Note 14)	-	-	9.8	323	mW
Power Supply Rejection Ratio (1 kHz) (Note 15)	PSRR	-	55	-	dB
Common Mode Voltage					
Nominal Common Mode Voltage	VQ	-	VA/2	-	VDC
Maximum DC Current Source/Sink from VQ		-	1	-	µA
VQ Output Impedance		-	25	-	kΩ
Positive Voltage Reference					
FILT+ Nominal Voltage	FILT+	-	VA	-	VDC
Maximum DC Current Source/Sink from FILT+		-	10	-	µA
FILT+ Output Impedance		-	18	-	kΩ
Mute Control					
MUTEA, MUTEB Low-Level Output Voltage		-	0	-	V
MUTEA, MUTEB High-Level Output Voltage		-	VA	-	V
Maximum MUTEA & MUTEB Drive Current		-	3	-	mA

14. Power Down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

15. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

Parameter (Note 16)	Symbol	Min	Typ	Max	Units
High-Level Input Voltage Serial Port	V_{IH}	0.7xVD	-	-	V
Control Port		0.7xVLC	-	-	V
Low-Level Input Voltage Serial Port	V_{IL}	-	-	0.2xVD	V
Control Port		-	-	0.2xVLC	V
High-Level Output Voltage at I_o = 2 mA Serial Port	V_{OH}	VD - 1.0	-	-	V
Control Port		VLC - 1.0	-	-	V
MUTEA, MUTEB		VA - 1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-10	-	10	µA

16. Serial Port signals include: SCLK, LRCK, SDOUT, SDIN
    Control Port signals include: SDA/CDOUT, SCL/CCLK, AD1/CDIN, AD0/$\overline{CS}$, $\overline{RST}$

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

(Logic "0" = AGND = 0 V; Logic "1" = VD, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rate	Single-Speed Mode	Fs	4	-	54	kHz
	Double-Speed Mode	Fs	50	-	108	kHz
	Quad-Speed Mode	Fs	100	-	216	kHz
MCLK Specifications						
MCLK Frequency	tand-Alone Mode	fmclk	1.024	-	55.296	MHz
(Note 17)	Control Port Mode	fmclk	1.024	-	55.296	MHz
MCLK Duty Cycle			40	50	60	ns
Master Mode						
LRCK Duty Cycle			-	50	-	%
SCLK Period (Note 18)		t_{sclkw}	-	$\frac{1}{(64)Fs}$	-	s
SCLK Duty Cycle			-	50	-	%
SCLK falling to LRCK edge		t_{mslr}	-20	-	20	ns
SCLK falling to SDOUT valid		t_{sdo}	-	-	32	ns
SDIN valid to SCLK rising setup time		t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time		t_{sdih}	20	-	-	ns
Slave Mode						
LRCK Duty Cycle			40	50	60	%
SCLK Period (Note 17)	Single-Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	s
	Double-Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	s
	Quad-Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	s
SCLK Duty Cycle			45	50	55	ns
SCLK falling to LRCK edge		t_{slrd}	-20	-	20	ns
SDOUT valid before SCLK rising		t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising		t_{hld}	5	-	-	ns
SDIN valid to SCLK rising setup time		t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time		t_{sdih}	20	-	-	ns

17. In Control Port Mode, MCLK Frequency and Functional Mode Select bits must be configured according to Table 5, Table 8, and Table 12.

18. $t_{sclkw} = t_{sclkh} + t_{sclkl}$ in Figures 5 and 7.
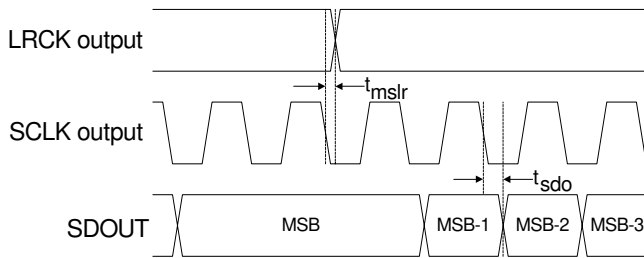
Figure 4. Master Mode, Left-Justified SAI
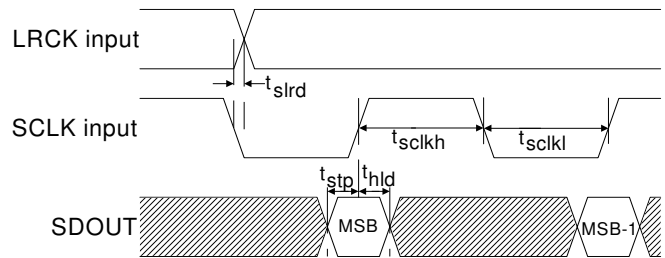
Figure 5. Slave Mode, Left-Justified SAI
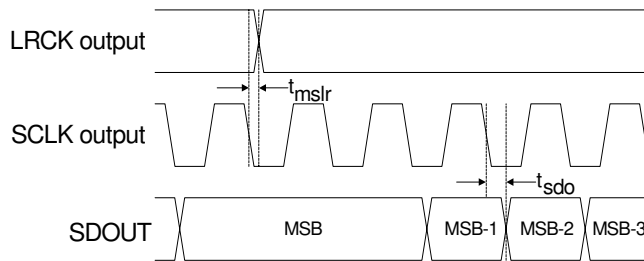
Figure 6. Master Mode, I²S SAI
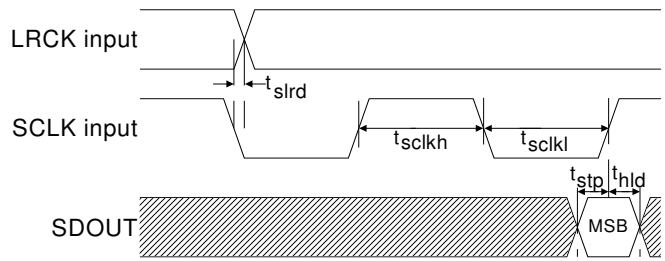
Figure 7. Slave Mode, I²S SAI
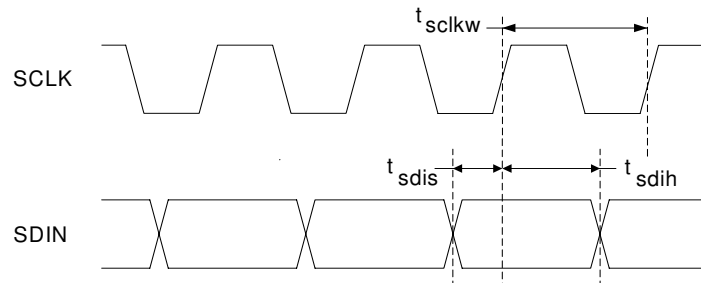
Figure 8. Master and Slave Mode SDIN vrs. SCLK
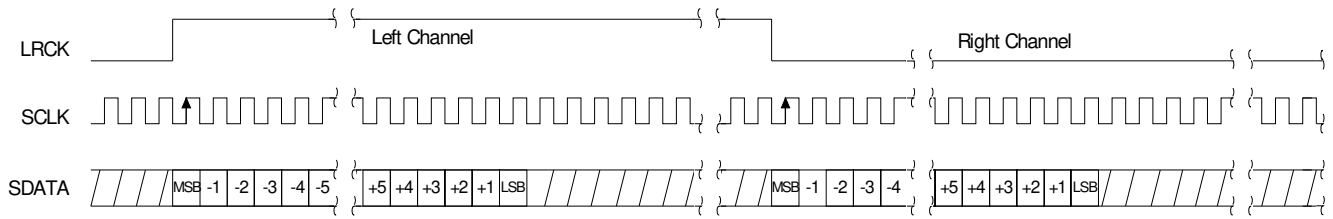
Figure 9. Format 0, Left-Justified up to 24-Bit Data
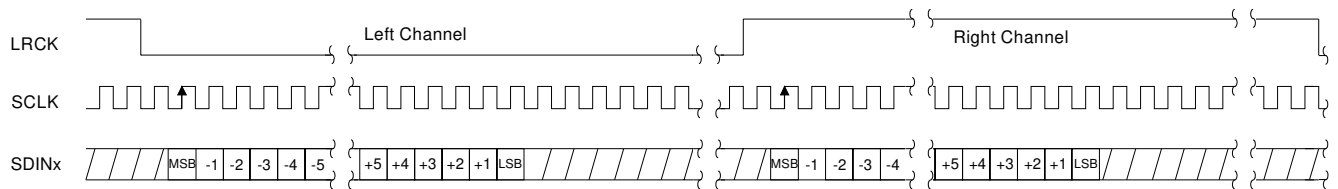
Figure 10. Format 1, I²S up to 24-Bit Data
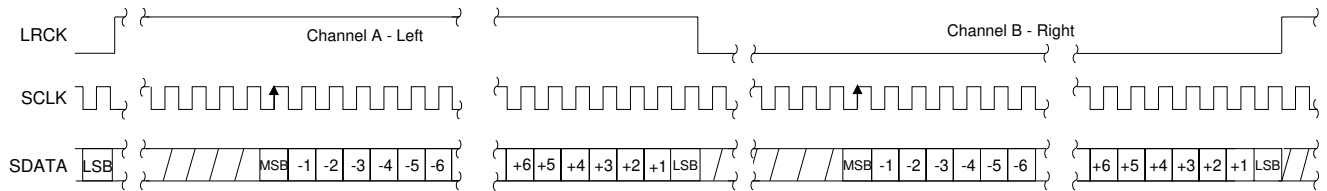
Figure 11. Format 2, Right-Justified 16-Bit Data. (Available in Control Port Mode only)
Format 3, Right-Justified 24-Bit Data. (Available in Control Port Mode only)

SWITCHING CHARACTERISTICS - I²C MODE CONTROL PORT

(Inputs: logic 0 = DGND, logic 1 = VLC)

Parameter	Symbol	Min	Max	Unit
I²C Mode				
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 19)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	1	µs
Fall Time of Both SDA and SCL Lines	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

19. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
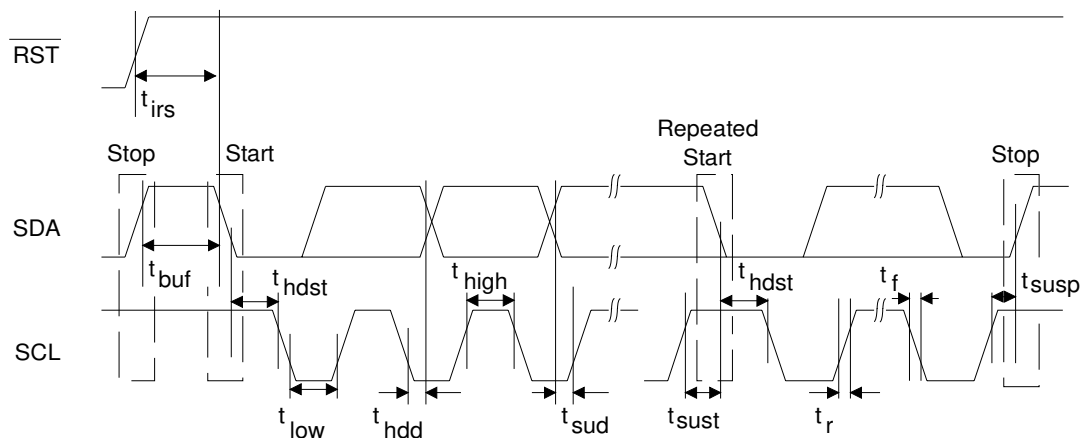
Figure 12. I²C Mode Control Port Timing

SWITCHING CHARACTERISTICS - SPI^{TM} CONTROL PORT

(Inputs: logic 0 = DGND, logic 1 = VLC)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency		f_{sclk}	-	6	MHz
RST Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to CS Falling	(Note 20)	t_{spi}	500	-	ns
CS High Time Between Transmissions		t_{csh}	1.0	-	µs
CS Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	82	-	ns
CCLK High Time		t_{sch}	82	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 21)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 22)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 22)	t_{f2}	-	100	ns

20. t_{spi} only needed before first falling edge of CS after RST rising edge. t_{spi} = 0 at all other times.

21. Data must be held for sufficient time to bridge the transition time of CCLK.
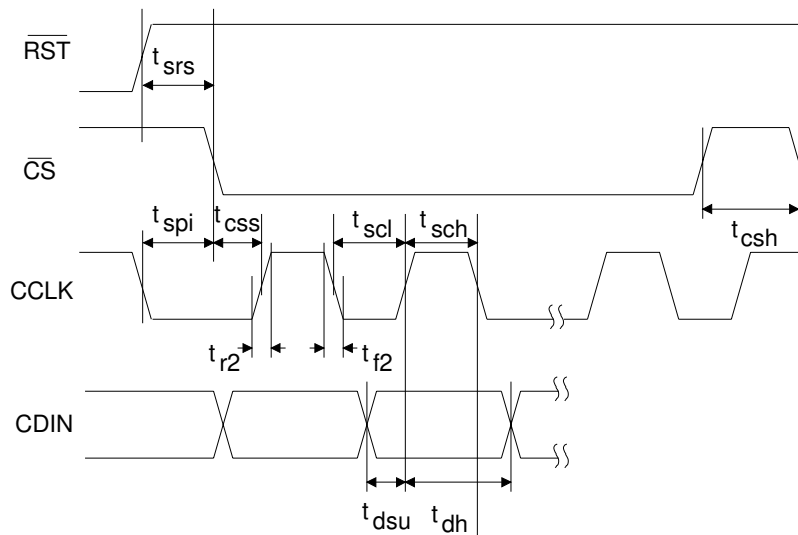
22. For F_{SCK} < 1 MHz

Figure 13. SPI Control Port Timing

5. APPLICATIONS

5.1 Stand-Alone Mode

5.1.1 Recommended Power-Up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

5.1.2 Master/Slave Mode

The CS4270 supports operation in either Master Mode or Slave Mode.

In Master Mode, LRCK and SCLK are outputs and are synchronously generated on-chip. LRCK is equal to Fs and SCLK is equal to 64x Fs.

In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. It is recommended that SCLK be 48x or 64x Fs to maximize system performance.

In Stand-Alone Mode, the CS4270 will enter Slave Mode when SDOUT (M/$\overline{\text{S}}$) is pulled low through a 47 kΩ resistor. Master Mode may be accessed by placing a 47 kΩ pull-up to VD on the SDOUT (M/$\overline{\text{S}}$) pin.

Configuration of clock ratios in each of these modes is outlined in Table 2.

5.1.3 System Clocking

The CS4270 will operate at sampling frequencies from 4 kHz to 216 kHz. This range is divided into three speed modes as shown in Table 1

.

Mode	Sampling Frequency
Single-Speed	4-54 kHz
Double-Speed	50-108 kHz
Quad-Speed	100-216 kHz

Table 1. Speed Modes

5.1.4 Clock Ratio Selection

Depending on whether the CS4270 is in Master or Slave Mode, different MCLK/LRCK and SCLK/LRCK ratios may be used. These ratios are shown in the Table 2.

Master Mode					
	MCLK/LRCK	SCLK/LRCK	LRCK	MDIV2	MDIV1
Single-Speed	256	64	Fs	0	0
	384	64	Fs	0	1
	512	64	Fs	1	0
	1024	64	Fs	1	1
Double-Speed	128	64	Fs	0	0
	192	64	Fs	0	1
	256	64	Fs	1	0
	512	64	Fs	1	1
Quad-Speed	64	64	Fs	0	0
	96	64	Fs	0	1
	128	64	Fs	1	0
	256	64	Fs	1	1
Slave Mode					
	MCLK/LRCK	SCLK/LRCK	LRCK	MDIV2	MDIV1
Single-Speed	256	32, 48, 64, 128	Fs	0	0
	384	32, 48, 64, 96	Fs	0	1
	512	32, 48, 64, 128	Fs	1	0
	1024	32, 48, 64, 96	Fs	1	1
Double-Speed	128	32, 48, 64	Fs	0	0
	192	32, 48, 64	Fs	0	1
	256	32, 48, 64	Fs	1	0
	512	32, 48, 64	Fs	1	1
Quad-Speed	64	32, 48, 64	Fs	0	0
	96	32, 48, 64	Fs	0	1
	128	32, 48, 64	Fs	1	0
	256	32, 48, 64	Fs	1	1

Table 2. Clock Ratios - Stand-Alone Mode

5.1.5 Interpolation Filter

In Stand-Alone Mode, the fast roll-off interpolation filter is used. Filter specifications can be found in Section 4. Plots of the data are contained in Section 9. "Filter Plots" on page 41.

5.1.6 High-Pass Filter

The operational amplifiers in the input circuitry driving the CS4270 may generate a small DC offset into the ADC. The CS4270 includes a high-pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system. In Stand-Alone Mode, the high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter This function cannot be disabled in Stand-Alone Mode.

5.1.7 Mode Selection & De-Emphasis

The sample rate, Fs, can be adjusted from 4 kHz to 216 kHz and De-emphasis, optimized for 44.1 kHz, is available in Single-Speed Mode. In Stand-Alone Master Mode, the CS4270 must be set to the proper mode via the mode pins, M1 and M0. In Slave Mode, the CS4270 auto-detects Speed Mode and the M0 pin becomes De-emphasis select. Stand-alone definitions of the mode pins are shown in Table 3.

Mode 1	Mode 0	Mode	Sample Rate (Fs)	De-Emphasis
0	0	Single-Speed Mode	4 kHz - 54 kHz	Off
0	1	Single-Speed Mode	4 kHz - 54 kHz	44.1 kHz
1	0	Double-Speed Mode	50 kHz - 108 kHz	Off
1	1	Quad-Speed Mode	100 kHz - 216 kHz	Off

Table 3. CS4270 Stand-Alone Mode Control

5.1.8 Serial Audio Interface Format Selection

Either I²S or Left-Justified serial audio data format may be selected in Stand-Alone Mode. The selection will affect both the input and output format. Placing a 10 kΩ pull-up to VD on the I²S/$\overline{\text{LJ}}$ pin will select the I²S format, while placing a 10 kΩ pull-down to DGND on the I²S/$\overline{\text{LJ}}$ pin will select the Left-Justified format.

5.2 Control Port Mode

5.2.1 Recommended Power-Up Sequence - Access to Control Port Mode

1. Pull $\overline{\text{RST}}$ low until the power supply, MCLK, and LRCK are stable.

2. Release $\overline{\text{RST}}$. The Control Port will be accessible.

3. Set the power down bit (register 0x02h, bit 0) to "1" for 1 ms minimum within 10 ms after releasing $\overline{\text{RST}}$ and then set to "0" prior to reading or writing to other registers.

4. Initiate a SPI or I²C transaction as described in Section 6.1 or Section 6.2, respectively.

5.2.2 Master / Slave Mode Selection

The CS4270 supports operation in either Master Mode or Slave Mode.

In Master Mode, LRCK and SCLK are outputs and are synchronously generated on-chip. LRCK is equal to Fs and SCLK is equal to 64x Fs.

In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. It is recommended that SCLK be 48x or 64x Fs to maximize system performance.

Configuration of clock ratios in each of these modes will be outlined in the Table 10 and Table 9.

In Control Port Mode the CS4270 will default to Slave Mode. The user may change this default setting by changing the status of the M/$\overline{\text{S}}$ bits in the Functional Control Register (03h).

5.2.3 System Clocking

The CS4270 will operate at sampling frequencies from 4 kHz to 216 kHz. This range is divided into three speed modes as shown in Table 4.

Mode	Sampling Frequency
Single-Speed	4-54 kHz
Double-Speed	50-108 kHz
Quad-Speed	100-216 kHz

Table 4. Speed Modes

5.2.4 Clock Ratio Selection

In Control Port Master Mode, the user must configure the mode bits (MCLK Freq<2:0>) to set the speed mode and select the appropriate clock ratios. Depending on whether the CS4270 is in Master or Slave Mode, different MCLK/LRCK and SCLK/LRCK ratios may be used. These ratios as well as the Control Port Register Bits are shown in Table 5, Table 9 and Section 8.3 on page 36.

Master Mode						
	MCLK/LRCK	SCLK/LRCK	LRCK	MCLK Freq<2>	MCLK Freq<1>	MCLK Freq<0>
Single-Speed	256	64	Fs	0	0	0
	384	64	Fs	0	0	1
	512	64	Fs	0	1	0
	768	64	Fs	0	1	1
	1024	64	Fs	1	0	0
Double-Speed	128	64	Fs	0	0	0
	192	64	Fs	0	0	1
	256	64	Fs	0	1	0
	384	64	Fs	0	1	1
	512	64	Fs	1	0	0
Quad-Speed	64	64	Fs	0	0	0
	96	64	Fs	0	0	1
	128	64	Fs	0	1	0
	192	64	Fs	0	1	1
	256	64	Fs	1	0	0
Slave Mode						
	MCLK/LRCK	SCLK/LRCK	LRCK	MCLK Freq<2>	MCLK Freq<1>	MCLK Freq<0>
Single-Speed	256	32, 64, 128	Fs	0	0	0
	384	32, 48, 64, 96, 128	Fs	0	0	1
	512	32, 64, 128	Fs	0	1	0
	768	32, 48, 64, 96, 128	Fs	0	1	1
	1024	32, 64, 128	Fs	1	0	0

Table 5. Clock Ratios - Control Port Mode