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CIRRUS LOGIC®

CS4271

24-Bit, 192 kHz Stereo Audio CODEC

D/A Features

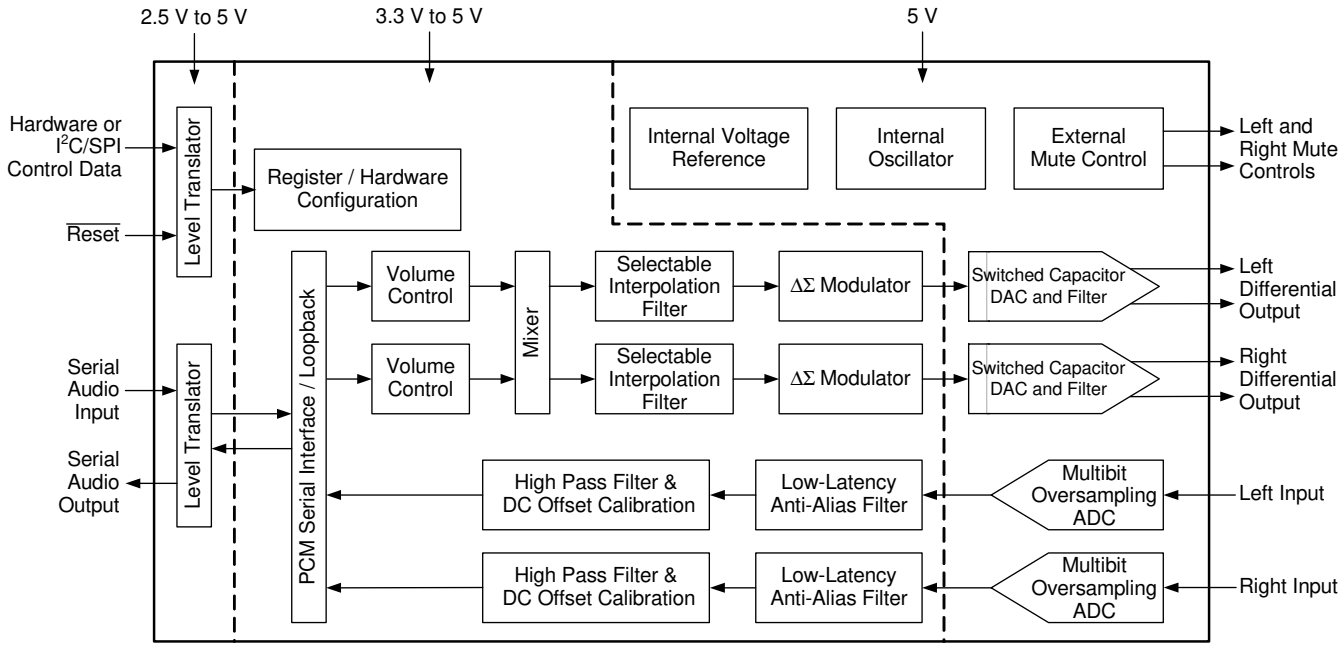
- High Performance
  - 114 dB Dynamic Range
  - -100 dB THD+N
- Up to 192 kHz Sampling Rates
- Differential Analog Architecture
- Volume Control with Soft Ramp
  - 1 dB Step Size
  - Zero Crossing Click-free Transitions
- Selectable Digital Filters
  - Fast and Slow Roll Off
- ATAPI Mixing Functions
- Selectable Serial Audio Interface Formats
  - Left Justified up to 24-bit
  - I^2S up to 24-bit
  - Right Justified 16-, 18-, 20-, and 24-Bit
- Control Output for External Muting
- Selectable 50/15 µs De-emphasis

A/D Features

- High Performance
  - 108 dB Dynamic Range
  - -98 dB THD+N
- Up to 192 kHz Sampling Rates
- Single-Ended Analog Architecture
- Multi-bit Delta Sigma Conversion
- High-pass Filter or DC Offset Calibration
- Low-Latency Digital Anti-alias Filtering
- Automatic Dithering of 16-bit Data
- Selectable Serial Audio Interface Formats
  - Left Justified up to 24-bit
  - I^2S up to 24-bit

System Features

- Direct Interface with 5V to 2.5V Logic Levels
- Internal Digital Loopback
- On-chip Oscillator
- Stand-Alone or Control Port Functionality



Stand-Alone Mode Feature Set

- System Features
  - Serial Audio Port Master or Slave Operation
  - Internal Oscillator for Master Clock
- D/A Features
  - Auto-mute on Static Samples
  - 44.1 kHz 50/15 µs De-emphasis Available
  - Selectable Serial Audio Interface Formats
    - Left Justified up to 24-bit
    - I^2S up to 24-bit
- A/D Features
  - Automatic Dithering for 16-bit Data
  - High-pass Filter
  - Selectable Serial Audio Interface Formats
    - Left Justified up to 24-bit
    - I^2S up to 24-bit

Software Mode Feature Set

- System Features
  - Serial Audio Port Master or Slave Operation
  - Internal Oscillator for Master Clock
  - Internal Digital Loopback Available
- D/A Features
  - Selectable Auto-mute
  - Selectable Interpolation Filters
  - Selectable 32-, 44.1-, and 48-kHz De-emphasis Filters
  - Configurable ATAPI Mixing Functions
  - Configurable Volume and Muting Controls
  - Selectable Serial Audio Interface Formats
    - Left Justified up to 24-bit
    - I^2S up to 24-bit
    - Right Justified 16, 18, 20, and 24-bit
- A/D Features
  - Selectable Dithering for 16-bit Data
  - Selectable High-pass Filter or DC Offset Calibration
  - Selectable Serial Audio Interface Formats
    - Left Justified up to 24-bit
    - I^2S up to 24-bit

General Description

The CS4271 is a high-performance, integrated audio CODEC. The CS4271 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 192 kHz.

The D/A offers a volume control that operates with a 1 dB step size. It incorporates selectable soft ramp and zero crossing transition functions to eliminate clicks and pops.

The D/A's integrated digital mixing functions allow a variety of output configurations ranging from a channel swap to a stereo-to-mono downmix.

Standard 50/15 µs de-emphasis is available for sampling rates of 32, 44.1, and 48 kHz for compatibility with digital audio programs mastered using the 50/15 µs pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4271 and other devices operating over a wide range of logic levels.

An on-chip oscillator eliminates the need for an external crystal oscillator circuit. This can reduce overall design cost and conserve circuit board space. The CS4271 automatically uses the on-chip oscillator in the absence of an applied master clock, making this feature easy to use.

Independently addressable high-pass filters are available for the right and left channel of the A/D. This allows the A/D to be used in a wide variety of applications where one audio channel and one DC measurement channel is desired.

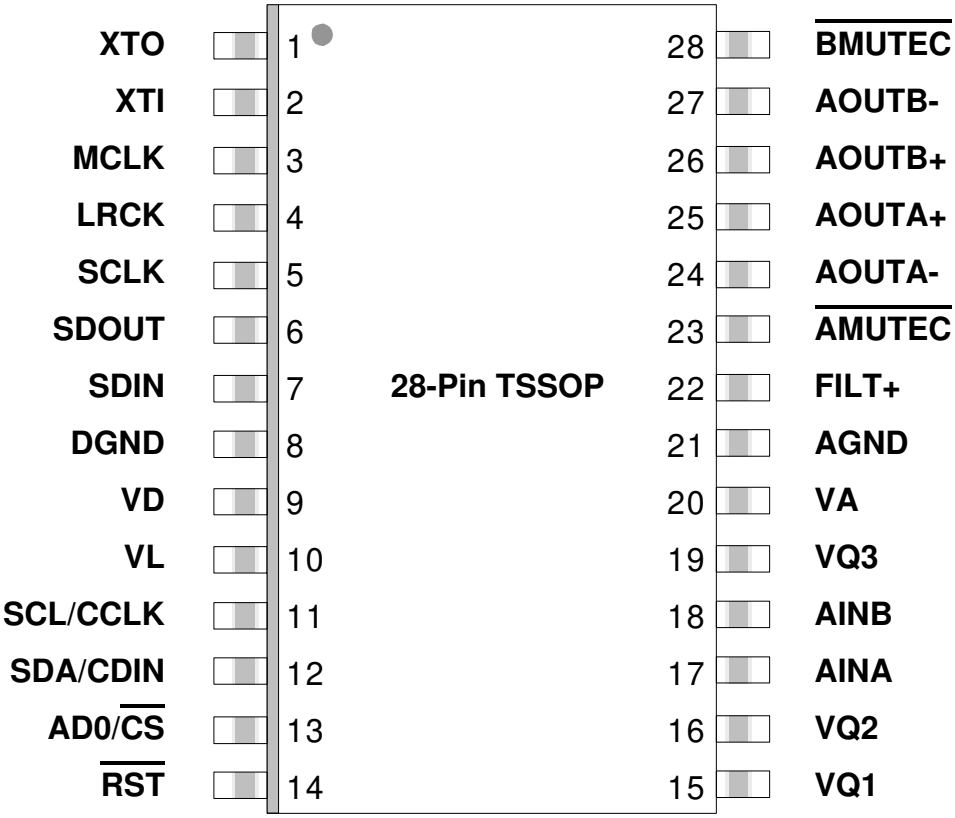
The CS4271's wide dynamic range, negligible distortion, and low noise make it ideal for applications such as A/V receivers, DVD-R, CD-R, digital mixing consoles, effects processors, set-top box systems, and automotive audio systems.

Ordering Information

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4271	24-Bit, 192 kHz Stereo Audio CODEC	28-pin TSSOP	YES	Commercial	-10° to +70° C	Tube	CS4271-CZZ
						Tape & Reel	CS4271-CZZR
				Automotive	-40° to +85° C	Tube	CS4271-DZZ
						Tape & Reel	CS4271-DZZR
CDB4271	CS4271 Evaluation Board		No	-	-	-	CDB4271

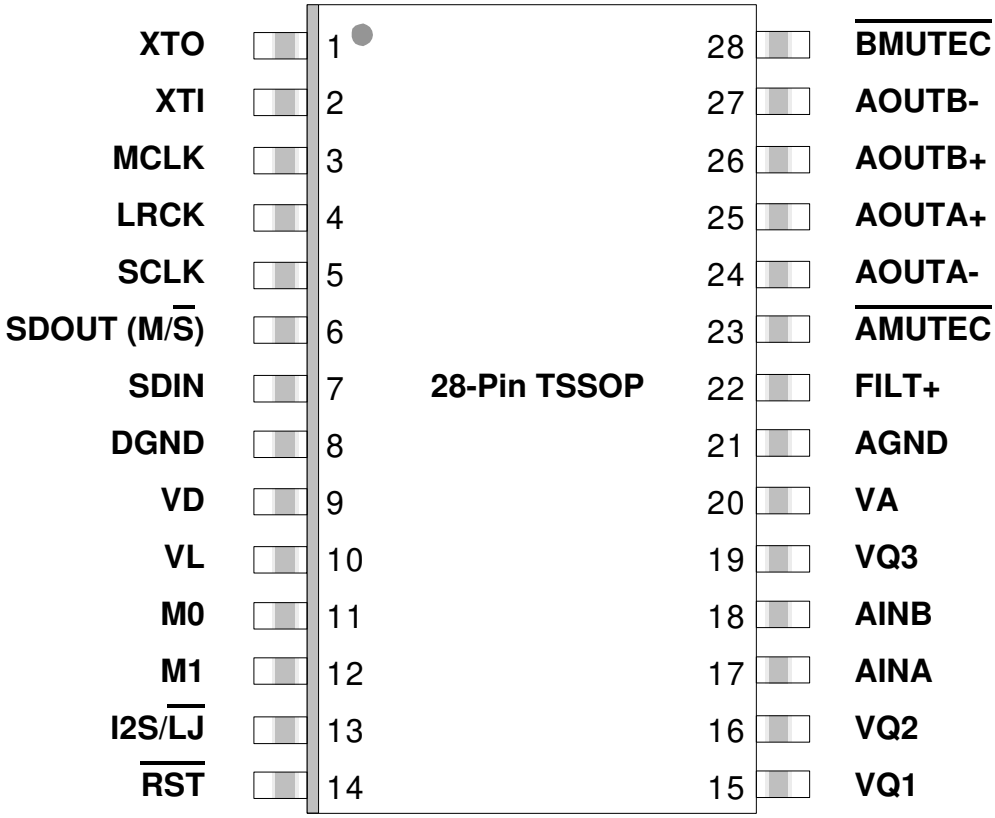
TABLE OF CONTENTS

1. PIN DESCRIPTIONS - SOFTWARE MODE



Pin Name	#	Pin Description
XTO **XTI**	1,2	**Crystal Connections** (*Input/Output*) - I/O pins for an external crystal which may be used to generate MCLK. See "Crystal Applications (XTI/XTO)" on page 24 or "Crystal Applications (XTI/XTO)" on page 27.
MCLK	3	**Master Clock** (*Input/Output*) -Clock source for the delta-sigma modulators. See "Crystal Applications (XTI/XTO)" on page 24 or "Crystal Applications (XTI/XTO)" on page 27.
LRCK	4	**Left Right Clock** *(Input/Output)* **-** Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	5	**Serial Clock** *(Input/Output)* **-** Serial clock for the serial audio interface.
SDOUT	6	**Serial Audio Data Output** (*Output*) **-** Output for two's complement serial audio data.
SDIN	7	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
DGND	8	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VD	9	**Digital Power** (*Input*) **-** Positive power for the internal digital section.
VL	10	**Logic Power** (*Input*) - Positive power for the digital input/output interface.
SCL/CCLK	11	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
SDA/CDIN	12	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C mode. CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{\text{CS}}$	13	**Address Bit 0 (I²C)** / **Control Port Chip Select (SPI)** *(Input)* - AD0 is a chip address pin in I²C mode; $\overline{\text{CS}}$ is the chip select signal for SPI format.
$\overline{\text{RST}}$	14	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VQ1	15	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
VQ2	16	**Quiescent Voltage** (*Input*) **-** Connection for internal quiescent reference voltage.
AINA **AINB**	17, 18	**Analog Input** (*Input*) **-** The full scale input level is specified in the ADC Analog Characteristics specification table.
VQ3	19	**Quiescent Voltage** (*Input*) **-** Connection for internal quiescent reference voltage.
VA	20	**Analog Power** *(Input)* **-** Positive power for the internal analog section.
AGND	21	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
FILT+	22	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
$\overline{\text{AMUTEC}}$	23	**Channel A Mute Control** *(Output)* **-** This pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
AOUTA- **AOUTA+** **AOUTB+** **AOUTB-**	24, 25, 26, 27	**Differential Analog Audio Output** (*Output*) - The full scale differential output level is specified in the DAC Analog Characteristics specification table.
$\overline{\text{BMUTEC}}$	28	**Channel B Mute Control** *(Output)* **-** This pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.

2. PIN DESCRIPTIONS - STAND-ALONE MODE



Pin Name	#	Pin Description
XTO **XTI**	1,2	**Crystal Connections** (*Input/Output*) - I/O pins for an external crystal which may be used to generate the master clock. See "Crystal Applications (XTI/XTO)" on page 24 or "Crystal Applications (XTI/XTO)" on page 27.
MCLK	3	**Master Clock** (*Input/Output*) -Clock source for the delta-sigma modulators. See "Crystal Applications (XTI/XTO)" on page 24 or "Crystal Applications (XTI/XTO)" on page 27.
LRCK	4	**Left Right Clock** *(Input/Output)* **-** Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	5	**Serial Clock** *(Input/Output)* **-** Serial clock for the serial audio interface.
SDOUT **(M/S)**	6	**Serial Audio Data Output** (*Output*) **-** Output for two's complement serial audio data. This pin must be pulled-up or pulled-down to select Master or Slave Mode. See "Master/Slave Mode" on page 24.
SDIN	7	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
DGND	8	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VD	9	**Digital Power** (*Input*) **-** Positive power for the internal digital section.
VL	10	**Logic Power** (*Input*) - Positive power for the digital input/output interface.
M0	11	**Mode Select 0** (*Input*) - In conjunction with M1, selects operating mode. Functionality is described in the Hardware Mode Speed Configuration table.
M1	12	**Mode Select 1** (*Input*) - In conjunction with M0, selects operating mode. Functionality is described in the Hardware Mode Speed Configuration table.
I2S/$\overline{\text{LJ}}$	13	**Serial Audio Interface Select** *(Input)* - Selects either the left-justified or I^2S format for the Serial Audio Interface.
$\overline{\text{RST}}$	14	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VQ1	15	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
VQ2	16	**Quiescent Voltage** (*Input*) **-** Connection for internal quiescent reference voltage.
AINA **AINB**	17, 18	**Analog Input** (*Input*) **-** The full scale input level is specified in the ADC Analog Characteristics specification table.
VQ3	19	**Quiescent Voltage** (*Input*) **-** Connection for internal quiescent reference voltage.
VA	20	**Analog Power** *(Input)* **-** Positive power for the internal analog section.
AGND	21	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
FILT+	22	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
$\overline{\text{AMUTEC}}$	23	**Channel A Mute Control** *(Output)* **-** This pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
AOUTA- **AOUTA+** **AOUTB+** **AOUTB-**	24, 25, 26, 27	**Differential Analog Audio Output** (*Output*) - The full scale differential output level is specified in the Analog Characteristics specification table.
$\overline{\text{BMUTEC}}$	28	**Channel B Mute Control** *(Output)* **-** This pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.

3. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS (AGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Nom	Max	Units
DC Power Supplies: Positive Analog	VA	4.75	5.0	5.25	V
Positive Digital	VD	3.1	3.3	5.25	V
Positive Logic	VL	2.37	3.3	5.25	V
Ambient Operating Temperature (Power Applied)					
Commercial Grade	T_A	-10	-	+70	°C
Automotive Grade		-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS (GND = 0 V, All voltages with respect to ground.) (Note 1)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Analog	VA	-0.3	-	+6.0	V
Logic	VL	-0.3	-	+6.0	V
Digital	VD	-0.3	-	+6.0	V
Input Current (Note 2)	I_{in}	-	-	±10	mA
Analog Input Voltage	V_{IN}	GND-0.3	-	VA+0.3	V
Digital Input Voltage	V_{IND}	-0.3	-	VL+0.3	V
Ambient Operating Temperature (Power Applied)	T_A	-50	-	+95	°C
Storage Temperature	T_{stg}	-65	-	+150	°C

Notes: 1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

DAC ANALOG CHARACTERISTICS - COMMERCIAL GRADE (Notes 3 to 7)

Parameter			Symbol	Min	Typ	Max	Unit
Dynamic Performance							
Dynamic Range	24-Bits	A-Weighted		108	114	-	dB
		unweighted		105	111	-	dB
	16-Bits	unweighted		-	94	-	dB
Total Harmonic Distortion + Noise		0 dB	THD+N	-	-100	-94	dB
		-20 dB		-	-91	-	dB
		-60 dB		-	-51	-45	dB
Idle Channel Noise / Signal-to-Noise Ratio				-	114	-	dB
Interchannel Isolation		(1 kHz)		-	100	-	dB
DC Accuracy							
Interchannel Gain Mismatch			ICGM	-	0.1	-	dB
Gain Drift				-	100	-	ppm/°C
Analog Output Characteristics and Specifications							
Full Scale Differential Output Voltage			V_{FS}	0.91xVA	0.96xVA	1.01xVA	Vpp
Output Resistance		(note 7)	Z_{out}	-	100	-	Ω
Minimum AC-Load Resistance			R_L	-	3	-	kΩ
Maximum Load Capacitance			C_L	-	100	-	pF

Notes: 3. One-half LSB of Triangular PDF dither is added to data.

4. Performance measurements taken with a full-scale 997 Hz sine wave under Test load R_L = 3 kΩ, C_L = 10 pF

5. Measurement bandwidth is 10 Hz to 20 kHz.

6. Logic “0” = GND = 0V; Logic “1” = VL; VL = VA unless otherwise noted.

7. V_{FS} is tested under load R_L but does not include attenuation due to Z_{OUT}

DAC ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE (Notes 3 to 7)

Parameter			Symbol	Min	Typ	Max	Unit
Dynamic Performance							
Dynamic Range	24-Bits	A-Weighted		106	114	-	dB
		unweighted		103	111	-	dB
	16-Bits	unweighted		-	94	-	dB
Total Harmonic Distortion + Noise		0 dB	THD+N	-	-100	-92	dB
		-20 dB		-	-91	-	dB
		-60 dB		-	-51	-43	dB
Idle Channel Noise / Signal-to-Noise Ratio				-	114	-	dB
Interchannel Isolation		(1 kHz)		-	100	-	dB
DC Accuracy							
Interchannel Gain Mismatch			ICGM	-	0.1	-	dB
Gain Drift				-	100	-	ppm/°C
Analog Output Characteristics and Specifications							
Full Scale Differential Output Voltage			V_{FS}	0.91xVA	0.96xVA	1.01xVA	Vpp
Output Resistance		(note 7)	Z_{out}	-	100	-	Ω
Minimum AC-Load Resistance			R_L	-	3	-	kΩ
Maximum Load Capacitance			C_L	-	100	-	pF

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(Note 12)

Parameter		Fast Roll-Off Min	Fast Roll-Off Typ	Fast Roll-Off Max	Unit
Single Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.454	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
StopBand		.547	-	-	Fs
StopBand Attenuation	(Note 10)	90	-	-	dB
Group Delay		-	12/Fs	-	s
De-emphasis Error (Note 11)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
Double Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.430	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 10)	80	-	-	dB
Group Delay		-	4.6/Fs	-	s
Quad Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.105	Fs
	to -3 dB corner	0	-	.490	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.635	-	-	Fs
StopBand Attenuation	(Note 10)	90	-	-	dB
Group Delay		-	4.7/Fs	-	s

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(cont) (Note 12)

Parameter		Slow Roll-Off (Note 8) Min	Typ	Max	Unit
Single Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	0.417	Fs
	to -3 dB corner	0	-	0.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 10)	64	-	-	dB
Group Delay		-	6.5/Fs	-	s
De-emphasis Error (Note 11)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
Double Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.296	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.792	-	-	Fs
StopBand Attenuation	(Note 10)	70	-	-	dB
Group Delay		-	3.9/Fs	-	s
Quad Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.104	Fs
	to -3 dB corner	0	-	.481	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.868	-	-	Fs
StopBand Attenuation	(Note 10)	75	-	-	dB
Group Delay		-	4.2/Fs	-	s

Notes:
8. Slow Roll-Off interpolation filter is only available in control port mode.
9. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 21 to 44) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
10. Single and Double Speed Mode Measurement Bandwidth is from stopband to 3 Fs.
Quad Speed Mode Measurement Bandwidth is from stopband to 1.34 Fs.
11. De-emphasis is available only in Single Speed Mode; Only 44.1 kHz De-emphasis is available in Stand-Alone Mode.
12. Plots of this data are contained in the “Appendix” on page 47. See Figure 21 through Figure 44.

ADC ANALOG CHARACTERISTICS - COMMERCIAL GRADE

Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Input is 1 kHz sine wave.

Parameter		Symbol	Min	Typ	Max	Unit
Single Speed Mode	**Fs = 48 kHz**					
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
Total Harmonic Distortion + Noise	(Note 13)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
Double Speed Mode	**Fs = 96 kHz**					
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
40kHz bandwidth	unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 13)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
40kHz bandwidth	-1 dB		-	-95	-	dB
Quad Speed Mode	**Fs = 192 kHz**					
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
40kHz bandwidth	unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 13)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
40kHz bandwidth	-1 dB		-	-95	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
Interchannel Phase Deviation			-	0.0001	-	Degree
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error				-	±5	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		-	0	-	LSB
	HPF disabled		-	100	-	LSB
Analog Input Characteristics						
Full-scale Input Voltage			0.51xVA	0.565xVA	0.62xVA	Vpp
Input Impedance			18	-	-	kΩ

Notes: 13. Referred to the typical full-scale input voltage.

ADC ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE

Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Input is 1 kHz sine wave.)

Parameter		Symbol	Min	Typ	Max	Unit
Single Speed Mode	**Fs = 48 kHz**					
Dynamic Range	A-weighted		101	108	-	dB
	unweighted		98	105	-	dB
Total Harmonic Distortion + Noise	(Note 14)	THD+N				
	-1 dB		-	-98	-91	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
Double Speed Mode	**Fs = 96 kHz**					
Dynamic Range	A-weighted		101	108	-	dB
	unweighted		98	105	-	dB
40kHz bandwidth	unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 14)	THD+N				
	-1 dB		-	-98	-91	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
40kHz bandwidth	-1 dB		-	-95	-	dB
Quad Speed Mode	**Fs = 192 kHz**					
Dynamic Range	A-weighted		101	108	-	dB
	unweighted		98	105	-	dB
40kHz bandwidth	unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 14)	THD+N				
	-1 dB		-	-98	-91	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
40kHz bandwidth	-1 dB		-	-95	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
Interchannel Phase Deviation			-	0.0001	-	Degree
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error				-	±5	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		-	0	-	LSB
	HPF disabled		-	100	-	LSB
Analog Input Characteristics						
Full-scale Input Voltage			0.51xVA	0.565xVA	0.62xVA	Vpp
Input Impedance			18	-	-	kΩ

Notes: 14. Referred to the typical full-scale input voltage.

ADC DIGITAL FILTER CHARACTERISTICS (Note 17)

Parameter			Symbol	Min	Typ	Max	Unit
Single Speed Mode							
Passband	(-0.1 dB).	(Note 15)		0	-	0.47	Fs
Passband Ripple.				-	-	±0.035	dB
Stopband.		(Note 15)		0.58	-	-	Fs
Stopband Attenuation.				-95	-	-	dB
Group Delay.			t_{gd}	-	12/Fs	-	s
Double Speed Mode							
Passband	(-0.1 dB).	(Note 15)		0	-	0.45	Fs
Passband Ripple.				-	-	±0.035	dB
Stopband.		(Note 15)		0.68	-	-	Fs
Stopband Attenuation.				-92	-	-	dB
Group Delay.			t_{gd}	-	9/Fs	-	s
Quad Speed Mode							
Passband	(-0.1 dB).	(Note 15)		0	-	0.24	Fs
Passband Ripple.				-	-	±0.035	dB
Stopband.		(Note 15)		0.78	-	-	Fs
Stopband Attenuation.				-97	-	-	dB
Group Delay.			t_{gd}	-	5/Fs	-	s
High Pass Filter Characteristics							
Frequency Response	-3.0 dB.			-	1	-	Hz
	-0.13 dB.	(Note 16)			20	-	Hz
Phase Deviation	@ 20 Hz.	(Note 16)		-	10	-	Deg
Passband Ripple.				-	-	0	dB
Filter Settling Time.					10^5/Fs		s

Notes: 15. The filter frequency response scales precisely with Fs.

16. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

17. Plots of this data are contained in the “Appendix” on page 47. See Figure 45 through Figure 56.

DC ELECTRICAL CHARACTERISTICS

(GND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply						
Power Supply Current	VA	I_A	-	45	53	mA
(Normal Operation)	VL,VD = 5 V	I_D	-	41.5	49	mA
	VL,VD = 3.3 V	I_D	-	24	28	mA
Power Supply Current	VA	I_A	-	0.025	-	mA
(Power-Down Mode)(Note 18)	VL,VD=5 V	I_D	-	1.76	-	mA
Power Consumption	VL, VD=5 V	-	-	433	510	mW
(Normal Operation)	VL, VD = 3.3 V	-	-	305	358	mW
	(Power-Down Mode)	-	-	9	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 19)	PSRR	-	60	-	dB
Quiescent Voltage						
Nominal Quiescent Voltage		VQ	-	0.48xVA	-	VDC
Maximum DC Current Source/Sink from VQ			-	1	-	µA
VQ Output Impedance			-	25	-	kΩ
FILT+						
FILT+ Nominal Voltage		FILT+	-	VA	-	VDC
MUTEC						
MUTEC Low-Level Output Voltage			-	0	-	V
MUTEC High-Level Output Voltage			-	VA	-	V
Maximum MUTEC Drive Current			-	3	-	mA

Notes: 18. Power Down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

19. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VL)	V_{IL}	-	-	30%	V
High-Level Output Voltage at I_o = 2 mA		V_{OH}	VL - 1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA		V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	±10	µA

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT (Logic "0" = GND = 0 V; Logic "1" = VL, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rate	Single Speed Mode	Fs	4	-	50	kHz
	Double Speed Mode	Fs	50	-	100	kHz
	Quad Speed Mode	Fs	100	-	200	kHz
MCLK Specifications						
MCLK Frequency	Stand-Alone Mode	f_{mclk}	1.024	-	25.600	MHz
(note 20)	Control Port Mode	f_{mclk}	1.024	-	51.200	MHz
MCLK Input Pulse Width High/Low	Stand-Alone Mode	t_{clkhl}	16	-	-	ns
(note 20)	Control Port Mode	t_{clkhl}	8	-	-	ns
MCLK Output Duty Cycle			45	50	55	%
Master Mode						
LRCK Duty Cycle			-	50	-	%
SCLK Duty Cycle			-	50	-	%
SCLK falling to LRCK edge		t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid		t_{sdo}	0	-	32	ns
SDIN valid to SCLK rising setup time		t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time		t_{sdih}	20	-	-	ns
Slave Mode						
LRCK Duty Cycle			40	50	60	%
SCLK Period (note 20)	Single Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	s
	Double Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	s
	Quad Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	s
SCLK Pulse Width High		t_{sclkh}	30	-	-	ns
SCLK Pulse Width Low		t_{sclkl}	48	-	-	ns
SCLK falling to LRCK edge		t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid		t_{sdo}	0	-	32	ns
SDIN valid to SCLK rising setup time		t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time		t_{sdih}	20	-	-	ns
Crystal Oscillator Specifications (XTI/XTO)						
Crystal Frequency Range		f_{osc}	16.384	-	25.600	MHz

Notes: 20. In Control Port Mode, the Ratio[1:0] bits must be configured according to tables 8 and 9 on pages 28 and 29.

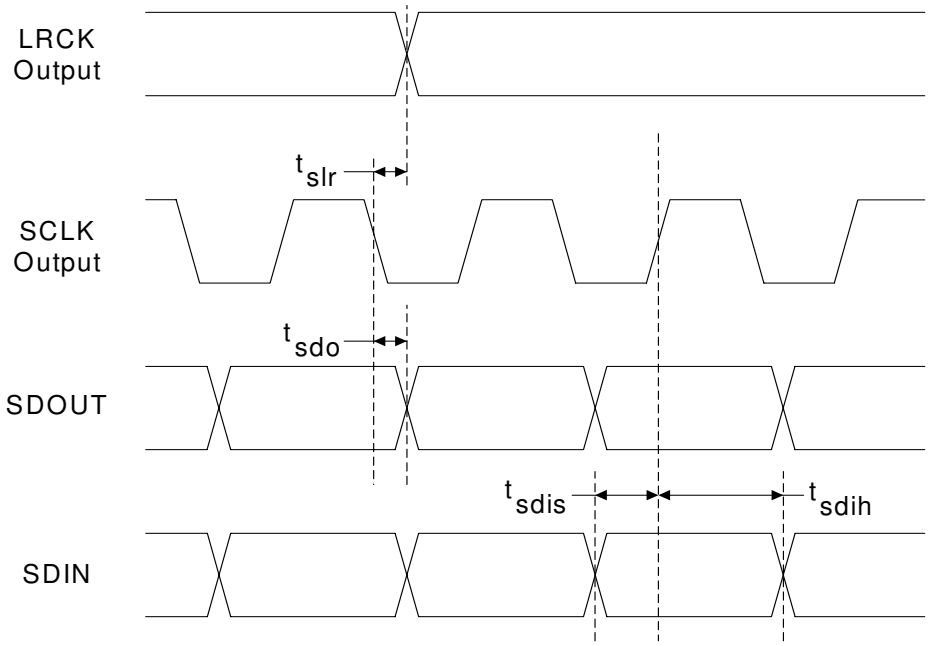


Figure 1. Master Mode Serial Audio Port Timing

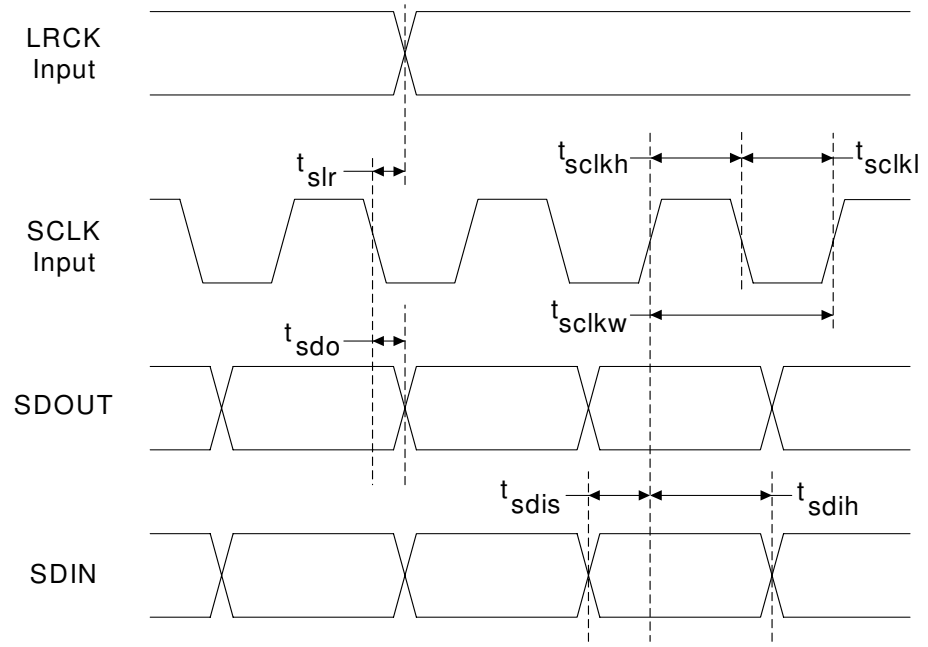


Figure 2. Slave Mode Serial Audio Port Timing

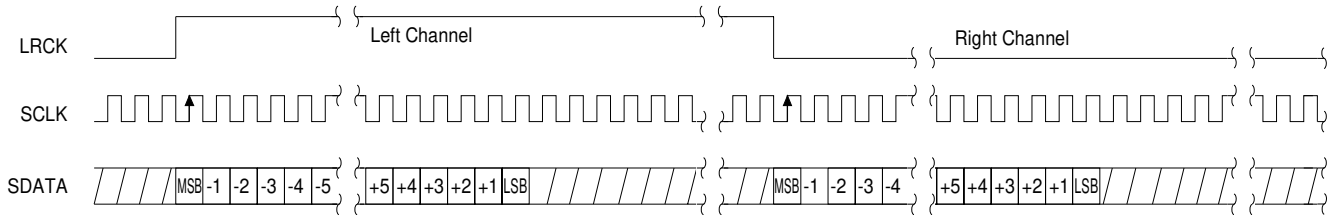


Figure 3. Format 0, Left Justified up to 24-Bit Data

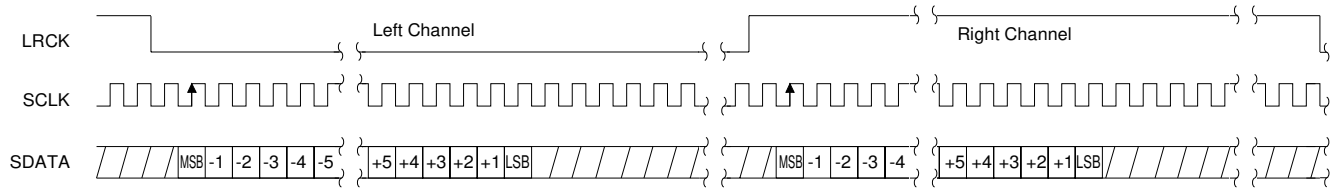


Figure 4. Format 1, I²S up to 24-Bit Data

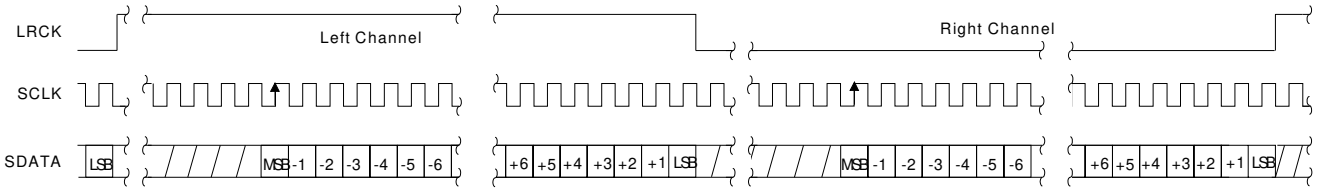


Figure 5. Format 2, Right Justified 16-Bit Data. (Available in Control Port Mode only)
Format 3, Right Justified 24-Bit Data. (Available in Control Port Mode only)
Format 4, Right Justified 20-Bit Data. (Available in Control Port Mode only)
Format 5, Right Justified 18-Bit Data. (Available in Control Port Mode only)

SWITCHING CHARACTERISTICS - I²C MODE CONTROL PORT

(Inputs: logic 0 = AGND, logic 1 = VL)

Parameter	Symbol	Min	Max	Unit
I²C Mode				
SCL Clock Frequency.	f_{scl}	-	100	KHz
$\overline{RST}$ Rising Edge to Start.	t_{irs}	500	-	ns
Bus Free Time Between Transmissions.	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse).	t_{hdst}	4.0	-	µs
Clock Low time.	t_{low}	4.7	-	µs
Clock High Time.	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition.	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling. (Note 21)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising.	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines.	t_r	-	1	µs
Fall Time of Both SDA and SCL Lines.	t_f	-	300	ns
Setup Time for Stop Condition.	t_{susp}	4.7	-	µs

Notes: 21. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

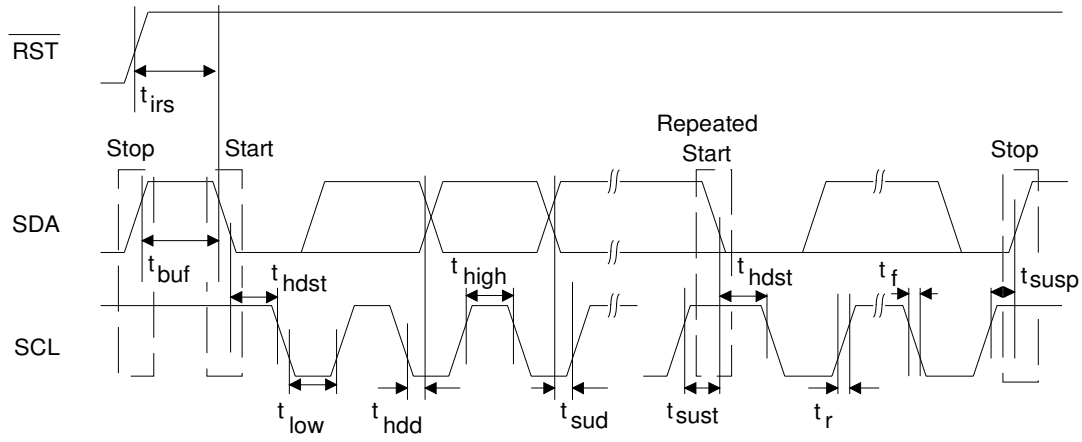


Figure 6. I²C Mode Control Port Timing

SWITCHING CHARACTERISTICS - SPI CONTROL PORT

(Inputs: logic 0 = AGND, logic 1 = VL)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency.		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to CS Falling.		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling.	(Note 22)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions.		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge.		t_{css}	20	-	ns
CCLK Low Time.		t_{scl}	82	-	ns
CCLK High Time.		t_{sch}	82	-	ns
CDIN to CCLK Rising Setup Time.		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time.	(Note 23)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN.	(Note 24)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN.	(Note 24)	t_{f2}	-	100	ns

Notes: 22. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

23. Data must be held for sufficient time to bridge the transition time of CCLK.

24. For F_{SCK} < 1 MHz

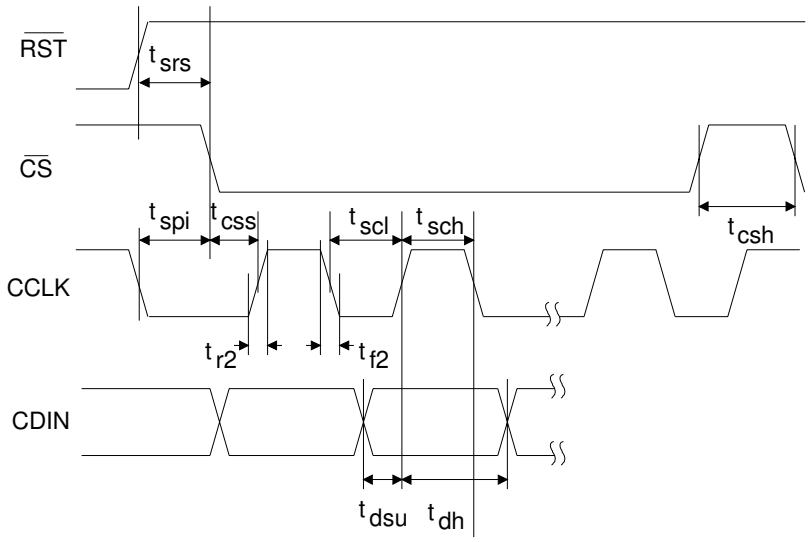


Figure 7. SPI Control Port Timing

4. TYPICAL CONNECTION DIAGRAM

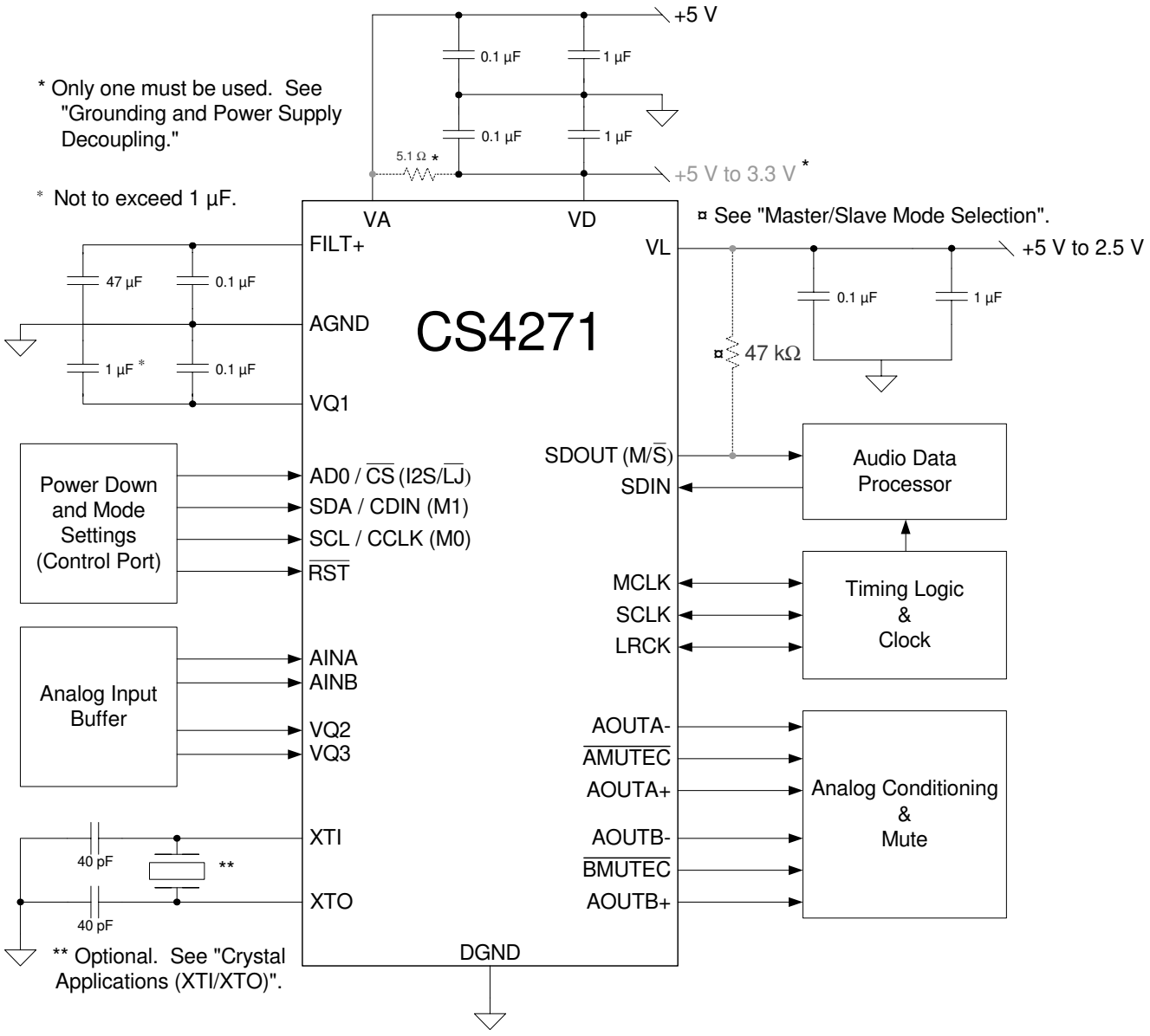


Figure 8. CS4271 Typical Connection Diagram

5. APPLICATIONS

5.1 Stand-Alone Mode

5.1.1 Recommended Power-Up Sequence

1) When using the CS4271 with an external MCLK, hold $\overline{\text{RST}}$ low until the power supply, MCLK, and LRCK are stable. When using the CS4271 with internally generated MCLK, hold $\overline{\text{RST}}$ low until the power supply is stable.
2) Bring $\overline{\text{RST}}$ high. If the internally generated MCLK is being used, it will appear on the MCLK pin prior to 1 ms from the release of $\overline{\text{RST}}$.

5.1.2 Master/Slave Mode

The CS4271 supports operation in either Master Mode or Slave Mode.

In Master Mode, LRCK and SCLK are outputs and are synchronously generated on-chip. LRCK is equal to Fs and SCLK is equal to 64x Fs.

In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. It is recommended that SCLK be 64x Fs to maximize system performance.

In Stand-Alone Mode, the CS4271 will default to Slave Mode. Master Mode may be accessed by placing a 47 kΩ pull-up to VL on the SDOUT (M/$\overline{\text{S}}$) pin.

Configuration of clock ratios in each of these modes will be outlined in the Tables 3 and 4.

5.1.3 System Clocking

The CS4271 will operate at sampling frequencies from 4 kHz to 200 kHz. This range is divided into three speed modes as shown in Table 1 below.

Table 1. Speed Modes

Mode	Sampling Frequency
Single Speed	4-50 kHz
Double Speed	50-100 kHz
Quad Speed	100-200 kHz

5.1.3.1 Crystal Applications (XTI/XTO)

An external crystal may be used in conjunction with the CS4271 to generate the master clock signal. To accomplish this, a 20 pF fundamental mode parallel resonant crystal must be connected between the XTI and XTO pins as shown in the Typical Connection Diagram on page 23. This crystal must oscillate at the frequency shown in Table 2. In this configuration, MCLK is a buffered output and, as shown in the Typical Connection Diagram, nothing other than the crystal and its load capacitors should be connected to XTI and XTO. The MCLK signal will appear on the MCLK pin prior to 1 ms from the release of $\overline{\text{RST}}$.

Table 2. Crystal Frequencies

Mode	Crystal Frequency
Single Speed	512 x Fs
Double Speed	256 x Fs
Quad Speed	128 x Fs

To operate the CS4271 with an externally generated MCLK signal, no crystal should be used, XTI should be connected to ground and XTO should be left unconnected. In this configuration, MCLK is an input and must be driven externally with an appropriate speed clock.

5.1.3.2 Clock Ratio Selection

Depending on the use of an external crystal, or whether the CS4271 is in Master or Slave Mode, different MCKL/LRCK and SCLK/LRCK ratios may be used. These ratios are shown in the Tables 3 and 4 below.

Table 3. Clock Ratios - Stand Alone Mode With External Crystal

External Crystal Used, MCLK=Output			
Master Mode			
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**
Single Speed	256	64	Fs
Double Speed	128	64	Fs
Quad Speed	128	64	Fs
Slave Mode			
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**
Single Speed	256	32, 64, 128	Fs
Double Speed	128	32, 64	Fs
Quad Speed	128	32, 64	Fs

Table 4. Clock Ratios - Stand Alone Mode Without External Crystal

External Crystal Not Used, MCLK=Input			
Master Mode			
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**
Single Speed	256	64	Fs
Double Speed	128	64	Fs
Quad Speed	64	32	Fs
Slave Mode			
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**
Single Speed	256	32, 64, 128	Fs
	384	32, 48, 64, 96, 128	Fs
	512	32, 64, 128	Fs
Double Speed	128	32, 64	Fs
	192	32, 48, 64	Fs
	256	32, 64	Fs
Quad Speed	64	32	Fs
	96	48	Fs
	128	32, 64	Fs