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CS42888

108 dB, 192 kHz 4-In, 8-Out CODEC

FEATURES

- Four 24-bit A/D, Eight 24-bit D/A Converters
- ADC Dynamic Range
  - 105 dB Differential
  - 102 dB Single-Ended
- DAC Dynamic Range
  - 108 dB Differential
  - 105 dB Single-Ended
- ADC/DAC THD+N
  - -98 dB Differential
  - -95 dB Single-Ended
- Compatible with Industry-Standard Time Division Multiplexed (TDM) Serial Interface
- System Sampling Rates up to 192 kHz
- Programmable ADC High-Pass Filter for DC Offset Calibration
- Logarithmic Digital Volume Control
- I²C™ & SPI™ Host Control Port
- Supports Logic Levels Between 5 V and 1.8 V
- Popguard® Technology

GENERAL DESCRIPTION

The CS42888 CODEC provides four multi-bit analog-to-digital and eight multi-bit digital-to-analog delta-sigma converters. The CODEC is capable of operation with either differential or single-ended inputs and outputs, in a 64-pin LQFP package.

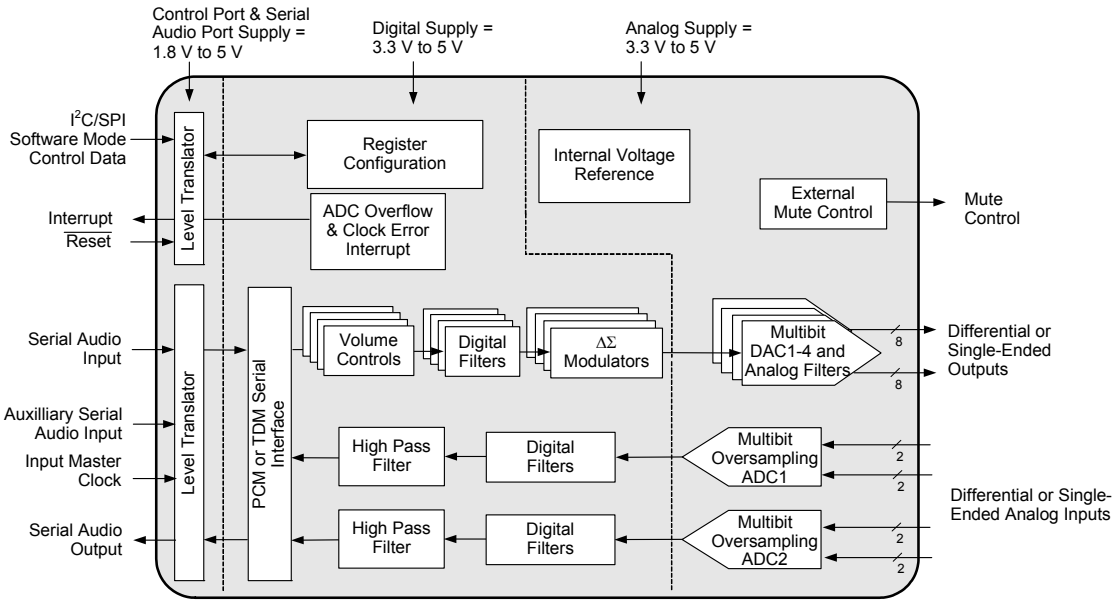
Four fully differential, or single-ended, inputs are available on stereo ADC1and ADC2. Digital volume control is provided for each ADC channel, with selectable overflow detection.

All eight DAC channels provide digital volume control and can operate with differential or single-ended outputs.

An auxiliary serial input is available for an additional two channels of PCM data.

The CS42888 is available in a 64-pin LQFP package in Commercial (-10°C to +70°C) and Automotive (-40°C to +105°C) grades. The CDB42448 Customer Demonstration Board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 62 for complete ordering information.

The CS42888 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, and automotive audio systems.



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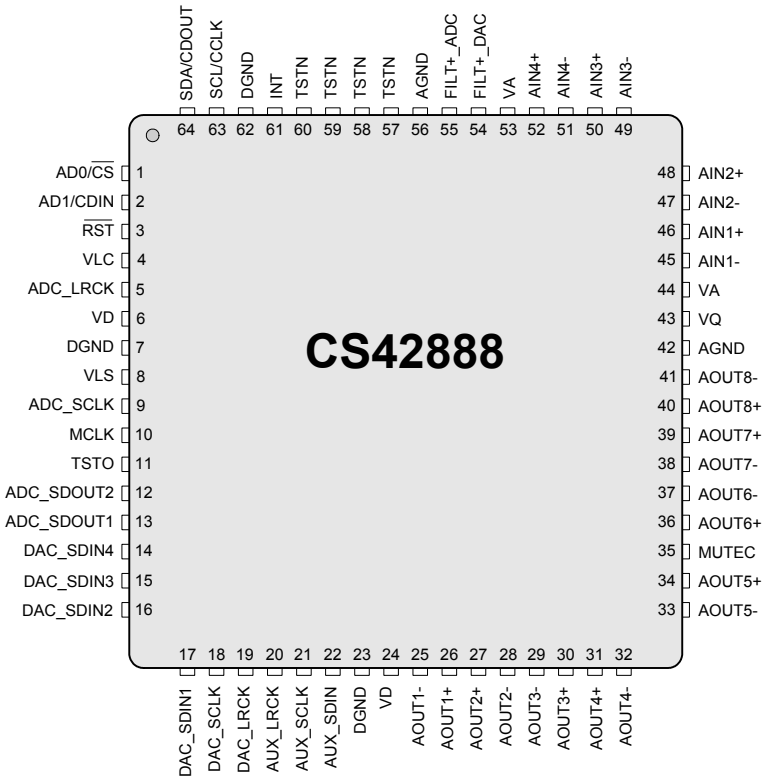
1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
AD0/$\overline{CS}$	1	**Address Bit [0]/ Chip Select** (*Input*) - Chip address bit in I²C Mode. Control signal used to select the chip in SPI Mode.
AD1/CDIN	2	**Address Bit [1]/ SPI Data Input** (*Input*) - Chip address bit in I²C Mode. Input for SPI data.
$\overline{RST}$	3	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
VLC	4	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port. See "Digital I/O Pin Characteristics" on page 8.
ADC_LRCK	5	**ADC Left/Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the ADC serial audio data line. Signals the start of a new TDM frame in the TDM digital interface format.
VD	6, 24	**Digital Power** (*Input*) - Positive terminal of the power supply for the digital section.
DGND	7, 23 62	**Digital Ground** (*Input*) - Ground terminal of the power supply for the digital section.
VLS	8	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial interfaces. See "Digital I/O Pin Characteristics" on page 8.
ADC_SCLK	9	**ADC Serial Clock** *(Input/Output)* - Serial clock for the ADC serial audio interface. Input frequency must be 256xFs in the TDM digital interface format.
MCLK	10	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators and digital filters.
TSTO	11	**Test Out** - This pin is an output used for test purposes only. This pin must be not be connected to any external trace or other connection.
ADC_SDOUT1 ADC_SDOUT2	13 12	**Serial Audio Data Output** *(Output)* - Outputs for two's complement serial audio data.

DAC_SDIN1 DAC_SDIN2 DAC_SDIN3 DAC_SDIN4	17 16 15 14	**DAC Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
DAC_SCLK	18	**DAC Serial Clock** *(Input/Output)* - Serial clock for the DAC serial audio interface. Input frequency must be 256xFs in the TDM digital interface format.
DAC_LRCK	19	**DAC Left/Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the DAC serial audio data line. Signals the start of a new TDM frame in the TDM digital interface format.
AUX_LRCK	20	**Auxiliary Left/Right Clock** (*Output*) - Determines which channel, Left or Right, is currently active on the Auxiliary serial audio data line. Derived from the ADC serial port and equals Fs.
AUX_SCLK	21	**Auxiliary Serial Clock** *(Output)* - Serial clock for the Auxiliary serial audio interface.
AUX_SDIN	22	**Auxiliary Serial Input** (*Input*) - Provides an additional serial input for two's complement serial audio data. Used only in the TDM digital interface format.
AOUT1 +,- AOUT2 +,- AOUT3 +,- AOUT4 +,- AOUT5 +,- AOUT6 +,- AOUT7 +,- AOUT8 +,-	26, 25 27, 28 30, 29 31, 32 34, 33 36, 37 39, 38 40, 41	**Differential Analog Output** (*Output*) - The full-scale analog output level is specified in the Analog Characteristics table. Each leg of the differential outputs may also be used single-ended.
MUTEC	35	**Mute Control** (*Output*) - Used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system.
AGND	42, 56	**Analog Ground** (*Input*) - Ground reference for the analog section.
VQ	43	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
VA	44, 53	**Analog Power** (*Input*) - Positive power supply for the analog section. See "Digital I/O Pin Characteristics" on page 8.
AIN1 +,- AIN2 +,- AIN3 +,- AIN4 +,-	46, 45 48, 47 50, 49 52, 51	**Differential Analog Input** (*Input*) - Signals are presented differentially or single-ended to the Delta-Sigma modulators. The full-scale input level is specified in the Analog Characteristics specification table.
FILT+_DAC	54	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits of the DAC.
FILT+_ADC	55	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits of the ADC.
TSTN	57, 58 59, 60	**Test In** - This pin is an input used for test purposes only. It must be tied to ground for normal operation.
INT	61	**Interrupt** (*Output*) - Signals either an ADC overflow condition has occurred in one or more of the ADC inputs, or a clocking error has occurred in the DAC/ADC as specified in the Interrupt register.
SCL/CCLK	63	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA/CDOUT	64	**Serial Control Data I/O** (*Input/Output*) - Input/Output for I²C data. Output for SPI data.

1.1 Digital I/O Pin Characteristics

Various pins on the CS42888 are powered from separate power supply rails. The logic level for each input should adhere to the corresponding power rail and should not exceed the maximum ratings.

Power Rail	Pin Name	I/O	Driver	Receiver
VLC	$\overline{\text{RST}}$	Input	-	1.8 V - 5.0 V, CMOS
	SCL/CCLK	Input	-	1.8 V - 5.0 V, CMOS, with Hysteresis
	SDA/CDOUT	Input/ Output	1.8 V - 5.0 V, CMOS/Open Drain	1.8 V - 5.0 V, CMOS, with Hysteresis
	AD0/$\overline{\text{CS}}$	Input	-	1.8 V - 5.0 V, CMOS
	AD1/CDIN	Input	-	1.8 V - 5.0 V, CMOS
	INT	Output	1.8 V - 5.0 V, CMOS/Open Drain	-
VLS	MCLK	Input	-	1.8 V - 5.0 V, CMOS
	ADC_LRCK	Input/ Output	1.8 V - 5.0 V, CMOS	1.8 V - 5.0 V, CMOS
	ADC_SCLK	Input/ Output	1.8 V - 5.0 V, CMOS	1.8 V - 5.0 V, CMOS
	ADC_SDOUT1-2	Input/ Output	1.8 V - 5.0 V, CMOS	-
	DAC_LRCK	Input/ Output	1.8 V - 5.0 V, CMOS	1.8 V - 5.0 V, CMOS
	DAC_SCLK	Input/ Output	1.8 V - 5.0 V, CMOS	1.8 V - 5.0 V, CMOS
	DAC_SDIN1-4	Input	-	1.8 V - 5.0 V, CMOS
	AUX_LRCK	Output	1.8 V - 5.0 V, CMOS	-
	AUX_SCLK	Output	1.8 V - 5.0 V, CMOS	-
	AUX_SDIN	Input	-	1.8 V - 5.0 V, CMOS
VA	MUTEC	Output	3.3 V - 5.0 V, CMOS	-

Table 1. I/O Power Rails

2. TYPICAL CONNECTION DIAGRAM

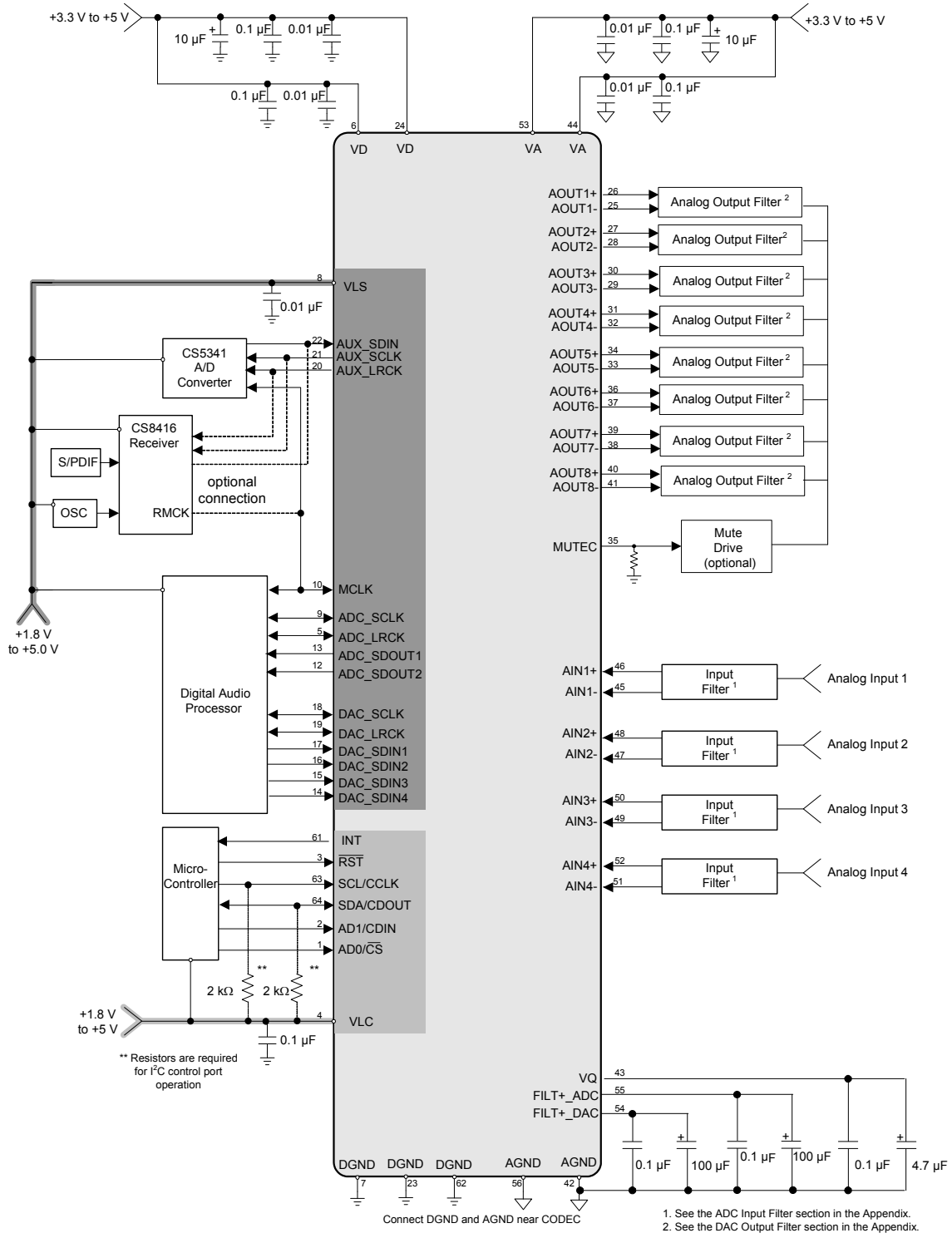


Figure 1. Typical Connection Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Analog	(Note 1)	VA	3.14	5.25	V
Digital		VD	3.14	5.25	V
Serial Audio Interface	(Note 2)	VLS	1.71	5.25	V
Control Port Interface		VLC	1.71	5.25	V
Ambient Temperature					
Commercial Automotive	-CQZ -DQZ	T_A	-10 -40	+70 +105	°C °C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	Serial Port Interface	VLS	-0.3	6.0	V
	Control Port Interface	VLC	-0.3	6.0	V
Input Current	(Note 3)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 4)	V_{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage (Note 4)	Serial Port Interface	V_{IND-S}	-0.3	VLS+ 0.4	V
	Control Port Interface	V_{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)		T_A	-50	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. Typical Analog input/output performance will slightly degrade at VA = 3.3 V.
2. The ADC_SDOUT may not meet timing requirements in TDM, Double-Speed Mode.
3. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
4. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (COMMERCIAL)

(Test Conditions (unless otherwise specified): T_A = -10°C to +70°C; VD = VLS = VLC = 3.3 V±5%, VA = 5 V±5%; Full-scale input sine wave: 1 kHz through the active input filter in Figure 25 on page 52 and Figure 26 on page 52; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential			Single-Ended			Unit
		Min	Typ	Max	Min	Typ	Max	
Fs=48 kHz, 96 kHz, 192 kHz								
Dynamic Range	A-weighted	99	105	-	96	102	-	dB
	unweighted	96	102	-	93	99	-	dB
40 kHz bandwidth	unweighted	-	99	-		96	-	dB
Total Harmonic Distortion + Noise	-1 dB	-	-98	-92	-	-95	-89	dB
(Note 5)	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
40 kHz bandwidth	-1 dB	-	-90	-	-	-90	-	dB
ADC1-2 Interchannel Isolation		-	90	-	-	90	-	dB
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Analog Input								
Full-Scale Input Voltage		1.06*VA	1.12*VA	1.18*VA	0.53*VA	0.56*VA	0.59*VA	Vpp
Differential Input Impedance	(Notes 6 & 8)	23	29	32				kΩ
Single-Ended Input Impedance	(Notes 7 & 8)	-	-	-	23	29	32	kΩ
Common Mode Rejection Ratio (CMRR)		-	82	-	-	-	-	dB

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE)

(Test Conditions (unless otherwise specified): T_A = -40°C to +85°C; VD = VLS = VLC = 3.3 V±5%, VA = 5 V±5%; Full-scale input sine wave: 1 kHz through the active input filter in Figure 25 on page 52 and Figure 26 on page 52; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs=48 kHz, 96 kHz, 192 kHz								
Dynamic Range	A-weighted	97	105	-	94	102	-	dB
	unweighted	94	102	-	91	99	-	dB
40 kHz bandwidth	unweighted	-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise (Note 5)	-1 dB	-	-98	-90	-	-95	-87	dB
	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
40 kHz bandwidth	-1 dB	-	-87	-	-	-87	-	dB
ADC1-2 Interchannel Isolation		-	90	-	-	90	-	dB
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Analog Input								
Full-Scale Input Voltage		1.04*VA	1.12*VA	1.20*VA	0.52*VA	0.56*VA	0.60*VA	Vpp
Differential Input Impedance (Notes 6 & 8)		23	29	32				kΩ
Single-Ended Input Impedance (Notes 7 & 8)		-	-	-	23	29	32	kΩ
Common Mode Rejection Ratio (CMRR)		-	82	-	-	-	-	dB

Notes:

5. Referred to the typical full-scale voltage.
6. Measured between AINx+ and AINx-.
7. Measured between AINxx and AGND.
8. The input impedance scales inversely proportionate to the sample rate of the ADC modulator.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Notes 9, 10)		Min	Typ	Max	Unit
Single-Speed Mode (Note 10)					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.08	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay		-	12/Fs	-	s
Double-Speed Mode (Note 10)					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.16	dB
Stopband		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay		-	9/Fs	-	s
Quad-Speed Mode (Note 10)					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.2604	Fs
Passband Ripple		-	-	0.16	dB
Stopband		0.5000	-	-	Fs
Stopband Attenuation		60	-	-	dB
Total Group Delay		-	5/Fs	-	s
High-Pass Filter Characteristics					
Frequency Response	-3.0 dB -0.13 dB	-	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time		-	10^5/Fs	0	s

Notes:

9. Filter response is guaranteed by design.
10. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 31 to 42) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL)

(Test Conditions (unless otherwise specified): T_A = -10°C to +70°C; VD = VLS = VLC = 3.3 V±5%, VA = 5 V±5%; Full-scale 997 Hz output sine wave (see Note 12) into passive filter in Figure 31 on page 55 and active filter in Figure 31 on page 55; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs = 48 kHz, 96 kHz, 192 kHz								
Dynamic Range								
18 to 24-Bit	A-weighted	102	108	-	99	105	-	dB
	unweighted	99	105	-	96	102	-	dB
16-Bit	A-weighted	-	99	-	-	96	-	dB
	unweighted	-	96	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-98	-92	-	-95	-89	dB
	-20 dB	-	-85	-	-	-82	-	dB
	-60 dB	-	-45	-	-	-42	-	dB
16-Bit	0 dB	-	-93	-	-	-90	-	dB
	-20 dB	-	-76	-	-	-73	-	dB
	-60 dB	-	-36		-	-33	-	dB
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB
Analog Output								
Full-Scale Output		1.235•VA	1.300•VA	1.365•VA	0.618•VA	0.650•VA	0.683•VA	Vpp
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin	(Note 11)	-	-	10	-	-	10	µA
AC-Load Resistance (R_L)	(Note 13)	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)	(Note 13)	-	-	100	-	-	100	pF

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE)

(Test Conditions (unless otherwise specified): T_A = -40°C to +85°C; VD = VLS = VLC = 3.3 V±5%, VA = 5 V±5%; Full-scale 997 Hz output sine wave (see Note 12) in Figure 31 on page 55 and Figure 31 on page 55; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs = 48 kHz, 96 kHz, 192 kHz								
Dynamic Range								
18 to 24-Bit	A-weighted	100	108	-	97	105	-	dB
	unweighted	97	105	-	94	102	-	dB
16-Bit	A-weighted	-	99	-	-	96	-	dB
	unweighted	-	96	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-98	-90	-	-95	-87	dB
	-20 dB	-	-85	-	-	-82	-	dB
	-60 dB	-	-45	-	-	-42	-	dB
16-Bit	0 dB	-	-93	-	-	-90	-	dB
	-20 dB	-	-76	-	-	-73	-	dB
	-60 dB	-	-36	-	-	-33	-	dB
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB
Analog Output								
Full-Scale Output		1.210•VA	1.300•VA	1.392•VA	0.605•VA	0.650•VA	0.696•VA	Vpp
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin	(Note 11)	-	-	10	-	-	10	µA
AC-Load Resistance (R_L)	(Note 13)	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)	(Note 13)	-	-	100	-	-	100	pF

Notes:

11. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC-blocking capacitors.
12. One LSB of triangular PDF dither is added to data.
13. Guaranteed by design. See Figure 2. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the dominant pole of the two-pole amp in the output stage. Increasing this value beyond the recommended 100 pF can cause the internal op-amp to become unstable. See "External Filters" on page 52 for a recommended output filter.

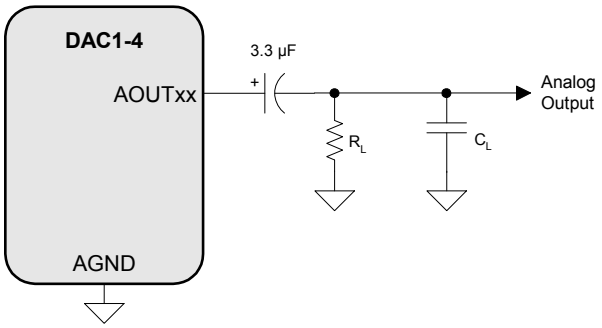


Figure 2. Output Test Circuit for Maximum Load

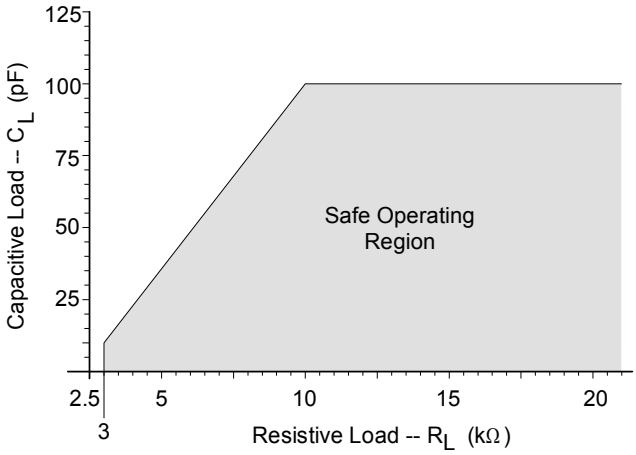


Figure 3. Maximum Loading

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Notes 9, 14)		Min	Typ	Max	Unit
Single-Speed Mode					
Passband (Frequency Response)	to -0.05 dB corner	0	-	0.4780	Fs
	to -3 dB corner	0	-	0.4996	Fs
Frequency Response 10 Hz to 20 kHz		-0.2	-	+0.08	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation	(Note 15)	50	-	-	dB
Group Delay		-	10/Fs	-	s
De-emphasis Error (Note 16)	Fs = 32 kHz	-	-	+1.5/+0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.25	dB
	Fs = 48 kHz	-	-	-0.2/-0.4	dB
Double-Speed Mode					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4650	Fs
	to -3 dB corner	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz		-0.2	-	+0.7	dB
StopBand		0.5770	-	-	Fs
StopBand Attenuation	(Note 15)	55	-	-	dB
Group Delay		-	5/Fs	-	s
Quad-Speed Mode					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.397	Fs
	to -3 dB corner	0	-	0.476	Fs
Frequency Response 10 Hz to 20 kHz		-0.2	-	+0.05	dB
StopBand		0.7	-	-	Fs
StopBand Attenuation	(Note 15)	51	-	-	dB
Group Delay		-	2.5/Fs	-	s

Notes:

14. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 43 to 54) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
15. Single- and Double-Speed Mode Measurement Bandwidth is from Stopband to 3 Fs. Quad-Speed Mode Measurement Bandwidth is from Stopband to 1.34 Fs.
16. De-emphasis is only available in Single-Speed Mode.

SWITCHING SPECIFICATIONS - ADC/DAC PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLS, ADC_SDOUT C_{LOAD} = 15 pF.)

Parameters (Note 21)	Symbol	Min	Max	Units
Slave Mode				
$\overline{\text{RST}}$ pin Low Pulse Width (Note 17)		1	-	ms
MCLK Frequency		0.512	50	MHz
MCLK Duty Cycle (Note 18)		45	55	%
Input Sample Rate (LRCK) Single-Speed Mode	F_s	4	50	kHz
Double-Speed Mode (Note 19)	F_s	50	100	kHz
Quad-Speed Mode (Note 20)	F_s	100	200	kHz
LRCK Duty Cycle		45	55	%
SCLK Duty Cycle		45	55	%
SCLK High Time	t_{sckh}	8	-	ns
SCLK Low Time	t_{sckl}	8	-	ns
LRCK Rising Edge to SCLK Rising Edge	t_{fss} t_{lcks}	5	-	ns
SCLK Rising Edge to LRCK Falling Edge	t_{fsh}	16	-	ns
SCLK Falling Edge to ADC_SDOUT Output Valid	t_{dpd}	-	35	ns
DAC_SDIN Setup Time Before SCLK Rising Edge	t_{ds}	3	-	ns
DAC_SDIN Hold Time After SCLK Rising Edge	t_{dh}	5	-	ns
DAC_SDIN Hold Time After SCLK Rising Edge	t_{dh1}	5	-	ns
ADC_SDOUT Hold Time After SCLK Rising Edge	t_{dh2}	10	-	ns
ADC_SDOUT Valid Before SCLK Rising Edge	t_{dval}	15	-	ns
Master Mode				
Output Sample Rate (LRCK) All Speed Modes	F_s	-	MCLK / 256	kHz
LRCK Duty Cycle		45	55	%
SCLK Frequency		-	64 x Fs	MHz
SCLK Duty Cycle		45	55	%
LRCK Edge to SCLK Rising Edge	t_{lcks}	-	5	ns
SCLK Falling Edge to ADC_SDOUT Output Valid	t_{dpd}	-	35	ns
DAC_SDIN Setup Time Before SCLK Rising Edge	t_{ds}	3	-	ns
DAC_SDIN Hold Time After SCLK Rising Edge	t_{dh1}	5	-	ns

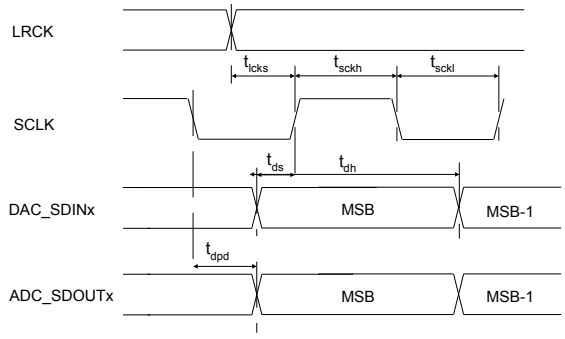


Figure 4. Serial Audio Interface Slave Mode Timing

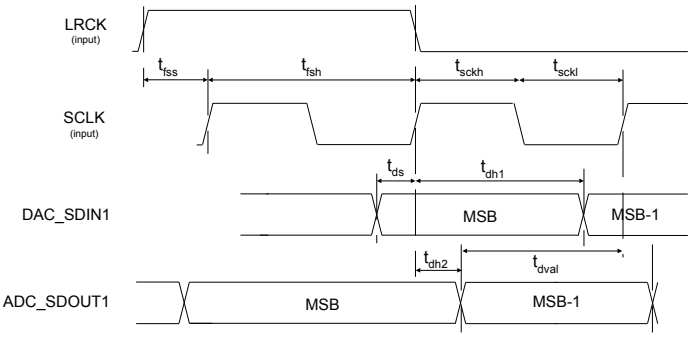


Figure 5. TDM Serial Audio Interface Timing

Notes:

17. After powering up the CS42888, $\overline{\text{RST}}$ should be held low after the power supplies and clocks are settled.
18. See Table 10 on page 42 and Table 11 on page 43 for suggested MCLK frequencies.
19. When operating in TDM interface format, VLS is limited to nominal 2.5 V to 5.0 V operation only.
20. ADC - I²S, Left-Justified, Right-Justified interface formats only. DAC - I²S, Left-Justified, Right-Justified and Time Division Multiplexed interface formats only.
21. “LRCK” and “SCLK” shall refer to the ADC and DAC left/right clock and serial clock, respectively.

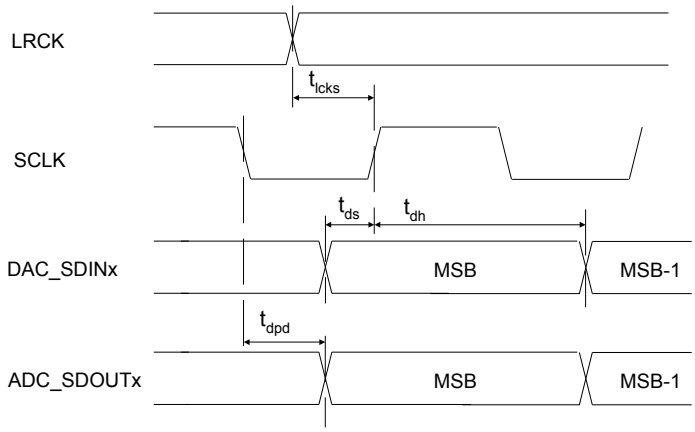


Figure 6. Serial Audio Interface Master Mode Timing

SWITCHING CHARACTERISTICS - AUX PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLS.)

Parameters		Symbol	Min	Max	Units
Master Mode					
Output Sample Rate (AUX_LRCK)	All Speed Modes	F_s	-	ADC_LRCK	kHz
AUX_SCLK Frequency			-	64·ADC_LRCK	kHz
AUX_SCLK Duty Cycle			45	55	%
AUX_LRCK Edge to SCLK Rising Edge		t_{lcks}	-	5	ns
AUX_SDIN Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
AUX_SDIN Hold Time After SCLK Rising Edge		t_{dh}	5	-	ns

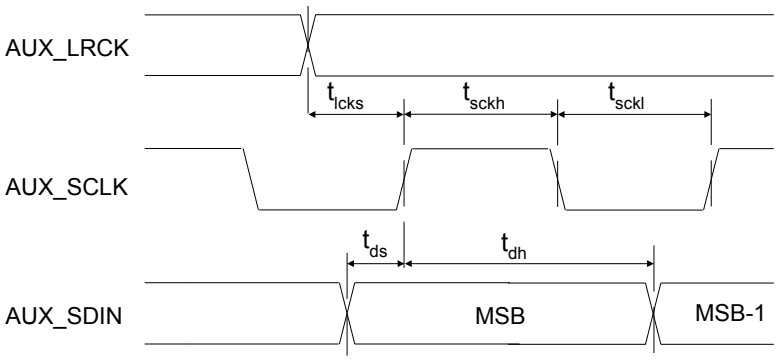


Figure 7. Serial Audio Interface Slave Mode Timing

SWITCHING SPECIFICATIONS - CONTROL PORT - I²C MODE

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, SDA C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 22)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA (Note 23)	t_{rc}	-	1	µs
Fall Time SCL and SDA (Note 23)	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

22. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.
23. Guaranteed by design.

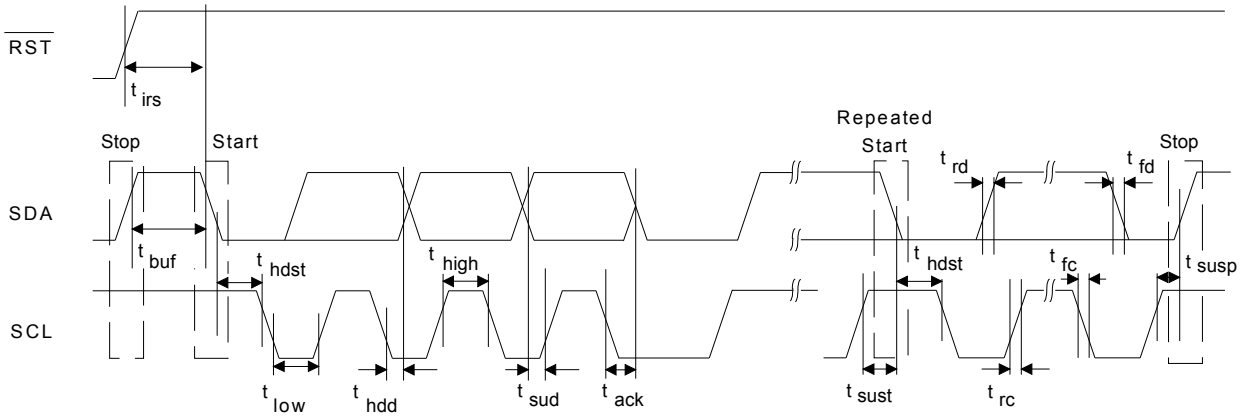


Figure 8. Control Port Timing - I²C Format

SWITCHING SPECIFICATIONS - CONTROL PORT - SPI FORMAT

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, CDOUT C_L = 30 pF)

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	20	-	ns
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 24)	t_{dh}	15	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	50	ns
Rise Time of CDOUT		t_{r1}	-	25	ns
Fall Time of CDOUT		t_{f1}	-	25	ns
Rise Time of CCLK and CDIN	(Note 25)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 25)	t_{f2}	-	100	ns

Notes:

24. Data must be held for sufficient time to bridge the transition time of CCLK.
25. For f_{sck} <1 MHz.

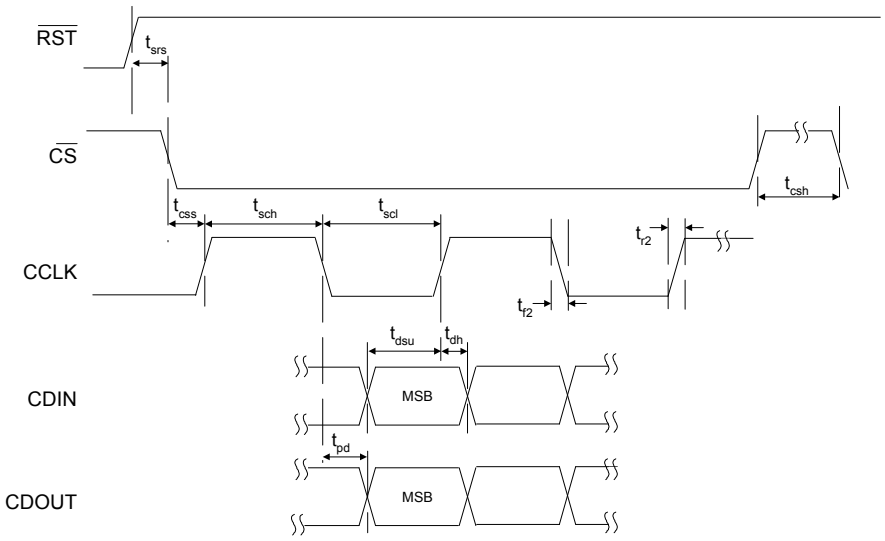


Figure 9. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 26)						
Power Supply Current	VA = 5.0 V	I_A	-	80	-	mA
	VLS = VLC = VD = 3.3 V (Note 27)	I_{DT}	-	60.6	-	mA
Power Dissipation	All Supplies = 5 V		-	600	850	mW
Power Supply Rejection Ratio (Note 28)	1 kHz	PSRR	-	60	-	dB
	60 Hz		-	40	-	dB
Power-Down Mode (Note 29)						
Power Dissipation	All Supplies = VA = 5 V		-	1.25	-	mW
VQ Characteristics						
Nominal Voltage			-	0.5•VA	-	V
Output Impedance			-	23	-	kΩ
DC Current Source/Sink (Note 30)			-	-	10	µA
FILT+_ADC Nominal Voltage			-	VA	-	V
FILT+_DAC Nominal Voltage			-	VA	-	V

Notes:

26. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS input to the DAC and AUX port, and a 1 kHz, -1 dB analog input to the ADC port sampled at the highest F_s for each speed mode. DAC outputs are open, unless otherwise specified.
27. I_{DT} measured with no external loading on pin 64 (SDA).
28. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.
29. Power-Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static and no analog input.
30. Guaranteed by design. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through the electrolytic de-coupling capacitors.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 31)		Symbol	Min	Typ	Max	Units
High-Level Output Voltage at I_o=2 mA	Serial Port	V_{OH}	VLS-1.0	-	-	V
	Control Port		VLC-1.0	-	-	V
	MUTEC		VA-1.0	-	-	V
Low-Level Output Voltage at I_o=2 mA	Serial Port	V_{OL}	-	-	0.4	V
	Control Port		-	-	0.4	V
	MUTEC		-	-	0.4	V
High-Level Input Voltage	Serial Port	V_{IH}	0.7xVLS	-	-	V
	Control Port		0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.2xVLS	V
	Control Port		-	-	0.2xVLC	V
Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance (Note 23)			-	-	10	pF
MUTEC Drive Current			-	3	-	mA

Notes:

31. See "Digital I/O Pin Characteristics" on page 8 for serial and control port power rails.

4. APPLICATIONS

4.1 Overview

The CS42888 is a highly integrated mixed signal 24-bit audio CODEC comprised of 4 analog-to-digital converters (ADC) implemented using multi-bit delta-sigma techniques and 8 digital-to-analog converters (DAC) also implemented using multi-bit delta-sigma techniques.

Other functions integrated within the CODEC include independent digital volume controls for each DAC, digital de-emphasis filters for the DAC, digital volume control with gain on each ADC channel, ADC high-pass filters, an on-chip voltage reference, and Popguard technology that minimizes the effects of output transients on power-up and power-down.

All serial data is transmitted through two independent serial ports: the DAC serial port and the ADC serial port. Each serial port can be configured independently to operate at different sample and clock rates, but both must run synchronous to each other.

The serial audio interface ports allow up to 8 DAC channels and 6 ADC channels in a Time-Division Multiplexed (TDM) interface format. In the One-Line Mode (OLM) interface format, the CS42888 will allow up to 6 ADC channels on one data line and up to 8 DAC channels on 2 data lines.

The CS42888 features an Auxiliary Port used to accommodate an additional two channels of PCM data on the ADC_SDOUT data line in the TDM digital interface format. See “AUX Port Digital Interface Formats” on page 33 for details.

The CS42888 operates in one of three oversampling modes based on the input sample rate. When operating the CODEC as a slave, mode selection is determined automatically based on the MCLK frequency setting. When operating as a master, mode selection is determined by the ADC and DAC FM bits in register “Functional Mode (Address 03h)” on page 42. Single-Speed Mode (SSM) supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed Mode (DSM) supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed Mode (QSM) supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x (**Note:** QSM for the ADC is only supported in the I²S, Left-Justified, Right-Justified interface formats. QSM for the DAC is supported in the I²S, Left-Justified, Right-Justified and Time Division Multiplexed interface formats).

All functions can be configured through software via a serial control port operable in SPI Mode or in I²C Mode.

Figure 2 on page 16 shows the recommended connections for the CS42888. See “Register Description” on page 40 for the default register settings and options.

4.2 Analog Inputs

4.2.1 Line-Level Inputs

AINx+ and AINx- are the line-level differential analog inputs internally biased to VQ, approximately VA/2. Figure 10 on page 25 shows the full-scale analog input levels. The CS42888 also accommodates single-ended signals on all inputs, AIN1-AIN4. See “ADC Input Filter” on page 52 for the recommended input filters.

For single-ended operation on ADC1-ADC2 (AIN1 to AIN4), the ADCx_SINGLE bit in the register “ADC Control & DAC De-Emphasis (Address 05h)” on page 44 must be set appropriately (see Figure 26 on page 52 for required external components).

The gain/attenuation of the signal can be adjusted for each AINx independently through the “AINX Volume Control (Address 11h-14h)” on page 48.

The ADC output data is in 2's complement binary format. For differential inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively, and cause the ADC Overflow bit in the register "Status (Address 19h) (Read Only)" on page 49 to be set to a '1'. For single-ended inputs, the analog input level must remain at or below full scale to avoid wraparound of the resulting ADC codes. The ADC Overflow bit is reserved in single-ended mode.

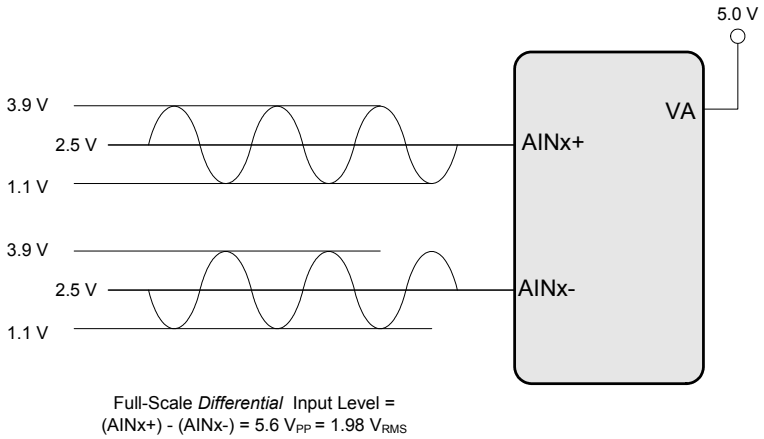


Figure 10. Full-Scale Input

4.2.2 High-Pass Filter and DC Offset Calibration

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the high-pass filter is disabled during normal operation, the current value of the DC offset for the corresponding channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS42888 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

The high-pass filter for ADC1/ADC2 can be enabled and disabled. The high-pass filters are controlled using the HPF_FREEZE bit in the register "ADC Control & DAC De-Emphasis (Address 05h)" on page 44.

4.3 Analog Outputs

4.3.1 Initialization

The initialization and Power-Down sequence flow chart is shown in Figure 11 on page 26. The CS42888 enters a power-down state upon initial power-up. The interpolation and decimation filters, delta-sigma modulators and control port registers are reset. The internal voltage reference, multi-bit digital-to-analog and analog-to-digital converters and switched-capacitor low-pass filters are powered down.

The device remains in the power-down state until the RST pin is brought high. The control port is accessible once RST is high, and the desired register settings can be loaded per the interface descriptions in the "Control Port Description and Timing" on page 33.

VQ will quickly charge to VA/2 upon initial power up. Once MCLK is valid and the PDN bit is set to '0'b, the internal voltage reference, FILT+_ADC and FILT+_DAC, will ramp up to approximately VA. Power is applied to the D/A converters and switched-capacitor filters, and the analog outputs are clamped to the quiescent voltage, VQ. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to