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CS4299

CrystalClear® SoundFusion™ Audio Codec '97

Features

- AC '97 2.1 Compatible
- Industry Leading Mixed Signal Technology
- 20-bit Stereo Digital-to-Analog Converters
- 18-bit Stereo Analog-to-Digital Converters
- Sample Rate Converters
- Four Analog Line-level Stereo Inputs for LINE_IN, CD, VIDEO, and AUX
- Two Analog Line-level Mono Inputs for Modem and Internal PC Beep
- Dual Stereo Line-level Outputs for LINE_OUT and ALT_LINE_OUT
- Dual Microphone Inputs
- High Quality Pseudo-Differential CD Input
- Extensive Power Management Support
- Meets or Exceeds the Microsoft® PC 99 Audio Performance Requirements
- S/PDIF Digital Audio Output
- CrystalClear® 3D Stereo Enhancement

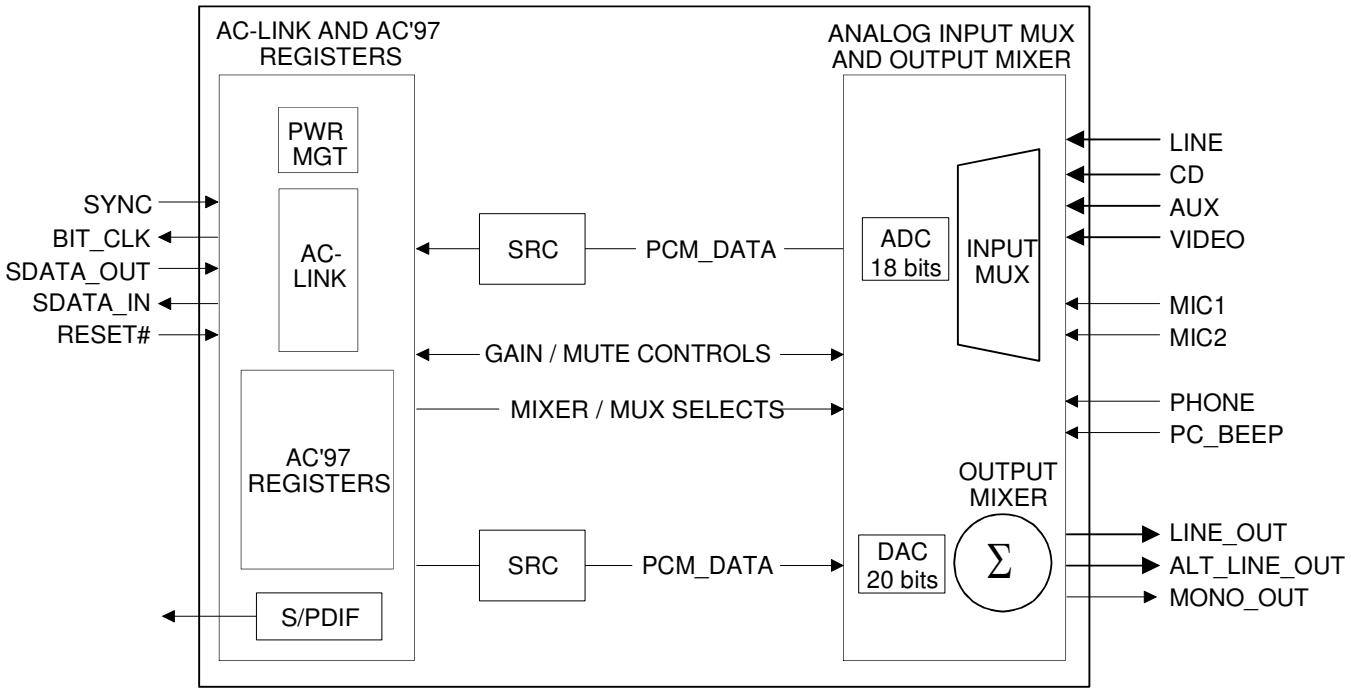
Description

The CS4299 is an AC '97 2.1 compatible stereo audio codec designed for PC multimedia systems. Using the industry leading CrystalClear® delta-sigma and mixed signal technology, the CS4299 enables the design of PC 99-compliant desktop, portable, and entertainment PCs.

Coupling the CS4299 with a PCI audio accelerator or core logic supporting the AC '97 interface, implements a cost effective, superior quality, audio solution. The CS4299 surpasses PC 99 and AC '97 2.1 audio quality standards.

ORDERING INFO

CS4299-BQZ lead-free 48-pin LQFP 9x9x1.4 mm
CS4299-JQZ lead-free 48-pin LQFP 9x9x1.4 mm



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1 Characteristics and specifications

ANALOG CHARACTERISTICS Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V ±5%, DVdd = 3.3 V ±5%; 1 kHz Input Sine wave; Sample Frequency, Fs = 48 kHz; Z_{AL}=100 kΩ/ 1000 pF load, C_{DL} = 18 pF load (Note 1); Measurement bandwidth is 20 Hz - 20 kHz, 18-bit linear coding for ADC functions, 20-bit linear coding for DAC functions; Mixer registers set for unity gain.

Parameter (Note 2)	Symbol	Path (Note 3)	CS4299-BQZ			CS4299-JQZ			Unit
			Min	Typ	Max	Min	Typ	Max	
Full Scale Input Voltage									
Line Inputs		A-D	-	1.00	-	0.91	1.00	-	V_{RMS}
Mic Inputs		A-D	-	1.00	-	0.91	1.00	-	V_{RMS}
Mic Inputs (20 dB internal gain)		A-D	-	0.10	-	0.091	0.10	-	V_{RMS}
Full Scale Output Voltage									
Line,Alternate Line, and Mono Outputs		D-A	0.85	1.0	1.15	0.91	1.0	1.13	V_{RMS}
Frequency Response (Note 4)	FR								
Analog Ac = ± 0.25 dB		A-A	20	-	20,000	20	-	20,000	Hz
DAC Ac = ± 0.25 dB		D-A	20	-	20,000	20	-	20,000	Hz
ADC Ac = ± 0.25 dB		A-D	20	-	20,000	20	-	20,000	Hz
Dynamic Range	DR								
Stereo Analog inputs to LINE_OUT		A-A	-	90	-	-	90	-	dB FS A
Mono Analog inputs to LINE_OUT		A-A	-	85	-	-	85	-	dB FS A
DAC Dynamic Range		D-A	-	85	-	-	87	-	dB FS A
ADC Dynamic Range		A-D	-	80	-	-	85	-	dB FS A
DAC SNR (-20 dB FS input w/ CCIR-RMS filter on output)	SNR	D-A	-	70	-	-	-	-	dB
Total Harmonic Distortion + Noise (-3 dB FS input signal):	THD+N								
Line/Alternate Line Output		A-A	-	-	-72	-	-	-74	dB FS
DAC		D-A	-	-	-72	-	-	-74	dB FS
ADC (all inputs except phone/mic)		A-D	-	-	-72	-	-	-74	dB FS
ADC (phone/mic)		A-D	-	-	-72	-	-	-74	dB FS
Power Supply Rejection Ratio (1 kHz, 0.5 V_{RMS} w/ 5 V DC offset) (Note 4)			-	40	-	-	40	-	dB
Interchannel Isolation			-	60	-	-	88	-	dB
Spurious Tone (Note 4)			-	-100	-	-	-100	-	dB FS
Input Impedance (Note 4)			10	-	-	10	-	-	kΩ
External Load Impedance			10	-	-	10	-	-	kΩ
Output Impedance (Note 4)			-	730	-	-	730	-	Ω
Input Capacitance (Note 4)			-	5	-	-	5	-	pF
Vrefout			2.0	2.28	2.5	2.0	2.28	2.5	V

Notes:

1. Z_{AL} refers to the analog output pin loading and C_{DL} refers to the digital output pin loading.
2. Parameter definitions are given in the Section 10, *Parameter and Term Definitions*.
3. Path refers to the signal path used to generate this data. These paths are defined in the Section 10, *Parameter and Term Definitions*.
4. This specification is guaranteed by silicon characterization, it is not production tested.

ABSOLUTE MAXIMUM RATINGS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter		Min	Min -BQZ	Typ	Max	Max -BQZ	Unit
Power Supplies	+3.3 V Digital	-0.3	-0.3	-	6.0	6.0	V
	+5 V Digital	-0.3	-0.3	-	6.0	6.0	V
	Analog	-0.3	-0.3	-	6.0	6.0	V
Total Power Dissipation	(Supplies, Inputs, Outputs)	-	-	-	1.25	1.25	W
Input Current per Pin	(Except Supply Pins)	-10	-10	-	10	10	mA
Output Current per Pin	(Except Supply Pins)	-15	-15	-	15	15	mA
Analog Input voltage		-0.3	-0.3	-	AVdd+ 0.3	AVdd+ 0.3	V
Digital Input voltage		-0.3	-0.3	-	DVdd + 0.3	DVdd + 0.3	V
Ambient Temperature	(Power Applied)	-55	-40	-	110	85	°C
Storage Temperature		-65	-65	-	150	150	°C

RECOMMENDED OPERATING CONDITIONS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter		Symbol	Min	Min -BQZ	Typ	Max	Max -BQZ	Unit
Power Supplies	+3.3 V Digital	DVdd1, DVdd2	3.135	3.135	3.3	3.465	3.465	V
	+5 V Digital	DVdd1, DVdd2	4.75	4.75	5	5.25	5.25	V
	Analog	AVdd1, AVdd2	4.75	4.75	5	5.25	5.25	V
Operating Ambient Temperature			0	-40	-	70	85	°C

DIGITAL CHARACTERISTICS (AVss = DVss = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	V_{il}	-	-	0.8	V
High level input voltage	V_{ih}	0.65 x DVdd	-	-	V
High level output voltage	V_{oh}	0.90 x DVdd	0.99 x DVdd	-	V
Low level output voltage	V_{ol}	-	0.03	0.10 x DVdd	V
Input Leakage Current (AC-link inputs)		-10	-	10	µA
Output Leakage Current (Tri-stated AC-link outputs)		-10	-	10	µA
Output buffer drive current					
BIT_CLK, S/PDIF_OUT		-	24	-	mA
SDATA_IN, EAPD (Note 4)		-	4	-	mA

AC '97 SERIAL PORT TIMING

Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V, DVdd = 3.3 V; C_L = 55 pF load.

Parameter	Symbol	Min	Typ	Max	Unit
RESET Timing					
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK start-up delay	$T_{rst2clk}$	-	40.0	-	µs
1st SYNC active to CODEC READY set	$T_{sync2crd}$	-	62.5	-	µs
Vdd stable to Reset inactive	$T_{vdd2rst\#}$	100	-	-	µs
Clocks					
BIT_CLK frequency	F_{clk}	-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter (depends on XTAL_IN source)		-	-	750	ps
BIT_CLK high pulse width	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width	T_{clk_low}	36	40.7	45	ns
SYNC frequency	F_{sync}	-	48	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs
Data Setup and Hold					
Output Propagation delay from rising edge of BIT_CLK	T_{co}	8	10	12	ns
Input setup time from falling edge of BIT_CLK	T_{isetup}	10	-	-	ns
Input hold time from falling edge of BIT_CLK	T_{ihold}	0	-	-	ns
Input Signal rise time	T_{irise}	2	-	6	ns
Input Signal fall time	T_{ifall}	2	-	6	ns
Output Signal rise time (Note 4)	T_{orise}	2	4	6	ns
Output Signal fall time (Note 4)	T_{ofall}	2	4	6	ns
Misc. Timing Parameters					
End of Slot 2 to BIT_CLK, SDATA_IN low (PR4)	T_{s2_pdown}	-	.28	1.0	µs
SYNC pulse width (PR4) Warm Reset	T_{sync_pr4}	1.0	-	-	µs
SYNC inactive (PR4) to BIT_CLK start-up delay	$T_{sync2clk}$	162.8	285	-	ns
Setup to trailing edge of RESET# (ATE test mode) (Note 4)	$T_{setup2rst}$	15	-	-	ns
Rising edge of RESET# to Hi-Z delay (Note 4)	T_{off}	-	-	25	ns

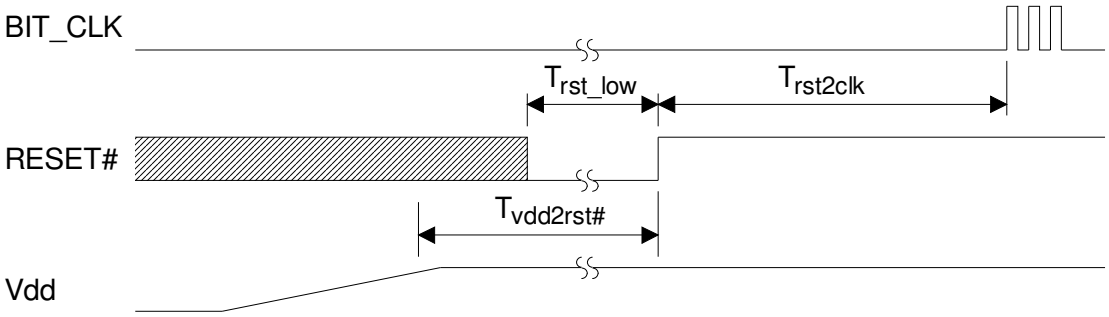

Figure 1-1. Power Up Timing

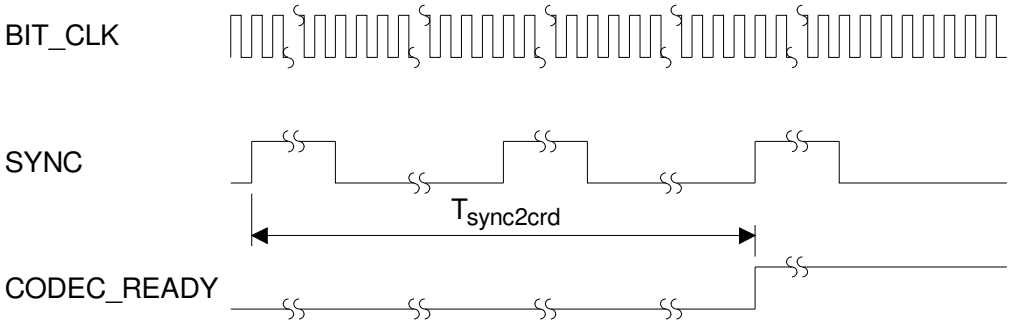

Figure 1-2. Codec Ready from Startup or Fault Condition

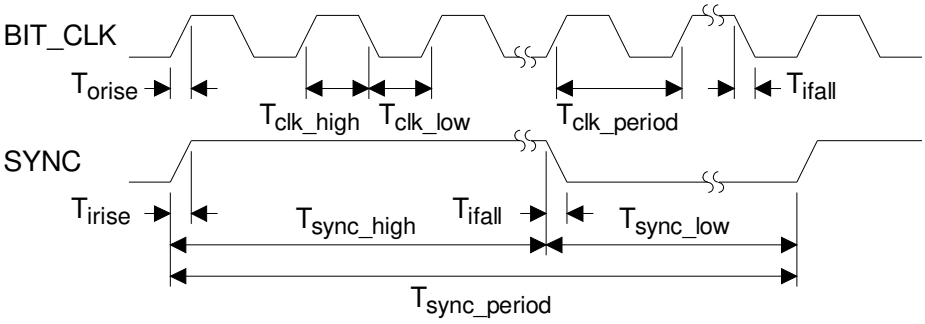

Figure 1-3. Clocks

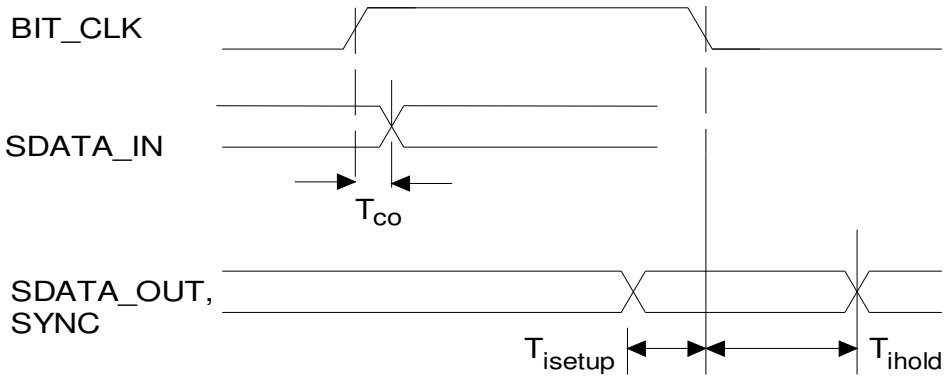

Figure 1-4. Data Setup and Hold

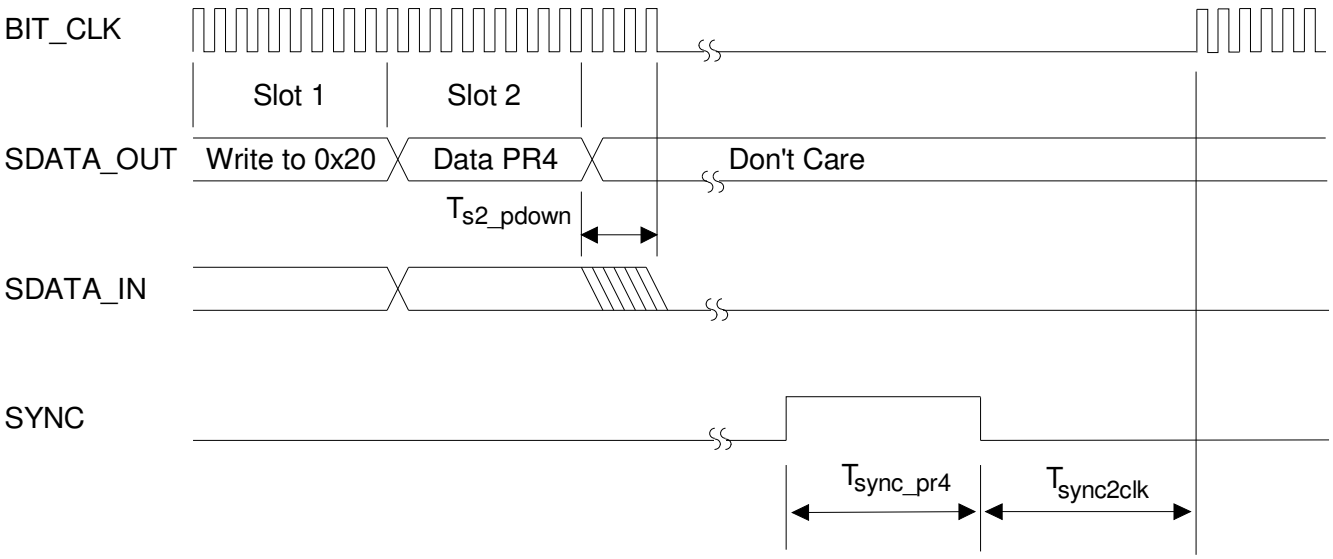

Figure 1-5. PR4 Powerdown and Warm Reset

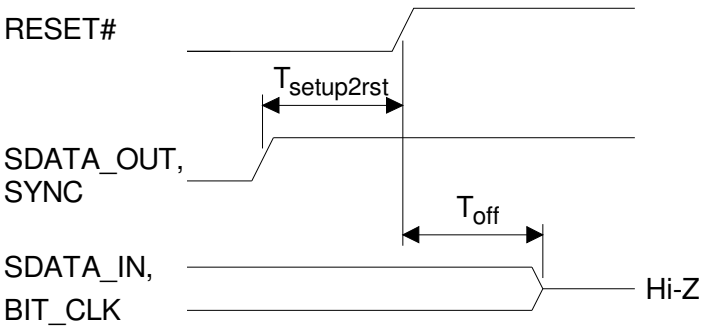

Figure 1-6. Test Mode

2 General Description

The CS4299 is a mixed-signal serial audio Codec compliant to the Intel® *Audio Codec '97 Specification*, revision 2.1 [1]. It is designed to be paired with a digital controller, typically located on the PCI bus or integrated within the system core logic chip set. The controller is responsible for all communications between the CS4299 and the remainder of the system. The CS4299 contains two distinct functional sections: digital and analog. The digital section includes the AC-link interface, S/PDIF interface, serial data port, Sample Rate Converters, and power management support. The analog section includes the analog input multiplexer (mux), stereo output mixer, mono output mixer, stereo Analog-to-Digital Converters (ADCs), stereo Digital-to-Analog Converters (DACs), and their associated volume controls.

2.1 AC-Link

All communication with the CS4299 is established with a 5-wire digital interface to the controller, as shown in Fig. 2-1. This interface is called the AC-link. All clocking for the serial communication is synchronous to the BIT_CLK signal. BIT_CLK is generated by the primary audio codec and is used to clock the controller and any secondary audio codecs. Both input and output AC-link audio frames are organized as a sequence of 256 serial bits forming 13 groups referred to as 'slots'. During each audio frame, data is passed bi-directionally between the CS4299 and the controller. The input frame is driven from the CS4299 on the SDATA_IN line. The output frame is driven from the controller on the SDATA_OUT line. The controller is also responsible for issuing reset commands via the RESET# signal. Following a Cold Reset, the CS4299 is responsible for notifying the controller that it is ready for operation after synchronizing its internal functions. The CS4299 AC-link signals must use the same digital supply voltage as the controller chip, either +5 V or +3.3 V. See Section 3, *AC Link Frame Definition*, for detailed AC-link information.

2.2 Control registers

The CS4299 contains a set of AC '97 compliant control registers and a set of Cirrus Logic defined control registers. These registers control the basic functions and features of the CS4299. Read accesses of the control registers by the AC '97 controller are accomplished with the requested register index in Slot 1 of a SDATA_OUT frame. The following SDATA_IN frame will contain the read data in its Slot 2. Write operations are similar, with the register index in Slot 1 and the write data in Slot 2 of a SDATA_OUT frame. The function of each input and output frame is detailed in Section 3, *AC Link Frame Definition*. Individual register descriptions are found in Section 4, *Register Interface*.

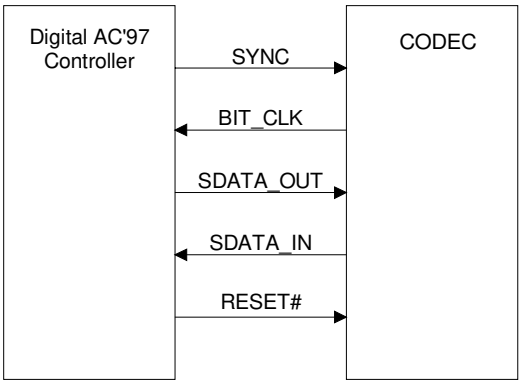

Figure 2-1. AC-link Connections

2.3 Sample Rate Converters

The Sample Rate Converters (SRCs) provide high accuracy digital filters supporting sample frequencies other than 48 kHz to be captured from the CS4299 or played from the controller. AC '97 requires support for two audio rates (44.1 and 48kHz). In addition, the Intel® I/O Controller Hub (ICHx) specification requires support for five more audio rates (8, 11.025, 16, 22.05, and 32). The CS4299 supports all these rate, as shown in Table 4-7 on page 27.

2.4 Output Mixer

The CS4299 has two output mixers, illustrated in Fig. 2-2. The stereo output mixer sums together the analog inputs to the CS4299, including the PC_BEEP and PHONE signals, according to the settings in the volume control registers. The stereo output mix is sent to the LINE_OUT and ALT_LINE_OUT pins on the CS4299. The mono output mixer generates a monophonic sum of the left and right channels from the stereo input mixer. The mono output mix is sent to the MONO_ OUT output pin on the CS4299.

2.5 Input Mux

The input multiplexer controls which analog input is sent to the ADCs. The output of the input mux is converted to stereo 18-bit digital PCM data and sent to the controller by means of the AC-link SDATA_IN signal.

2.6 Volume Control

The CS4299 volume registers control analog input levels to the input mixer and analog output levels, including the master volume level, and the alternate volume level. The PC_BEEP volume control uses 3 dB steps with a range of 0 dB to -45 dB attenuation. All other analog volume controls use 1.5 dB steps. The analog inputs have a mixing range of +12 dB signal gain to -34.5 dB signal attenuation. The analog output volume controls have from 0 dB to -94.5 dB attenuation for LINE_ OUT and from 0 dB to -46.5 dB attenuation for ALT_LINE_OUT and MONO_OUT.

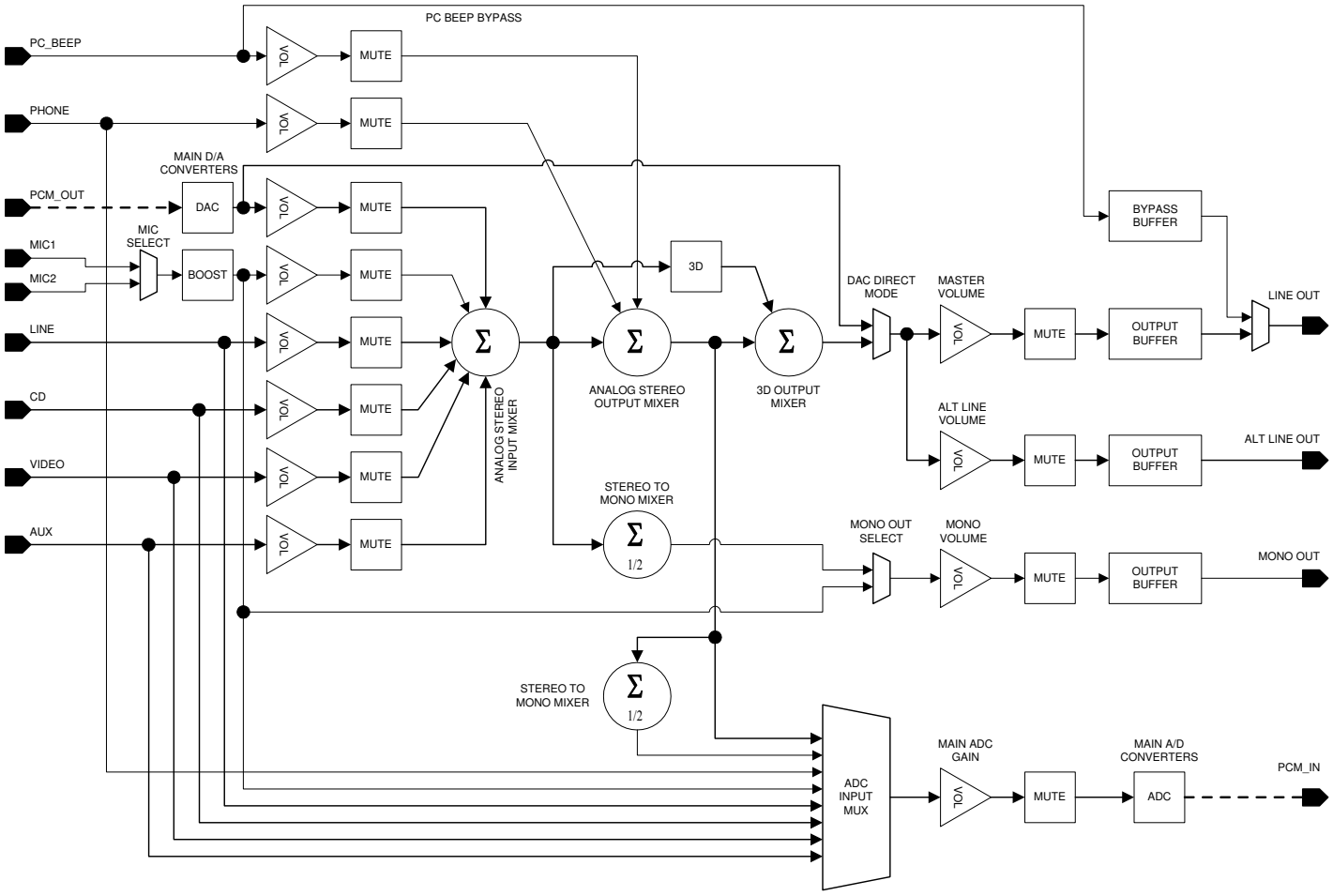

Figure 2-2. Mixer Diagram

3 AC Link Frame Definition

The AC-link is a bidirectional serial port with data organized into frames consisting of one 16-bit and twelve 20-bit time-division multiplexed slots. The first slot, called the tag slot, contains bits indicating if the CS4299 is ready to receive data (input frame) and which, if any, other slots contain valid data. Slots 1 through 12 contain audio or control/status data. Both the serial data output and input frames are defined from the controller perspective, not from the CS4299 perspective.

The controller synchronizes the beginning of a frame with the assertion of the SYNC signal. Fig. 3-1 shows the position of each bit location within the frame. The first bit position in a new serial data frame is F0 and the last bit position in the serial data frame is F255. When SYNC goes active (high) and is sampled active by the CS4299 (on the falling edge of BIT_CLK), both devices are synchronized to a new serial data frame. The data on the SDATA_OUT pin at this clock edge is the final bit of the previous frame's serial data. On the next rising edge of BIT_CLK, the first bit of Slot 0 is driven by the controller on the SDATA_OUT pin. On the next falling edge of BIT_CLK, the CS4299 latches this data in, as the first bit of the frame.

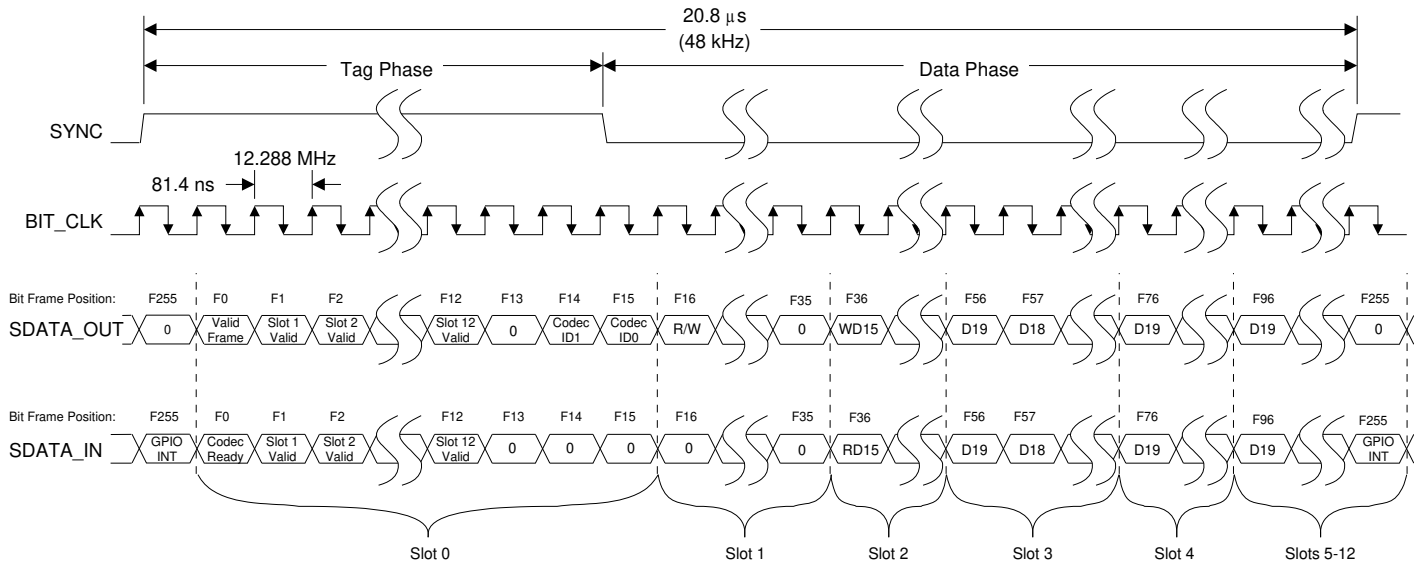

Figure 3-1. AC-link Input and Output Framing

3.1 AC-Link Serial Data Output Frame

In the serial data output frame, data is passed on the SDATA_OUT pin to the CS4299 from the AC '97 controller. Fig. 3-1 illustrates the serial port timing.

The PCM playback data being passed to the CS4299 is shifted out MSB first in the most significant bits of each slot. Any PCM data from the AC '97 controller that is not 20 bits wide should be left justified in its corresponding slot and dithered or zero-padded in the unused bit positions.

Bits that are reserved should always be 'cleared' by the AC '97 controller.

3.1.1 Serial Data Output Slot Tags (Slot 0)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Valid Frame	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	Slot 5 Valid	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	Slot 9 Valid	Slot 10 Valid	Reserved			Codec ID1	Codec ID0

Valid Frame — The Valid Frame bit determines if any of the following slots contain either valid playback data for the CS4299 DACs or data for read/write operations. When 'set', at least one of the other AC-link slots contain valid data. If this bit is 'clear', the remainder of the frame is ignored.

Slot [1:2] Valid — The Slot [1:2] Valid bits indicate the validity of data in their corresponding serial data output slots. If a bit is 'set', the corresponding output slot contains valid data. If a bit is 'cleared', the corresponding slot will be ignored.

Slot [3:10] Valid — The Slot [3:10] Valid bits indicate Slot [3:10] contains valid playback data for the CS4299. If a Slot Valid bit is 'set', the named slot contains valid audio data. If the bit is 'clear', the slot will be ignored. The CS4299 supports alternate slot mapping as defined in the AC '97 2.1 specification. For more information, see the *AC Mode Control Register (Index 5Eh)*.

Codec ID[1:0] — The Codec ID[1:0] bits display the Codec ID of the audio codec being accessed during the current AC-link frame. Codec ID[1:0] = 00 indicates the primary codec is being accessed. Codec ID[1:0] = 01, 10, or 11 indicates one of three possible secondary codecs is being accessed. A non-zero value of one or more of the Codec ID bits indicates a valid Read or Write Address in Slot 1, and the Slot 1 R/W bit indicates presence or absence of valid Data in Slot 2.

3.1.2 Command Address Port (Slot 1)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/$\overline{W}$	RI6	RI5	RI4	RI3	RI2	RI1	RI0	0	0	0	0	0	0	0	0	0	0	0	0

R/$\overline{W}$ — Read/$\overline{Write}$. When this bit is 'set', a read of the AC '97 register specified by the register index bits will occur in the AC '97 2.1 audio codec. When the bit is 'cleared', a write will occur. For any read or write access to occur, the Frame Valid bit (F0) must be 'set' and the Codec ID[1:0] bits (F[14:15]) must match the Codec ID of the AC '97 2.1 audio codec being accessed. Additionally, for a primary codec, the Slot 1 Valid bit (F1) must be 'set' for a read access and both the Slot 1 Valid bit (F1) and the Slot 2 Valid bit (F2) must be 'set' for a write access. For a secondary codec, both the Slot 1 Valid bit (F1) and the Slot 2 Valid bit (F2) must be 'cleared' for read and write accesses. See Fig. 3-1 for bit frame positions.

RI[6:0] — Register Index. The RI[6:0] bits contain the 7-bit register index to the AC '97 registers in the CS4299. All registers are defined at word addressable boundaries. The RI0 bit must be 'clear' to access CS4299 registers.

3.1.3 Command Data Port (Slot 2)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	Reserved			

WD[15:0] — Write Data. The WD[15:0] bits contain the 16-bit value to be written to the register. If an access is a read, this slot is ignored.

NOTE: For any write to an AC '97 register, the write is defined to be an 'atomic' access. This means that when the Slot 1 Valid bit in output Slot 0 is 'set', the Slot 2 Valid bit in output slot 0 should always be 'set' during the same audio frame. No write access may be split across 2 frames.

3.1.4 PCM Playback Data (Slots 3-10)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD[19:0] — Playback Data. The PD[19:0] bits contain the 20-bit PCM playback (2's complement) data for the left and right DACs and/or the S/PDIF transmitter. Table 4-8 on page 28 lists a cross reference for each function and its respective slot. The mapping of a given slot to a DAC is determined by the state of the ID[1:0] bits in the *Extended Audio ID Register (Index 28h)* and by the SM[1:0] and AMAP bits in the *AC Mode Control Register (Index 5Eh).*

3.2 AC-Link Audio Input Frame

In the serial data input frame, data is passed on the SDATA_IN pin from the CS4299 to the AC '97 controller. The data format for the input frame is very similar to the output frame. Fig. 3-1 illustrates the serial port timing.

The PCM capture data from the CS4299 is shifted out MSB first in the most significant 18 bits of each slot. The least significant 2 bits in each slot will be 'cleared'. If the host requests PCM data from the AC '97 Controller that is less than 18 bits wide, the controller should dither and round or just round (but not truncate) to the desired bit depth.

Bits that are reserved or not implemented in the CS4299 will always be returned 'cleared'.

3.2.1 Serial Data Input Slot Tag Bits (Slot 0)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Codec Ready	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	Slot 5 Valid	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	Slot 9 Valid	Slot 10 Valid	0	0	0	0	0

Codec Ready — The Codec Ready bit indicates the readiness of the CS4299 AC-link. Immediately after a Cold Reset this bit will be 'clear'. Once the CS4299 clocks and voltages are stable, this bit will be 'set'. Until the Codec Ready bit is 'set', no AC-link transactions should be attempted by the controller. The Codec Ready bit does not indicate readiness of the DACs, ADCs, Vref, or any other analog function. Those must be checked in the *Powerdown Control/Status Register (Index 26h)* by the controller before any access is made to the mixer registers. Any accesses to the CS4299 while Codec Ready is 'clear' are ignored.

Slot 1 Valid — When 'set', the Slot 1 Valid bit indicates Slot 1 contains a valid read back address.

Slot 2 Valid — When 'set', the Slot 2 Valid bit indicates Slot 2 contains valid register read data.

Slot [3:10] Valid — When 'set', the Slot [3:10] Valid bits indicate Slot [3:10] contains valid capture data from the CS4299 ADCs. Only if a Slot [3:10] Valid bit is 'set' will the corresponding input slot contain valid data.

3.2.2 Status Address Port (Slot 1)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RI6	RI5	RI4	RI3	RI2	RI1	RI0	SR3	SR4	SR5	SR6	SR7	SR8	SR9	SR10	0	Reserved		

RI[6:0] — Register Index. The RI[6:0] bits echo the AC '97 register address when a register read has been requested in the previous frame. The CS4299 will only echo the register index for a read access. Write accesses will not return valid data in Slot 1.

SR[3:10] — Slot Request. If SRx is 'set', this indicates the CS4299 SRC does not need a new sample on the next AC-link frame for that particular slot. If SRx is 'clear', the SRC indicates a new sample is needed on the following frame. If the VRA bit in the *Extended Audio Status/Control Register (Index 2Ah)* is 'clear', the SR[3:10] bits are always 0. When VRA is 'set', the SRC is enabled and the SR[3:10] bits are used to request data.

3.2.3 Status Data Port (Slot 2)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	Reserved			

RD[15:0] Read Data. The RD[15:0] bits contain the register data requested by the controller from the previous read request. All read requests will return the read address in the input Slot 1 and the register data in the input Slot 2 on the following serial data frame.

3.2.4 PCM Capture Data (Slot 3-10)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CD17	CD16	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	0	0

CD[17:0] Capture Data. The D[17:0] bits contain 18-bit PCM (2's complement) capture data. The mapping of a given slot to an ADC is determined by the state of the ID[1:0] bits in the *Extended Audio ID Register (Index 28h)* and the SM[1:0] and AMAP bits in the *AC Mode Control Register (Index 5Eh)*. The definition of each slot can be found in Table 4-8 on page 28.

3.3 AC-Link Protocol Violation - Loss of SYNC

The CS4299 is designed to handle SYNC protocol violations. The following are situations where the SYNC protocol has been violated:

- The SYNC signal is not sampled high for exactly 16 BIT_CLK clock cycles at the start of an audio frame.
- The SYNC signal is not sampled high on the 256th BIT_CLK clock period after the previous SYNC assertion.
- The SYNC signal goes active high before the 256th BIT_CLK clock period after the previous SYNC assertion.

Upon loss of synchronization with the controller, the CS4299 will 'clear' the Codec Ready bit in the serial data input frame until two valid frames are detected. During this detection period, the CS4299 will ignore all register reads and writes and will discontinue the transmission of PCM capture data. In addition, if the LOSM bit in the *Misc. Crystal Control Register (Index 60h)* is 'set' (default), the CS4299 will mute all analog outputs. If the LOSM bit is 'clear', the analog outputs will not be muted.

4 Register Interface

Table 4-1. Mixer Registers

Reg	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	SE4	SE3	SE2	SE1	SE0	0	ID8	ID7	0	0	ID4	0	0	0	0	1990h
02h	Master Volume	Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	Alternate Volume	Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono Volume	Mute	0	0	0	0	0	0	0	0	0	MM5	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	0	0	0	0	0	0	0	0	0	0	PV3	PV2	PV1	PV0	0	0000h
0Ch	Phone Volume	Mute	0	0	0	0	0	0	0	0	0	0	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	0	0	0	0	0	0	0	0	20dB	0	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	0	0	0	0	0	SL2	SL1	SL0	0	0	0	0	0	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	0	0	0	GL3	GL2	GL1	GL0	0	0	0	0	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	0	0	3D	0	0	0	MIX	MS	LPBK	0	0	0	0	0	0	0	0000h
22h	3D Control	0	0	0	0	0	0	0	0	0	0	0	0	S3	S2	S1	S0	0000h
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	0	0	0	0	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	ID1	ID0	0	0	0	0	AMAP	0	0	0	0	0	0	0	0	VRA	0201h
2Ah	Extended Audio Ctrl/Stat	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VRA	0000h
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM L/R ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
Cirrus Logic Defined Registers:																		
5E	AC Mode Control	0	0	0	0	0	0	0	DDM	AMAP	0	SM1	SM0	0	0	0	0	0080h
60	Misc. Crystal Control	0	0	0	0	Reserved				0	0	Reserved		0	Reserved		LOSM	0023h
68	S/PDIF Control	SPEN	Val	0	Fs	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Emph	Copy	/Audio	Pro	0000h
7Ch	Vendor ID1(CR)	F7	F6	F5	F4	F3	F4	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4352h
7Eh	Vendor ID2(Y-)	T7	T6	T5	T4	T3	T2	T1	T0	0	DID2	DID1	DID0	0	REV2	REV1	REV0	5931h

4.1 *Reset Register (Index 00h)*

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	SE4	SE3	SE2	SE1	SE0	0	ID8	ID7	0	0	ID4	0	0	0	0

SE[4:0] Crystal 3D Stereo Enhancement. SE[4:0] = 00110, indicating this feature is present.

ID8 18-bit ADC Resolution. The ID8 bit is 'set', indicating this feature is present.

ID7 20-bit DAC resolution. The ID7 bit is 'set', indicating this feature is present.

ID4 Headphone Output (Alt Line Out). The ID4 bit is 'set', indicating this feature is present.

Default 1990h. The data in this register is read-only data.

Any write to this register causes a Register Reset to the default state of the audio *(Index 00h - 38h)* and vendor specific *(Index 5Ah - 7Ah)* registers. A read from this register returns configuration information about the CS4299.

4.2 *Master Volume Register (Index 02h)*

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0

Mute Master Mute. Setting this bit mutes the LINE_OUT_L/R output signals.

ML[5:0] Master Volume Left. These bits control the left master output volume. Each step corresponds to 1.5 dB gain adjustment, with 00000 = 0 dB. The total range is 0 dB to -94.5 dB attenuation.

MR[5:0] Master Volume Right. These bits control the right master output volume. Each step corresponds to 1.5 dB gain adjustment, with 00000 = 0 dB. The total range is 0 dB to -94.5 dB attenuation.

Default 8000h. This value corresponds to 0 dB attenuation and Mute 'set'.

4.3 Alternate Volume Register (Index 04h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0

Mute — Alternate Mute. Setting this bit mutes the ALT_LINE_OUT_L/R output signals.

ML[4:0] — Alternate Volume Left. These bits control the left alternate output volume. Each step corresponds to 1.5 dB gain adjustment, with 00000 = 0 dB. The total range is 0 dB to -46.5 dB attenuation. See Table 4-2 for further attenuation levels.

ML5 — Alternate Volume Left Max Attenuation. Setting ML5 sets the left channel attenuation to -46.5 dB by forcing ML[4:0] to a '1' state. ML[5:0] will read back 011111 when ML5 has been 'set'. Table 4-2 summarizes this behavior.

MR[4:0] — Alternate Volume Right. These bits control the right alternate output volume. Each step corresponds to 1.5 dB gain adjustment, with 00000 = 0 dB. The total range is 0 dB to -46.5 dB attenuation. See Table 4-2 for further attenuation levels.

MR5 — Alternate Volume Right Max Attenuation. Setting MR5 sets the right channel attenuation to -46.5 dB by forcing MR[4:0] to a '1' state. MR[5:0] will read back 011111 when MR5 has been 'set'. Table 4-2 summarizes this behavior.

Default — 8000h. This value corresponds to 0 dB attenuation and Mute 'set'.

Table 4-2. Analog Mixer Output Attenuation

Mx[5:0] Write	Mx[5:0] Read	Gain Level
000000	000000	0 dB
000001	000001	-1.5 dB
…	…	...
011111	011111	-46.5 dB
100000	011111	-46.5 dB
...	...	...
111111	011111	-46.5 dB

4.4 Mono Volume Register (Index 06h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	0	MM5	MM4	MM3	MM2	MM1	MM0

Mute — Mono Mute. Setting this bit mutes the MONO_OUT signal.

MM[5:0] — Mono Volume. These bits control the mono output volume. Each step corresponds to 1.5 dB gain adjustment, with a total available range from 0 dB to -46.5 dB attenuation. See Table 4-2 for further attenuation levels.

MM5 — Mono Volume Max Attenuation. Setting the MM5 bit sets the mono attenuation to -46.5 dB by forcing MM[4:0] to a '1' state. MM[5:0] will read back 011111 when MM5 has been 'set'. Table 4-2 summarizes this behavior.

Default — 8000h. This value corresponds to 0 dB attenuation and Mute 'set'.

4.5 PC_BEEP Volume Register (Index 0Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	0	0	PV3	PV2	PV1	PV0	0

Mute — PC_BEEP Mute. Setting this bit mutes the PC_BEEP input signal.

PV[3:0] — PC_BEEP Volume Control. The PV[3:0] bits are used to control the gain levels of the PC_BEEP input source to the Input Mixer. Each step corresponds to 3 dB gain adjustment, with 0000 = 0 dB. The total range is 0 dB to -45 dB attenuation.

Default — 0000h. This value corresponds to 0 dB attenuation and Mute ‘clear’.

This register has no effect on the PC_BEEP volume during RESET#.

4.6 Phone Volume Register (Index 0Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	0	0	GN4	GN3	GN2	GN1	GN0

Mute — Phone Mute. Setting this bit mutes the Phone input signal.

GN[4:0] — Phone Volume Control. The GN[4:0] bits are used to control the gain levels of the Phone input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 4-4 on page 22 for further details.

Default — 8008h. This value corresponds to 0 dB gain and Mute ‘set’.

4.7 *Microphone Volume Register (Index 0Eh)*

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	20dB	0	GN4	GN3	GN2	GN1	GN0

Mute — Microphone Mute. Setting this bit mutes the MIC1 or MIC2 signal. The selection of the MIC1 or MIC2 input pin is controlled by the MS bit in the *General Purpose Register (Index 20h)*.

GN[4:0] — Microphone Volume Control. The GN[4:0] bits are used to control the gain level of the Microphone input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 4-3 for further details.

20dB — Microphone 20 dB Boost. When ‘set’, the 20dB bit enables the +20 dB microphone boost block. This bit allows for variable boost of 0 dB or +20 dB. Table 4-3 summarizes this behavior.

Default — 8008h. This value corresponds to 0 dB gain and Mute ‘set’.

Table 4-3. Microphone Input Gain Values

GN[4:0]	Gain Level	
	20 dB = 0	20 dB = 1
00000	+12.0 dB	+32.0 dB
00001	+10.5 dB	+30.5 dB
…	…	...
00111	+1.5 dB	+21.5 dB
01000	0.0 dB	+20.0 dB
01001	-1.5 dB	+18.5 dB
…	…	...
11111	-34.5 dB	-14.5 dB

4.8 Stereo Analog Mixer Input Gain Registers (Index 10h - 18h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0

Mute — Stereo Input Mute. Setting this bit mutes the respective input signal, both right and left inputs.

GL[4:0] — Left Volume Control. The GL[4:0] bits are used to control the gain level of the left analog input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 4-4 for further details.

GR[4:0] — Right Volume Control. The GR[4:0] bits are used to control the gain level of the right analog input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 4-4 for further details.

Default — 8808h. This value corresponds to 0 dB gain and Mute ‘set’.

The Stereo Analog Mixer Input Gain Registers are listed in Table 4-5.

Table 4-4. Analog Mixer Input Gain Values

Gx[4:0]	Gain Level
00000	+12.0 dB
00001	+10.5 dB
…	…
00111	+1.5 dB
01000	0.0 dB
01001	-1.5 dB
…	…
11111	-34.5 dB

Table 4-5. Stereo Volume Register Index

Register Index	Function
10h	Line In Volume
12h	CD Volume
14h	Video Volume
16h	Aux Volume
18h	PCM Out Volume

4.9 *Input Mux Select Register (Index 1Ah)*

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	SL2	SL1	SL0	0	0	0	0	0	SR2	SR1	SR0

SL[2:0] Left Channel Source. The SL[2:0] bits select the left channel source to pass to the ADCs for recording. See Table 4-6 for possible values.

SR[2:0] Right Channel Source. The SR[2:0] bits select the right channel source to pass to the ADCs for recording. See Table 4-6 for possible values.

Default 0000h. This value selects the Mic input for both channels.

Table 4-6. Input Mux Selection

Sx[2:0]	Record Source
000	Mic
001	CD Input
010	Video Input
011	Aux Input
100	Line Input
101	Stereo Mix
110	Mono Mix
111	Phone Input

4.10 *Record Gain Register (Index 1Ch)*

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	GL3	GL2	GL1	GL0	0	0	0	0	GR3	GR2	GR1	GR0

Mute Record Gain Mute. Setting this bit mutes the input to the L/R ADCs.

GL[3:0] Left ADC Gain. The GL[3:0] bits control the input gain on the left channel of the analog source, applied after the input mux and before the ADCs. Each step corresponds to 1.5 dB gain adjustment, with 0000 = 0 dB. The total range is 0 dB to +22.5 dB gain.

GR[3:0] Right ADC Gain. The GR[3:0] bits control the input gain on the right channel of the analog source, applied after the input mux and before the ADCs. Each step corresponds to 1.5 dB gain adjustment, with 0000 = 0 dB. The total range is 0 dB to +22.5 dB gain.

Default 8000h. This value corresponds to 0 dB gain and Mute ‘set’.

4.11 General Purpose Register (Index 20h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	3D	0	0	0	MIX	MS	LPBK	0	0	0	0	0	0	0

3D — 3D Enable. When 'set', the 3D bit enables the CrystalClear™ 3D stereo enhancement. This function is not available in DAC Direct Mode (DDM).

MIX — Mono Output Select. The MIX bit selects the source for the Mono Out output. When 'set', the microphone input is selected. When 'clear', the stereo-to-mono mixer is selected.

MS — Microphone Select. The MS bit determines which of the two Mic inputs are passed to the mixer. When 'set', the MIC2 input is selected. When 'clear', the MIC1 input is selected.

LPBK — Loopback Enable. When 'set', the LPBK bit enables the ADC/DAC Loopback Mode. This bit routes the output of the ADCs to the input of the DACs without involving the AC-link.

Default — 0000h

4.12 3D Control Register (Index 22h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	S3	S2	S1	S0

S[3:0] — Spacial Enhancement Depth. These bits control the amount of "space" added to the output stereo signal. When S[3:0] = 0000, the minimum amount of spatial enhancement is added. When S[3:0] = 1111, the maximum amount of spatial enhancement is added. The 3D function is enabled and disabled by the 3D bit in the *General Purpose Register (Index 20h)*.

Default — 0000h. This value corresponds to minimum spatial enhancement added to the output signal.

4.13 *Powerdown Control/Status Register (Index 26h)*

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	0	0	0	0	REF	ANL	DAC	ADC

EAPD — External Amplifier Power Down. The EAPD pin follows this bit and is generally used to power down external amplifiers.

PR6 — Alternate Line Out Powerdown. When ‘set’, the alternate line out buffer is powered down.

PR5 — Internal Clock Disable. When ‘set’, this bit completely powers down both the analog and digital sections of the CS4299. The only way to recover from setting this bit is through a Cold Reset (driving the RESET# signal active).

PR4 — AC-link Powerdown. When ‘set’, the AC link is powered down (BIT_CLK off). The AC-link can be restarted through a Warm Reset using the SYNC signal, or a Cold Reset using the RESET# signal (primary audio codec only).

PR3 — Analog Mixer Powerdown (Vref off). When ‘set’, the analog mixer and voltage reference are powered down. When clearing this bit, the ANL, ADC, and DAC bits should be checked before writing any mixer registers.

PR2 — Analog Mixer Powerdown (Vref on). When ‘set’, the analog mixer is powered down (the voltage reference is still active). When clearing this bit, the ANL bit should be checked before writing any mixer registers.

PR1 — Front DACs Powerdown. When ‘set’, the DACs are powered down. When clearing this bit, the DAC bit should be checked before sending any data to the DACs.

PR0 — L/R ADCs and Input Mux Powerdown. When ‘set’, the ADCs and the ADC input muxes are powered down. When clearing this bit, no valid data will be sent down the AC link until the ADC bit goes high.

REF — Voltage Reference Ready Status. When ‘set’, indicates the voltage reference is at a nominal level.

ANL — Analog Ready Status. When ‘set’, the analog output mixer, input multiplexer, and volume controls are ready. When clear, no volume control registers should be written.

DAC — Front DAC Ready Status. When ‘set’, the DACs are ready to receive data across the AC link. When clear, the DACs will not accept any valid data.

ADC — L/R ADC Ready Status. When ‘set’, the ADCs are ready to send data across the AC link. When clear, no data will be sent to the Controller.

Default — 0000h. This value indicates all blocks are powered on. The lower four bits will change as the CS4299 finishes an initialization and calibration sequence.

The PR[6:0] and the EAPD bits are powerdown control for different sections of the CS4299 as well as external amplifiers. The REF, ANL, DAC, and ADC bits are read-only status bits which, when ‘set’, indicate that a particular section of the CS4299 is ready. After the controller receives the Codec Ready bit in input Slot 0, these status bits must be checked before writing to any mixer registers. See Section 5, *Power Management*, for more information on the powerdown functions.